TI Designs

System on Module for Industrial Power Line Communication (CENELEC Frequency Band)

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDM-SOMPLC-INDUSTRIAL-CENELEC	Design Folder
TMDSPLCKIT-V4	Tool Folder
TMS320F28035	Product Folder
AFE031	Product Folder
TPS62240	Product Folder
TPS3828-33	Product Folder
SN74LVC2G07	Product Folder

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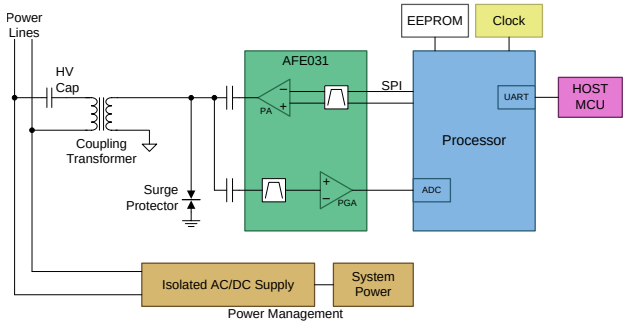
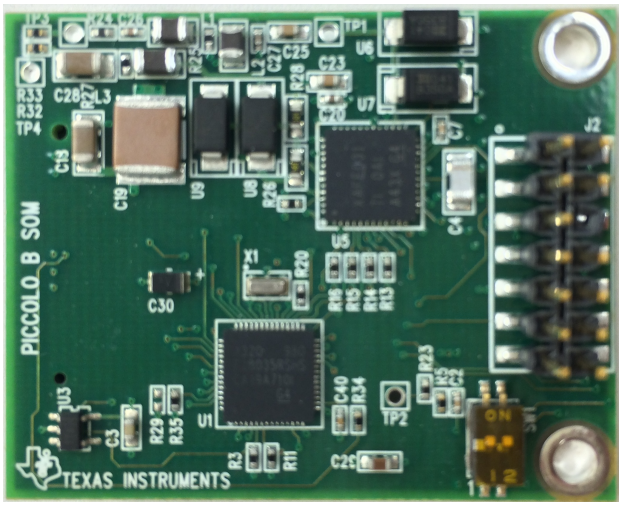
Design Features

- Small size: 1.5 × 1.9 in
- PLC-Lite Compatible
- Data Rates up to 21.4 kbps (Half-Band FEC OFF)
- Transmission with OFDM and FEC
- ROBO Mode Provides Repetition Code
- Convolutional Encoder and Viterbi Decoder
- Bit Interleaving for Noise Effect Reduction
- CRC8 in Headers for Error Detection
- Automatic Gain Control
- Supports PLC-Lite PHY, CSMA/CA MAC layer
- Serial Interface for Host Data Port: UART and HCT
- USB or JTAG for Custom Firmware Download

Featured Applications

- Solar Inverter
- Lighting Control
- Motor Control





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1 SOMPLC Description

The SOMPLC-F28PLC83 is a single-board system on module (SOM) for power line communication (PLC) in the CENELEC frequency band. This single hardware design supports TI proprietary industrial PLC solution (PLC-Lite). TI's certified PLC software is available along with the SOMPLC-TMS320F28035. Engineers can take the SOM design and integrate it into their overall system board or keep the design as an add-on board to their application. The only additional hardware required is the AC mains line coupling circuitry. The included hardware schematics and Gerber files simplify the task for engineers to add PLCs to their end system. OEMs will benefit from having the ability to rapidly evaluate and prototype PLC technology in their application.

2 System Description

The SOMPLC-TMS320F28035 enables easy development of software-based PLC modems. The SOM module has the TMS320F28035 device with an integrated analog front end (AFE031).

2.1 PLC Development Kit Components

The development kit includes the following hardware:

- Two sets of development board, each set containing:
  - SOMPLC-TMS320F28035 (TMS320F28035 + AFE031)
  - One docking board

The development kit includes the following software:

- PLC-Lite binaries
  - plc_lite.out/hex
- PC software and GUI
  - Zero configuration GUI v2.92 or higher

The development kit includes the following documents:

- PLC-Lite software API specifications
  - Host message protocol specifications
- PLC-Lite hardware documents
  - AFE daughter card schematics and Gerber files
  - Docking board schematics and Gerber files
  - Bill of materials (BOM)

2.2 System Installation Requirements

To install software package to communicate with the PLC development kit, the PC must meet the following minimum requirements:

- Microsoft® Windows® XP® (SP2) or Windows 2000® (SP4)
- Intel® Pentium® IV 1-GHz processor
- 128-MB RAM (256-MB RAM recommended)
- USB 2.0 interface (if using a JTAG debug interface)
- Screen resolution 1024×768 or better
- 1 MB of free space on the HDD for the applications (more for LOG files)

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2.3 Motivation of PLC-Lite on SOMPLC-TMS320F28035

PLC-Lite is TI's proprietary PLC solution targeting for industrial applications such as solar inverter, lighting control, motor control, and so on. The key feature of the industrial applications is to communicate with each other in localized networks. Using global PLC standards such as PRIME, G3-PLC, and IEEE 1901.2 would be a solution for communication method, but typically the standards include complicated protocol stacks that might not be needed for industrial applications.

The motivation for this TI design is to create light-weight and flexible communication method (named PLC-Lite) for industrial applications, which includes a minimum set of protocol stacks (PHY or MAC) only. This method greatly reduces memory and flash requirements, allowing the PLC-Lite to fit on the SOMPLC-TMS320F28035, one of TI's low-end DSP devices.

3 Boot Modes (SW1 Positions)

Boot mode can be selected using the switch SW1. The available settings are described in Figure 1.

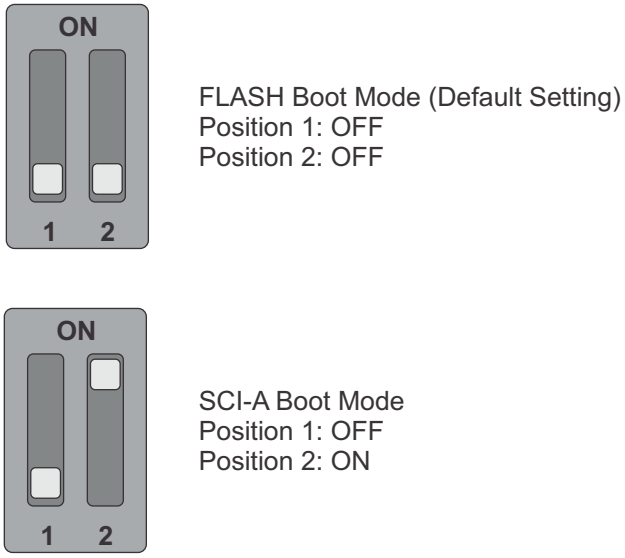

Figure 1. Boot Modes

4 UART SCI Communication

To communicate with the SCI, the following requirements must be met:

- Baud Rate = 57600
- Message Data Bits = 8
- Stop Bits = One
- Parity = None
- Handshake = None
- RTS Enable = True

NOTE: The SOMPLC does not have an RS-232 driver. Consider communications to RS-232 devices external to this design.

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5 PLC SOM Programming

Depending on the end use of the SOM, different versions of the PLC software may be programmed to the module.

For this design, download the PLC-Lite software package from the link given in Section 11 and check out the PLC-Lite binaries (.hex, .out, and .sbin) under installation directory.

5.1 Using the XDS100 and CodeSkin to program the F28035 MCU

Programming with this method eliminates the need for CCS to load the release(.out) file. A .hex release file is used instead and therefore the installation of Code Composer Studio™ (CCS) is not necessary.

1. Install the desired Texas Instruments PLC Development Package from www.ti.com/plc.
2. Download, install, and start the latest C2Prog from http://www.codeskin.com.
3. Set switch SW1 to *FLASH Boot Mode* as described in Section 3.
4. Connect a Texas Instruments XDS100 class emulator to the SOM module using the 14-pin JTAG header.
5. Power up SOM module by applying both 15 V and 3.3 V through the 34-pin host connector.
6. Program the *.hex (located in c:\Texas Instruments\<PackageName>\SW\bin) as shown in Figure 2. Select "28035,34" in the *Target* pull-down and "JTAG" in the *Options* pull-down.

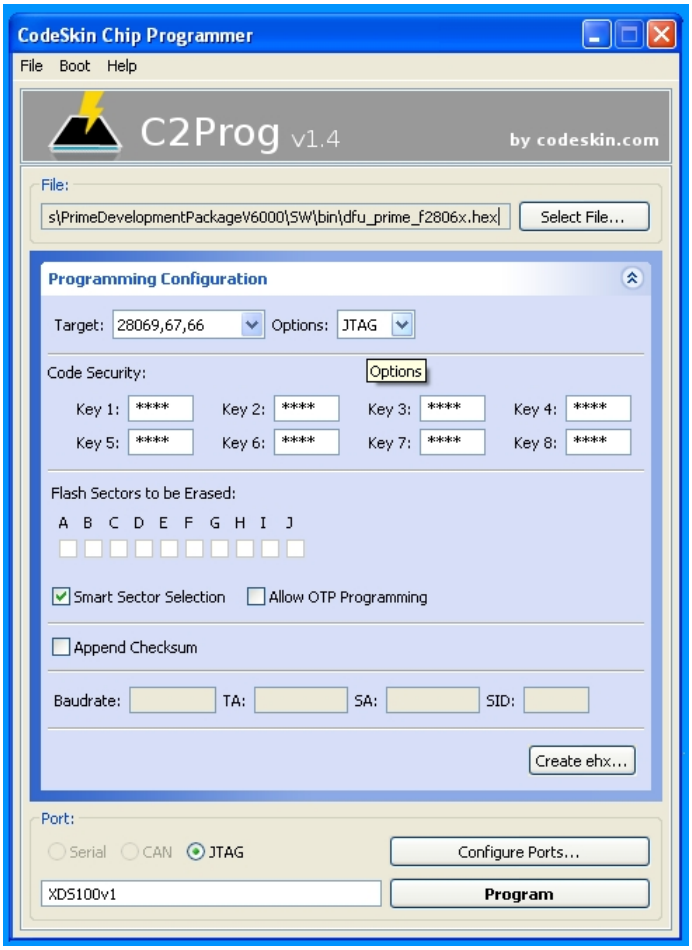

Figure 2. Selecting PLC-Lite Binary to be Flashed (through XDS100)

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7. Click on the *Configure Ports* button and set the JTAG port to “XDS100v1” or “XDS100v2”.

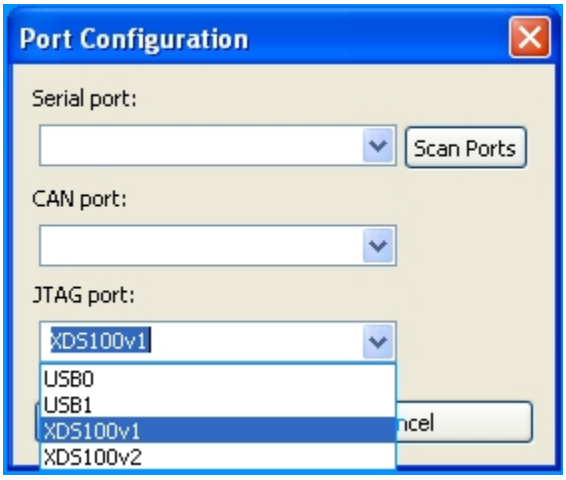

Figure 3. Selecting JTAG Port (via XDS100)

8. Start flashing the F28035.

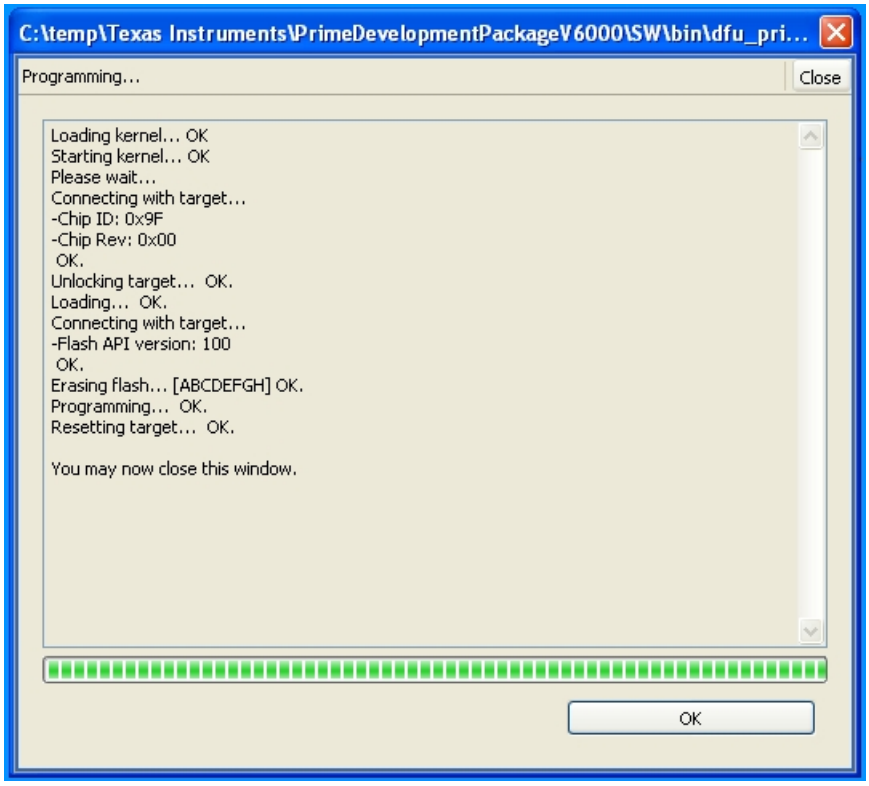

Figure 4. Flashing PLC-Lite Firmware (via XDS100)

9. The programming procedure is now complete. Power cycle the device.

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5.2 Using CCS and JTAG Emulator to Program the F28035 MCU

If the XDS100 emulator is not available, use CCS v4.2.4 or higher and a XDS510 or XDS560 emulator to program the device. Install CCS before following these procedures:

1. Install the desired Texas Instruments PLC Development Package from www.ti.com/plc.
2. Set switch SW1 to *FLASH Boot Mode* as described in Section 3. When used, a JTAG emulator is capable of interrupting the set boot mode to gain control of the MCU. When the programming procedure is complete, set the mode to *FLASH Boot Mode* for the SOM module to continue to work properly.
3. Power up the SOM module by applying both 15 V and 3.3 V through the 34-pin host connector.
4. Connect the emulator to the SOM module with the 14-pin JTAG cable.
5. Open CCS.
6. Create a F28069 target configuration.
7. Connect to the F28069 device.
8. Load the PLC specific .out firmware (located in c:\Texas Instruments\<PackageName>\SW\bin). CCS will automatically flash the firmware onto the F28069 device.

5.3 Using a Serial Port (RS-232/SCI) to program the F28035 MCU

Some user situations may require the SOM module to connect directly to a computer's serial port using RS-232 communications. In this scenario, have a host board that is capable of converting the RS-232 communications protocol to work with the F28069 SCI-A port. In most cases, this conversion is performed by using an external RS-232 driver device such as the MAX3221ECPWR by Texas Instruments. Once in place, follow these steps:

1. Install the desired Texas Instruments PLC Development Package from www.ti.com/plc
2. Download, install and start the latest C2Prog from www.codeskin.com
3. Make sure the SOM module is not powered on. Set switch SW1 to *SCI-A Boot Mode* as described in Section 3.
4. Connect the SOM module to the RS-232 host using the appropriate cable.
5. Power up the SOM module by applying both 15 V and 3.3 V through the 34-pin host connector.

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6. Program the *.hex (located in c:\Texas Instruments\<PackageName>\SW\bin) as shown in Figure 5. If the UART cable is used, select serial port. Otherwise, if the USB serial cable is used, select JTAG port.

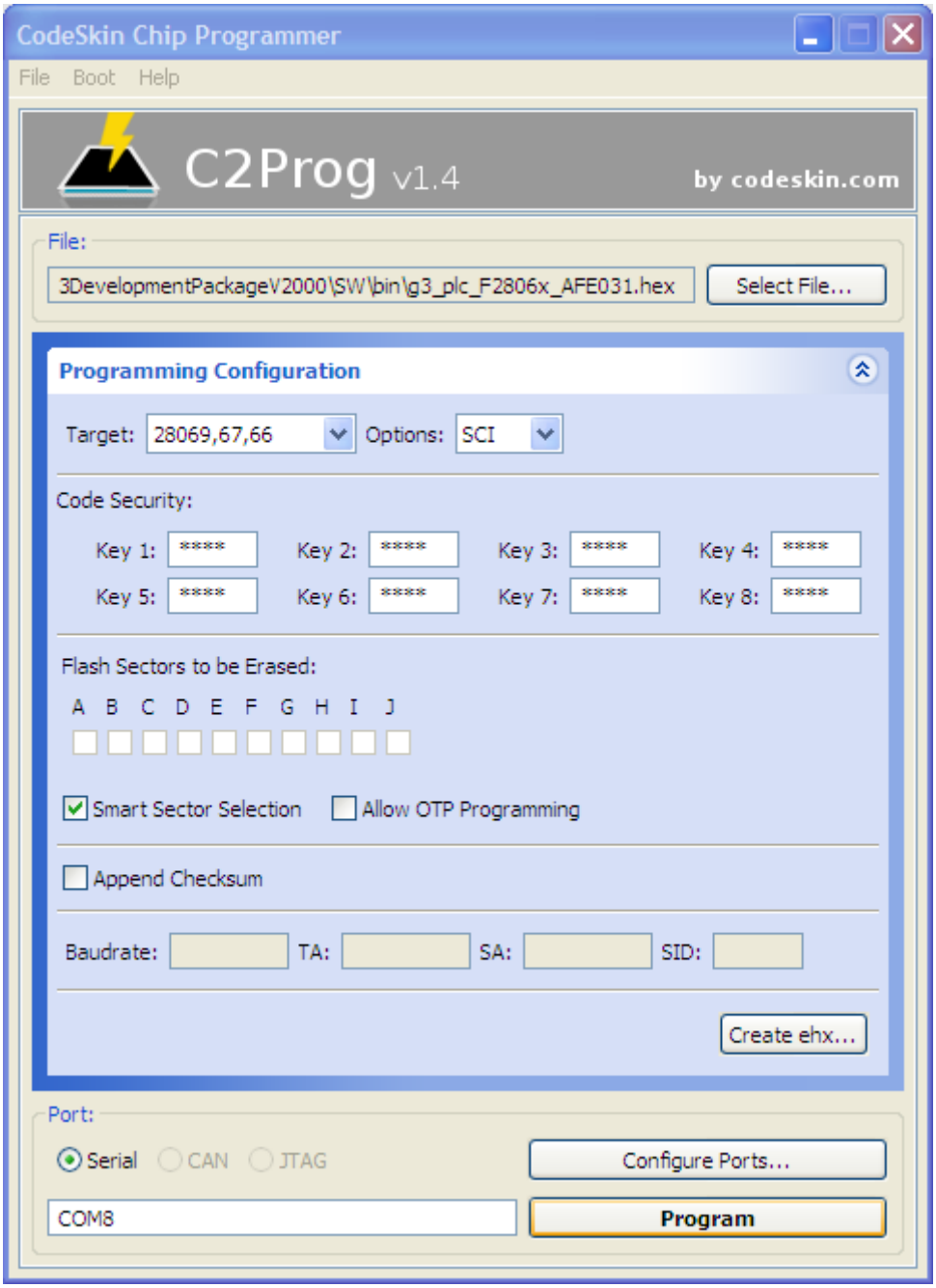

Figure 5. Selecting PLC-Lite Binary to be Flashed (via SCI)

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7. Start flashing the F28035.

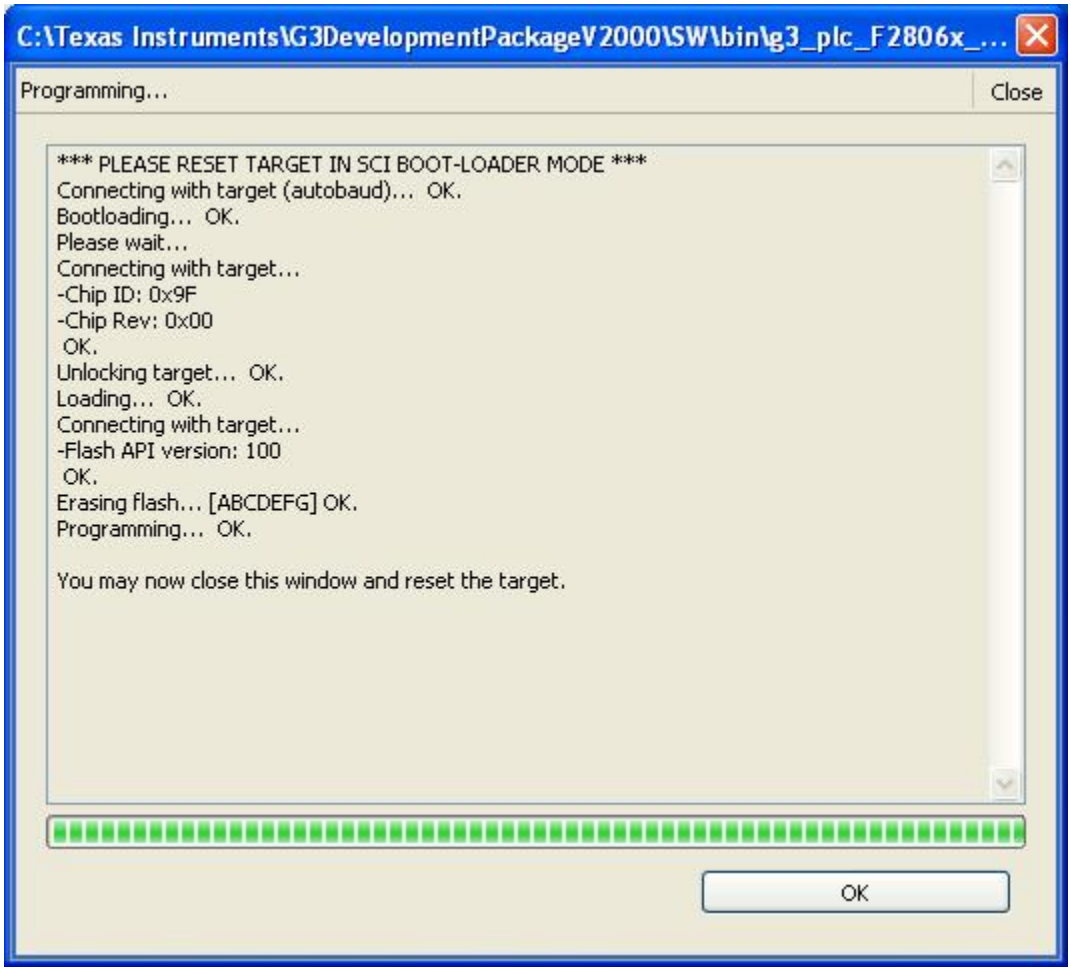

Figure 6. Flashing PLC-LITE Firmware (via SCI)

8. Once the flashing is done, close the program and remove the power supply from the SOM module.
9. Make sure the SOM module is not powered off. Set switch SW1 to *FLASH Boot Mode* as described in Section 3.
10. Now that the programming procedure is complete, apply power to the SOM module.

6 Test Setup

To test the SOM modules, the operator will need the following items:

- A host computer running Windows XP or Windows 7® and two available USB ports.
- Two SOM docking stations
- A 15-V external power supply for each docking station
- A PLC for each docking station
- A USB cable for connecting to host PC for each docking station
  - A single host PC can be shared between the two kits
- Zero-configuration GUI
  - Requires a modified .config file

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6.1 Setup

1. Plug in the included SOM module to each 34-pin SOM module connector.

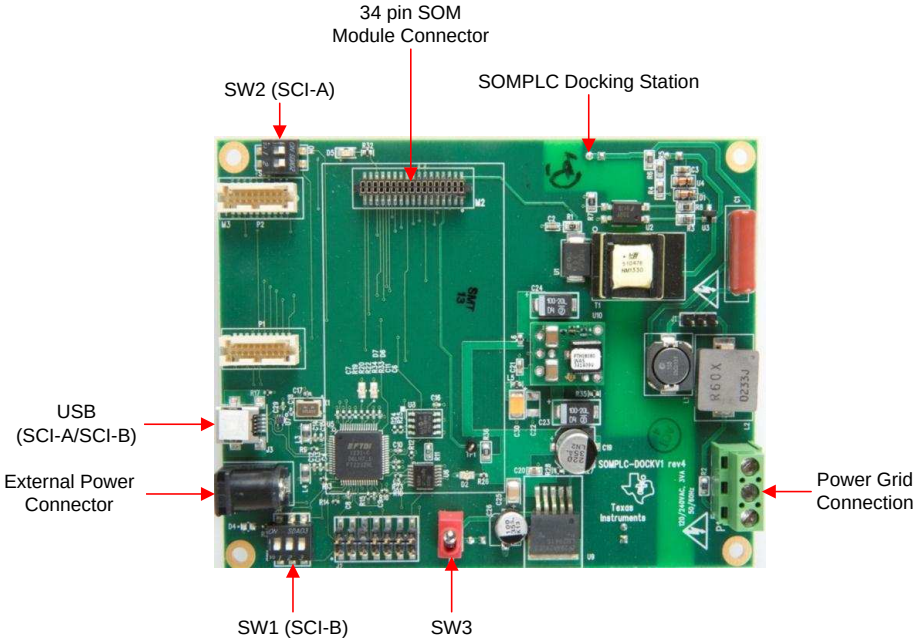

Figure 7. SOMPLC Docking Station

2. Connect *Neutral* and *Line* (marked with words on the AC Power Cable) to the power grid connector P1 of each kit. Make sure the neutral and line connections are not shorted.

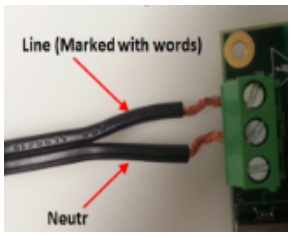

Figure 8. Line Connection

3. Ensure the position of switches SW1 and SW2 are set to default setting as shown in Figure 9 to communicate to the PC GUI via SCI-A.

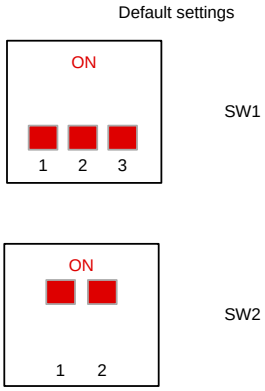

Figure 9. Software Configuration

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6.2 Power Up

1. Connect the 15-V wall-mounted power supply to the AC receptacle of each kit.
2. Turn on switch SW3 of each kit to power the boards.

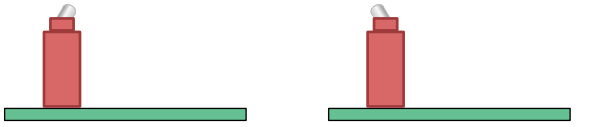

Figure 10. SW3

6.3 Connecting to a PC

1. Plug in the micro-USB to the kit and connect the USB cable to the PC. Repeat this step for the second kit.

NOTE: If asked to install USB-Serial drivers, proceed to install the drivers. The drivers can be found in C:\Texas Instruments\<PackageName>\XDS100 Drivers. Reboot the PC after the drivers are installed, even if Windows does not ask to.

2. Verify the modems have been installed correctly by using the Device Manager (Start→Control Panel→System→Device Manager→Ports).

NOTE: The four ports highlighted in Figure 11 are for two boards.

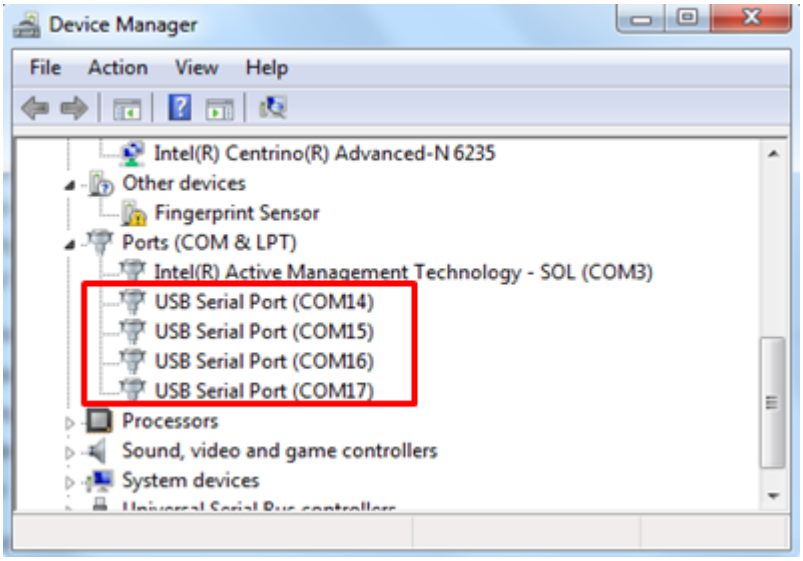

Figure 11. Device Manager: Port Configuration

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6.4 GUI Test Setup

1. Install the *Zero Configuration* tool from C:\TexasInstruments\<PackageName>\Tools, and launch it. If using one PC to operate, launch two instances, one for each modem.

NOTE: When the zero-configuration GUI opens, it will use the first available COM port to attach to a PLC.

2. Ensure *Diagnostic Port/Data Port* configures to SCI-A by pressing *CTRL+A* in the GUI window.

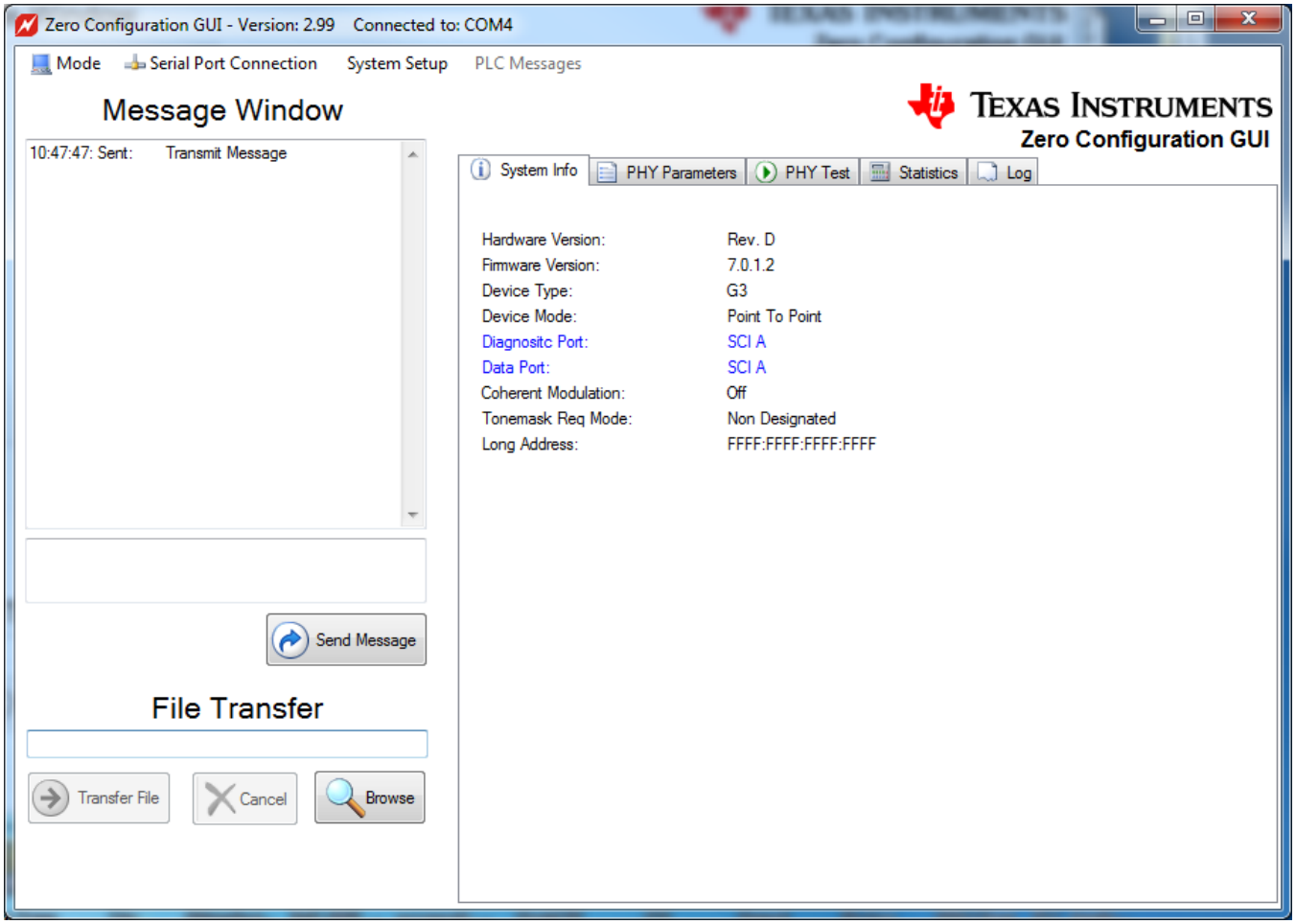

Figure 12. Zero-Configuration GUI

3. Connect each PLC kit to the power line. Ensure that the devices are connected on the same power line phase.

WARNING

HIGH VOLTAGE!

Use caution when connecting to the power grid. If there is concern about connecting to the power grid, use a power strip to connect the two modems together. In this case, the power strip does not need to be plugged into the power grid.

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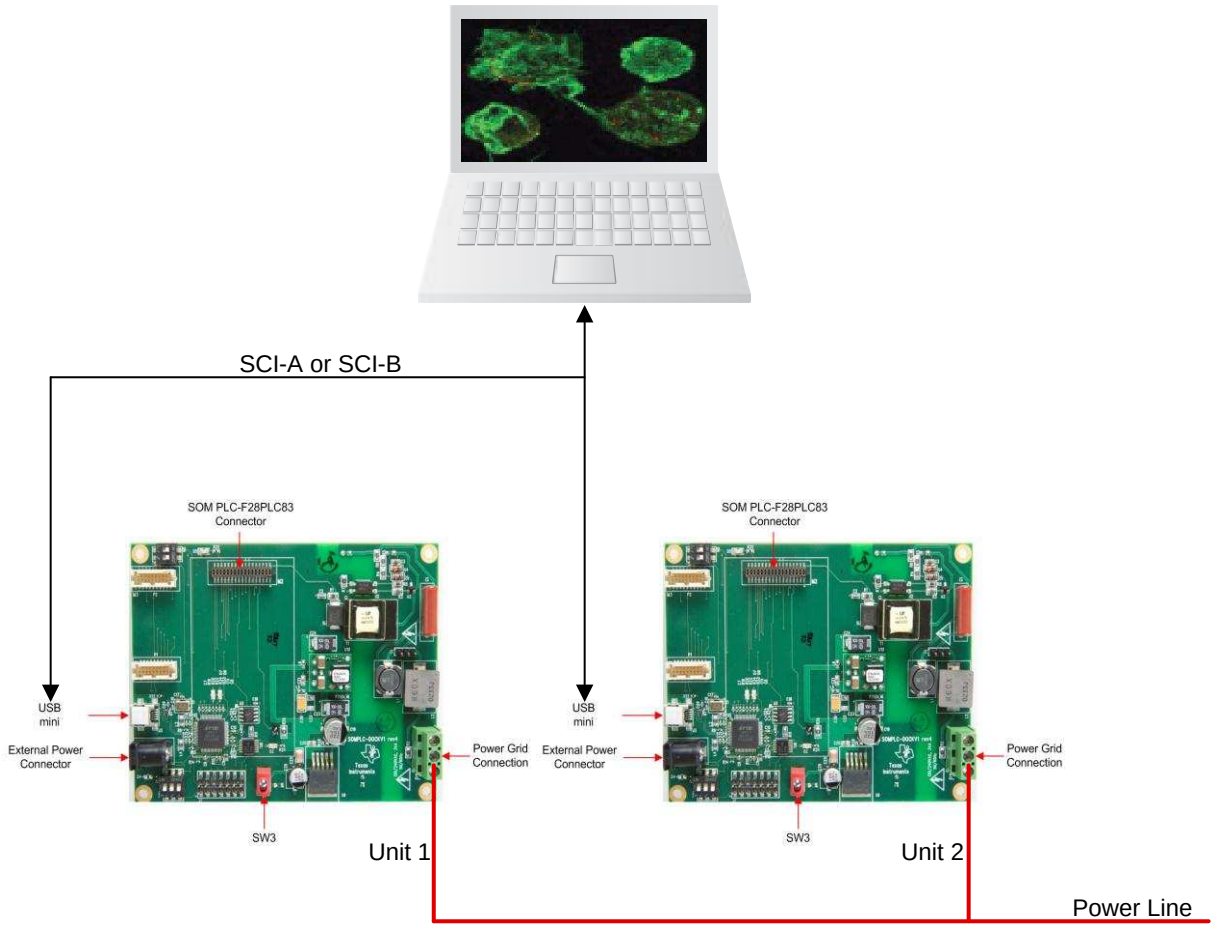

Figure 13. Testing Set-up

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7 Using Demo Application – Zero Configuration GUI

The zero configuration GUI is a Windows application that allows users to immediately transfer text and files, examine the current system information, display the PHY parameters, change the PHY modulation, and display the file and text transfer statistics and save log information.

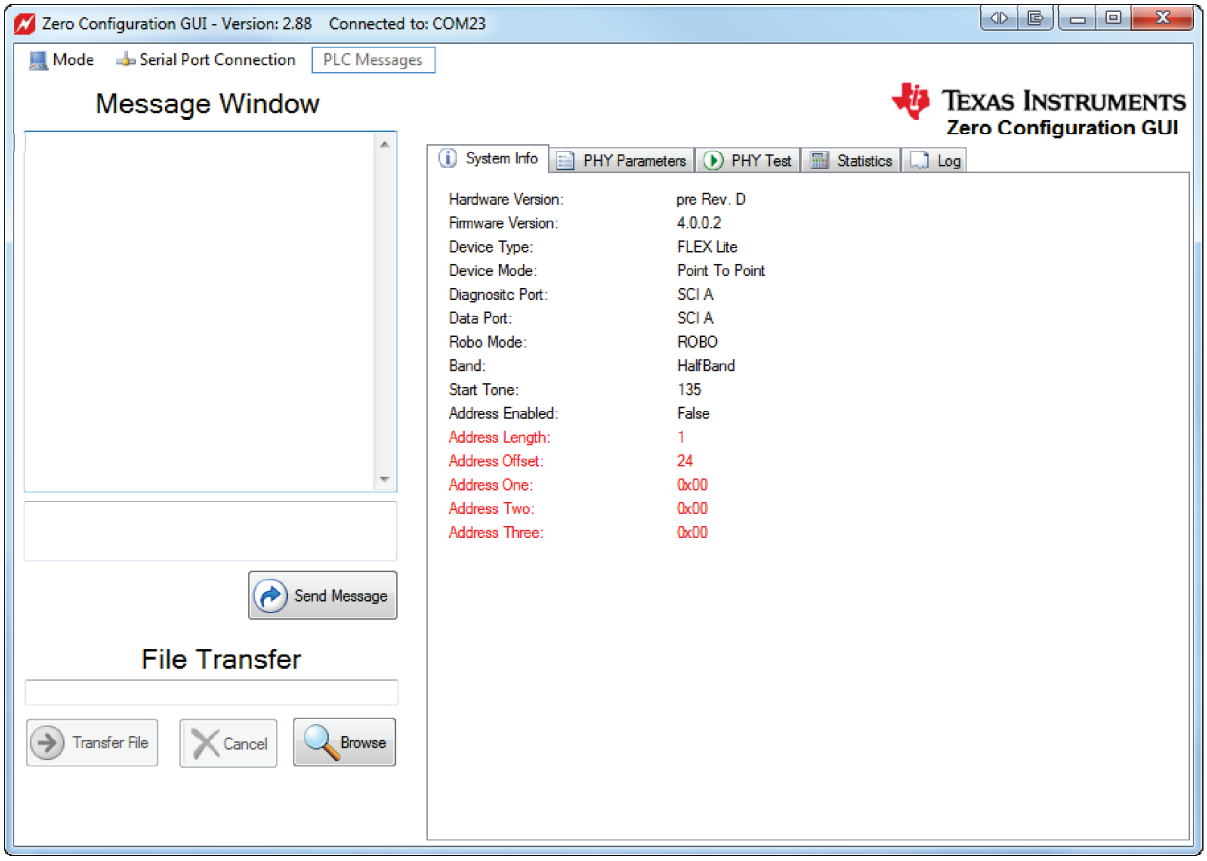

Figure 14. Zero Configuration GUI – Starting Screen

NOTE: Both transmit and receive stations should be running the zero configuration GUI and should not be paired with the PLC quality meter (PQM).

7.1 Configuration

No software or PLC configuration is needed to use the zero configuration GUI. The first available COM port on the PC, which may be a USB-to-Serial port or a standard COM port, connects to the PLC. If no available serial ports are found on the PC, the zero configuration GUI will display an error (as shown in Figure 15) and exit.

Figure 15. Message Box for No Serial Ports Found

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If the COM port selected does not respond, the zero configuration GUI will display a timeout error and remain active as shown in Figure 16.

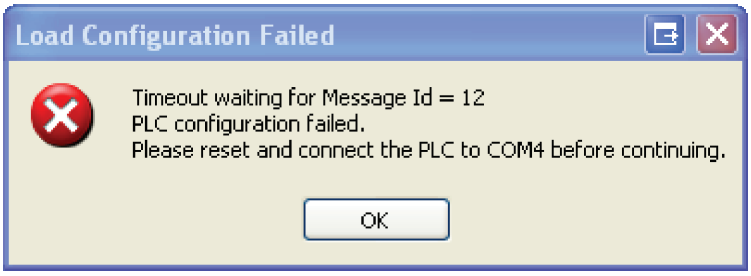

Figure 16. Message Box for Load Configuration Failed

If the PLC is connected to another COM port, the user may use the Serial Port Connection drop-down menu to connect to the desired COM port. If the PLC is not connected, connect the PLC to the desired port and try again. Once the PLC is connected to the correct COM port, reset the PLC.

7.2 Main Screen

The zero configuration GUI consists of the main screen where the user can transfer text and files. The tabs on the right display significant information about the PLC. The COM port attached is displayed in the title bar. The first available and unopened COM port is automatically chosen. The Serial Port Connection drop-down menu may be used to change the selection to another COM port. From this screen the user can transfer text messages and files with another PLC controlled by the zero configuration GUI.

The user may also change the mode by using the Mode drop-down menu. The three modes are zero configuration, intermediate, and expert.

- In the zero configuration mode, any available COM port 1 to 99 works with the zero configuration GUI.
- The intermediate mode GUI uses the same COM port as the zero configuration GUI. When the intermediate mode exits, the zero configuration reopens the COM port and takes control once again.
- The expert is currently disabled for this release.

7.3 Hot Keys

Several hot keys are available. The alpha key is not case sensitive.

<Ctrl + I> — Closes the GUI and executes the intermediate GUI.

<Ctrl + R> — Resets the file transfer statistics. The statistics received in the link quality report are not reset. This key stroke combination resets the statistics screen, regardless of which screen has focus in the GUI.

<Ctrl + T> — Toggles the expert mode menu items on and off, depending on their current state.

<Ctrl + S> — Sends a system information request to the PLC and updates the system info panel when the request is received.

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7.4 System Info Panel

The PLC system information is displayed in the first tab. Right clicking on the *System Info* panel reveals a context menu with one menu item, *Refresh System Information*. This item will resend a system information request to the PLC and refresh the *System Info* panel with the updated information. Pressing *Ctrl+S* performs the same function without displaying the context menu.

Any value changed will be displayed in red text as shown in Figure 17.

Figure 17. Zero Configuration GUI – System Info Panel

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7.5 PHY Parameters Panel

The second tab displays the PHY TX (transmit) and RX (receive) parameters. The TX modulation may be changed using the radio boxes. Changing the modulation schemes affects the reliability and baud rate of the power line transmission.

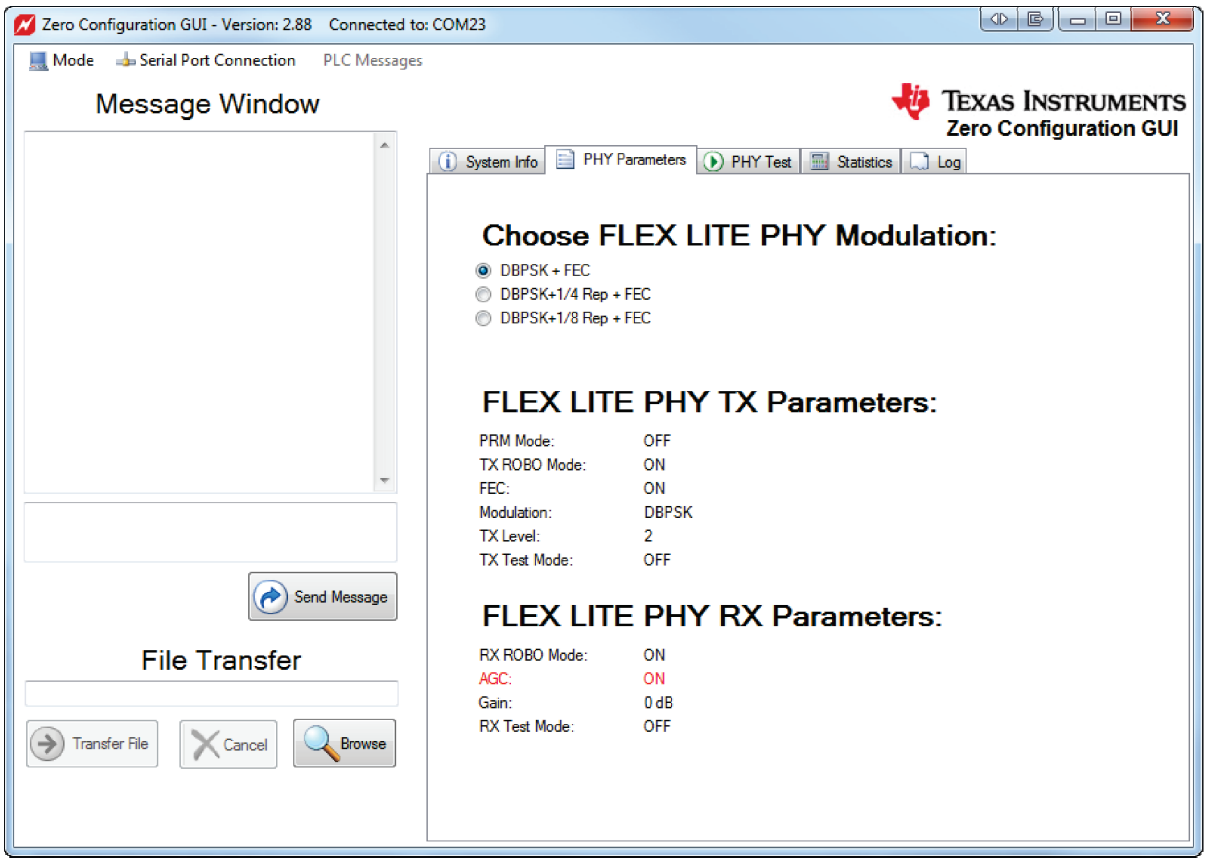

Figure 18. Zero Configuration GUI – PHY Parameters Panel

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7.6 Statistics Panel

The *Statistic* panel displays information concerning the text and file transfers. Items that have changed are displayed in red. Right clicking on the *Statistics* panel reveals a context menu with one menu item, *Reset Application Totals*. This item resets totals. Pressing *Ctrl+R* performs the same function without displaying the context menu.

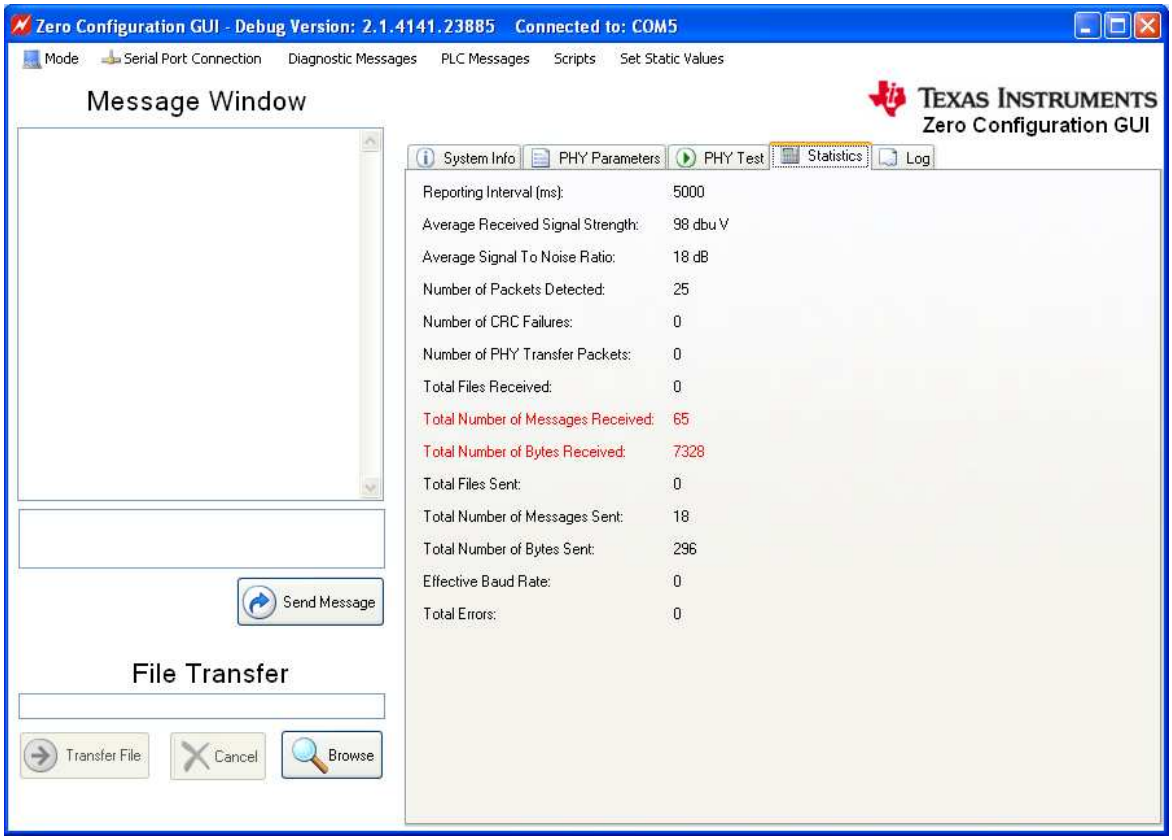

Figure 19. Zero Configuration GUI – Statistics Panel

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7.7 PHY Test Panel

The *PHY Test* panel tests communications between two PLCs using PHY packets. One PLC transmits the PHY packets while the other receives the PHY packets. To start the test, click on the *Start Flex Lite PHY Transmit* button on either PLC. The statistics will disappear from the panel since there are no statistics collected on the transmitting PLC. See the example in Figure 20.

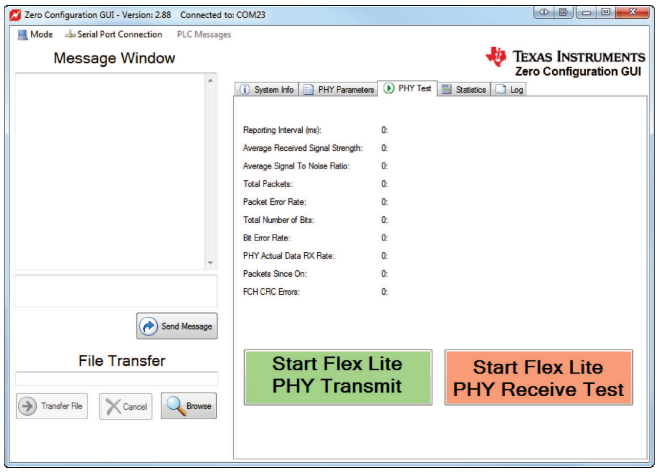

Figure 20. Zero Configuration GUI – PHY Test Panel

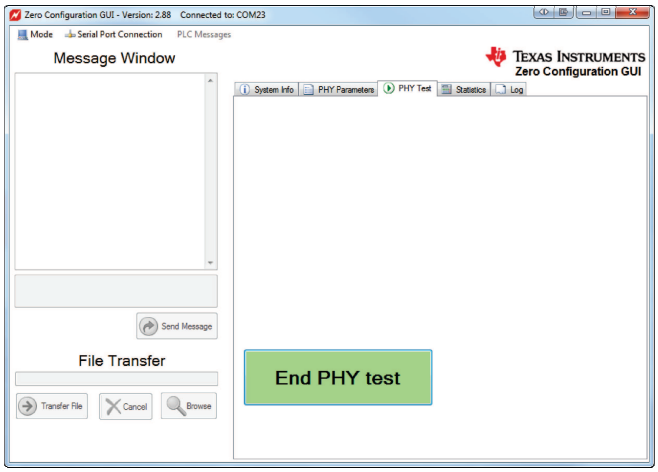

Figure 21. Zero Configuration GUI – PHY TX Transmitting

NOTE: Text and file transfers will not work during PHY testing.

On the receiving PLC, click the *Start Flex Lite PHY Receive Test* button. This button changes to *End PHY test*, and the statistics will start updating. See the example in Figure 22.

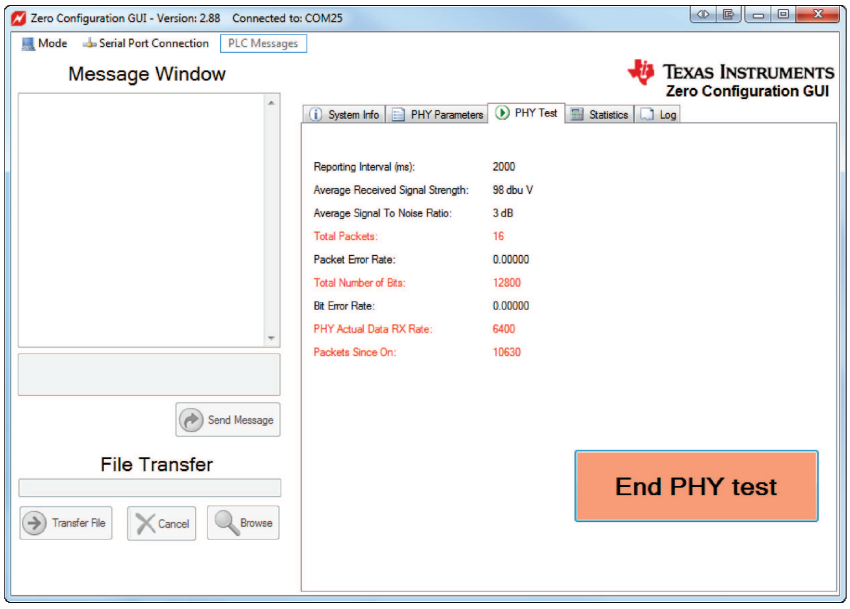

Figure 22. Zero Configuration GUI – PHY RX Receiving

To end the test click the *End PHY test* button on both PLC.

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7.8 Log Panel

The *Log* panel holds about 100,000 characters and then refreshes the display. This action prevents the panel from consuming large amounts of memory and keeps the *Log* panel responsive to new input.

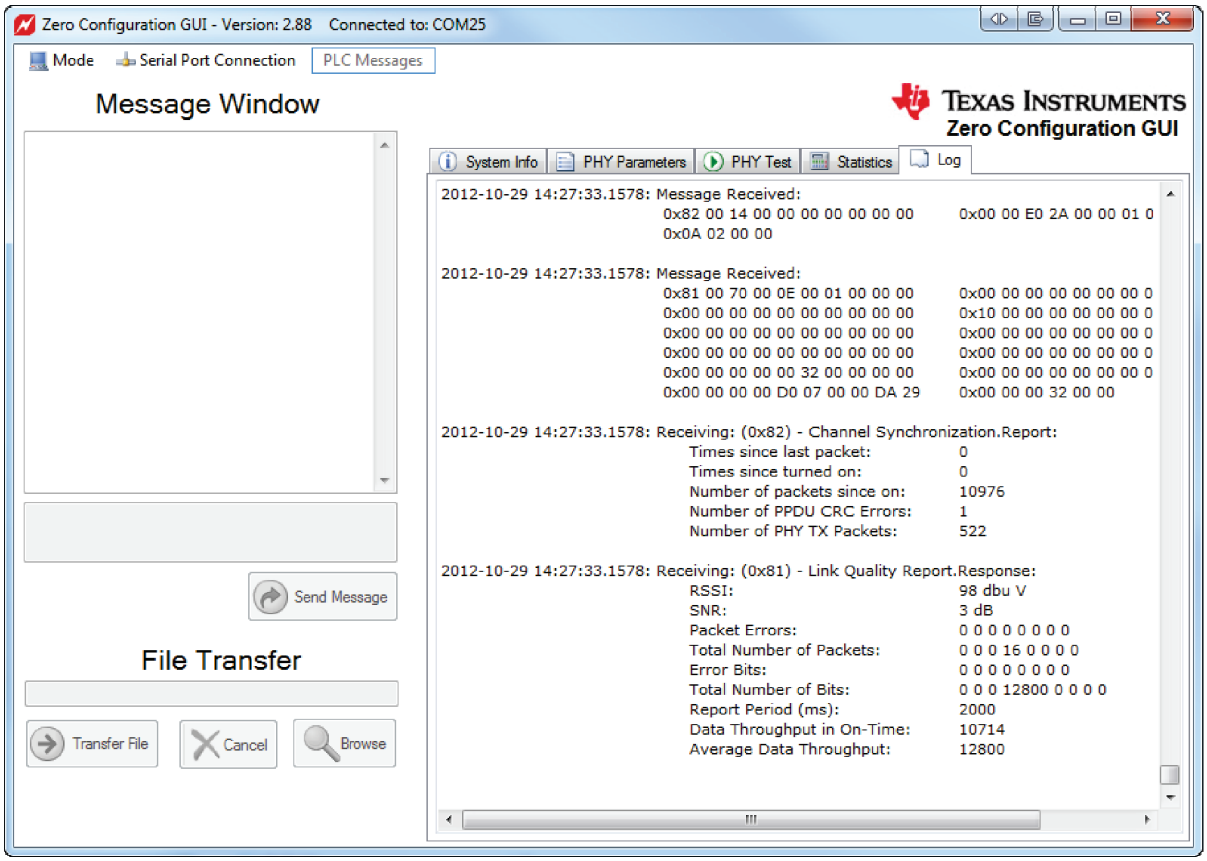

Figure 23. Zero Configuration GUI – Log Panel

The *Log* panel by default displays very little information, but right clicking on the panel displays the *Log* panel context menu. Use this menu to display the formatted messages sent and received by the zero configuration GUI. The following is the list of features exposed by the *Log* panel context menu:

Enable Message Data Display — This feature enables the Log panel to display the message transfers, both sending and receiving. Depending on the other options selected, the raw data, formatted data, or both will be displayed. This option is off by default.

Enable Logging to a File — When selected, this feature prompts the user for a file to save the logged information. When enabled, all data messages sent and received are saved and written to the log.

Log Full Message Data — This feature displays the formatted message data in the Log panel. No data is displayed unless the Enable Message Data Display is enabled.

Log Condensed Data — This feature only displays the message type and no actual message data. This action reduces the amount of data logged to the screen.

Log Raw Message Data — This feature displays the unformatted message data as a byte stream.

Clear Display — This feature clears the Log panel. This action does not affect data being logged to a file.

Save to File — This feature saves the current contents of the log panel to a file of the user's choosing.

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7.9 Sending Text Messages

To transfer text between two connected PLC devices using the zero configuration GUI, type text in the small text box and click on the Send Message button. Pressing Enter while entering the text adds a line. The key will not send the text message.

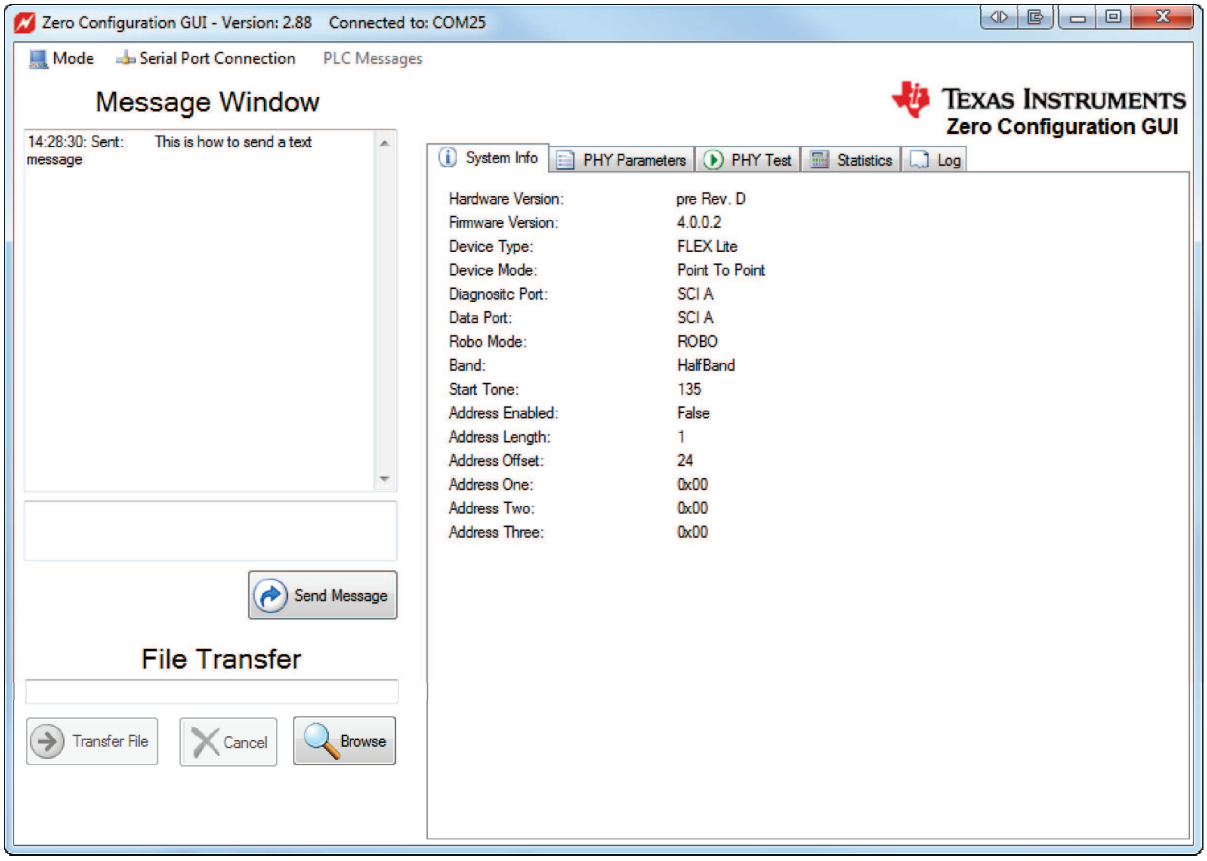

Figure 24. Zero Configuration GUI – Send Text Message

When the text is sent, the text is moved to the top text box and displayed by the receiving PLC.

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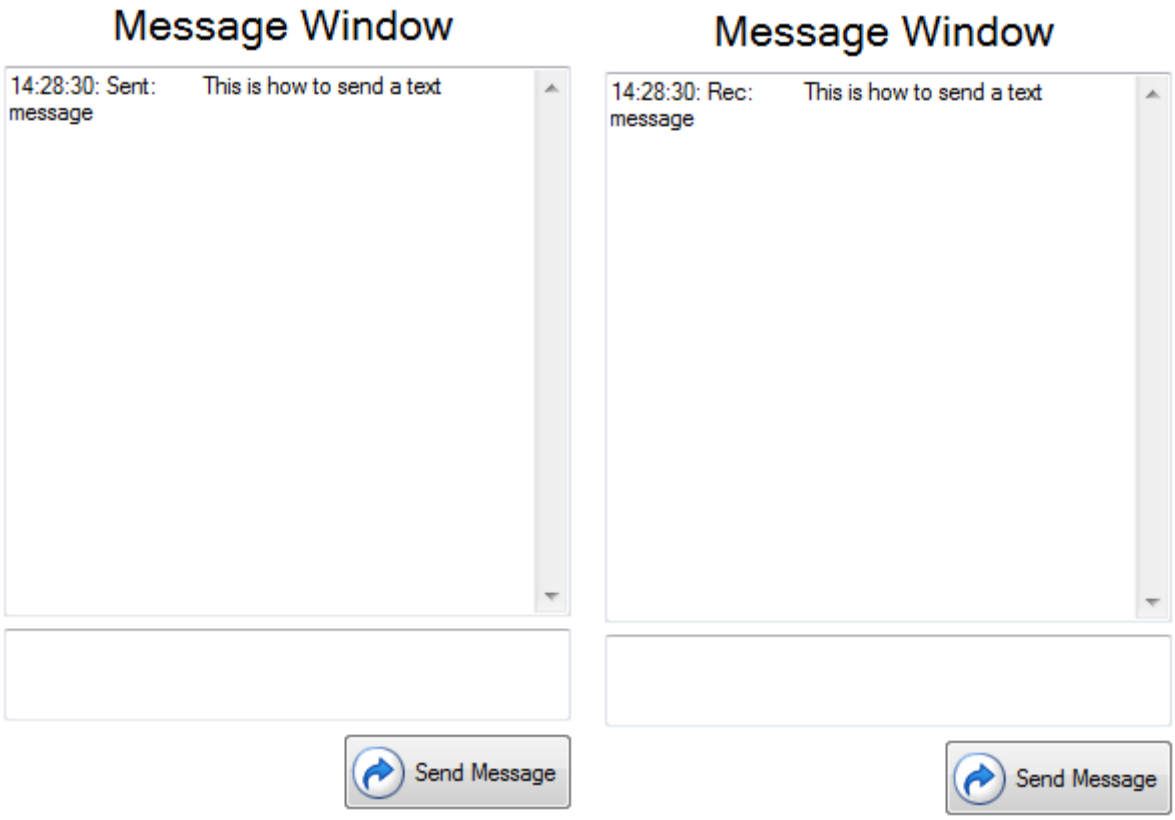

Figure 25. Zero Configuration GUI – Message Window

The form on the left in Figure 25 is the sender and the form on the right is the receiver. The user may send text from either PLC device.

Figure 26. Message Box for Failed Text Message

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7.10 File Transfers

The *File Transfer* function is contained in the bottom left-hand corner. Click on the *Browse* button to choose the file to transfer. Only one file at a time may be chosen for the file transfer.

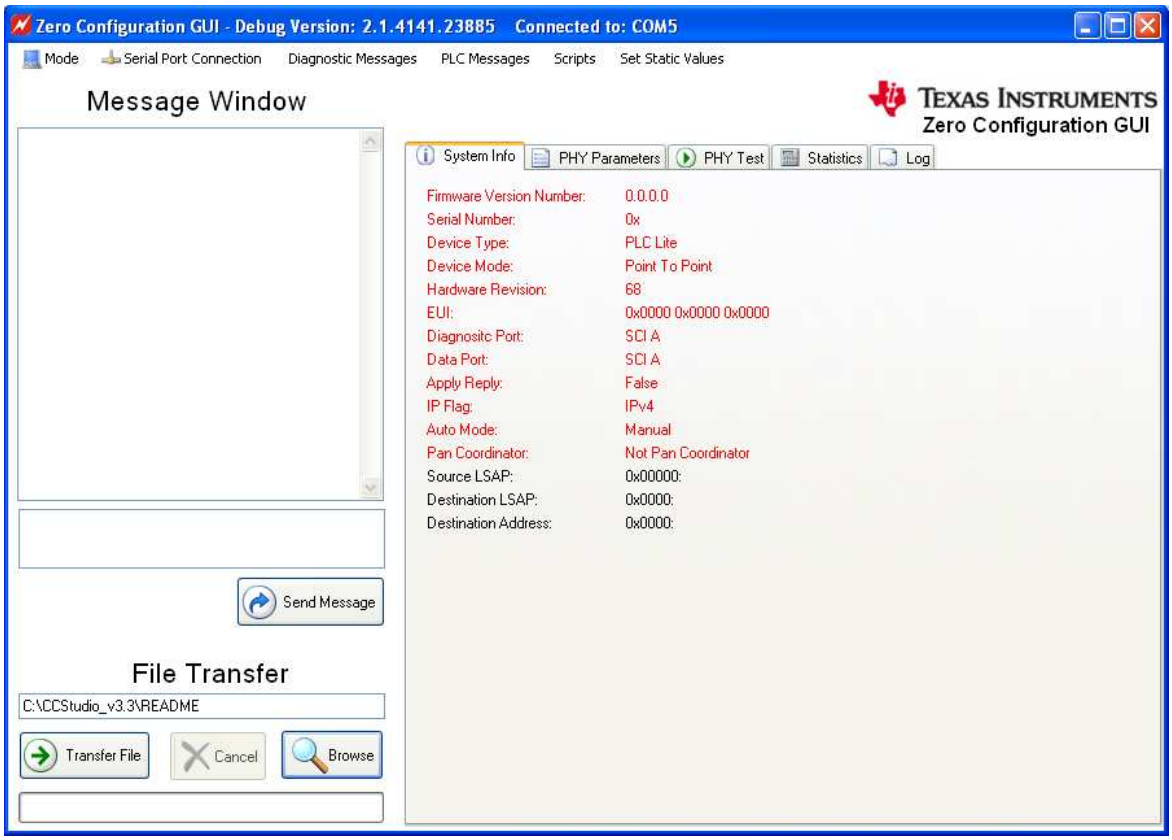

Figure 27. Zero Configuration GUI – File Transfer Window

NOTE: The file location for transmit and receive should be different when using a single PC. The total length of the file name and path should not exceed 80 characters.

After the file is chosen, click on the *Transfer File* button. The zero configuration GUI must control the other PLC.

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When the transfer starts, the GUI displays a progress bar on both zero configuration GUIs. The GUI in Figure 28 is the receiving zero configuration GUI and displays the path and file name where the received file is being copied. The user is not allowed to change the directory path of the received file.

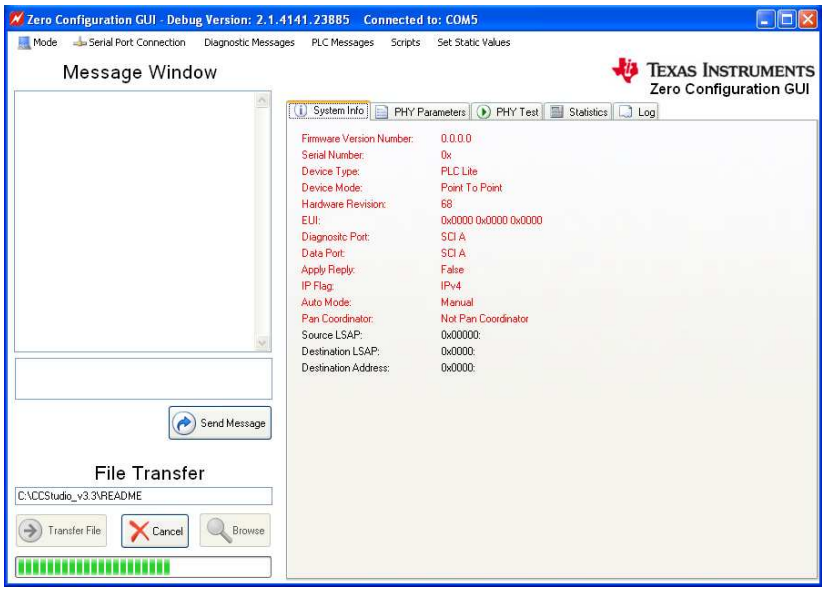

Figure 28. Zero Configuration GUI – File Transferring

When the file transfer is complete, both zero configuration GUIs display the message box shown in Figure 29.

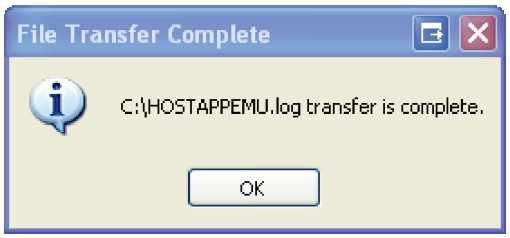

Figure 29. Message Box for File Transfer Complete

If the file transfer fails, the sending GUI displays the message box as shown in Figure 30.

Figure 30. Message Box for Unable to Transfer Files

The user can cancel the file transfer by clicking the *Cancel* button on either GUI.

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8 Using the Intermediate GUI

The intermediate mode is chosen from the *Mode* drop-down menu.

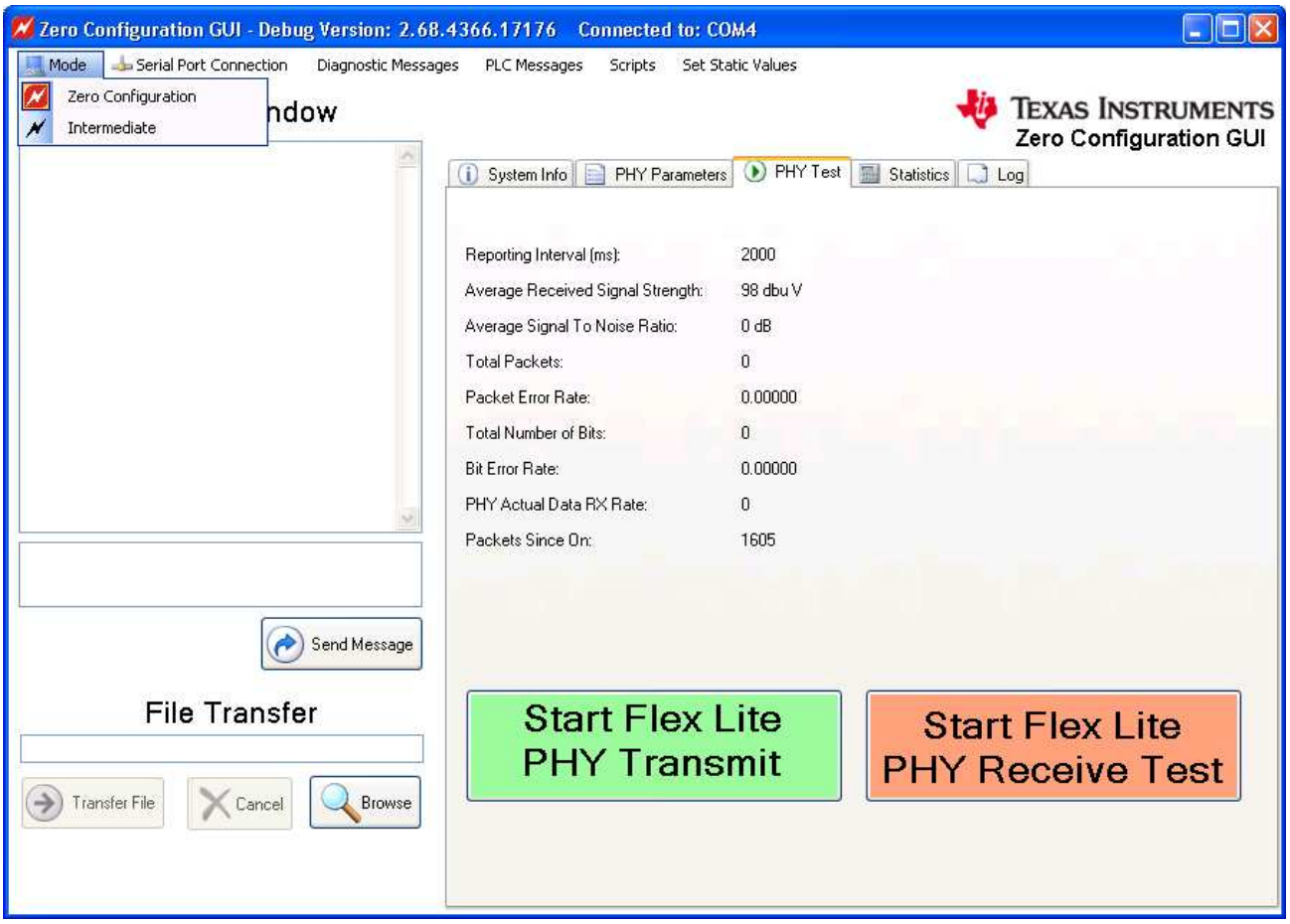

Figure 31. Choosing the Intermediate GUI

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8.1 User Interface

The intermediate GUI consists of the following:

- Main menu: All operations are initiated from the main menu with toolbars and buttons.
- Graphical displays of PHY parameters: PHY parameters configuration (see Figure 32).
  - RSSI graph: Plot is in dBuV, limited between 70 and 98 dBuV.
  - SNR graph: Plot is in dB.
  - Bit error rate graph: Plots of PHY layer bit error rate, one line for each MCS (only applicable to PHY test mode operation).
  - Packet error rate graph: Plots of PHY layer packet error rate, one line for each MCS
- PHY statistics: This panel provides statistics in the physical link.
- Transfer statistics: This panel provides statistics when a file transfer is in operation.
- System information: This panel provides system version information and PHY or MAC configurations.

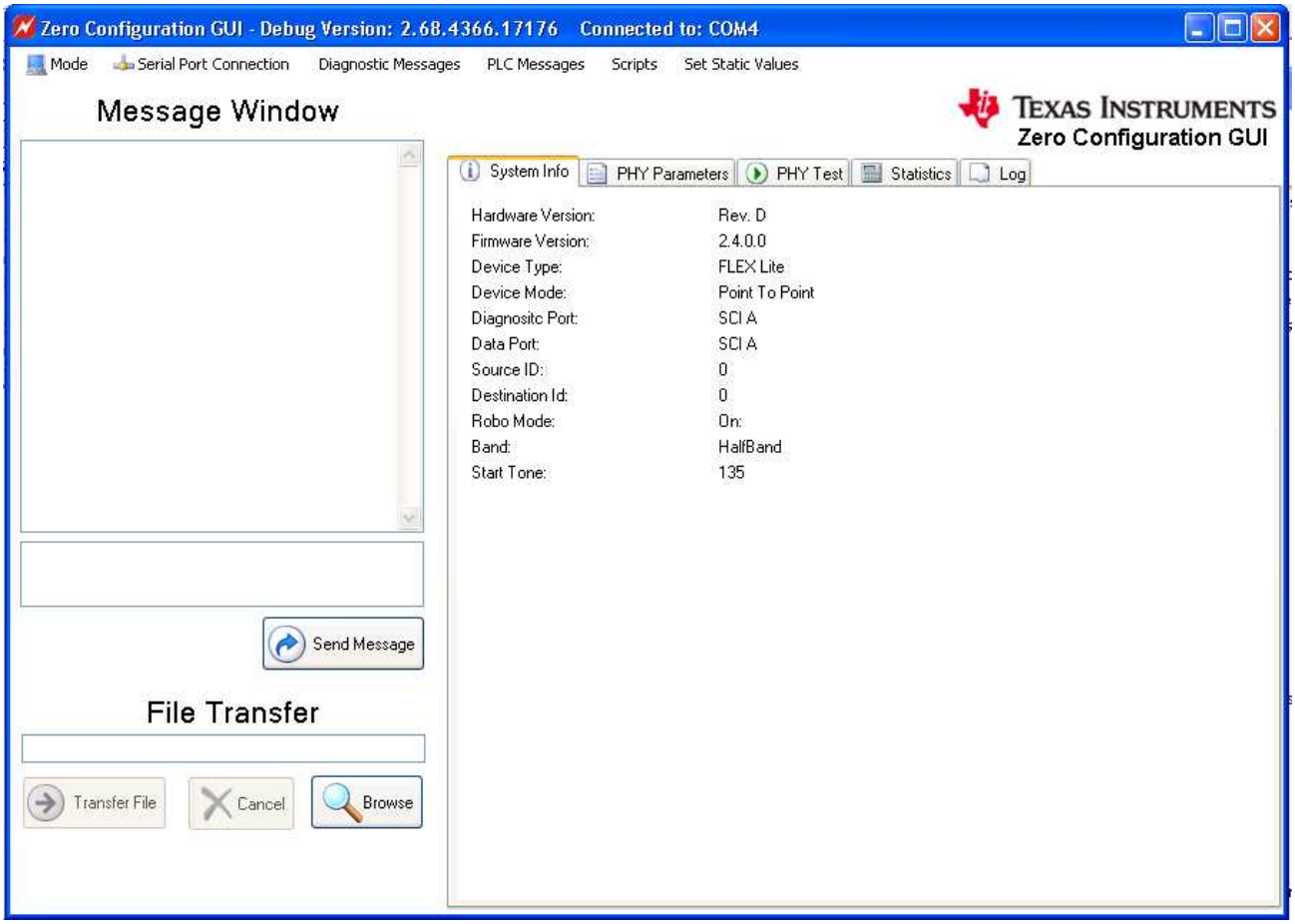

Figure 32. Intermediate GUI – User Interface

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8.2 System Configuration

The system configuration provides a way to configure the PLC-Lite device (*Menu→Options→Set System Config*).

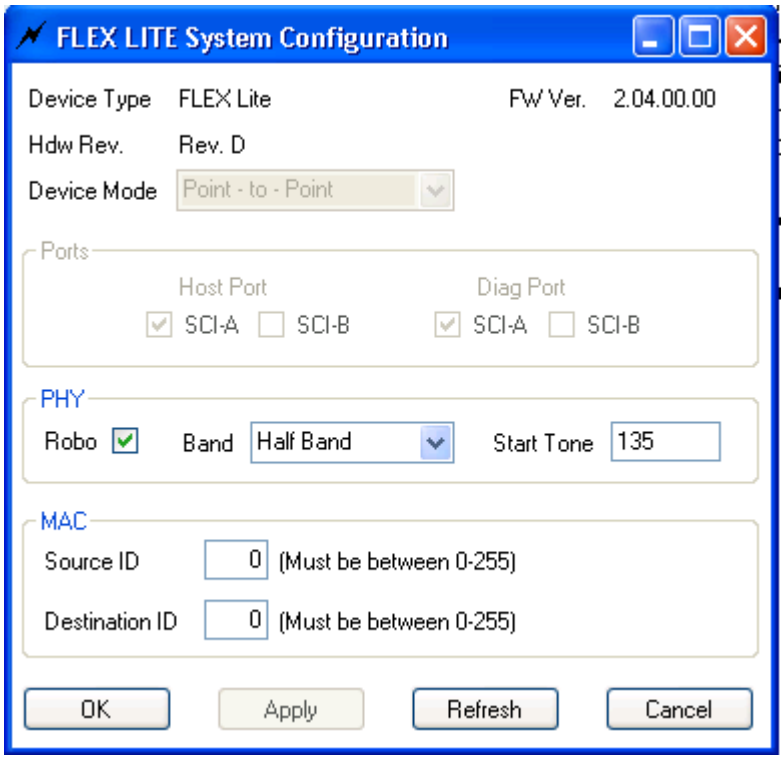

Figure 33. Intermediate GUI – System Configuration

The following describes the configuration settings:

- PHY settings
  - ROBO: Set the PHY mode (ROBO or Non-ROBO)
  - Band: Set the band to Cenelec-A/B/C/D half-band
  - Start tone: Set the start tone index. The start frequency is calculated as (start tone index) × 500 kHz/1024. Examples include:
    - Cenelec-A upper half band (65.9 to 89.3kHz): (start tone index) = 135
    - Cenelec-BC half-band (99.1 to 122.6kHz): (start tone index) = 203
- MAC settings
  - Source ID: MAC ID of the source device
  - Destination ID: MAC ID of the destination device

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8.3 Getting System Information

The *Get System Info* option (*Menu→Options→Get System Info*) retrieves the current system information values from the PLC. These values are represented in the system information view. These values may be set using the *Set System Config* option (*Menu→Options→Set System Config*).

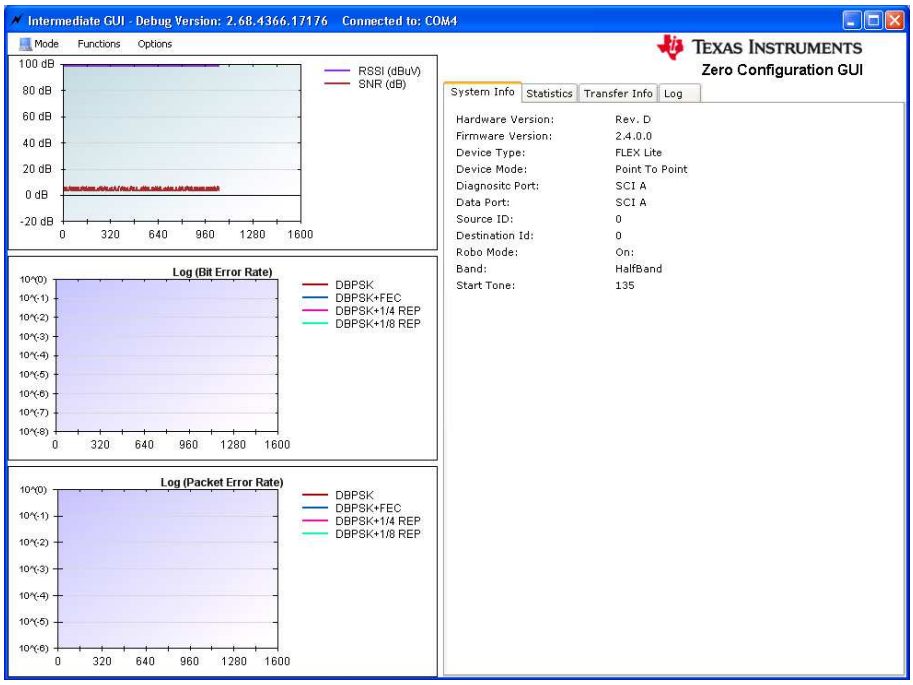

Figure 34. Intermediate GUI – System Information

8.4 Control Setup

The *Control Setup* option (*Menu→Options→Control Setup*) allows the following:

- Channel status update: Select the *Enable Synchronization Parameter* check box for a status display in the statistic window.
- Link quality report update: Select the *Enable Link Quality Report* check box for RSSI, SNR, BER, and PER to display in the *Statistics* window.
- Period between statistics update: Enter the duration (in seconds) in *Report Output Period*.

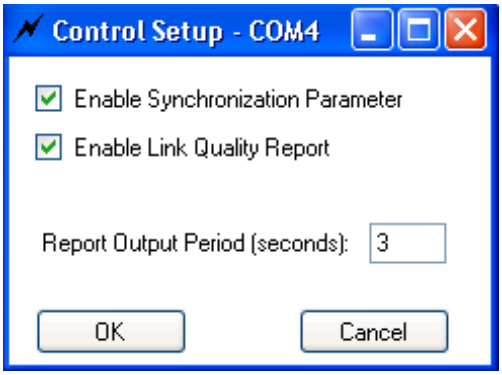

Figure 35. Intermediate GUI – Control Setup

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8.5 Configuring PHY Parameters

The *FLEX LITE PHY Parameters* configuration (*Menu→Options→PHY Parameters*) is used for configuring the PHY TX and RX parameters.

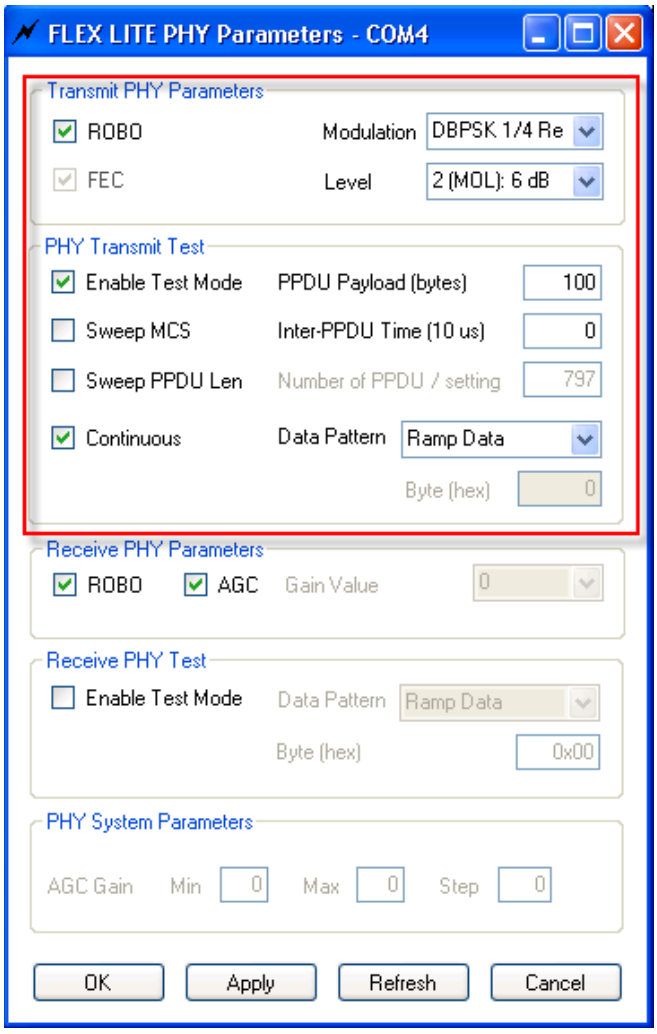

Figure 36. Intermediate GUI: PHY TX Parameters

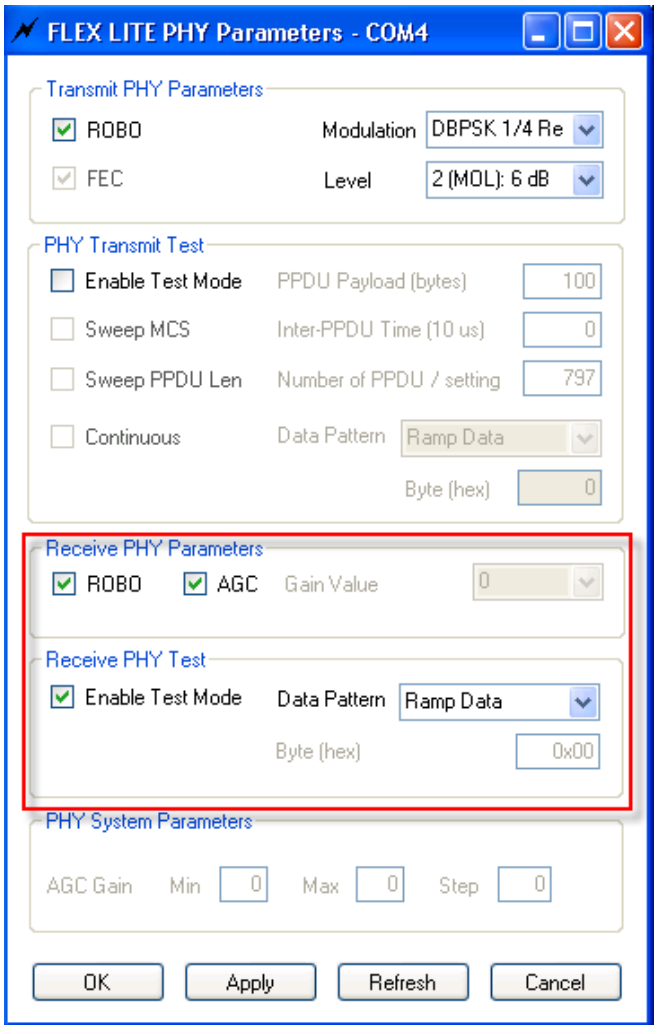

Figure 37. Intermediate GUI: PHY RX Parameters

The following describes the PHY TX parameters that can be configured:

- ROBO: PHY robust mode
- Modulation: DBPSK. If ROBO mode is selected, then DBPSK + 1/4 repetition or DBPS + 1/8 repetition can be selected.
- FEC: ON or OFF. If ROBO mode is selected, this field is not valid since FEC is always on.
- Level: Transmit Level
  - 0: Maximum output level (MOL)
  - 1: MOL – 3 dB
  - 2: MOL – 6 dB
  - 3: MOL – 9 dB
  - 4: MOL – 12 dB
  - 5: MOL – 15 dB
  - 6: MOL – 18 dB
  - 7: MOL – 21 dB

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The following describes the PHY TX parameters that can be configured for PHY TX test mode only:

- Test mode: When enabled, this mode configures the transmitter in test mode and transmits a fixed data pattern (selected in the data pattern box) for BER testing.
- Sweep PPDU length: When enabled, the test will sweep through all valid PPDU length in increasing order for the modulation used.
- Continuous: When enabled, the test will continuously transmit PPDUs as specified. When disabled, the test will transmit the “number of PPDUs per setting” as specified and stop.
- Data pattern: When PHY test mode is enabled, the data pattern for the packet payload to be transmitted can be selected. The following data patterns are available:
  - A ramp data pattern from 0 to 255
  - A fixed data byte set by octet value. The data pattern is repeated for the duration of the payload

NOTE: This field will be ignored when the sweep PPDU length is selected.

- Inter-PPDU time: The gap time between PPDU is in units of 10 microseconds.
- Number of PPDUs per setting: The number of PPDU per setting during a PPDU length sweep.

The following describes the PHY RX parameters that can be configured:

- Automatic gain control (AGC): If selected, the receiver performs AGC. If unselected, manual gain setting is used. Valid gain values are from 0 to 7 with step of 6 dB.

The following describes the PHY RX parameters that can be configured in PHY RX test mode only:

- Test mode: When enabled, the receiver compares to the receive packet using the data pattern selected and computes BER for BER testing.
- Data pattern: When test mode is enabled, this parameter can select the data pattern used for comparison in computing BER. A ramp data pattern from 0 to 255 or a fixed data byte set by octet value.

NOTE: This pattern should be identical to the selection in the transmitter for valid BER result.

The following describes the PHY system parameters:

- AGC gain min: Minimum AGC gain in dB
- AGC gain max: Maximum AGC gain in dB
- AGC gain step: Step size of AGC in dB

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8.6 Testing PHY Performance

The PHY performance can be tested in a point-to-point configuration where the system configuration steps described in Section 7.6 should be used. One modem must be configured as a transmitter in test mode and the other modem as a receiver in test mode (*Menu→Options→PHY Parameters*). The hardware should be set up as described in Section 6. Figure 38 shows an example of PHY test with DBPSK+FEC, transmitting at a level of 6 dB, PPDU length of 100 bytes, and an inter-PPDU interval of 0 ms in continuous mode.

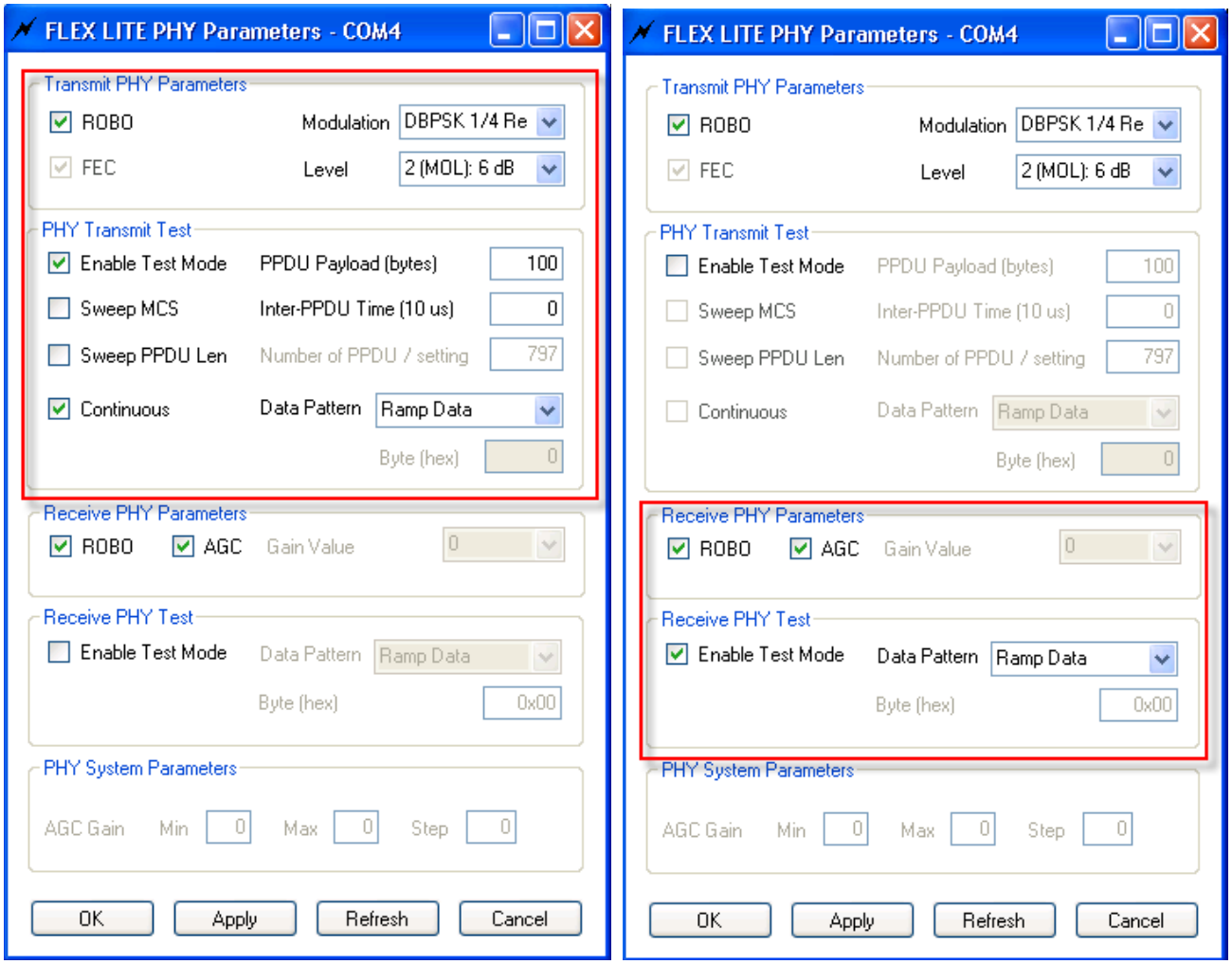

Figure 38. Intermediate GUI – PHY TX and RX Test Mode Setup

NOTE: This example does not support concurrent bi-directional data transfer.

By enabling the channel status and link quality report and setting report period (as described in Section 7.5), the PHY performance (SNR, RSSI, PER, and BER) will be displayed in the graphs and the statistics will be displayed in the statistics panel.

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8.7 Sending and Receiving Message

The *Send Message* function (*Menu→Function→Send Message*) sends a small text message from one device to another in point-to-point configuration. The function is intended to test and verify communication between the two systems in a point-to-point configuration. To specify an ID for both TX and RX stations, if the user is using more than one kit to establish a network, select *Set System Config* in the *Options* menu. If the user is only using one kit for point-to-point test, ignore this step.

For the RX station, Source ID is the RX ID, Destination ID is the TX ID. For the TX station, Source ID is the TX ID, Destination ID is the RX ID. For more information, refer to Section 8.2. When this option is selected, the user may fill in a message and press send, and the other host will display the message (see Figure 39).

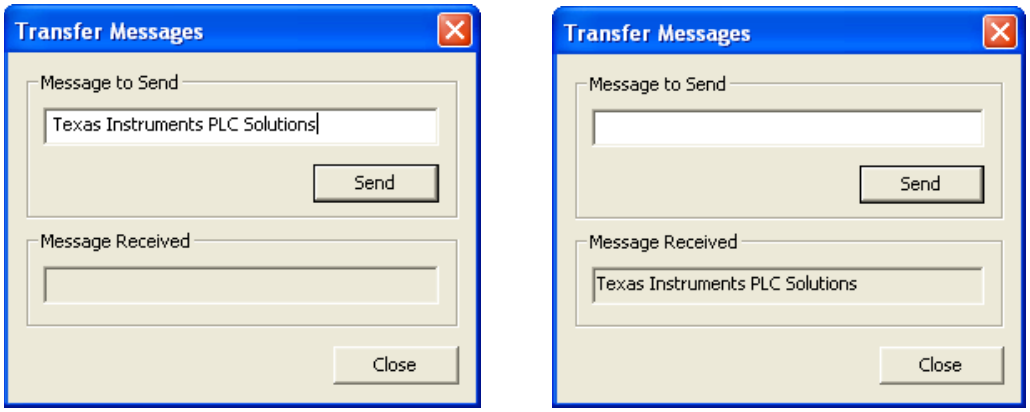

Figure 39. Intermediate GUI – Message Sending

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8.8 Sending and Receiving Files

The *Send File* function (*Menu→Function→Send File*) sends a file from one device to another in a point-to-point configuration. This function is not a guaranteed error-free delivery (the file received may have dropped packets) and is a means to push data from one board to another. The receiver will note both the payload CRC and missing packet errors and will attempt to notify the sender of these errors.

To specify an ID for both TX and RX stations, if the user is using more than one kit to establish a network, select *Set System Config* in the *Options* menu. If the user is only using one kit for point-to-point test, ignore this step.

For the RX station, Source ID is the RX ID, Destination ID is the TX ID. For the TX station, Source ID is the TX ID, Destination ID is the RX ID. For more information, see Section 8.2.

Once the file transfer begins, a file transfer status window is displayed (Figure 40), and the *Transfer Information* section reflects transfer statistics (Figure 41).

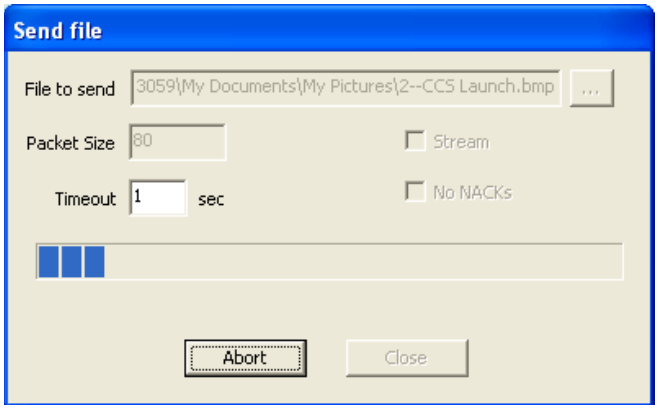

Figure 40. Intermediate GUI – File Transferring

Figure 41. Intermediate GUI – File Transferring Statistics

Statistics may be cleared by selecting *File→New* or by pressing the *New File* button. Either the sender or receiver can abort the transfer. The sender may abort by pressing the *Abort* button, and the receiver may abort by selecting the menu option *Functions→Abort File Receive*.

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9 PLC-Lite Hardware Resource Usages

Table 1. PLC-Lite GPIO Pins Configurations

GPIO PIN	CONNECTED TO	PLC-LITE BUILD USAGE
GPIO00		
GPIO01	TP	
GPIO02		
GPIO03	TP	
GPIO04	TP	
GPIO05		
GPIO06	AFE	
GPIO07	AFE	AFE031 DAC
GPIO08	AFE	
GPIO09		
GPIO10		
GPIO11		
GPIO12	AFE	AFE031 SD
GPIO13		
GPIO14		
GPIO15		
GPIO16	SPI (SPISIMOA)	AFE031
GPIO17	SPI (SPISOMIA)	AFE031
GPIO18	SPI (SPICLK)	AFE031
GPIO19	SPI (SPISTEA)	AFE031
GPIO20		
GPIO21		
GPIO22		
GPIO23		
GPIO24		
GPIO25		
GPIO26		
GPIO27		
GPIO28	SCI (SCIRXDA)	UART host port
GPIO29	SCI (SCITXDA)	UART host port
GPIO30		
GPIO31	LED2	System heart beat
GPIO32	(I2C) SDAA	
GPIO33	(I2C) SCLA	
GPIO34	LED1	Blink during TX and RX

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Table 2. PLCLite Peripherals and Interrupts Usage

PERIPHERALS	PLC-LITE BUILD USAGE	INTERRUPT
32-Bit CPU Timers		
Timer 0	TX delay	PIE1.7
Timer 1	Absolute timer (PLC-Lite PHY time stamp)	
Timer 2	Statistics report	
Watchdog Timer (Unused)		
ADC		
ADCINA0	RX ADC samples	PIE1.1
ADCINA2	Reserved	
ADCINA4	Reserved	
SCI		
SCIA	Host port	PIE9.1—RX PIE9.2—TX
SPI		
SPIA	AFE031	
I2C	Interface to EEPROM	
EPWM		
EPWM1	ADC trigger	PIE3.7
EPWM2	ADC trigger	
EPWM6	CSMA timer	
EPWM7	TX samples	
EQEP1	PHY TX task	PIE5.1
LVF	PHY RX task	PIE12.7

Table 3. PLC-Lite Flash Configurations and Usage

SECTORS	SIZE (WORDS)	PLC-LITE BUILD USAGE
ABC	24 K	PLC-Lite code: 20.6-K words
D	8 K	0
E	8 K	0
F	8 K	0
G	8 K	0
H	8 K	PHY algorithm code: 600 words

Table 4. PLC-Lite System Memory and MIPs Usage

MEM/MIPS	BENCHMARK
Flash	21.2-K words
RAM	8.7-K words
MIPS	Average: 45 MIPS Peak: 58 MIPS

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10 PHY Example Project

The PHY example project demonstrates the use of PHY library APIs when hardware is setup with two devices connected via power line. One device sends one packet, waits for one receive packet, and then transmits another packet. This process alternates between TX and RX. The packet size is 40 bytes with a repeating ramp data pattern using the following:

- ROBO mode: Non-ROBO
- Modulation: DBPSK with FEC enabled
- Transmit level: 3

NOTE: The user must have Code Studio Composer (CCS) 5.5 installed to compile the project.

Follow these steps to complete the PHY example project:

1. Unzip ti_PLC-Lite_phy_example.zip.
2. In CCS, import PHY test project test_tx_rx from the following directory: \dsp_28x\plc_lite\src\phy\test\test_tx_rx_swi\.
3. Skip this step if the user doesn't want to re-build the project and re-use the binary file from the delivered package. In CCS, select the Debug_AFE031_HB configuration, and build the project. The build should produce the following binary file:
   - \dsp_28x\plc_lite\src\phy\test\ test_tx_rx_swi\Debug_AFE031_HB\phy_tx_rx.out
4. In CCS, select the target configuration and connect target.
5. In CCS, load test_tx_rx.out.
6. In CCS, run the target to execute the code and LED flashes. The user may also disconnect the debugger and power cycle the board to execute the code.
7. Load the same code to the second board.
8. Connect the two boards via power line cables. After the code in the second board start to execute, both boards should alternate between RX and TX and the LEDs should blink.

10.1 Source File Description

- Test bench
  - Project file: located in \dsp_28x\plc_lite\src\phy\test\ test_tx_rx_swi\
  - Test bench: test_tx_rx.c demonstrates alternating PLC-Lite PHY TX and PHY RX using provided PHY library
  - Linker command: 28035_FLASH_lnk.cmd
  - Test example for flash
- Header files
  - PHY common: phy.h
  - PHY TX: phy_tx.h
  - PHY RX: phy_rx.h
  - HAL: hal_afe.h
  - Chip support library header files
- Libraries
  - PHY lib: phy_lin_hb.lib
  - HAL lib: hal_afe031_f2803x_hb.lib
  - Chip support lib: csl_f2803x.lib

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10.2 PHY Library Demonstration

The example of a PHY library project demonstrates packet transmission and reception at the physical layer in a TDD fashion.

1. Flash two F28035 boards with PHY library example executable.
2. Connect via power line.
3. Sequence of operation:
   - Board A sends a packet.
   - Board B receives packet and sends a packet back to Board A.
     - These steps will repeat.
   - LEDs on the DSP control card will blink if the packet continues to transmit and receive.

10.3 Hardware Resource Usage

The PHY library uses the following hardware resources:

- ADC
  - ADCINA0: PLC Receive
- CPU timers
  - CPU Timer 0: PHY timer
  - CPU Timer 1: PLC-Lite PHY system timer, 20 bits in 10-us increments
  - CPU Timer 2: Statistics report timer
- CPU Timers
  - EPWM1: ADC trigger
  - EPWM2: ADC trigger
  - EPWM6 Timer: CSMA/CA timer
  - EPWM7 Timer: PHY TX sampling (2 us)
- GPIO Peripherals
  - GPIO 7: AFE DAC select
  - GPIO 12: AFE SD
  - GPIO 16: SPISIMOA
  - GPIO 17: SPISOMIA
  - GPIO 18: SPICLKA
  - GPIO 19: SPISTEA
  - GPIO 28: SCIRXDA
  - GPIO 28: SCITXDA

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10.4 PHY Library Test Bench Steps

1. Initialize hardware (using F28035 specifics).
2. Configure flash.
3. Install ISR:
   - Timer 0 (HAL_afe_cpuTimer0_isr)
   - EPWM7 Timer (HAL_afe_pwm7Timer_isr)
   - ADCINT1 (HAL_afe_adc_isr)
   - PHY TX task and PHY RX task (PLC_LITE_tx_swi, PLC_LITE_rx_swi)
4. Initialize AFE:
   - HAL_afeInit
5. Initialize PHY library:
   - PHY_txInit
   - PHY_rxInit
6. Generate packet to transmit.
7. Start PHY RX to listen to the line.
   - PHY_rxStart (0xFFFF, cb_ppdu)

NOTE:
- Call back for PHY_rxStart - cb_ppdu.
- If status succeeds, do some processing if needed and release a buffer back to PHY:
  - PHY_rxPpduRelease
  - LED toggle
  - rxppdu_done = 1

8. Start the first packet transmission.
   - PHY_txPpdu (&PHY_tx_ppdu_s, cb_tx);

NOTE:
- Call back for PHY_txPpdu - cb_tx.
- If status succeeds, do some processing if needed:
  - LED toggle

9. Enable system interrupt.
10. Repeat the main loop.

10.5 ISR Descriptions

- CPU Timer 0 ISR
- EPWM7 Timer ISR
  - Interrupts every 2 µs
  - Every interrupt transmit one sample
  - Once symbol is finished, set txSymbDone
  - Once symbol is finished, trigger TX SWI
- ADC Channel ISR
  - Interrupt every 8 µs
  - Every interrupt process four samples
  - Once symbol is finished, set afeReadyFlag
  - Once symbol is finished, trigger RX SWI

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10.6 SWI Descriptions

- PLC_LITE_tx_swi—Start TX state machine run
  interrupt void PLC_LITE_tx_swi()

  {
  txSymbDone = 0;
  PHY_txSmRun();
  }
- PLC_LITE_rx_swi—Start RX state machine run

  {
  afeReadyFlag = 0;
  PHY_rxSmRun();
  }

10.7 Main Loop

When the RX package is finished, start another packet transmission.

```
While(1)
{
if (rxppdu_done == 1)
{
rxppdu_done = 0;
PHY_txPpdu(&PHY_tx_ppdu_s, cb_tx);
}
}
```


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11 User Application Integration Guide

The following serves as a guideline when integrating with user applications:

- Carefully arrange user-peripheral and hardware resources to avoid any conflict with PLC-Lite. The PLC-Lite PHY resource usage is listed in Section 9.
- Follow the PHY example project in Section 10 to see the initialization sequence and PLC-Lite PHY, HAL, and CSL library API usages.
- PLC-Lite PHY sampling rates:
  - TX: 500 kHz, through EPWM7 timer
  - RX: 500 kHz, through EPWM1 and EPWM2 triggered ADCIN0
- The following are critical interrupts for the PLC-Lite PHY to operate properly:
  - TX sampling interrupt: PIE group 3 (PIE3.7) occurs every 2 µs, and each interrupt takes 40 to 50 cycles or approximately 29 MIPS;
  - RX sampling interrupt: PIE group 1 (PIE1.1) occurs every 8 µs, and each interrupt takes 110 to 160 cycles or approximately 17 MIPS;
  - TX symbol interrupt: PIE group 5 (PIE5.1) occurs every 2.048 to 2.24 ms, and each interrupt takes approximately 64,000 cycles or 28 MIPS;
  - RX symbol interrupt: PIE group 12 (PIE12.7) occurs every 2.048 to 2.24 ms, and each interrupt takes approximately 78,000 cycles or 35 MIPS.
- (Optional) If UART is enabled: PIE group 9 (PIE9.1, PIE9.2).
- When the user application uses interrupts:
  - User interrupts should use PIE groups with a lower priority than the PLC-Lite PHY sampling interrupts.
  - If the user's interrupt timings are critical, those interrupts should have a higher priority than the PLC-Lite PHY symbol interrupts.
  - Always enable nested interrupts in user ISR by adding “EINT” at the beginning of the user ISR.
- All of the previous interrupt configurations are open to users in the HAL library. Should the user need to re-configure interrupts, their priorities should be in the following order:
  1. RX sampling interrupts
  2. TX sampling interrupts
  3. User interrupts
  4. TX symbol interrupts
  5. RX symbol interrupts

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12 Design Files

12.1 Schematics

To download the schematics. see the design files at TIDM-SOMPLC-INDUSTRIAL-CENELEC.

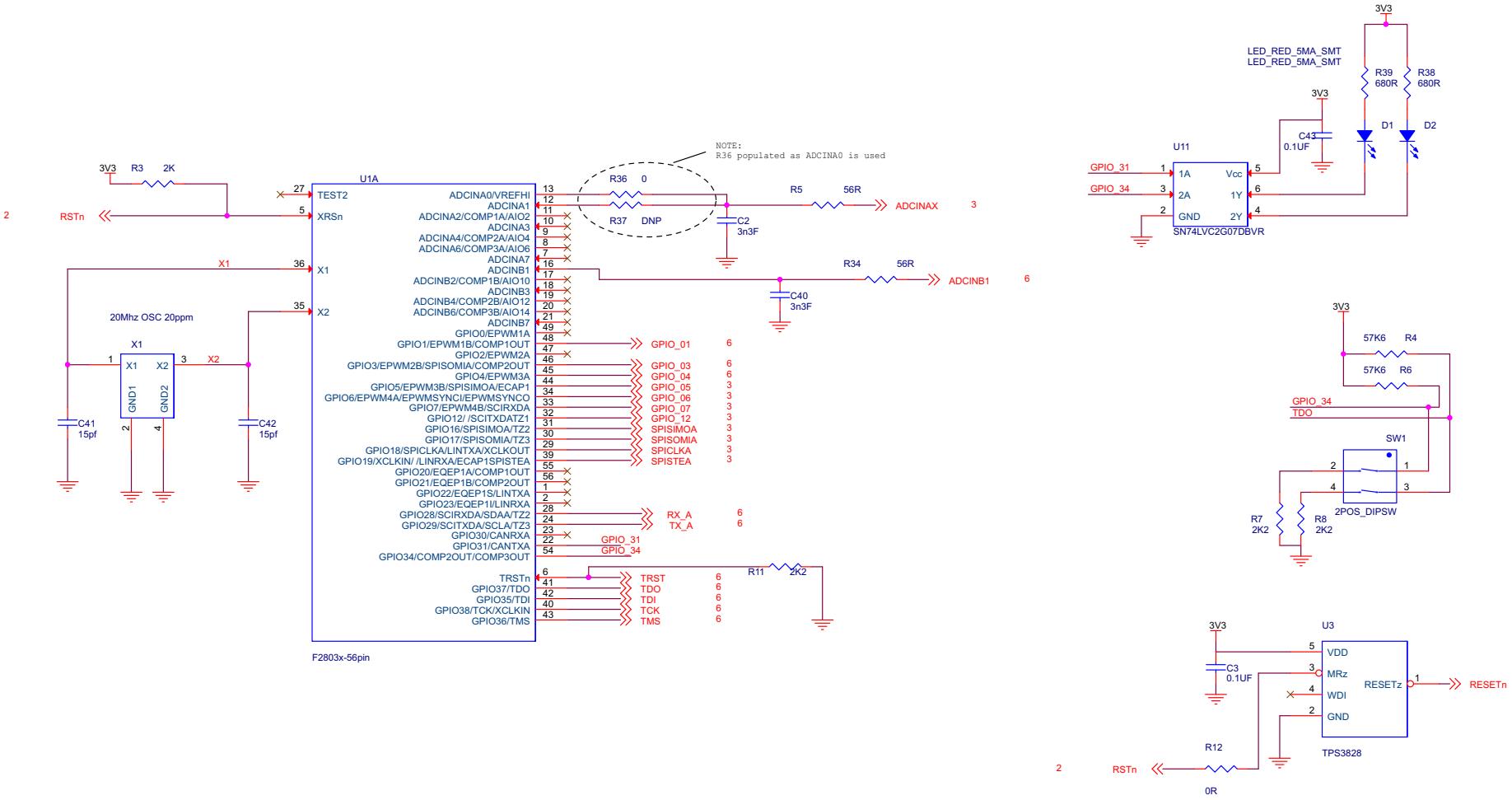

Figure 42. MCU Schematic

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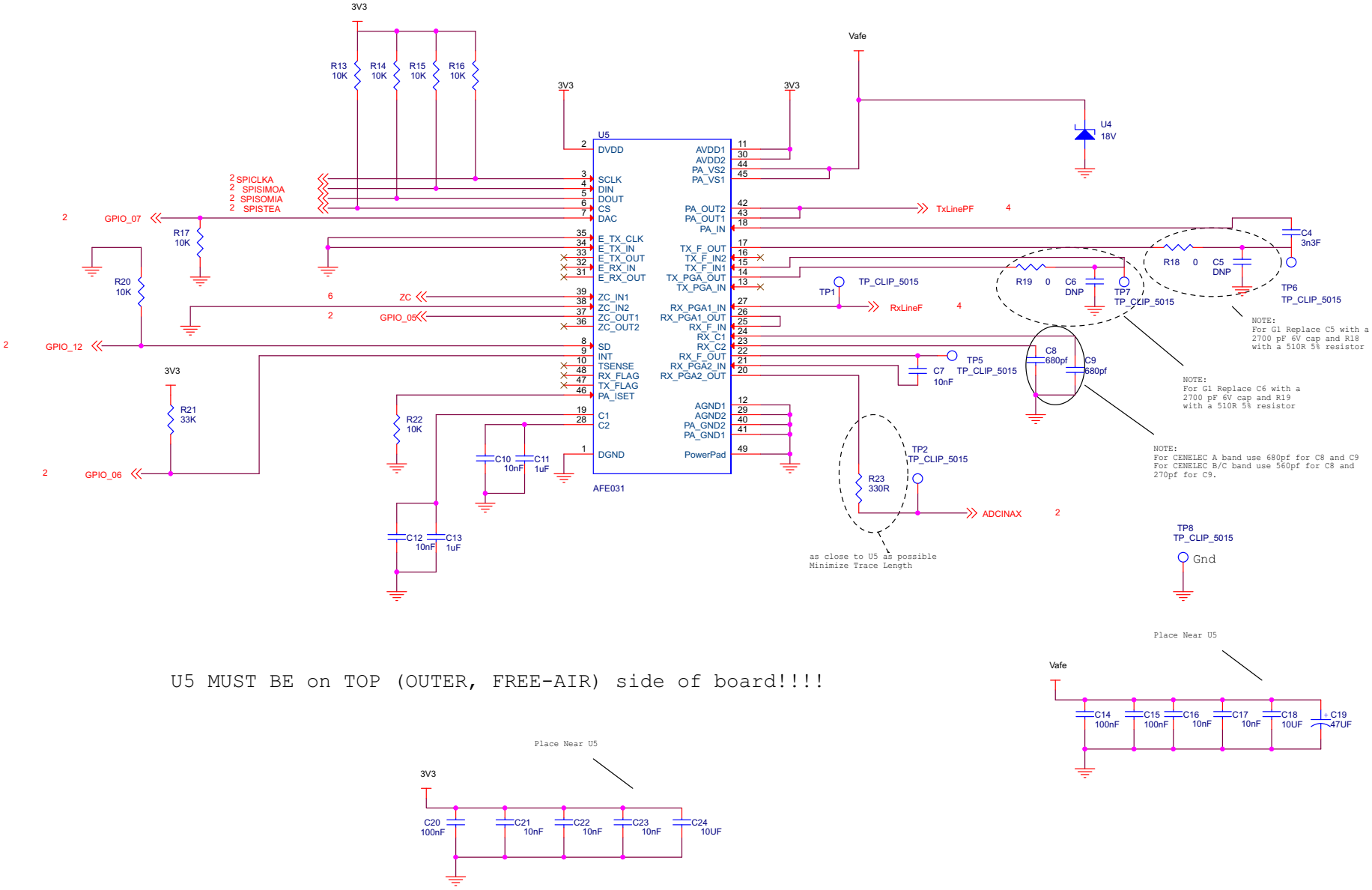

Figure 43. AFE031 Schematic

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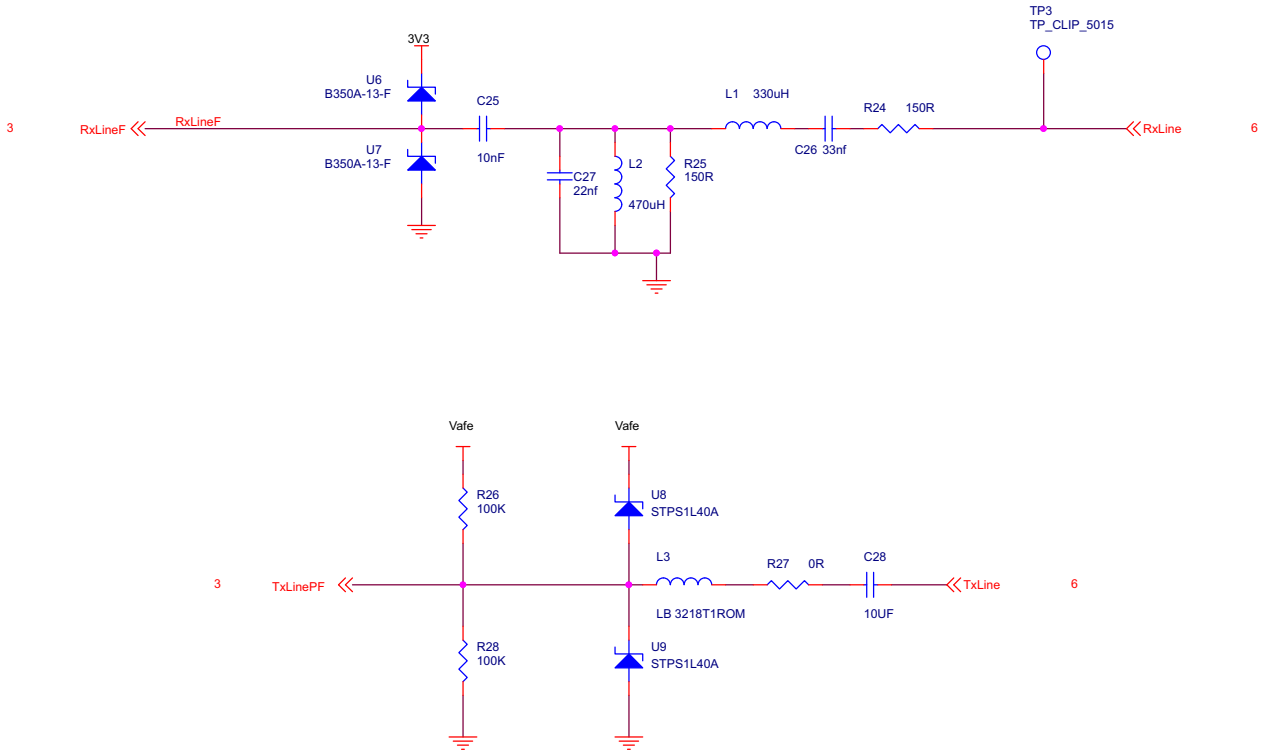

Figure 44. AFE1 (Passive RX Filter) Schematic

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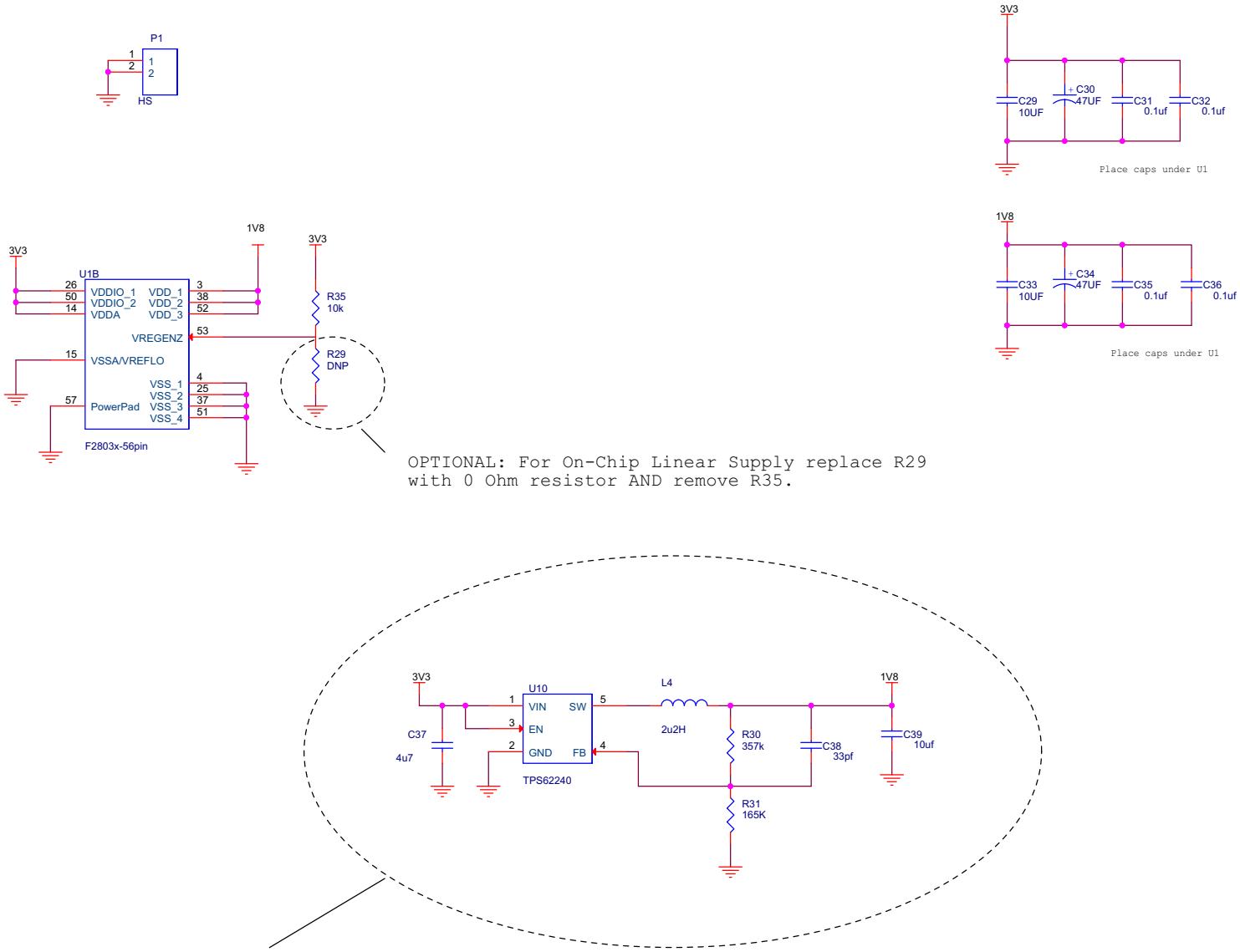

Figure 45. Power Schematic

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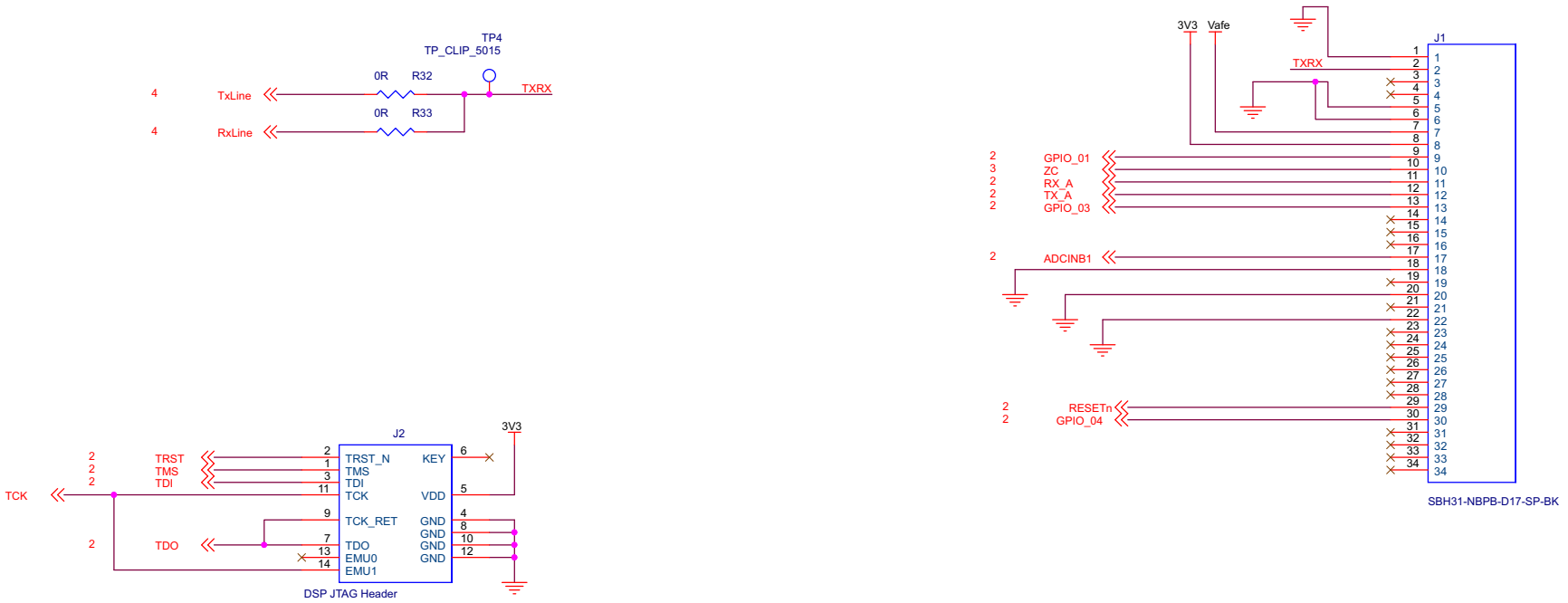

Figure 46. Connector Schematic

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12.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-SOMPLC-INDUSTRIAL-CENELEC.

Table 5. BOM

ITEM #	QTY	PART #	PART TYPE	PART REF	VENDOR	VENDOR PN	DESCRIPTION	VALUE	PCB FOOTPRINT	TOLERANCE	DISTRIBUTOR	DISTRIBUTOR PN
1	2	300-00017	CAP	C2, C40			Cap Ceramic 10 V, SMT 0402	3n3F	C0402	0		
2	2	100-00003	CAP	C3, C43	AVX	0603YC104KAT*A	Capacitor,0.1UF,16 V,10 %,X7R,0603	0.1 µF	C0603	10%	Digikey	478-1239-2-ND
3	1	300-00038	CAP	C4	Panasonic	ECH-U1H332JX5	CAP .0033 µF 50 V PPS FILM 1206 5%	3n3F	C1206	0	Digikey	PCF1334CT-ND
4	2	300-00057	CAP	C5, C6			Cap Ceramic SMT 0402	DNP	C0402	0		
5	1	300-00013	CAP	C7			Cap Ceramic 10 V, SMT 0402	10 nF	C0402	0		
6	2	300-00085	CAP	C8, C9	Yageo	CC0805KRX7R9BB681	CAP 680 pF 50 V CERAMIC X7R 0805	680 pf	C0805	0	Digikey	311-1126-1-ND
7	5	300-00040	CAP	C10, C12, C21, C22, C23	Murata	GRM188R71C103KA01D	CAP CER 10000 pF 16 V 10% X7R 0603	10 nF	C0603	0	Digikey	490-1525-2-ND
8	2	300-00036	CAP	C11, C13	Taiyo Yuden	UMK107BJ105KA-T	Cap Ceramic 50 V, SMT 0603	1 µF	C0603	0	Digikey	587-2400-1-ND
9	2	300-00041	CAP	C14, C15	Murata	GRM155F51E104ZA01D	CAP CER .1 µF (100 nf) 25 V Y5V 0402	100 nF	C0402	0	Digikey	490-3271-1-ND
10	2	300-00043	CAP	C16, C17	Murata	GRM188R71E103KA01D	CAP CER 10000 PF (10 NF) 25 V 10% X7R 0603	10 nF	C0603	0	Digikey	490-1520-1-ND
11	2	300-00039	CAP	C18, C28	Taiyo Yuden	GMK316F106ZL-T	Cap Ceramic 35 V, SMT 1206	10 µF	C1206	0	Digikey	587-1352-1-ND
12	1	300-00042	CAP	C19	TDK	C5750Y5V1E476Z	CAP CER 47 µF 25 V Y5V 2220	47 µf	C2220	0	Digikey	445-3486-2-ND
13	1	300-00014	CAP	C20	Kemet Electronics Corporation	C0402C104K8PACTU	Cap Ceramic 10 V, SMT 0402	100 nF	C0402	0	Digikey	399-3027-2-ND
14	1	300-00008	CAP	C24	Panasonic	ECJ-2FB0J106M	Capacitor,10UF,6.3 V,20 %, X5R,	10 µF	C0805	0.2		
15	1	300-00037	CAP	C25	AVX	06035C103KAT2A	Cap Ceramic 50 V, SMT 0603	10 nF	C0603	0	Digikey	478-1227-1-ND
16	1	300-00028	CAP	C26			Cap Ceramic SMT 0402	33 nF	C0402	0		
17	1	300-00026	CAP	C27			Cap Ceramic SMT 0402	22 nF	C0402	0		
18	2	300-00011	CAP	C29, C33	Panasonic	ECJ-1VB0J106M	CAP CERAMIC 10 µF 6.3 V X5R 0603	10 µF	C0603	20%	Digikey	rPCC2395CT-ND

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Table 5. BOM (continued)

ITEM #	QTY	PART #	PART TYPE	PART REF	VENDOR	VENDOR PN	DESCRIPTION	VALUE	PCB FOOTPRINT	TOLERANCE	DISTRIBUTOR	DISTRIBUTOR PN
19	2	300-00012	CAP	C30, C34	Vishay	298D476X0010P2T	CAP TANT 47 µF 10 V 20% 0805	47 µF	C0805P	0	Digikey	718-1608-1-ND
20	4	300-00044	CAP	C31, C32, C35, C36	Murata	GRM155R61A104KA01D	CAP CER .1 µF 10 V 10% X5R 0402	0.1 µF	C0402	0	Digikey	490-1318-1-ND
21	1	300-00063	CAP	C37	TDK	C1005X5R0G475K	CAP CER 4.7 µF 4.0V X5R 10% 0402	4u7	C0402	0	Digikey	445-5949-1-ND
22	1	300-00062	CAP	C38	Johanson Dielectrics Inc	250R07S330JV4T	CAP CER 33 pF 25 V S 0402 UHI Q	33 pF	C0402	0	Digikey	712-1298-1-ND
23	1	300-00064	CAP	C39	TDK	C1608X5R0J106M	CAP CER 10 µF 6.3 V X5R 20% 0603	10 µF	C0603	0	Digikey	445-4112-1-ND
24	2	300-00056	CAP	C41, C42	Murata	GRM1555C1H150JZ01D	CAP CER 15 pF 50 V 5% C0G 0402	15 pF	C0402		Digikey	490-1280-1-ND
25	2	200-00010	FET_DIODE	D1, D2	Panasonic	LNJ208R8ARA	LED, RED, 3.0 VR, 0.2 IF,SURF. MOUNT	LED_RED_5MA_SMT	LED0603H35			
26	1	320-00013	CONN	J1	Sullins Connector Solutions	SBH31-NBPB-D17-SP-BK	CONN HDR 1.27 mm 34POS GOLD SMD	SBH31-NBPB-D17-SP-BK	male	0	Digikey	S9108-ND
27	1	120-00068	CONN	J2	SAMTEC	TSM-107-01-S-DV	CONN. 2×7 Header, SMT, DSP JTAG, Pin 6 removed	DSP JTAG Header	hdr_14p	0		
28	1	330-00009	MAGNETICS	L1	Panasonic - ECG	ELJ-EA331KF	Inductor 330 uH 10% 1210 SMD	330 uH	IND1210	0	Digikey	PCD1432CT
29	1	330-00010	MAGNETICS	L2	Taiyo Yuden	CB2518T471K	Inductor Power 470 uH 1007	470 uH	IND0805	0	Digikey	PCD1432CT
30	1	330-00011	MAGNETICS	L3	Taiyo Yuden	LB3218T1R0M	INDUCTOR 1.0UH 1.075A 20% SMD	LB 3218T1ROM	IND0805	0	Digikey	587-2194-1
31	1	330-00021	MAGNETICS	L4	TDK	GLCR2012T2R2M-HC	INDUCTOR 2.2UH 350MA 20% 0805	2u2H	IND0805	0	Digikey	445-3625-1-ND
32	1	490-00002	Heat_Sink	P1			Heat slug for PLC Module V4	HS	custom	0		
33	1	310-00043	RES	R3			Resistors 2 K 5% - SMD, 0402	2 K	R0402	0		
34	2	310-00044	RES	R4, R6			Resistors 57K6 5% - SMD, 0402	57K6	R0402	0		
35	2	310-00041	RES	R5, R34			Resistors 56 R, 5% - SMD, 0402	56 R	R0402	0.05		

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Table 5. BOM (continued)

ITEM #	QTY	PART #	PART TYPE	PART REF	VENDOR	VENDOR PN	DESCRIPTION	VALUE	PCB FOOTPRINT	TOLERANCE	DISTRIBUTOR	DISTRIBUTOR PN
36	3	310-00045	RES	R7, R8, R11			Resistors 2K2 5% - SMD, 0402	2K2	R0402	0		
37	4	310-00029	RES	R12, R27, R32, R33			Resistors, 0 R, 5% - SMD, 0402	0 R	R0402	0		
38	7	310-00049	RES	R13, R14, R15, R16, R17, R20, R22			Resistor 10 K 5% - SMD,0402	10 K	R0402	0		
39	2	310-00102	RES	R18, R19	Panasonic - ECG	ERJ-2GE0R00X	RES 0.0 Ω 1/10 W 0402 SMD	0	R0402	0	Digikey	P0.0JCT-ND
40	1	310-00067	RES	R21			Resistor 33 K 5% - SMD,0402	33 K	R0402	0		
41	1	310-00063	RES	R23	vishay	CRCW0402330RJNED	RES 330 Ω 1/16 W 5% 0402 SMD	330 R	R0402	0	Digikey	541-330JCT-ND
42	2	310-00051	RES	R24, R25			Resistor 150 R 5% - SMD,0402	150 R	R0402	0		
43	2	110-00179	RES	R26, R28	Panasonic	ERJ-3GEYJ104V	Resistor,100K, 0.1 W, 5%, 0603	100 K	R0603	0.05	Digikey	P100KGTR-ND
44	2	310-00030	RES	R29, R37			Resistors, DNP - SMD, 0402 (DNP)	DNP	R0402	0		
45	1	310-00090	RES	R30	Panasonic	ERJ-2RKF3573X	RES 357 KΩ 1/10 W 1% 0402 SMD	357 k	R0402	0	Digikey	P357KLCT-ND
46	1	310-00091	RES	R31	Panasonic	ERJ-2RKF1653X	RES 165 KΩ 1/10 W 1% 0402 SMD	165 K	R0402	0	Digikey	P165KLCT-ND
47	1	310-00104	RES	R35	Panasonic	ERJ-2GEJ103X	RES 10 KΩ 1/10 W 5% 0402 SMD	10 k	R0402	0	Digikey	P10KJTR-ND
48	2	310-00011	RES	R38, R39			Resistors, 680 R, 5% - SMD, 0603	680 R	R0603	0.05		
49	1	206-00010	SWITCH	SW1	CTS	218-2LPST	Switch Dip Half Pitch 2POS	2POS_DIPSW	SMT218LP_2POS	0		CT2182LPST-ND
50	8	280-00005	MTG_HOLE_TP	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	TI	5015	PC Test Point Miniature SMT	TP_CLIP_5015	TP_5015	0		
51	1	402-00052	IC	U1	TI	TMX320F28035RSHS	Piccolo B 56 pin	F2803x-56 pin	PQFP56-RSH	0		
52	1	402-00005	IC	U11	TI	SN74LVC2G07DBV	IC,Dual Buffer/Driver With Open-Drain Outputs, SOT23-6	SN74LVC2G07DBVR	DBV6			296-13494-2

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Table 5. BOM (continued)

ITEM #	QTY	PART #	PART TYPE	PART REF	VENDOR	VENDOR PN	DESCRIPTION	VALUE	PCB FOOTPRINT	TOLERANCE	DISTRIBUTOR	DISTRIBUTOR PN
53	1	203-00037	POWER	U3	TI	TPS3828-33DBV	Reset Supervisor, SOT23-5	TPS3828	DBV5	0	Digikey	296-2638-1
54	1	400-00007	FET_DIODE	U4	On Semi	1SMB5931BT3	Diode Zener 3 W 18 V SMB	18 V	DO-214AA	0	Digikey	1SMB5931BT3GOSCT-ND
55	1	402-00028	IC	U5	TI	AFE031	AFE031 TI PLC Integrated AFE, 48 pin QFN RGZ	AFE031	RGZ	0		
56	2	400-00003	FET_DIODE	U6, U7	Diodes Inc	B350A-13-F	Diode Schottky 3 A 50 V SMA	B350A-13-F	DO-214AB	0	Digikey	B350A-FDICT-ND
57	2	400-00004	FET_DIODE	U8, U9	STMicroelectronics	STPS1L40A	Diode Schottky PWR 40 V 1 A SMA	STPS1L40A	DO-214AC	0	Digikey	497-3753-1-ND
58	1	402-00037	IC	U10	TI	TPS62240	2.25 MHz 300 mA Step Down Converter	TPS62240	DCC	0		(Cross Ref: 402-00036)
59	1	405-00014	OSC_XTAL	X1	Abracon Corporation	ABM3B-20.000MHZ	Crystal 20.000MHz	20-Mhz OSC 20 ppm	4-SMD		Digikey	300-8214-1-ND

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12.3 Layer Plots

To download the layer plots, see the design files at TIDM-SOMPLC-INDUSTRIAL-CENELEC.

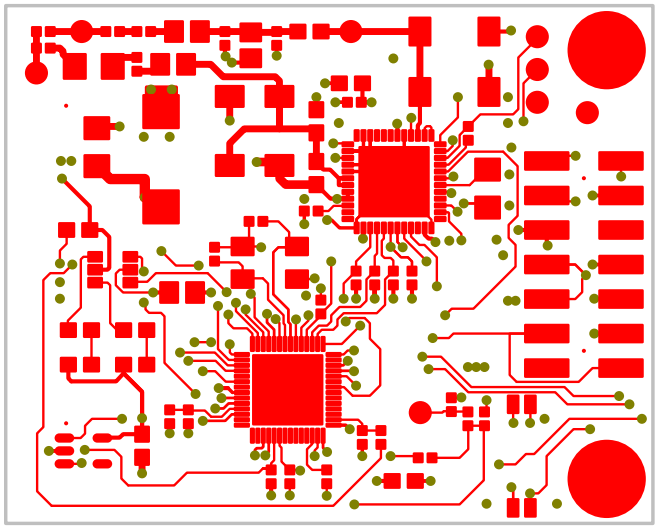

Figure 47. Primary Side

Figure 48. Inner Layer 2

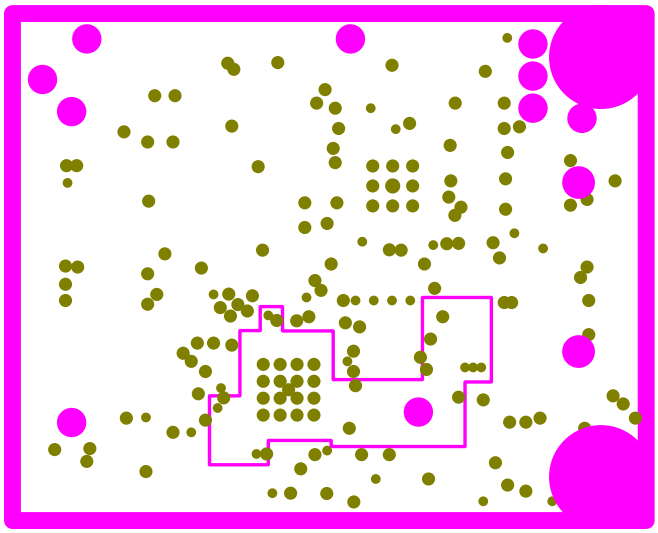

Figure 49. Inner Layer 3

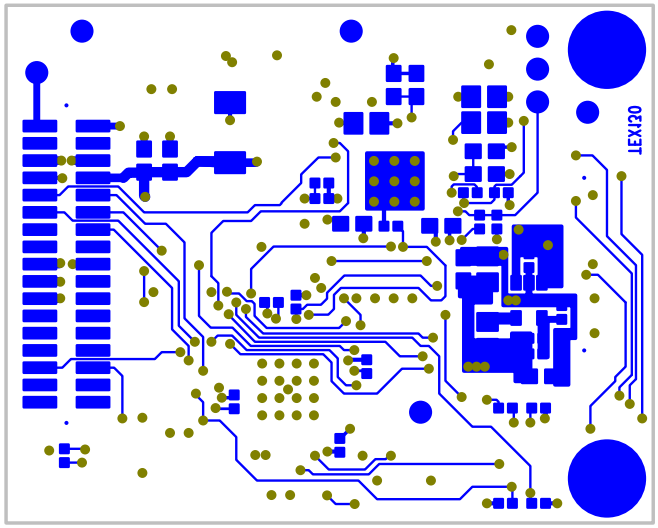

Figure 50. Secondary Side

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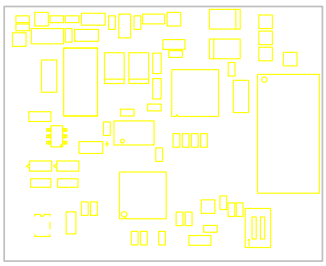

Figure 51. Top Layer

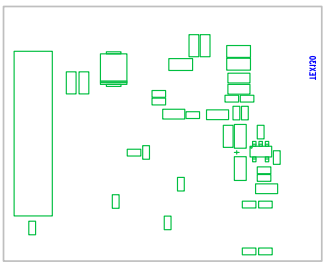

Figure 52. Bottom Layer

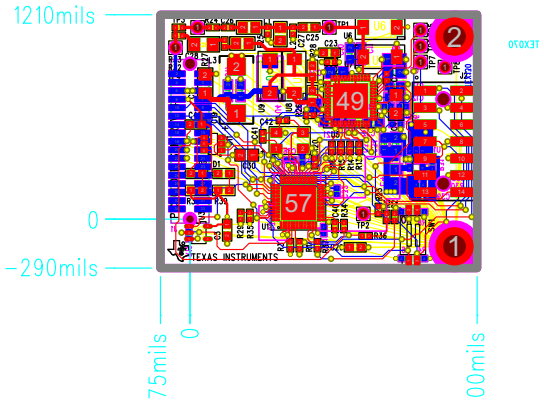

Figure 53. Composite

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12.4 Gerber Files

To download the Gerber files, see the design files at TIDM-SOMPLC-INDUSTRIAL-CENELEC.

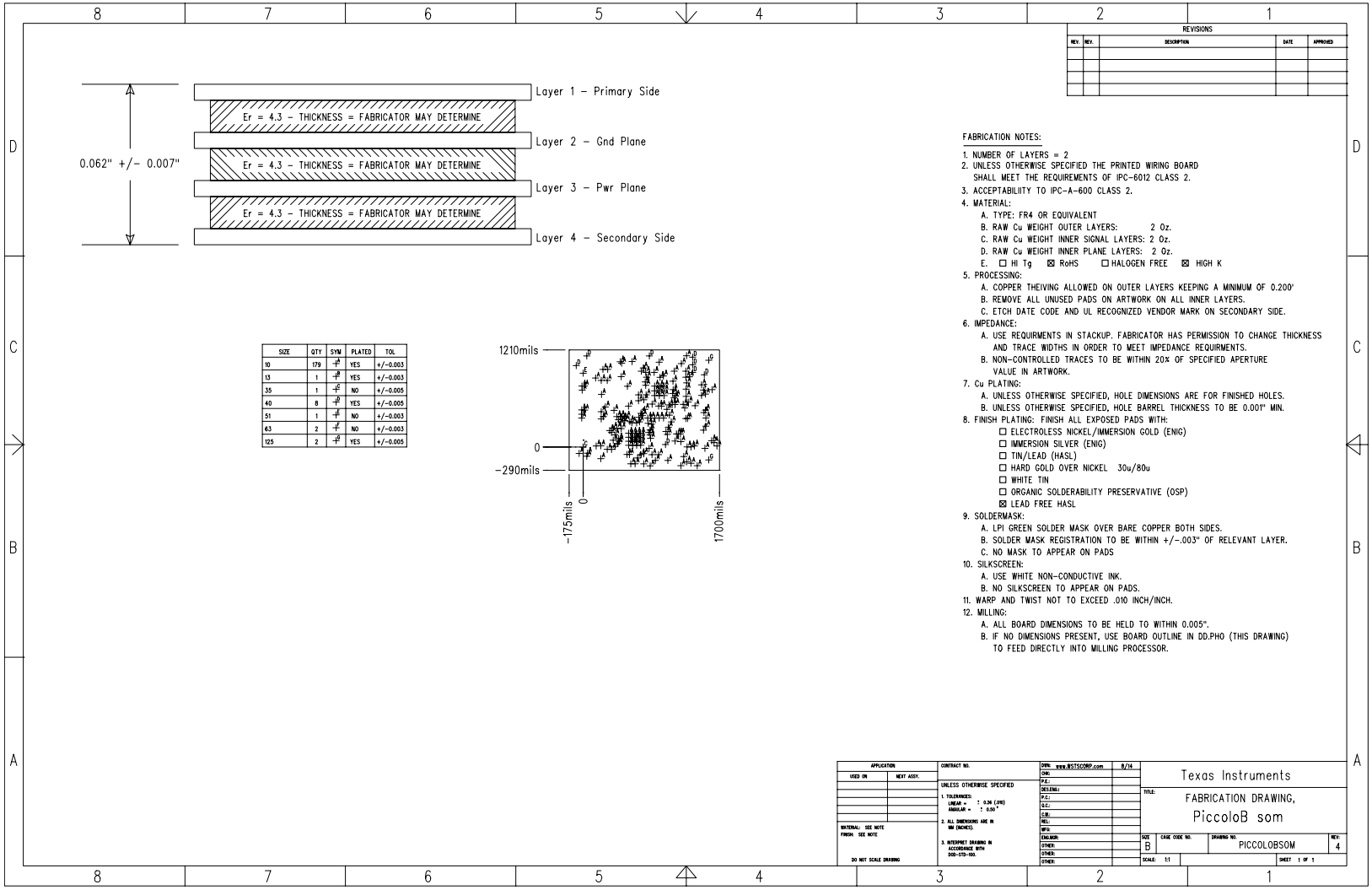

Figure 54. Fabrication Drawing

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12.5 Assembly Drawings

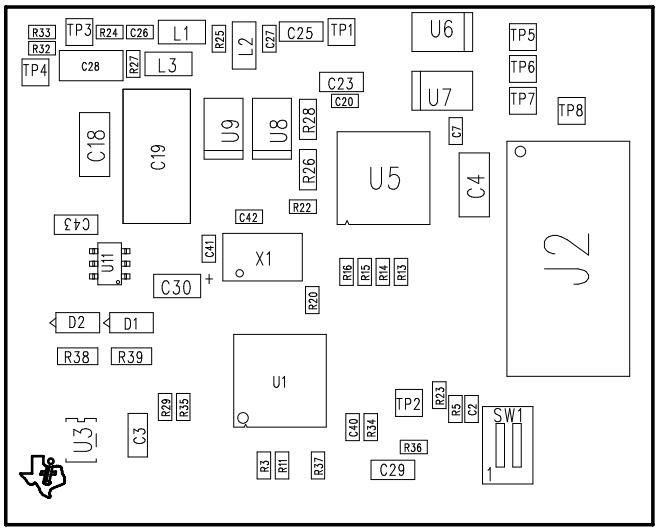

Figure 55. Primary Side Drawing

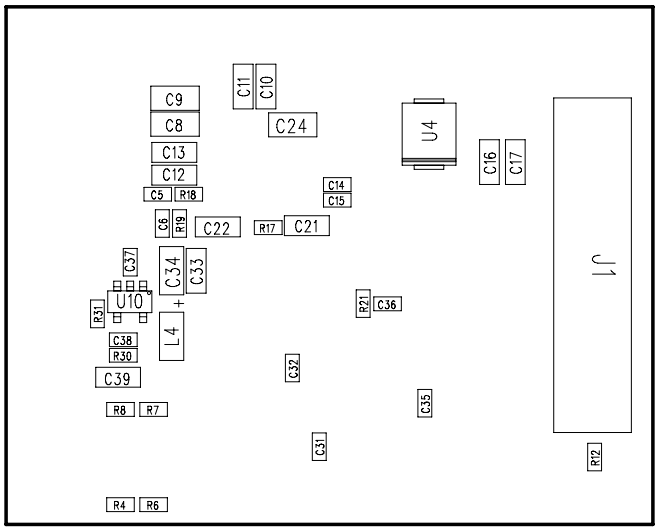

Figure 56. Secondary Side Drawing

13 Software Files

To download the software files, see the design files at TIDM-SOMPLC-INDUSTRIAL-CENELEC.

14 About the Author

WONSOO KIM is a system applications engineer at Texas Instruments, where he is responsible for providing technical support and training on power-line communication software and systems, driving solutions for Smart Grid and Energy Metering, and working on defining future requirements in roadmap. He received a Ph.D. degree in electrical and computer engineering from the University of Texas at Austin, TX.

NAVEEN KALA is a system applications engineer at Texas Instruments, where he is responsible for providing technical support and training on power-line communication hardware, driving solutions for Smart Grid and Energy Metering, and working on defining future requirements in roadmap. He received an MEng degree in electrical and computer engineering from the University of Iowa.

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