Design Guide: TIDA-00173

400- to 690-V AC Input 50-W Flyback Isolated Power Supply Reference Design for Motor Drives

Description

This reference design provides isolated +24 V (45 W), ± 16 V (4.5 W), and +6 V (0.5 W) outputs to power the control electronics in variable speed drives. The power supply can be either powered directly from 3-phase AC mains (380 Vac to 690 Vac) or can be powered from the DC-link voltage (400 Vdc to 1200 Vdc). This design uses a quasi-resonant flyback topology and is rated for 50-W total output power. The line and load regulation of the power supply is designed to be within 5% using primary-side regulation (eliminating costly feedback components). The power supply is designed to meet the clearance, creepage, and isolation test voltages as per IEC61800-5 requirements.

Resources

TIDA-00173	Design Folder
UCC28711	Product Folder
LMS33460	Product Folder

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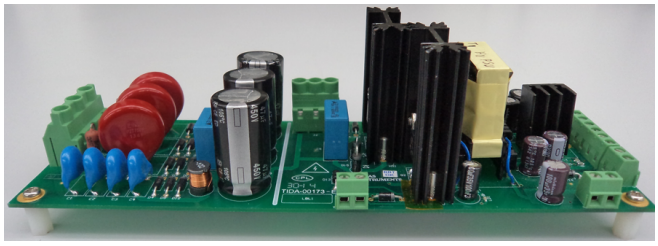
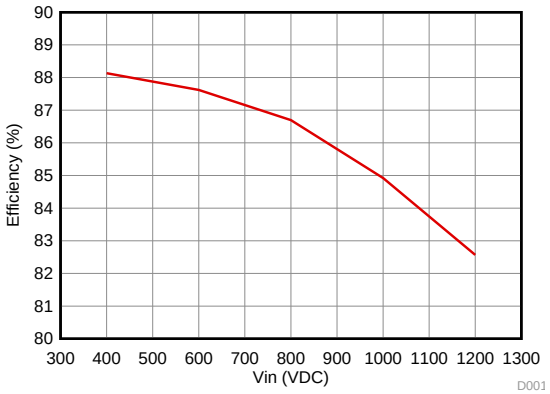
Features

- 50-W main power supply with isolated and nonisolated voltage rails to power control electronics within variable speed drive
- Can operate with dc (1200 V dc max) or ac input (380–690 V ac)
- < 5% load and line regulation
- Input UV/OV, output overload, and sc protection
- Protection against loss of feedback
- Lower-cost solution using UCC28711 through primary side regulation
  - Eliminates feedback loop
  - Use of 1000-V rated MOSFET
- Quasi-resonant mode controller improves EMI
- –10°C to 65°C max operating temperature range
- Designed to comply with IEC 61800-5

Applications

- Variable speed ac and dc drives
- Industrial inverters
- Solar inverters
- UPS systems
- Servo drives





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1 System Description

Variable-speed drive (VSD) consists of a power section, controller, user IO, display, and communication blocks. The power section contains a rectifier, a dc link, inrush current limiting, and an insulated-gate bipolar transistor (IGBT) based inverter. VSD can be based on single or dual controller architecture. When using single controller architecture, the same processor controls generation of pulse-width modulation (PWM), motion control, IO interface, and communication. When dual controller architecture is used, PWM and motion control have a dedicated controller and the other controller is used for application control. The main power supply, either powered directly from ac mains or from dc links, is used to generate multiple voltage rails. Multiple voltage rails are required for the operation of all the control electronics in the drive.

The traditional way of implementing the main power supply is to use flyback converters with PWM controller ICs, such as UCC3842, UCC3843, or UCC3844. Due to a regenerative action from the motor, the voltage rating of the MOSFET used in the flyback converter has to be > 1.5 kV, depending upon the voltage rating of the drive. Opto-couplers are used for isolated feedback and to regulate the output voltage. In case of failure of components used in the feedback path, the output may reach a dangerously high level, which would damage all the electronic components. Use of controllers like the UCC3842 device presents other challenges, for example, limiting the power during short circuit across wide input-voltage range and power dissipation in the resistors used in startup circuit.

The primary objective of this reference design is to create a power supply with reduced BOM cost and a reusable design for drives operating at both 400-V and 690-V inputs. Other benefits include:

- Topology to replace single high-voltage FET with two low-cost FETs
- Constant uniform power limit throughout the input range
- Reduced BOM cost by using UCC28711 through primary side regulation, thus eliminating isolated secondary feedback
- Protection against component failure in the feedback path

This reference design provides isolated 24 V, 16 V, –16 V, and 6 V outputs to power the control electronics in variable speed drives. The power supply can be either powered directly from 3-phase ac mains or can be powered from dc-link voltage. This design uses quasi-resonant flyback topology and is rated for 50-W output. The line and load regulation of the power supply is designed to be within 5%. The power supply is designed to meet the clearance, creepage, and isolation test voltages as per IEC61800-5 requirements.

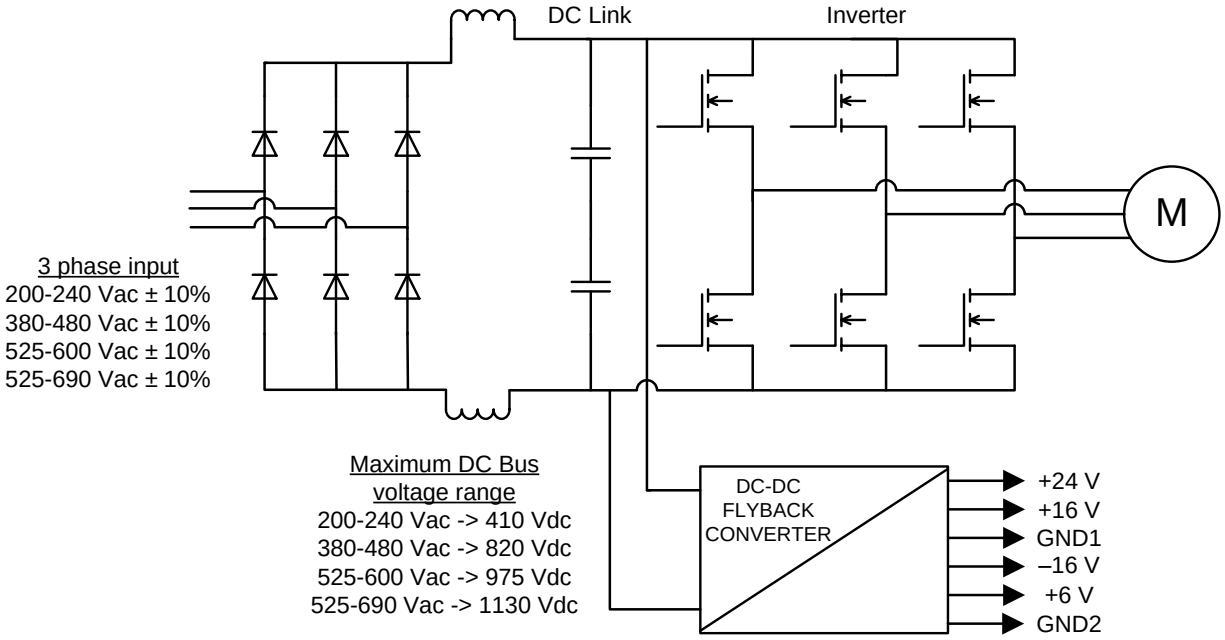

Figure 1. Variable-Speed Drive Topology

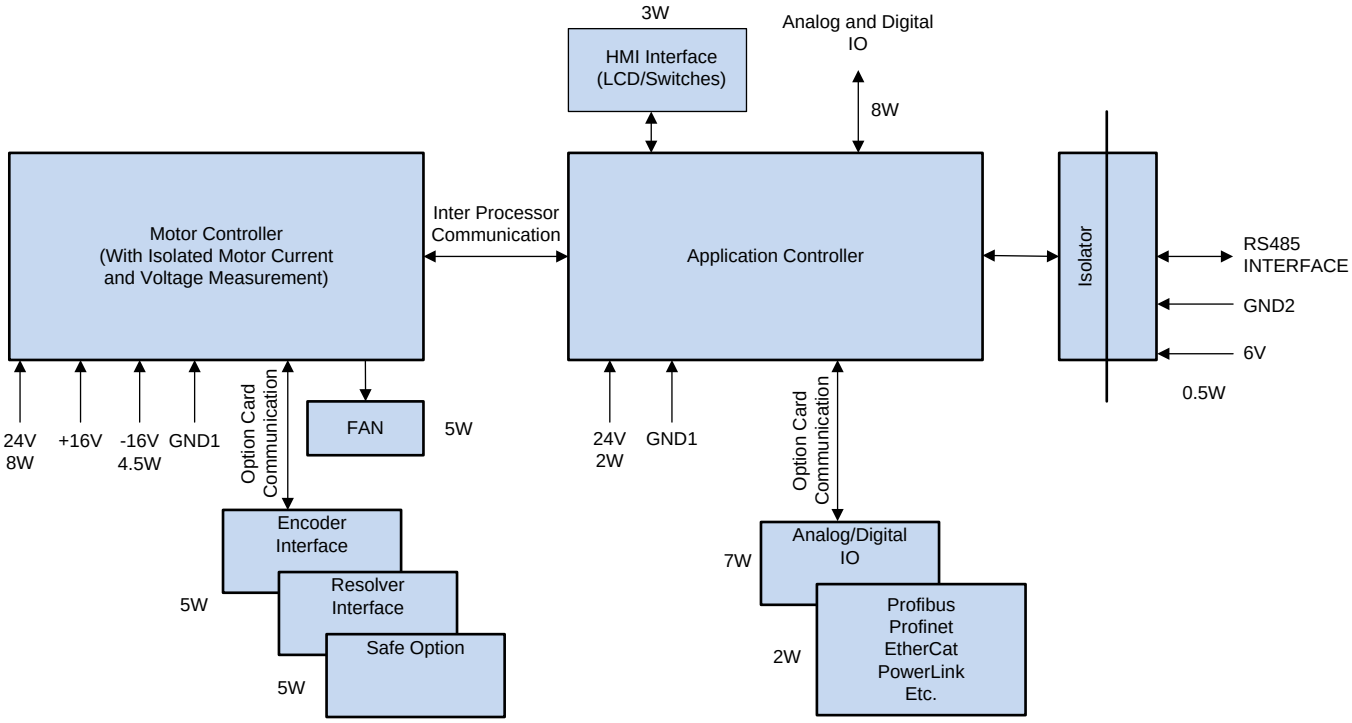

Figure 2. Drive Control Architecture with Typical Power Consumption

1.1 Requirements of Power Supply

The requirements of the main power supply to be used in drive applications are as follows:

- 400 V dc to 1200 V dc input
- 50-W output power
- > 40 kHz switching frequency
- Quasi-resonant mode controller
- 80% expected efficiency
- < 200 mV secondary ripple voltage
- < 5% load and line regulation
- Input UV/OV shutdown
- Output overload shutdown with power limit
- Can be powered from ac mains or from dc link
- Isolated measurement of dc link voltage (input) through indirect technique
- Detection of single phase scenario through dc link measurement
- EMC filter and surge protection required
- 65°C max ambient temperature
- Clearance and creepage as per IEC 61800-5-2

2 Design Features

This power-supply design is intended to replace the high-cost, high-voltage MOSFET with a low-cost, low-voltage MOSFET along with omission of feedback components. Also, the power supply is designed to operate across a wide input range, which will suit drives operating from 400 V and 690 V ac inputs. The power supply includes the following protection features:

- Output overvoltage fault
- Input undervoltage fault
- Internal overtemperature fault
- Primary overcurrent fault

2.1 Topology Selection

Flyback topology is the most widely used switch mode power supply (SMPS) topology in most of the variable speed drives. The power ratings are below 150 W and SMPS topologies only require a single magnetic element; therefore, serves the purpose of isolation, step-up or step-down conversions, and acts as an energy storage element. The attractive feature of using this topology is that no output inductors are required. Other advantages include easy creation of multiple output voltages, very low component count, and low cost.

With flyback converters using a single switching element, an expensive 1500 V (or more expensive for 690 V ac rated drives) MOSFET must be used to support the transformer flyback voltage on top of the high-input voltage and voltage generated through regenerative action.

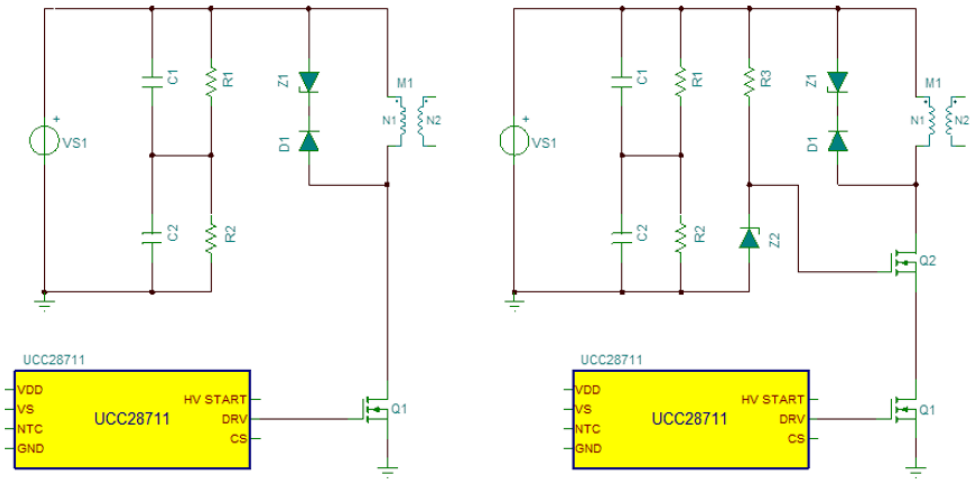

Figure 3. Flyback Controller with Single and Dual MOSFET Switch

In the case of cascode flyback converter (see Figure 3), MOSFET Q1 with low gate charge Qg, is connected in series with MOSFET Q2. In this case, the Q1 is driven directly from the PWM controller. With cascode configuration, it is possible to distribute the voltage stress across two devices, thus resulting in an overall voltage rating equal to the sum of the individual MOSFET voltages. Using the cascode technique with a low-cost 900-V MOSFET results in an overall voltage rating of 1800 V, which allows supply operation over the desired wide input-voltage range of 350 to 720 V ac. This simple circuit requires a limited control change, which is attained from the original TVS supplied from input supply.

2.2 Cascode Operation

2.2.1 Turn ON Sequence

When the gate-source voltage of MOSFET Q1 (Vgs1) is greater than its gate threshold voltage, Vth1, the Q1 fully enhances and is turned ON. As soon as the Q1 turns ON, the source of Q2 is connected to ground through Q1, which makes the zener voltage apply across the gate source of Q2, and it gets turned ON. Next, the cascode converter reaches the conduction state; then the current starts to flow through the primary winding of the flyback transformer and the two switches (Q1 and Q2). The voltage drop across both MOSFETs is equal to their on-state voltage drops.

2.2.2 Turn OFF Sequence

When the gate-source voltage Vgs1 is less than its gate threshold voltage Vth1, MOSFET Q1 is turned OFF. The current takes a path through the drain to the source capacitance of Q1. Now the drain source voltage Vds1 across Q1 starts to increase. At this time, the potential source terminal of HV MOSFET Q2 starts to build up. As the potential source terminal of Q2 builds up, the gate-source voltage Vgs2 of the MOSFET is reduced. When Q2 reaches its gate threshold voltage Vth2, the Q2 is turned OFF.

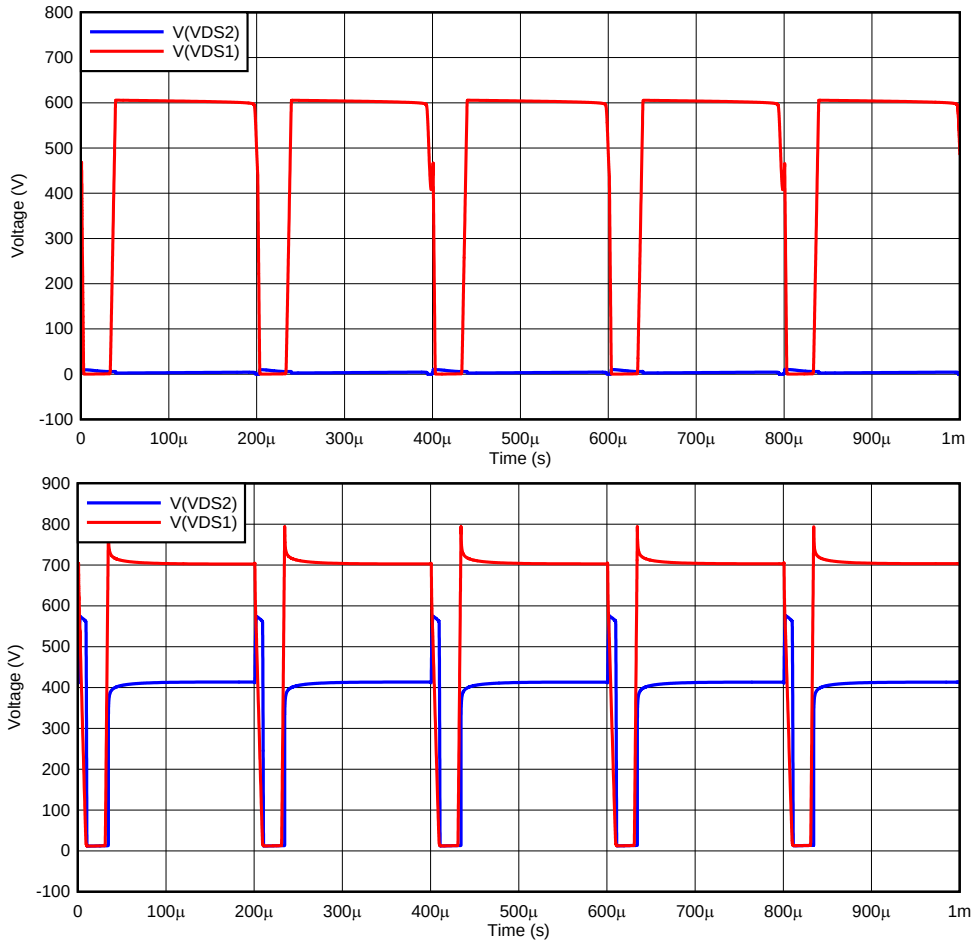

Figure 4. V_{DS} Voltage of MOSFETs During Low V_{IN} and High V_{IN}

2.3 Design Requirements

To translate the Requirements of Power Supply to the sub-system level, the requirements of the PWM controller, MOSFETs, and transformer are listed in Section 2.3.1 through Section 2.3.3.

2.3.1 PWM Controller

Accurate voltage and constant current regulation primary-side feedback

Primary-side feedback, eliminates the need for opto-coupler feedback circuits

Discontinuous conduction mode with valley switching to minimize switching losses

Protection functions

- Output and input overvoltage fault
- Input undervoltage fault
- Internal over-temperature fault
- Primary overcurrent fault
- Loss of feedback signal

2.3.2 Power MOSFETs

- Each MOSFET should have a rated V_{DS} ≥ 1000 V to support 1200 V dc input
- Should support 1.5 A (minimum) drain current

2.3.3 Transformer Specifications (as per IEC61800-5-1)

- Four isolated outputs:
  - V_{out1} = 24 V, 45 W
  - V_{out2} = ±16 V, 4.5 W
  - V_{out3} = 6 V, 0.5 W
  - V_{aux} = 16 V, 15 W (only when Vout1 is de-rated accordingly)
- Switching frequency = 50 kHz
- Primary to secondary isolation = 7.4 kV for 1.2, 50-μs impulse voltage
- Type test voltage:
  - Primary to Secondary = 3.6 kV_{RMS}
  - Secondary 1 to Secondary 2 = 1.8 kV_{RMS}
  - Secondary 1 to Secondary 3 = 1.8 kV_{RMS}
  - Secondary 2 to Secondary 3 = 1.8 kV_{RMS}
- Spacings:
  - Primary to Secondary clearance = 8 mm
  - Secondary 1 to Secondary 2 clearance = 5.5 mm
  - Secondary 2 to Secondary 3 clearance = 5.5 mm
  - Secondary 3 to Secondary 4 clearance = 5.5 mm
  - Creepage distance = 9.2 mm
- Functional isolation primary and secondaries = 2 kV dc
- dc isolation between secondaries = 2 kV dc

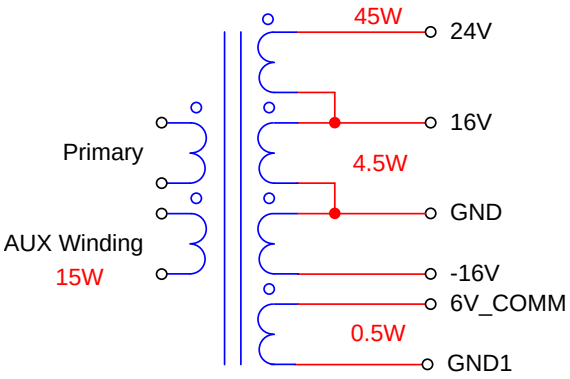

Figure 5. Transformer Configuration

3 Block Diagram

The simplified implementation diagram is shown in Figure 6. The transformer has three secondary windings (two isolated and one nonisolated). The auxiliary winding can be loaded up to 15 W, provided that the output from the main secondary is reduced from 45 W to 30 W. The power train consists of two MOSFETs in cascode connection. In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary.

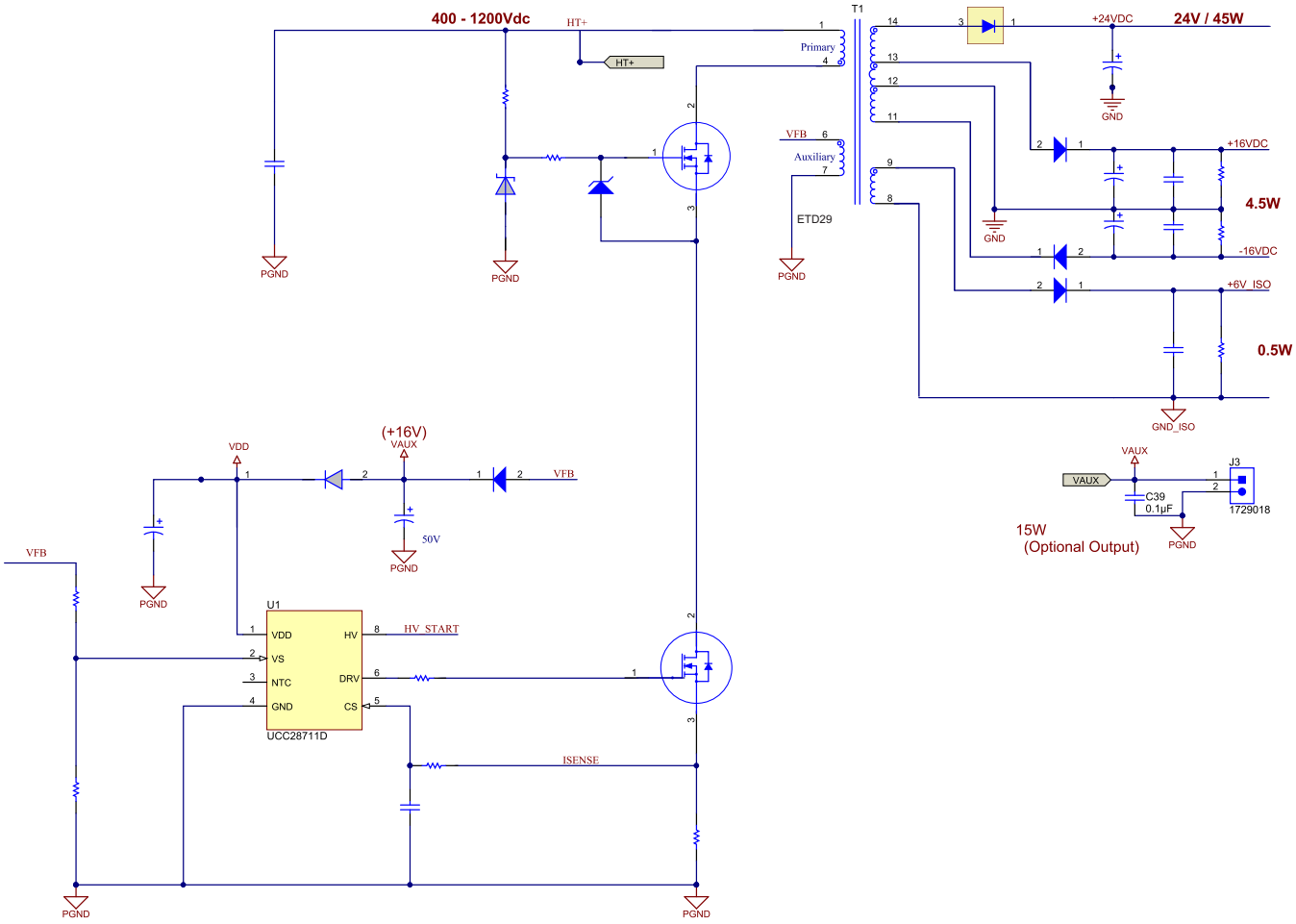

Figure 6. Simplified Diagram of the Solution

To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator inside the IC reliably blocks the leakage inductance reset and ringing. The discriminator continuously samples the auxiliary voltage during the down slope after the ringing is diminished and also captures the error signal when the secondary winding reaches zero current. The internal reference on VS is 4.05 V. Temperature compensation on the VS reference voltage of –0.8 mV/°C offsets the change in the output rectifier forward voltage with temperature. The feedback resistor divider is selected as outlined in the VS pin description (see Section 5.2.7).

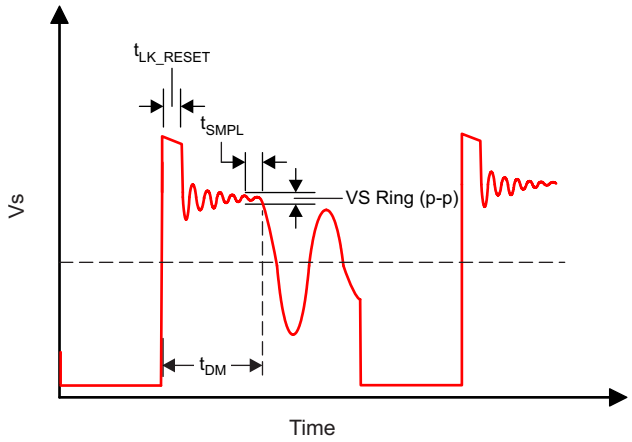

Figure 7. Aux Waveform — Sampling

3.1 Primary-Side Current Regulation

When the average output current reaches the regulation reference in the current control block, the controller operates in frequency modulation mode to control the output current at any output voltage at or below the voltage regulation target — as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.

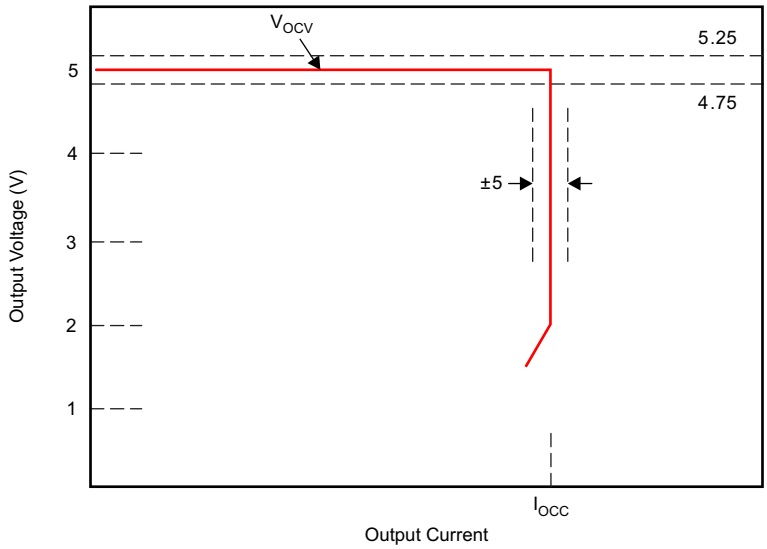

Figure 8. Power Limit

4 Highlighted Products

This reference design features the following devices, which were selected based on their specifications.

- **UCC28711**
  - Constant-Voltage, Constant-Current PWM Controller with Primary-Side Regulation
- **LMS33460**
  - 3-V Undervoltage Detector

For more information on each of these devices, see the respective product folders at www.TI.com or click on the links for the product folders on the first page of this reference design.

5 Component Selection and Circuit Design

5.1 Component Selection

The UCC28711 and LMS33460 components are selected based on their specifications.

5.1.1 UCC28711

The UCC28700 device is a flyback power-supply controller, which provides accurate voltage and constant current regulation with primary-side feedback, thus eliminating the need for opto-coupler feedback circuits. The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak-current modulation to provide high conversion efficiency across the load range. The controller has a maximum switching frequency of 130 kHz and allows for a shut-down operation using the NTC pin.

5.1.2 LMS33460

The LMS33460 device is an undervoltage detector with a 3.0-V threshold and extremely low power consumption. The LMS33460 device is specifically designed to accurately monitor power supplies. This IC generates an active output whenever the input voltage drops below 3.0 Volts. This device uses a precision on-chip voltage reference and a comparator to measure the input voltage. Built-in hysteresis helps prevent erratic operation in the presence of noise.

5.2 Circuit Design

The ac input is full-wave rectified by diodes D1 through D12. Resistors R1 through R3 provide in-rush current limiting and protection against catastrophic circuit failure. Capacitors C6 through C8 are used to filter the rectified ac supply. Three capacitors of 47 µF, 450 V are connected in a series to support more than 1200 V, although 450 V is the maximum value available on the market. To avoid an unbalanced voltage spread between capacitors, resistances are connected in parallel with each capacitor.

5.2.1 Input Diode Bridge

Equation 1 and Equation 2 determine the selected input bridge.

$$P_{inmax} = \frac{P_{out}}{\eta} = \frac{50}{0.8} = 62.5\,W \quad (1)$$

$$I_{inrms} = \frac{P_{inmax}}{1.732 \times V_{acmin} \times \cos\varnothing} = \frac{62.5}{1.732 \times 330 \times 0.6} = 0.182\,A \quad (2)$$

where

- cosø is the power factor, which is assumed to be 0.6

Equation 3 determines the minimum voltage rating of the rectifier.

$$V_{dcMIN} = (V_{acMAX} \times 1.414) + (0.15 \times V_{acMAX} \times 1.4141) = (480 \times 1.414) + (0.15 \times 480 \times 1.414) = 780\ V \quad (3)$$

Considering the raise in dc bus voltage due to regenerative action, two diodes of 1000 V with 1-A rating are used for the 3-phase bridge rectifier.

5.2.2 Selection of Input Capacitors (C_{IN})

The dc input bulk capacitor C1 is used to provide a smooth dc voltage by filtering low frequency ac ripple voltage. For calculating the input filter capacitor, a ripple voltage of 10% (40 V) is assumed.

Equation 4 determines the worst-case discharge time.

$$t_d = \frac{1}{6 \times 50} = 3.33\,ms \tag{4}$$

$$C_{IN} \geq \frac{2 \times \frac{P_{out}}{\eta} \times t_d}{(V_{min}^2 - 0.9 \times V_{min}^2)} = \frac{2 \times \frac{50}{0.8}(3.33m)}{(400^2 - 0.9 \times 400^2)} = 13.7\,\mu F \tag{5}$$

Equation 6 shows the calculation for RMS current. (See Section 5.2.11 for D_{MAX} and I_{pk} details)

$$I_{rms} = I_{pk} \times \sqrt{\frac{D_{max}}{3}} = 1 \times \sqrt{\frac{0.335}{3}} = 334\ mA \tag{6}$$

Three capacitors of 47 µF / 450 V (EEUED2W470) with a 1-A ripple current rating are connected in series to get an equivalent value of approximately 15 µF.

5.2.3 Input Filter

Equation 7 shows the required corner frequency of the filter.

$$f_c = f_{sw} \times 10^{\frac{Att}{40}}$$

where

- f_c is the desired corner frequency of the filter
- f_{sw} is the operating frequency of the power supply (50 kHz) (7)

With reasonable assumption of having 60 dB of attenuation at the switching frequency of the power supply, Equation 8 determines the cut off frequency of the filter

$$f_c = 50k \times 10^{\frac{-60}{40}} = 1.58\ kHz$$

(approximated to 1 kHz) (8)

Equation 8 leads to an inductance of 2 mH, which is split in two with 1 mH being placed on both the lines of the dc bus.

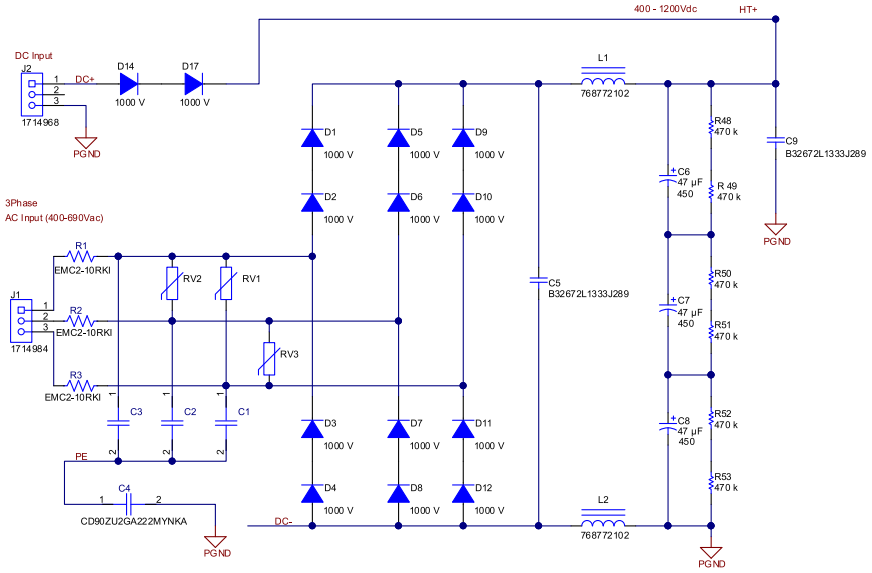

Figure 9. Input Section

5.2.4 Surge Protection

Considering 690 V ac input with 10% variation, MOV of 750 V ac with peak-current rating of 6500 A specified for 8/20 µsec waveform has been used to suppress surge at the input. For 400-V rated drives, the voltage rating of the MOV needs to be lowered.

5.2.5 VDD Capacitor Selection (C_{DD})

The capacitance on VDD supplies operating current to the device until the output of the converter reaches the target minimum operating voltage in constant-current regulation.

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in constant-current regulation. Now the auxiliary winding can sustain the voltage to the UCC28711 device. The total output current available to the load and available to charge the output capacitors is the constant-current regulation target. Equation 9 assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. There is an estimated 1 mA of gate-drive current shown in Equation 10 and 1 V of margin is added to VDD.

$$C_{DD} = \frac{(I_{RUN} + 1\,mA)\left(\frac{C_{OUT1} \times V_{OCC1}}{I_{OCC1}} + \frac{C_{OUT1} \times V_{OCC1}}{I_{OCC1}} + \frac{C_{OUT1} \times V_{OCC1}}{I_{OCC1}} + \frac{C_{OUT1} \times V_{OCC1}}{I_{OCC1}}\right)}{(V_{DD(ON)} - V_{DD(OFF)}) - 1\,V} \tag{9}$$

$$C_{DD} = \frac{(2\,mA + 1\,mA)\left(\frac{760\,\mu \times 24}{1.875} + \frac{100\,\mu \times 16}{0.14} + \frac{100\,\mu \times 16}{0.14} + \frac{100\,\mu \times 16}{0.083}\right)}{(21 - 8) - 1\,V} = 9.95\,\mu F \approx 10\,\mu F \tag{10}$$

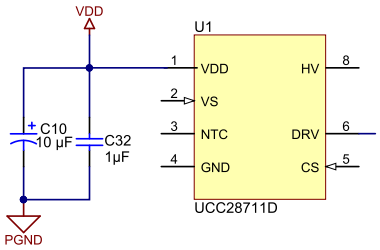

Figure 10. VDD Capacitor

After C_{DD} has been charged up to the device turn-on threshold ($V_{VDD(on)}$), the UCC28700 device will initiate three small gate drive pulses (DRV) and start sensing current and voltage (see Figure 11). If a fault is detected, such as an input under voltage or any other fault, the UCC28700 device will terminate the gate-drive pulses and discharge CDD to initiate an under-voltage lockout. This capacitor will be discharged with the run current of the UCC28700 (I_{RUN}) until the VDD turnoff threshold ($V_{VDD(off)}$) is reached. The CDD discharge time (t_{CDDD}) from the forced soft start is calculated in Equation 11 with the controller-run current (I_{RUN}) without out-gate driver switching and the VDD turnoff threshold ($V_{VDD(off)}$) of the controller. If no fault is detected, the UCC28700 device will continue driving QA and controlling the input and output currents. No soft start will be initiated.

I_{run} = 2.1 mA

$V_{VDD(off)}$ = 8 V

$$dt_{CDD} = C_{DD}\frac{V_{VDD(ON)} - V_{VDD(OFF)}}{\left(\frac{V_{INMAX}}{R_T} - I_{RUN}\right)} = 10\,\mu\frac{21 - 8}{\left(\frac{1100}{1.88M} - I_{RUN}\right)} = 60\ ms \tag{11}$$

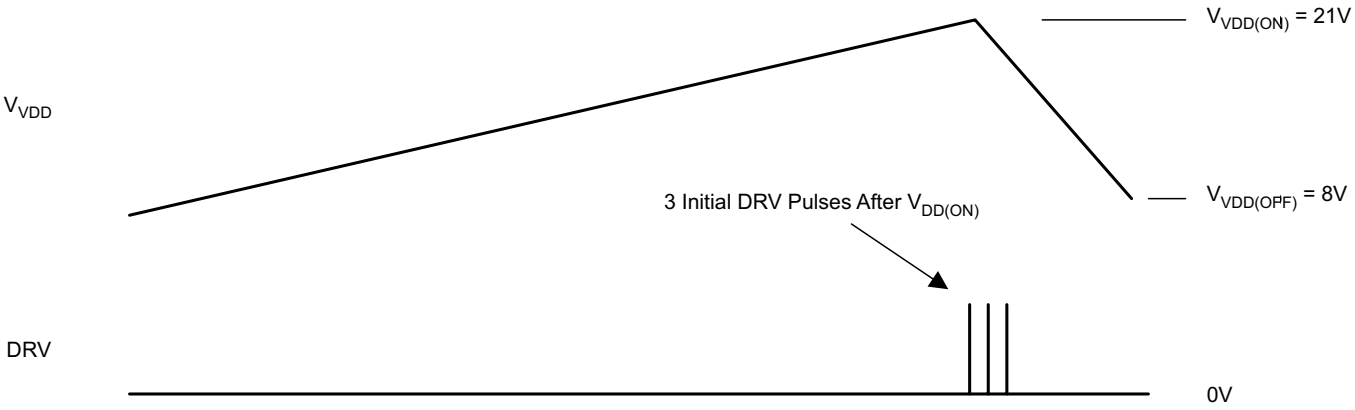

Figure 11. Power-ON Sequence

5.2.6 Current Sensing

For this design, a 0.75-Ω resistor is selected based on a nominal maximum current-sense signal of 0.75 V.

NOTE: The actual value shown in Equation 12 needs to be tuned based on the allowable power limit during fault conditions. In this design 0.91-Ω resistor is used to limit the power less than 65 W.

$$R_{CS} = \frac{0.75}{I_{PPK}} = 0.75\,\Omega \tag{12}$$

Equation 13 determines the nominal current sense resistor power dissipation.

$$P_{RCS} = I^2_{PRMS} \times R_{CS} = 0.334^2 \times 0.91 = 0.1\,W \tag{13}$$

The UCC28711 device operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin is 0.78 V to 0.195 V. There is additional protection if the CS pin reaches 1.5 V. This results in a UVLO reset and restart sequence.

The current-sense (CS) pin is connected through a series resistor (RLC) to the current-sense resistor (RCS). The current-sense threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. The series resistor RLC provides the function of feed-forward line compensation to eliminate change in IPP due to change in di/dt and the propagation delay of the internal comparator and MOSFET turnoff time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turnon current spike. The value of RCS is determined by the target output current in constant-current (CC) regulation. The value of R_{LC} is determined by Equation 14.

NOTE: The value determined in Equation 14 may require adjustments based on the noise and ringing on the current sense which is dependent on routing of the signals. 1 kΩ resistor is used in the design.

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} = \frac{25 \times 91\,k \times 0.91 \times 300\,n \times 18}{2.5\,m} = 4.44\,k \tag{14}$$

where

- R_{LC} is the line compensation resistor
- R_{S1} is the VS pin high-side resistor value
- R_{CS} is the current-sense resistor value
- T_D is the current-sense delay including MOSFET turn-off delay. Add 50 ns to the MOSFET delay.
- N_{PA} is the transformer primary-to-auxiliary turns ratio
- L_P is the transformer primary inductance.
- K_{LC} is the current-scaling constant (equal to 25 A/A according to data sheet of UCC28711)

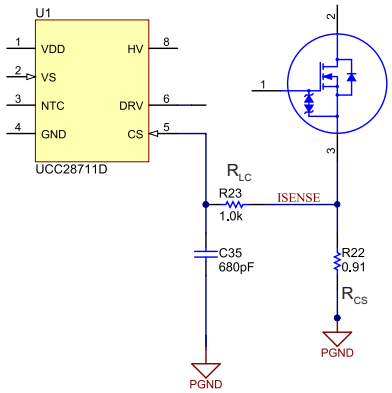

Figure 12. Current Sense

5.2.7 Primary-Side Regulation

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator (inside UCC28711) reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V; and VS is connected to a resistor divider from the auxiliary winding to the ground. The output-voltage feedback information is sampled at the end of the transformer secondary-current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. It is not recommended to place a filter capacitor on this input, which would interfere with accurate sensing of this waveform.

The VS pin senses the bulk-capacitor voltage to provide for ac-input run and stop thresholds. The VS pin also compensates the current-sense threshold across the ac-input range. The VS pin information is sensed during the MOSFET on-time. For the ac-input run or stop function, the run threshold on VS is 225 μA and the stop threshold is 80 μA. A wide separation of run and stop thresholds allows clean start-up and shut-down of the power supply with the line voltage.

The VS pin also senses the bulk capacitor voltage to provide for ac-input run and stop thresholds, and to compensate the current-sense threshold across the ac-input range. This information is sensed during the MOSFET on-time. For the ac-input run/stop function, the run threshold on VS is 225 μA and the stop threshold is 80 μA. A wide separation of run and stop thresholds allows clean start up and shut down of the power supply with the line voltage.

The values for the auxiliary voltage divider upper-resistor RS1 and lower-resistor RS2 can be determined by Equation 15 and Equation 16.

$$R_{S1} = \frac{V_{IN(RUN)}}{N_{PA} \times I_{VSL(RUN)}} = \frac{375}{18 \times 225\,\mu} = \approx 92k \quad (15)$$

(Rounded off to 91 k)

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio
- $V_{IN(run)}$ is the converter input start-up (run) voltage
- $I_{VSL(run)}$ is the run threshold for the current pulled out of the VS pin during the MOSFET on-time (equal to 220 μA max from UCC28711 data sheet)

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} = \frac{91\,k \times 4.05}{(0.66 \times 24.6) - 4.05} = 30.2\ k$$

(Rounded off to 30 k)

where

- V_{OCV} is the regulated output voltage of the converter
- V_F is the secondary rectifier forward voltage drop at near-zero current
- N_{AS} is the transformer auxiliary-to-secondary turns ratio
- R_{S1} is the VS divider high-side resistance
- V_{VSR} is the CV regulating level at the VS input (equal to 4.05-V typical from UCC28711 data sheet) (16)

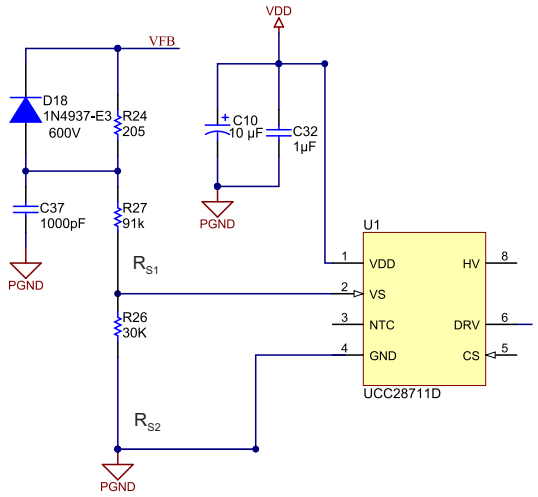

Figure 13. Primary Feedback

The output over-voltage function is determined by the voltage feedback on the VS pin. If the voltage sample on VS exceeds 115% of the nominal VOUT, the device stops switching and also stops the internal current consumption of IFAULT, which discharges the VDD capacitor to the UVLO turnoff threshold. After that, the device returns to the start state and a start-up sequence ensues.

Protection is included in the event of component failures on the VS pin. If complete loss of feedback information on the VS pin occurs, the controller stops switching and restarts.

5.2.8 MOSFET Gate-Drive

The DRV pin of UCC28711 device is connected to the MOSFET gate pin through a series resistor. The gate driver provides a gate-drive signal limited to 14 V. The turnon characteristic of the driver is a 25-mA current source, which limits the turnon dv/dt of the MOSFET drain. This reduces the leading-edge current spike, but still provides gate-drive current to overcome the Miller plateau. The gate-drive turnoff current is determined by the low-side driver $R_{DS(on)}$ and any external gate-drive resistance. In order to improve the efficiency and to reduce switching loss in the power device, an external BJT-based current buffer with a higher voltage rating (high Qg) may be used to drive the MOSFETs.

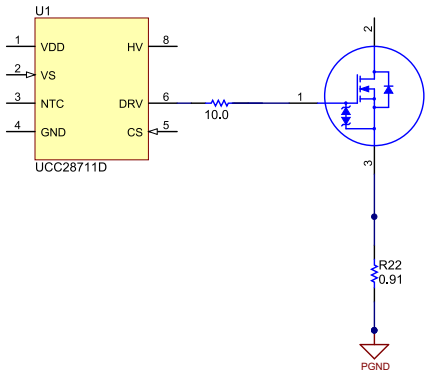

Figure 14. MOSFET Gate Drive

5.2.9 Overvoltage Detection

The LMS33460 device is a micropower, under-voltage sensing circuit with an open-drain output configuration, which requires a pull resistor. The LMS33460 features a voltage reference and a comparator with precise thresholds, and built-in hysteresis to prevent erratic-reset operation. This IC generates an active output whenever the input voltage drops below 3.0 V. The resistor divider shown in Figure 15 is derived with 1200 V dc as the over-voltage trip point. Zener diode D32 is used to clamp the input voltage at LMS33460 to less than 8 V (absolute max of the device) when the dc bus voltage is at its max of 1200 V dc.

The device has a minimum hysteresis voltage of 100 mV, which translates to approximately 11 V on the dc bus. Hysteresis can also be adjusted with R29.

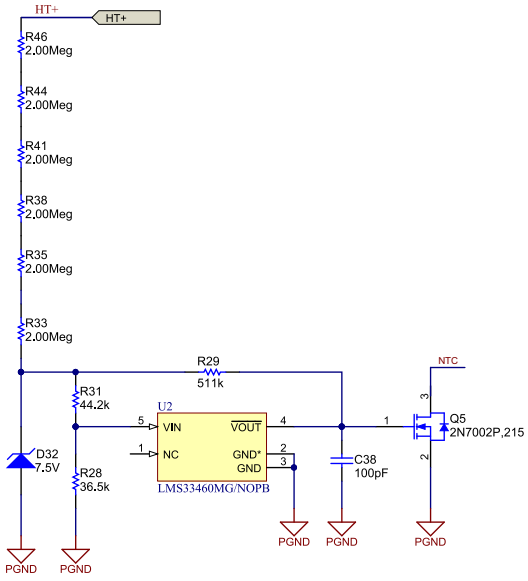

Figure 15. Undervoltage Protection

The UCC28711 device has an NTC input, which can be used to interface an external negative-temperature-coefficient resistor for remote temperature sensing to allow user-programmable external thermal shutdown. The shutdown threshold is 0.95 V with an internal 105-μA current source, which results in a 9.05-kΩ thermistor shutdown threshold.

Pulling the NTC pin to low shuts down the PWM action. The signal from LMS33460 is interfaced to the NTC pin to shut down the controller during over voltage.

5.2.10 HV Startup

The UCC28710 device has an internal 700-V start-up switch. Because the dc bus can be as high as 1200 V dc, an external Zener voltage regulator is used to limit the voltage at the HV pin to about 550 V dc. The typical startup current is approximately 300 μA, which provides fast charging of the VDD capacitor. The internal HV start-up device is active until VDD exceeds the turnon UVLO threshold of 21 V at which time the HV start-up device is turned off. In the off state, the leakage current is very low to minimize standby losses of the controller. When VDD falls below the 8.1-V UVLO turn-off threshold, the HV start-up device is turned on.

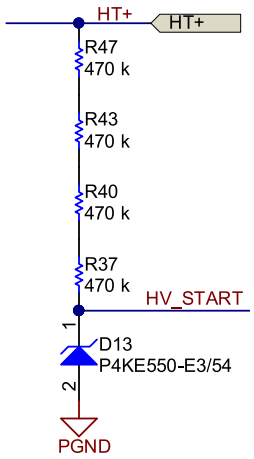

Figure 16. Start-Up Circuit

For drives with two capacitors connected in series in the dc link, the midpoint of the series can be connected to the HV pin of the UCC28711 device. The midpoint voltage will vary from 200 V to 600 V (for an input of 400 V dc to 1200 V dc), which would be within the limit of 700-V start-up switch of UCC28711.

5.2.11 Transformer Calculations

Equation 17 shows the calculation for the transformer turns ratio primary to secondary (a1) based on volt-second balance.

$$a1 = \frac{N_P}{N_S} = \sqrt{\frac{L_{PM}}{L_{SM}}} = \frac{D_{MAX} \times (Vin_{MIN} - V_{AON} - V_{RCS})}{D_{MAG} \times (V_{OUT} + V_{DG})} = \approx 12 \quad (17)$$

where

- L_{SM} is the secondary magnetizing inductance
- V_{AON} = 5 V, estimated voltage drop across FET during conduction
- V_{RCS} = 0.75 V, voltage drop across current sense resistor
- V_{DG} = 0.6 V, estimated forward voltage drop across output diode

Equation 18 shows the calculation for maximum duty cycle (D_{MAX}).

$$D_{MAX} = \frac{12 \times D_{MAG} \times (V_{OUT} + V_{DG})}{Vin_{MIN} - V_{AON} - V_{RCS}} = \frac{12 \times 0.425 \times 24.6}{375 - 5 - 0.75} = 0.335 \quad (18)$$

Equation 19 shows the calculation for the transformer primary-peak current (I_{PPK}) based on a minimum flyback input voltage.

$$I_{PPK} = \frac{2 \times P_{OUT}}{\eta \times Vin_{MIN} \times D_{MAX}} = \frac{2 \times 50\,W}{0.8 \times 375 \times 0.335} = 1\,A \quad (19)$$

Equation 20 shows the calculation for the selected primary magnetizing inductance (L_{PM}) based on minimum flyback input voltage, transformer, primary peak current, efficiency, and maximum switching frequency (f_{MAX}).

$$L_{PM} = \frac{\frac{2 \times P_{OUT}}{\eta}}{I_{PPK}^2 \times F_{MAX}} = \frac{\frac{2 \times 50\,W}{0.8}}{1^2 \times 50\,kHz} = 2.5\,mH \quad (20)$$

Equation 21 shows the calculation for the transformer auxiliary to secondary turn ratio (a2).

$$a2 = \frac{N_A}{N_S} = \frac{V_{DDMIN} + V_{DE}}{V_{OUT} + V_{DG}} = \frac{16 + 0.3}{24.6} = 0.66$$

where

- V_{DDMIN} = 16 V
- V_{DE} = 0.3 V, estimated auxiliary diode forward voltage drop (21)

Equation 22 shows the calculation for the transformer primary RMS current (I_{PRMS}).

$$I_{PRMS} = I_{PPK} \sqrt{\frac{D_{MAX}}{3}} = 1 \times \sqrt{\frac{0.335}{3}} = 0.334\,A \quad (22)$$

Equation 23 through Equation 26 show the calculations for the transformer secondary peak current RMS current (I_{SPK}).

$$I_{S1PK}\,(24\,V\,Output) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{90}{24.6 \times 0.425} = 8.6\,A$$

(3.23 A_{rms}) (23)

$$I_{S2PK}\,(\pm 16\,V\,Output) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{9}{33.2 \times 0.425} = 0.638\,A$$

(0.24 A_{rms}) (24)

$$I_{S3PK}\,(\pm 6\,V\,Output) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{1}{6.6 \times 0.425} = 0.357\,A$$

(0.134 A_{rms}) (25)

$$I_{AUX\_PK}\,(16\,V\,Output) = \frac{P_{OUT} \times 2}{V_{OUT} \times D_{MAG}} = \frac{30}{16.6 \times 0.425} = 4.25\,A$$

(1.6 A_{rms}) (26)

5.2.12 Output Diodes

5.2.12.1 +24 V Output Diode (D_{G1})

Equation 27 shows the calculation for the diode reverse voltage (V_{RDG}).

$$V_{RDG1} = V_{OUT1} + \frac{V_{INMAX}}{a1} = 24 + \frac{1200}{12} = 124\,V \quad (27)$$

Equation 28 shows the calculation for the peak output diode (I_{DGPK}).

$$I_{DG1PK} = I_{S1PK} = 8.6\,A \quad (28)$$

For this design, Schottky diode of 20 A, 200-V rating with a forward voltage drop (V_{FDG}) of 0.88 V is used.

V_{FDG} = 0.88 V

Equation 29 calculates the estimated diode power loss (P_{DG}).

$$P_{DG1} = \frac{P_{OUT1} \times V_{FDG}}{V_{OUT}} = \frac{45 \times 0.88}{24} = 1.65\,W \quad (29)$$

5.2.12.2 +16 V Auxiliary Output Diode (D_{G2})

Equation 30 shows the calculation for the diode reverse voltage (V_{RDG}).

$$V_{RDG2} = V_{AUX\_OUT} + \frac{V_{INMAX}}{a1} = 16 + \frac{1200}{12} = 116\,V \tag{30}$$

Equation 31 shows the calculation for the peak output diode (I_{DG2PK}).

$$I_{DG2PK} = I_{AUX\_PK} = 4.25\ A\ (1.6\ A_{rms}) \tag{31}$$

For this design a 3 A, 200-V super-fast rectifier (MURS320-13-F) with a forward voltage drop (V_{FDG}) of 875 mV at 3 A was selected.

Equation 32 determines the estimated diode power loss (P_{DG2}).

$$P_{DG2} = \frac{P_{AUX\_OUT} \times V_{FDG2}}{V_{AUX\_OUT}} = \frac{15 \times 0.875}{16} = 0.82\,W \tag{32}$$

The same diode has been used for ±16 V output and isolated +6 V output.

5.2.13 Output Capacitors

Equation 33 shows the calculation for selecting the output ESR based on 90% of the allowable output ripple voltage.

$$ESR_{COUT\_24V} = \frac{V_{ripple} \times 0.9}{I_{SPK}} = \frac{250\,m \times 0.9}{8.6\,A} = \approx 26\,m\Omega \tag{33}$$

Equation 34 through Equation 37 show the calculations for selecting the output capacitors, which was selected based on the required ripple voltage requirements.

$$C_{OUT\_24V} \geq \frac{20\,\mu \times \frac{P_{OUT}}{V_{OUT} \times 2}}{V_{ripple}} = \frac{20\,\mu \times \frac{45}{24 \times 2}}{0.025} = \approx 750\,\mu F \tag{34}$$

$$C_{OUT\_16V} \geq \frac{20\,\mu \times \frac{4.5}{16 \times 2}}{0.025} = \approx 120\,\mu F \tag{35}$$

$$C_{OUT\_6V} \geq \frac{20\,\mu \times \frac{0.5}{6 \times 2}}{0.01} = \approx 120\,\mu F \tag{36}$$

$$C_{OUT\_AUX} \geq \frac{20\,\mu \times \frac{15}{16 \times 2}}{0.1} = \approx 120\,\mu F \tag{37}$$

Equation 38 shows the calculation for estimating the total output capacitor RMS current (I_{COUT_RMS}).

$$I_{COUT\_RMS} = \sqrt{\left(\frac{I_{SPK} \times \sqrt{D_{MAG}}}{\sqrt{3}}\right)^2 - \left(\frac{P_{OUT}}{\sqrt{3}}\right)^2} \tag{38}$$

$$I_{COUT\_RMS\_24V} = \sqrt{\left(\frac{8.6 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{45}{24}\right)^2} = 2.6\,A \tag{39}$$

Two 330 µF, 35-V aluminum-electrolytic capacitors with ripple-current ratings of 1.43 A are connected in parallel at the output diode to support the ripple current.

$$I_{COUT\_RMS\_16V} = \sqrt{\left(\frac{0.638 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{4.5}{16}\right)^2} = 640\,mA \tag{40}$$

A 120 µF, 50-V capacitor with a ripple-current rating of 1.6 A is connected at both +16 V and –16 V outputs.

$$I_{COUT\_RMS\_6V} = \sqrt{\left(\frac{0.357 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{0.5}{6}\right)^2} = 0.1A \quad (41)$$

$$I_{COUT\_RMS\_AUX} = \sqrt{\left(\frac{4.25 \times \sqrt{0.425}}{\sqrt{3}}\right)^2 - \left(\frac{15}{16}\right)^2} = 1.3A \quad (42)$$

A 120 µF, 50-V capacitor with a ripple-current rating of 1.6 A is used in this design.

5.2.14 MOSFET Selection

To meet the voltage and current requirements, 950 V, 2-A rated MOSFET (STF2N95K5) with the following characteristics is chosen.

R_{DSON} = 4.2 Ω

C_{OSS} = 9 pF

I_{DRIVE} = 0.025 A, maximum FET gate drive turn ON current (limited by UCC28711)

Maximum gate-sink current is internally limited and is approximately 0.2 A

Q_g = 10 nC, gate charge just above the Miller plateau

Equation 43 determines the estimated VDS fall time.

$$t_f = \frac{Q_g}{I_{drive}} = \frac{10nC}{0.2A} = 50ns \quad (43)$$

5.2.14.1 FET Average Switching Loss (P_{sw})

$$P_{SW} = \frac{1}{2} V_{PK} \times I_{PK} \times T_F \times F_{SW} = \frac{1}{2} \times 800 \times 1 \times 50n \times 50kHz = 1W \quad (44)$$

5.2.14.2 Power Loss by Driving the FET Gate (P_g):

$P_g = 14\ V \times Q_g \times f_{max} = 14\ V \times 10\ nC \times 50\ kHz = 7\ mW$ (45)

Qg1, gate charge at 10-V drive clamp

V_g = 14 V

5.2.14.3 FET C_{oss} Power Dissipation (P_{coss})

Equation 46 and Equation 47 determine the average FET drain to source capacitance.

$$2 \times C_{OSS} \times \sqrt{\frac{V_{DS\_TEST}}{V_{DS}}} = 2 \times 9pF \times \sqrt{\frac{100}{800}} = 6.4pF \quad (46)$$

$$P_{COSS} = \frac{C_{OSS}}{2} \times V_{PK}^2 \times F_{MAX} = \frac{6.4p}{2} \times 800^2 \times 50kHz = 0.1W \quad (47)$$

5.2.14.4 Power Loss from R_{dson} (P_{RDSON})

$$P_{RDSON} = I_{PRMS}^2 \times R_{DSON} = 0.334^2 \times 4.2 = 0.47\,W \quad (48)$$

Total power loss per MOSFET = 1 + 0.1 + 0.47 = 1.57 W (49)

Thermal resistance of MOSFET, Junction to Case, Max = 2.78°C/W (50)

Thermal resistance of heat sink, Max = 15°C/W (51)

MOSFET temperature rise = 17.78 × 1.57 = 28°C/W (52)

With ambient temperature varying from –20°C/W to 65°C/W, the FET temperature should be in the range of 8°C to 93°C (less than 150°C as specified in MOSFET STF2N95K5 data sheet).

MOSFET with a voltage rating of ≥ 1000 V can be used if higher de-rating is required to enhance reliability.

5.2.15 Input-Voltage Sensing

ac input voltage and dc link voltage are measured in the drives for various reasons.

1. Detection of single phase failure
2. dc link undervoltage and overvoltage condition
3. For controlling the inverter output voltage

When the drive application does not mandate high-accuracy measurements, the flyback converter can be used to measure the ac input as well as the dc link voltage. When the primary switch is ON, the induced voltage at the secondary (see D24 in Figure 17) will be the dc link voltage times the turn ratio, which will also be proportional to the ac mains input voltage. This voltage is rectified and filtered with RC network. Voltage scaling can be performed based on the ADC input-voltage range.

At 1200 V dc input with a turns ratio of 18, the forward-induced voltage is determined by Equation 53 and Equation 54.

$$V_{dc_{MEAS}}(MAX) = \frac{1200}{18} = 66.67\,V \quad (53)$$

$$V_{dc_{MEAS}}(MIN) = \frac{400}{18} = 22.22\,V \quad (54)$$

The voltage determined in Equation 53 and Equation 54 is stepped down through a resistive divider $\frac{1k}{11k}$ to scale it to 6.06 V and 2.02 V. This step-down ratio can be adjusted based on the application requirements.

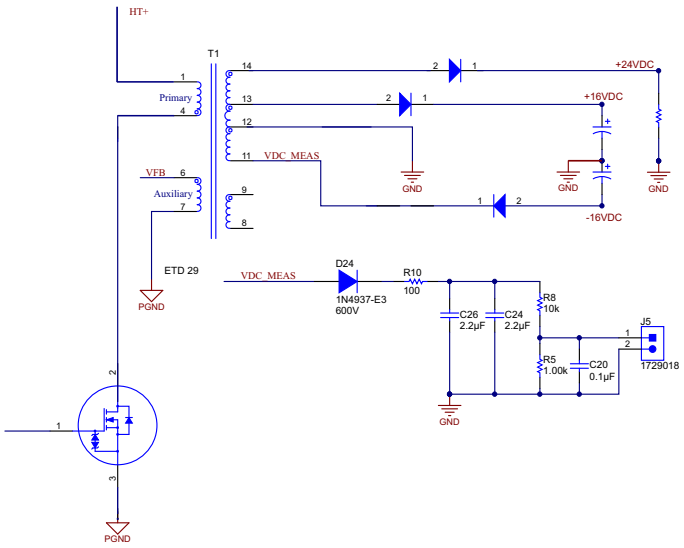

Figure 17. DC Link Voltage Measurement

5.2.16 Transformer Construction

Table 1. Magnetic Details

Core Type	Core Material	Bobbin
ETD29	CF138/N87	14 Pin (Vertical)

Table 2. Winding Details(1)

Winding	No. of Turns	Start Pin	End Pin	Inductance
W1	142	4	1	2.5 mH ± 10%
W2	8	6	7	–
W3 Tapped	4	14	13	–
	8	13	12	–
W4	8	12	11	–
W5	3	9	4	–

(1) Use of Litz wire would help in reducing losses in the transformer.

Electrical Requirements:

- Leakage inductance between pins 1 and 4 with all other pins shorted to 100 μH max
- Use triple insulated wire for W3, W4, W5

Winding Procedure:

- Wind 48 turns of primary (W1) in one layer, starting at pin 4 and finishing at pin 3
- Basic insulation
- Wind bias (W2) uniformly spread in one layer, starting at pin 6 and ending at pin 7
- Reinforced Insulation
- Wind W3 in one layer; start at pin 14 and wind 4 turns ending at pin 13; continue at pin 13 and wind 8 more turns to end at pin 12
- Basic insulation
- Wind W4 uniformly spread in one layer, starting at pin 12 and ending at pin 11
- Reinforced insulation
- Wind remaining 94 turns of primary (W1) in two layers, starting at pin 3 and finishing at pin 1
- Reinforced insulation
- Wind W5 uniformly spread in one layer, starting at pin 9 and ending at pin 8
- Reinforced insulation
- Gap core suitably to get required primary inductance
- Bond the core to avoid audible noise
- Vacuum impregnate with varnish
- Cut off pin 3 without damaging the termination on it

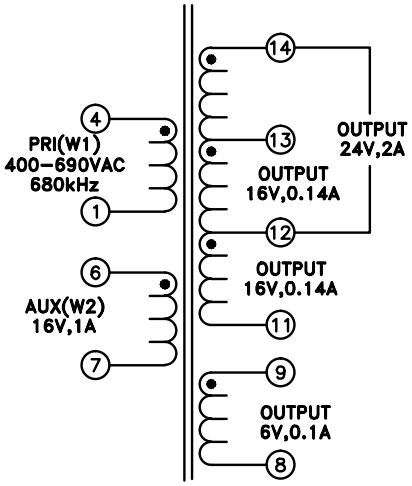

Figure 18. Transformer Pinout

6 Test Data

6.1 Functional Test Results

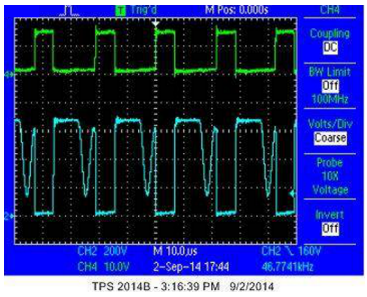

Figure 19. Lower FET Voltage at 400-V Input, 50-W Output (CH4: V_{gs} and CH2: V_{ds})

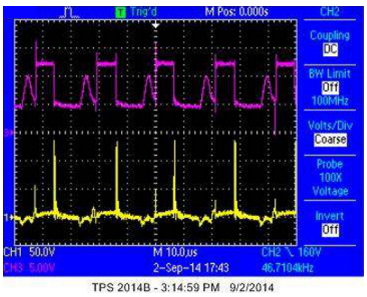

Figure 20. Upper FET Voltage at 400-V Input, 50-W Output (CH3: V_{gs} and CH1: V_{ds})

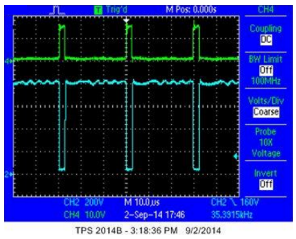

Figure 21. Lower FET Voltage at 1200-V Input, 50-W Output (CH4: V_{gs} and CH2: V_{ds})

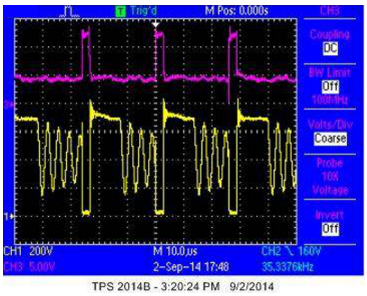

Figure 22. Upper FET Voltage at 1200-V Input, 50-W Output (CH3: V_{gs} and CH1: V_{ds})

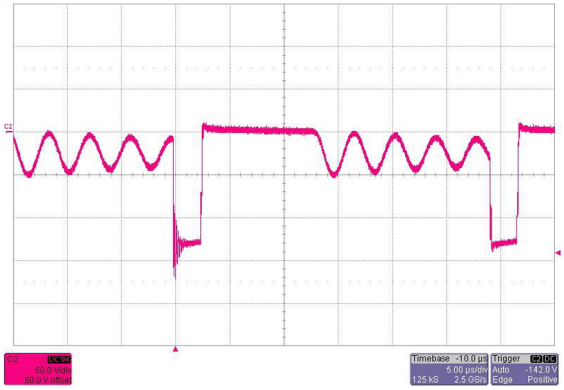

Figure 23. 24-V Output Diode Voltage Stress with V_{IN} = 1200 V DC and 50-W Output

6.2 Output Ripple Under Different Test Conditions

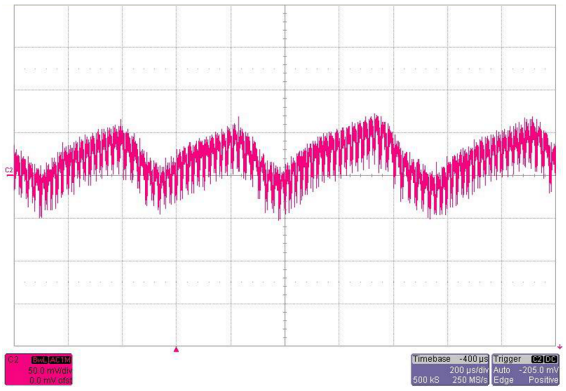

Figure 24. Ripple at 24-V Output with V_{IN} = 400 V DC and Full Load

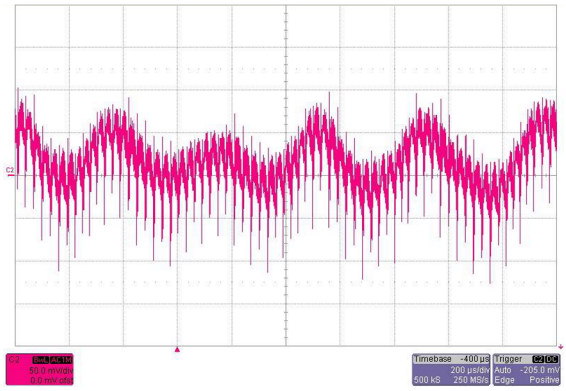

Figure 25. Ripple at 24-V Output with V_{IN} = 1200 V DC and Full Load

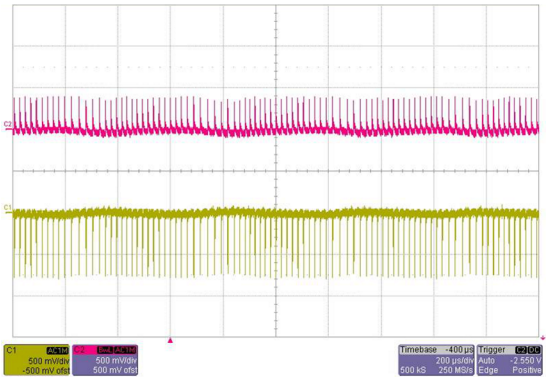

Figure 26. Ripple at ±16-V Output with V_{IN} = 400 V DC and Full Load (CH2: +16 V, CH1: –16 V)

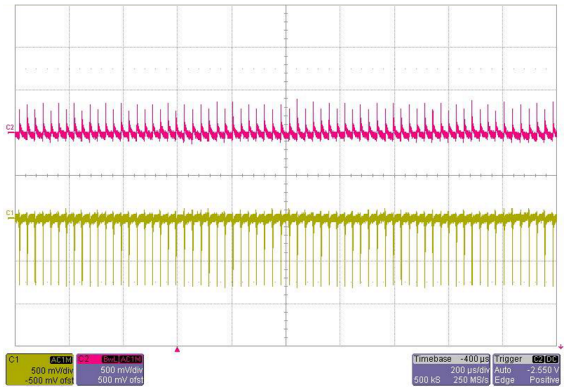

Figure 27. Ripple at ±16–V Output with V_{IN} = 1200 V DC and Full Load (CH2: +16 V, CH1: –16 V)

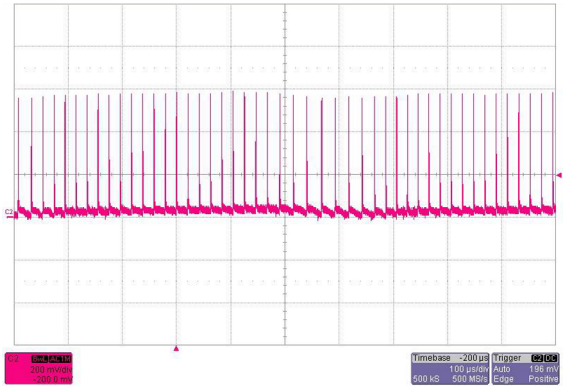

Figure 28. Ripple at +6-V Output with V_{IN} = 400 V DC and Full Load

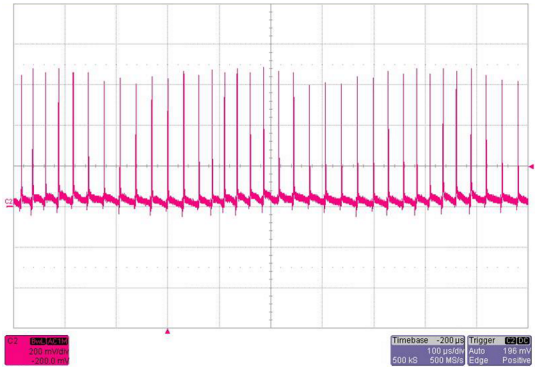

Figure 29. Ripple at +6-V Output with V_{IN} = 1200 V DC and Full Load

6.3 Efficiency

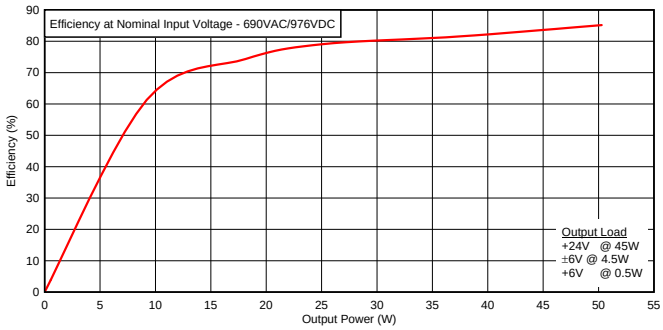

Figure 30. Efficiency vs Output Load at V_{IN} = 976 V DC

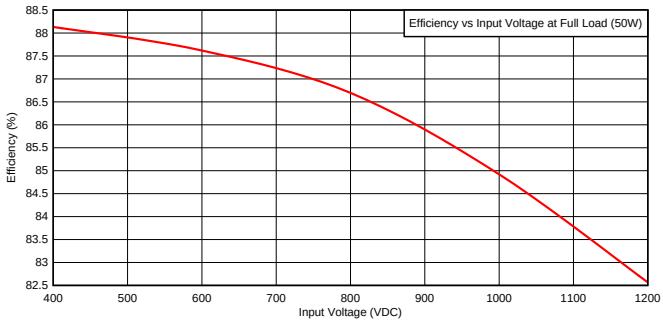

Figure 31. Efficiency vs Input Voltage at P_o = 50 W

6.4 Line Regulation

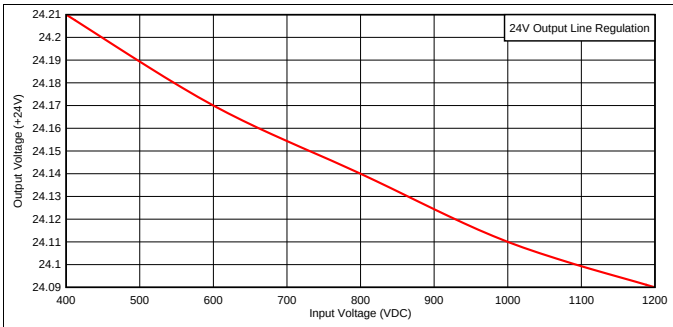

Figure 32. 24-V Output Line Regulation with 45-W Load

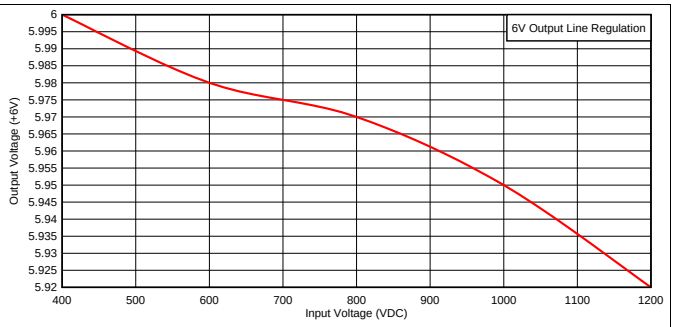

Figure 33. 6-V Output Line Regulation with 0.5-W Load

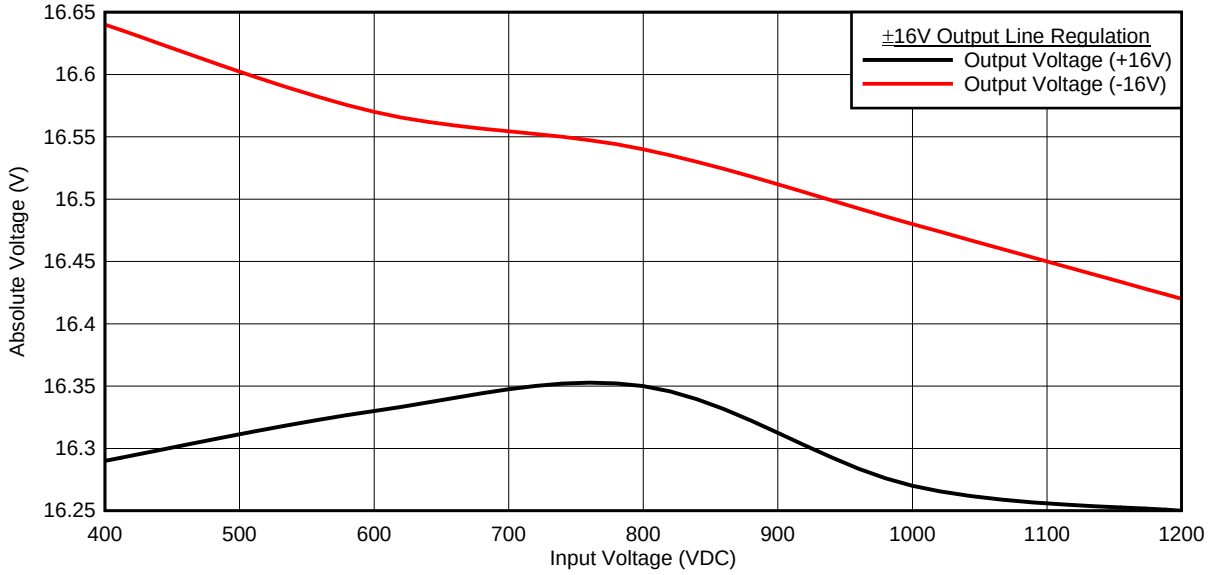

Figure 34. ±16-V Output Line Regulation with 4.5-W Load

6.5 Load Regulation

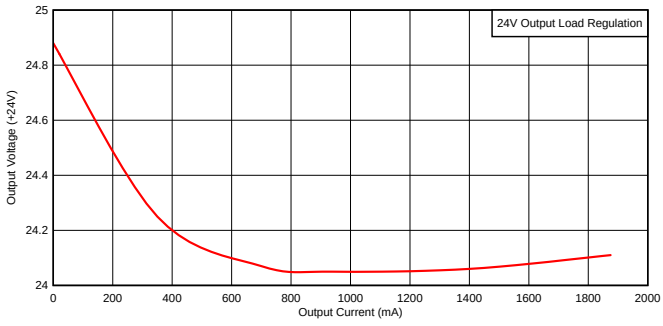

Figure 35. +24-V Output Load Regulation with V_{IN} = 976 V DC

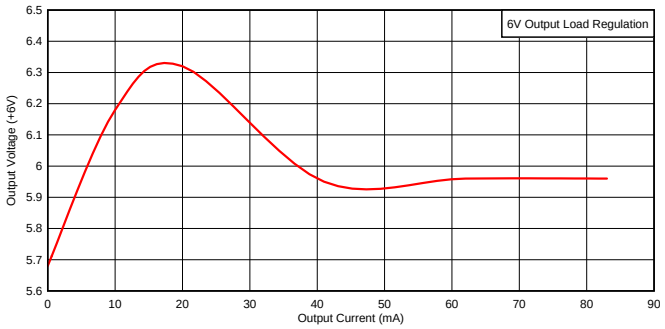

Figure 36. +6-V Output Load Regulation with V_{IN} = 976 V DC

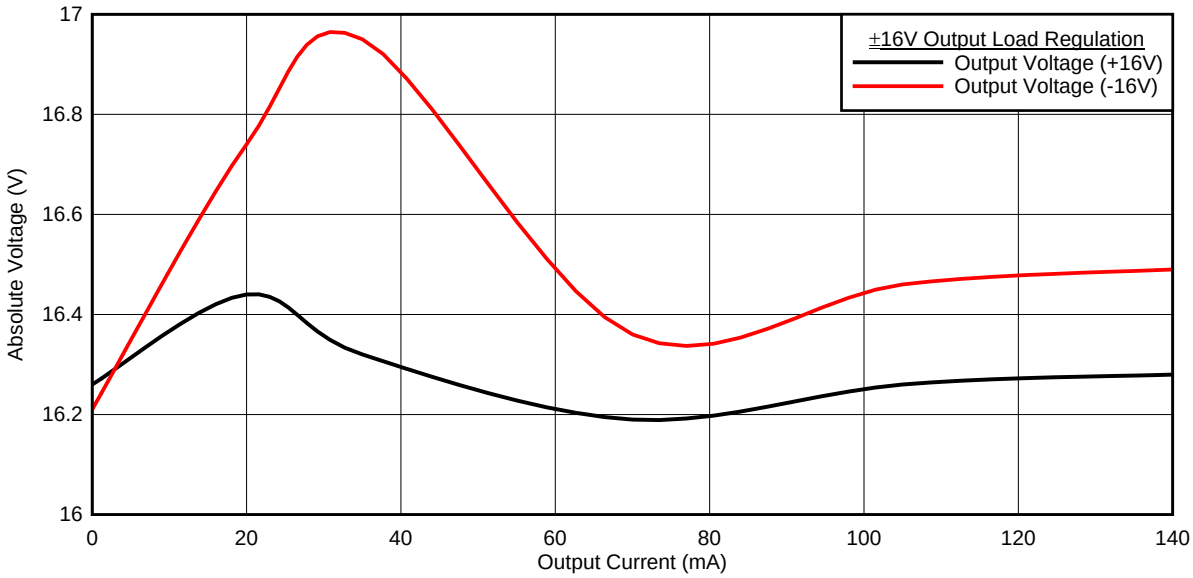

Figure 37. ±16-V Output Load Regulation with V_{IN} = 976 V DC

6.6 Overload Test and Output Power Limit

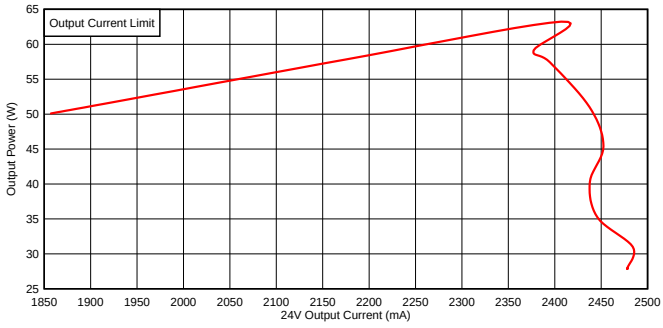

Figure 38. Overload and Current Limit at +24-V Output with V_{IN} = 976 V DC

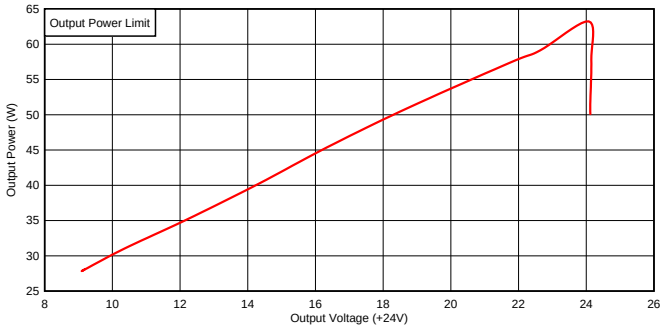

Figure 39. Overload at +24-V Output Voltage vs Output Power with V_{IN} = 976 V DC

6.7 dc Link Voltage Measurement

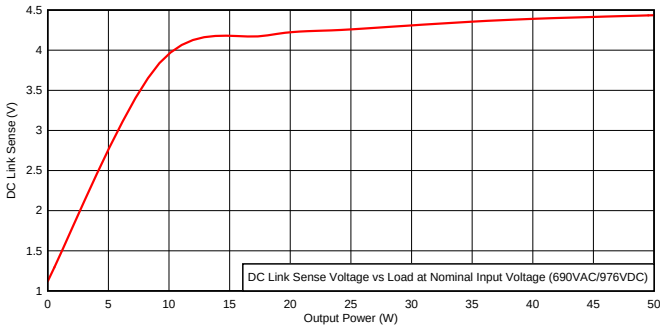

Figure 40. DC Link Voltage Measurement with Varying Output Load

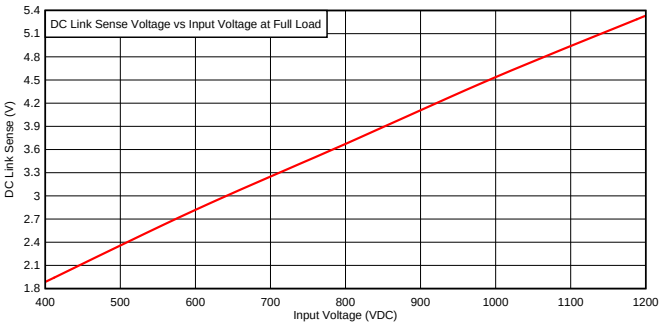

Figure 41. DC Link Voltage Measurement with Full Load

6.8 Undervoltage and Overvoltage Test

Figure 42 and Figure 43 capture the input overvoltage and under voltage limits. When the input voltage exceeds 1220 V dc, the PWM controller is shut down and it recovers when the input voltage falls back to approximately 950 V dc. The hysteresis in turnoff and turnon voltage can be adjusted by varying R29.

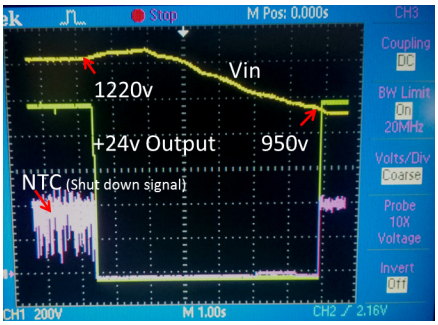

Figure 42. DC Link Voltage Measurement with Full Load

The power supply turns ON at approximately 375 V dc and shuts down when the input voltage reduces below 150 V dc. The ratio of turn ON to turn OFF is fixed for under-voltage shutdown operation and is controlled within the UCC28711 device .

Figure 43. DC Link Voltage Measurement with Full Load

7 Layout Guidelines for UCC28711

Good layout is critical for proper functioning of the power supply. Major guidelines on the layout for the proper functioning of the controller is described in Figure 44, Figure 45, and Figure 46.

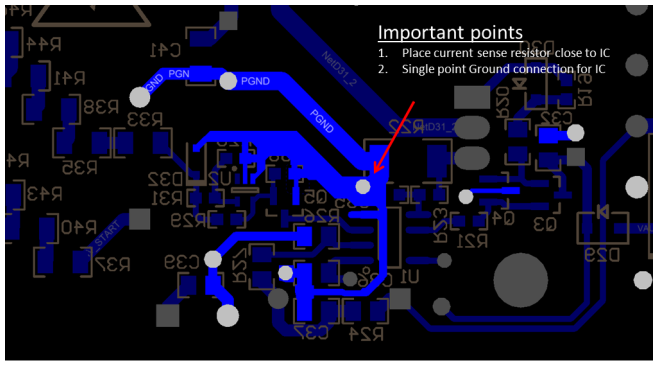

Figure 44. Layout Diagram One

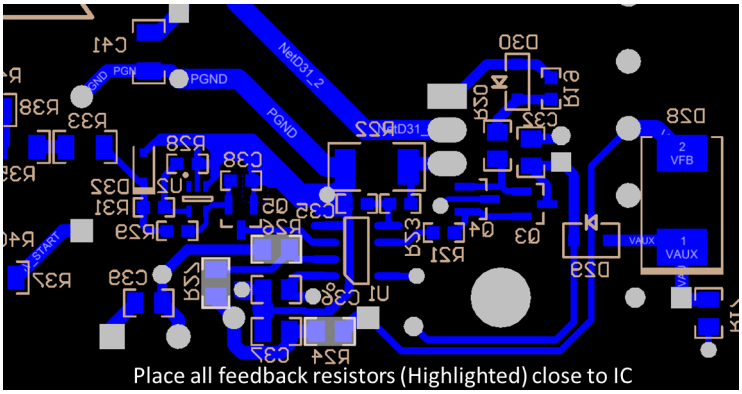

Figure 45. Layout Diagram Two

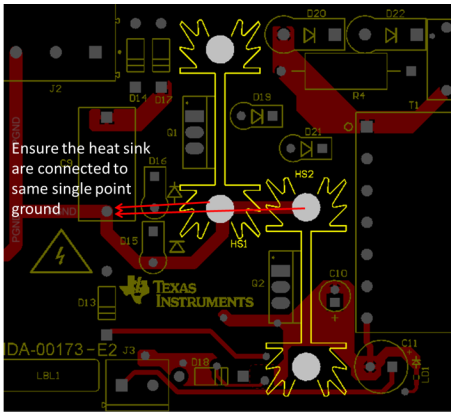

Figure 46. Layout Diagram Three

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00173.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00173.

8.3 Layer Plots

To download the layer plots, see the design files at TIDA-00173.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00173.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00173

9 Related Documentation

1. UCC28700 data sheet, *5-W USB Fly-back Design Review/Application Report* (SLUA653)
2. UCC28711 data sheet, *Constant-Voltage, Constant-Current Controller with Primary-Side Regulation* (SLUSB86)
3. LMS33460 data sheet, *LMS33460 3V Under Voltage Detector* (SNVS158)
4. MOSFET STF2N95K5 data sheet, *N-channel 950 V, 4.2 Ω typ., 2 A Zener-protected SuperMESH™ 5 Power MOSFETs in DPAK, TO-220FP, TO-220 and IPAK packages* (www.mouser.com)

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10 About the Author

SALIL CHELLAPPAN is a Lead Engineer, Member, and Group Technical Staff at Texas Instruments, where he is responsible for developing customized power solutions as part of the Power Design Services group. Salil brings to this role his extensive experience in power electronics, power conversion, EMI/EMC, power and signal integrity, and analog circuits design spanning many high-profile organizations. Salil holds a Bachelor of Technology degree from the University of Kerala.

N. NAVANEETH KUMAR is a Systems Architect at Texas Instruments, where he is responsible for developing subsystem solutions for motor controls within Industrial Systems. N. Navaneeth brings to this role his extensive experience in power electronics, EMC, analog and mixed signal designs. He has system-level product design experience in drives, solar inverters, UPS, and protection relays. N. Navaneeth earned his Bachelor of Electronics and Communication Engineering from Bharathiar University, India and his Master of Science in Electronic Product Development from Bolton University, UK.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2014) to B Revision	Page
• Changed *Input Section* image	12
• Changed *Start-Up Circuit* image	18
• Deleted the schematic, BOM, and layer plots from *Design Files*	31
• Added links to the schematic, BOM, and layer plots to *Design Files*	31

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