TI Designs

16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design

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Design Resources

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OPA140	Product Folder
OPA192	Product Folder
OPA350	Product Folder
ADS8864	Product Folder
MUX36D04	Product Folder
TINA-TI™	Product Folder

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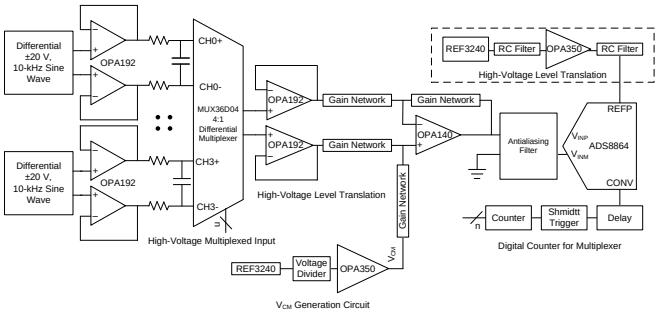
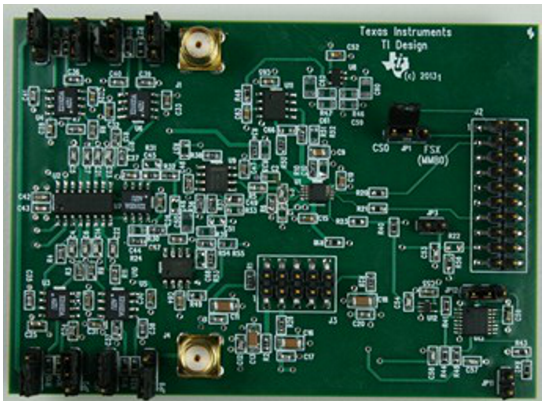
Circuit Description

This design is for a 16-bit, differential four-channel multiplexed data acquisition (DAQ) system at a 400-kSPS throughput for a high voltage differential input of ±20-V (differential 40 V_{pk-pk}) industrial applications. The circuit is realized with a 16-bit successive-approximation-register (SAR) analog-to-digital converter (ADC), a precision high voltage signal conditioning front end, and a four-channel differential multiplexer (MUX). The design details the process for optimizing the front-end drive circuit using the OPA192, OPA140, and MUX36D04 to achieve excellent dynamic performance with the ADS8864.





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1 Design Summary

The primary goal of this guide is to design a ±20-V, differential, four-channel multiplexed data acquisition (DAQ) system with the lowest distortion using the 16-bit ADS8864 analog-to-digital converter (ADC) at a throughput of 400 kSPS for a 10-kHz, full-scale, pure-sine-wave input. The design requirements for this design are:

- System supply voltage: ±15-V DC
- ADC supply voltage: 3.3-V DC
- ADC sampling rate: 400 kSPS
- ADC reference voltage (V_{REF}): 4.096-V DC
- System input signal: A high-voltage differential input signal with amplitude of V_{pk} = 10 V and frequency of f_{IN} = 10 kHz are applied to each differential input of the multiplexer

Table 1 summarizes the design goals and performance.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

PARAMETER	GOAL	CALCULATED OR SIMULATED	MEASURED
Integral nonlinearity (INL)	< ±1 LSB	—	< ±0.9 LSB
Total harmonic distortion (THD)	< –95 dB	—	–95 dB
16-bit, full-scale, channel-to-channel settling	< ±1 LSB	< ±1 LSB	< ±1.2 LSB
Signal-to-noise ratio (SNR)	> 86 dB	89 dB	87.46 dB (avg)
Effective number of bits (ENOB)	>14 bits	—	14.18

Figure 1 shows the measurement results of the ADC INL plot for the DAQ block.

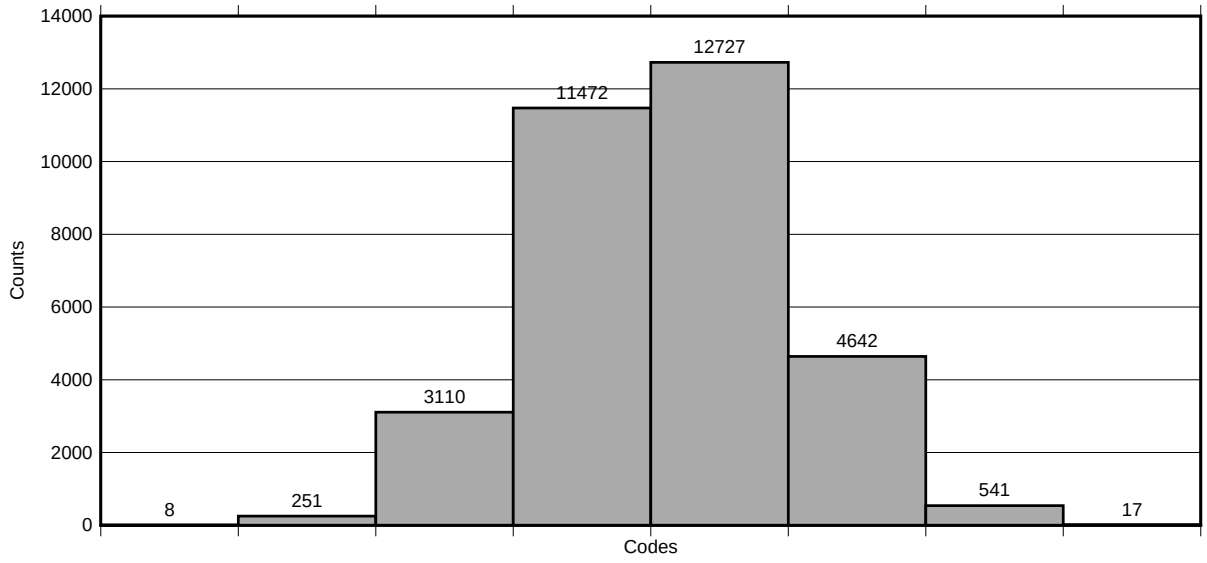

Figure 1. Measurement Result of ADC INL Plot for Multiplexed DAQ Block

2 Theory of Operation

The purpose of this TI Precision Design is to synthesize an optimal, high-voltage, multiplexed DAQ system for highest system linearity and fast settling. Figure 2 shows the overall system block diagram. The circuit is a multichannel, DAQ signal chain consisting of an input low-pass filter, multiplexer (MUX), MUX output buffer, attenuating SAR ADC driver, a digital counter for the MUX, and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low cost solution. The two primary design considerations to maximize the performance of a precision, multiplexed DAQ system are the MUX input analog front end (AFE) and the driver design for the high-voltage level translation SAR ADC. However, each analog circuit block must be carefully designed based on the ADC performance specifications to achieve the fastest settling at a 16-bit resolution and the lowest distortion system. The diagram in Figure 2 includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely-low impedance input filter design for the MUX. This understanding is detrimental when selecting an appropriate input filter and MUX to meet the system settling requirements. The next important step is designing the attenuating AFE used to level translate the high-voltage input signal to a low-voltage ADC input while maintaining the amplifier stability. The next step is to design a digital interface to switch the MUX input channels with minimum delay. The final design challenge is to design a high-precision reference driver circuit that provides the required V_{REF} reference voltage with low offset, drift ,and noise contributions.

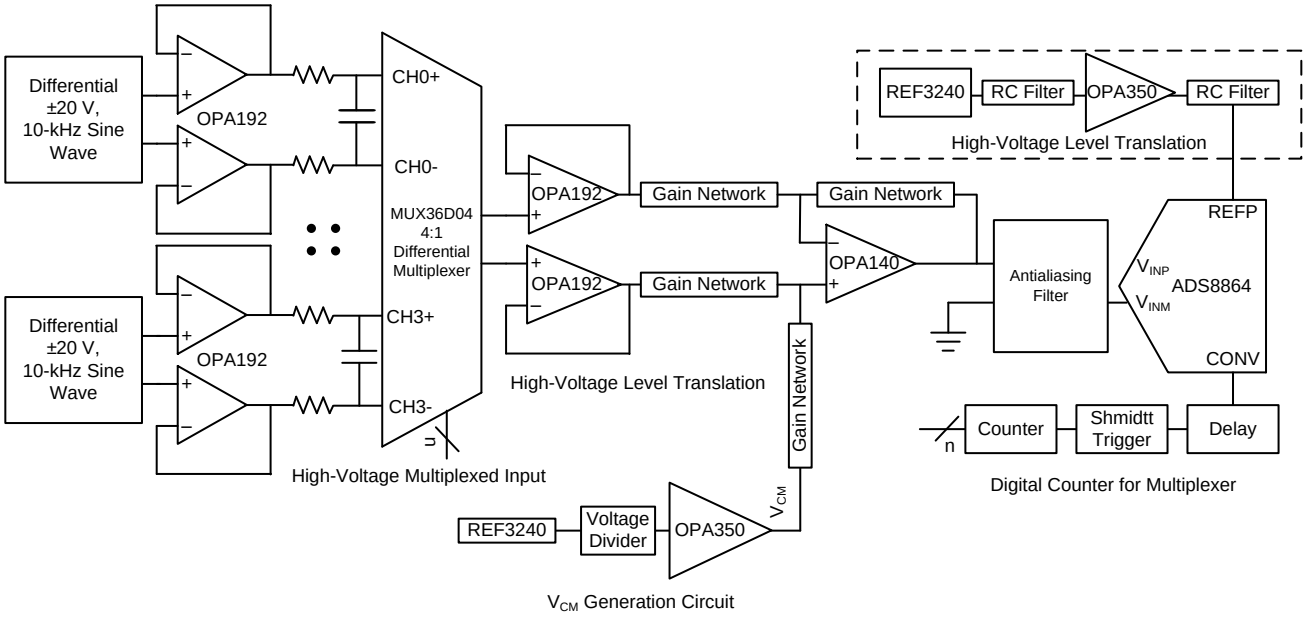

Figure 2. Block Diagram Highlighting Primary Design Criteria for Multiplexed DAQ Block

2.1 Understanding ADC Dynamic Performance

The main AC specifications under consideration for this design are signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and the effective number of bits (ENOB). Essentially, all these parameters are different ways of quantifying the noise and distortion performance of an ADC based on a fast-Fourier transform (FFT) analysis. Refer to the *Data Acquisition Optimized for Lowest Distortion, Lowest Noise, 18bit, 1MSPS Reference Design* for more details [1].

2.2 Understanding DAQ Linearity Requirements

The design that the preceding Figure 2 shows merges the four-channel differential input signals into a time-division-multiplexed signal by the multiplexer after configuring for continuous switching mode operation. The multiplexed input signals in most programmable logic controller (PLC) applications consist of large voltages that can vary anywhere within the input range of the design. This variation causes large voltage steps on the output of the MUX when switching between channels. The signal chain must be carefully designed to achieve the high linearity for each channel. For this reason, understanding the sources of nonlinearity in the signal chain and to design and select components that achieve the lowest distortion is important. This section systematically outlines the considerations for achieving a true 16-bit linearity in each block.

2.2.1 Low Impedance at Multiplexer Inputs

Figure 3 shows a simplified model for a MUX. Each channel of a MUX can be modeled as a series combination of capacitors and resistors. C_S and C_D represent the OFF switch source and drain capacitance respectively. R_{ON_MUX} is the ohmic resistance between terminal D (drain) and terminal S (source). Most MUX data sheets provide these specifications.

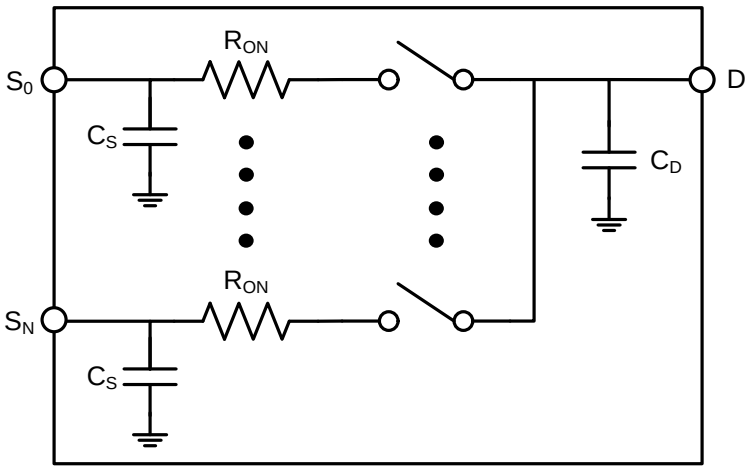

Figure 3. Simplified Multiplexer Model

Multiplexers usually feature a low R_{ON_MUX}, which results in a large drain capacitance C_D. This capacitance is switched from one channel to the next during the operation and must be recharged to the new input channel voltage. In a PLC application the input channel can be high impedance. The high input source impedance creates a low-pass filter, which does not allow the drain capacitance of the MUX to properly settle to the next channel input voltage. This occurrence introduces signal dependent distortion, which is further explained in the following paragraphs. So, in a precision data acquisition circuit, driving the MUX input (S_N) with a very low impedance driver is important, as Figure 4 shows.

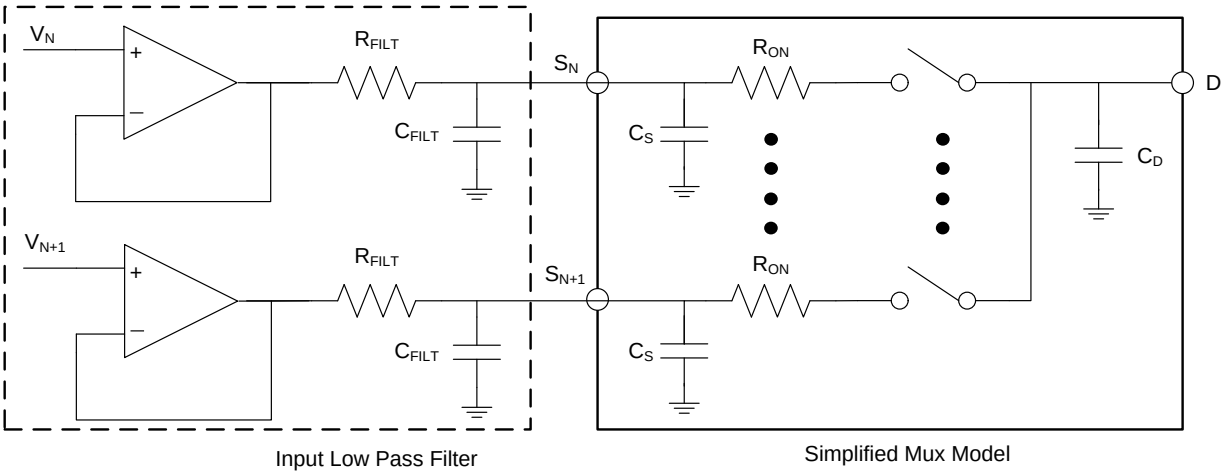

Figure 4. Charge Transfer Between Input Low-Pass Filter and Multiplexer Drain Capacitance

In this architecture, carefully selecting the value of C_{FILT} is important. If the value has not been correctly selected, the charge transfer between the filter capacitor and drain capacitance of the MUX introduces signal dependent distortion and a voltage error at the output of the MUX. Equation 1 is used to derive and express this signal dependent error:

Previous Input Channel Charge at MUX Output: $Q_D = C_D \times V_N$

Next Input Channel Charge at MUX Output: $Q_{N+1} = (C_{FILT} + C_S) \times V_{N+1}$

$$Q_{D+1} = Q_D + Q_{N+1} = \left((C_{FILT} + C_S) \times V_{N+1}\right) + (C_D \times V_N)$$

Next Input Channel MUX Output: $$V_{D+1} = \frac{\left[\left((C_{FILT} + C_S) \times V_{N+1}\right) + (C_D \times V_N)\right]}{C_{FILT} + C_D + C_S}$$

$$\Delta V_{ERROR} = V_{N+1} - V_{D+1} = \left[V_{N+1} - \left(\frac{\left((C_{FILT} + C_S) \times V_{N+1}\right) + (C_D + V_N)}{C_{FILT} + C_D + C_S}\right)\right] \quad (1)$$

Equation 1 clearly shows the previous channel charge as being a part of the next channel output voltage of the MUX; therefore, the input of the MUX must have very low impedance to settle to the next channel voltage to less than 1 LSB in the available acquisition time.

The value of the capacitor C_{FILT} must be chosen such that when MUX switches channels, the voltage droop on the input of the MUX is less than 5% to 10% of the peak-to-peak input full-scale voltage range (V_{FSR}). The buffer amplifier helps settle the remaining input signal within the acquisition time (see Equation 2).

$$\Delta V_{ERROR} < (0.1) \times V_{FSR} \quad (2)$$

The requirement in Equation 2 helps to provide instant charge transfer and reduces the overall step response required to be settled by the buffer amplifier. A minimum C_{FILT} component value can be calculated to meet the settling requirement based on the worst-case possible voltage step (V_{FSR}). After combining Equation 1 and Equation 2, the value of C_{FILT} can be calculated using Equation 3.

$$C_{FILT} > \left(\frac{C_D}{0.1}\right) - C_D - C_S \quad (3)$$

At this point in the design, understanding the trade-offs involved in selecting the values of C_{FILT} and R_{FILT} is important. If the value of C_{FILT} is high, it provides better attenuation against the kick-back noise when the MUX switches channels. However, C_{FILT} cannot be made arbitrarily high because it degrades the phase margin of the driving amplifier, making it unstable. Furthermore, the chosen capacitor must be of the COG- or NPO-type because these capacitors types have a high Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time. Therefore, the selected COG capacitor also places a physical limit on the capacitor value.

In the low-pass filter shown in the preceding Figure 4, the series resistor R_{FILT} acts as an isolation resistor, which helps to stabilize the driving amplifier. During transitions, the capacitor appears as an AC short and can draw significant current from the output of the amplifier. The R^{FILT} resistor also helps limit the output current from the amplifier during this condition. However, a higher value of R_{FILT} degrades the settling performance and must be balanced with the amplifier stability and output current limit to ensure that the settling does not exceed the required specifications. The settling performance can be simulated in spice software like
TI-TINA™ to make the correct trade-off.

The bandwidth of the filter (BW_{FILT}) can then be calculated based on the input filter resistor and capacitor (see Equation 4).

$$BW_{FILT} = \frac{1}{2\pi \times R_{FILT} \times C_{FILT}} \quad (4)$$

There is another MUX parameter that R_{FILT} interacts with that must be taken into account; a MUX leakage current, which is current that flows from the source and drain pins. While the MUX switch is OFF, the currents on each pin from both sides of the open switch are added; while ON, there is only one current flow present originating on the drain side of RON. When the switch is closed this leakage current introduces an offset error. Sizing the R_{FILT} too large can increase the offset voltage error; this will only be augmented if the MUX leakage current is also high, which overall degrades the ADC performance; the following Equation 5 demonstrates this relation.

$$\text{Offset Error (V)} = I_{LEAKAGE} \times R_{FILT} \quad (5)$$

The ultimate objective is for a low MUX leakage current because this decreases the offset error and in turn decreases the code offset error, which can have a great impact on performance in high-precision ADCs, such as the 16-bit ADS8865.

2.2.2 High Impedance at Multiplexer Output

In a multiplexed DAQ system the input channels are time multiplexed. Each channel output eventually interfaces with the ADC for conversion. Interfacing the output of the MUX with a high impedance input is important. For this reason, TI does not recommend connecting the output of the MUX directly to an inverting amplifier or to the ADC inputs, as the diagrams in Figure 5 and Figure 6 show.

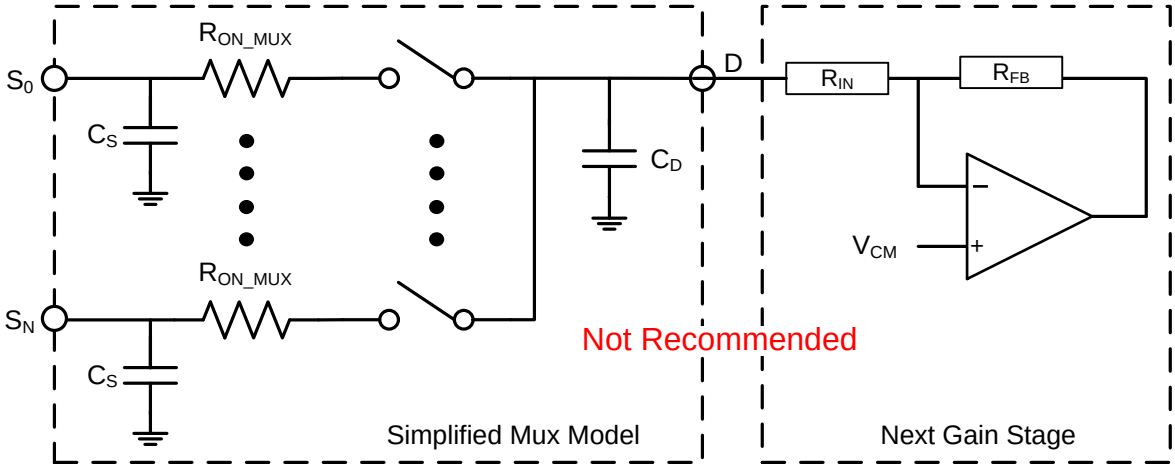

Figure 5. Low Output Impedance at MUX Output Introduces Distortion With Next Gain Stage (Not Recommended)

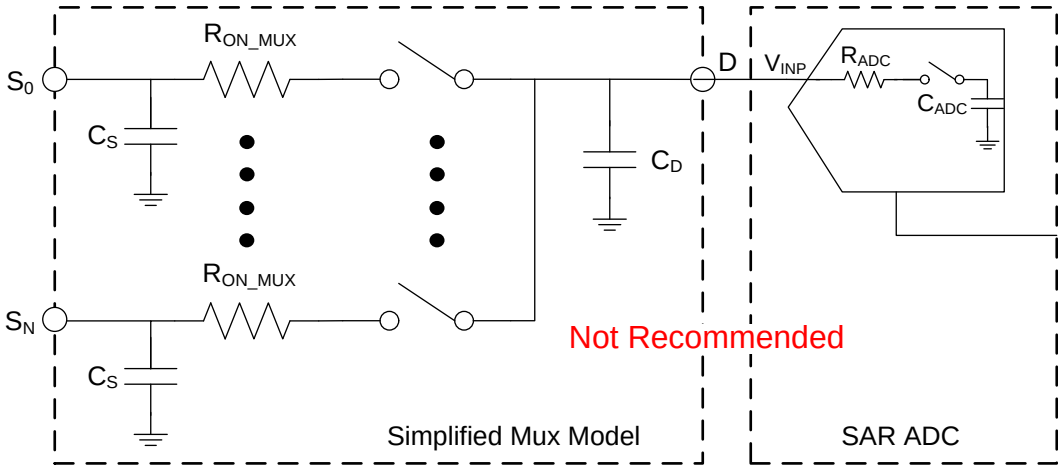

Figure 6. Low Output Impedance at MUX Output Introduces Distortion With SAR ADC (Not Recommended)

The switch resistance (R_{ON_MUX}) introduces finite gain error. Further, the switch resistance (R_{ON_MUX}) of each channel of the MUX varies over the input common-mode voltage. This value is specified in the typical data sheet curves of the MUX as R_{ON_MUX} flatness (ΔR_{ON_MUX} versus V_{Drain}). Figure 7 shows a typical shape of this curve. This change in R_{ON_MUX} introduces signal-dependent distortion (gain error linearity) based on the impedance at the output of the MUX.

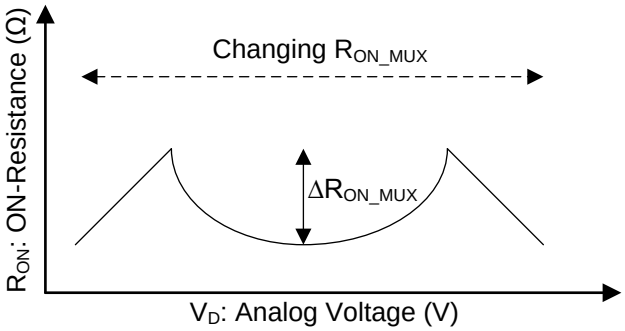

Figure 7. ON-Resistance vs V_D

The R_{ON_MUX} introduces gain error based on the input resistance, R_{IN}, of the circuit connected to the MUX "D" terminal (see Equation 6):

$$\text{Gain Error} = \left(1 - \frac{R_{IN}}{R_{IN} + R_{ON\_MUX}}\right) \times 100 \tag{6}$$

The R_{ON_MUX} flatness (ΔR_{ON_MUX} vs V_D) introduces gain linearity error (see Equation 7).

$$\text{Gain Error Nonlinearity} = \left(1 - \frac{R_{IN} + R_{ON\_MUX}}{R_{IN} + R_{ON\_MUX} + \Delta R_{ON\_MUX}}\right) \times 100 \tag{7}$$

Based on the preceding explanations and equations, interfacing to the output of the MUX with a high impedance stage is very important. This process eliminates any gain error and gain error nonlinearity introduced as a result of the MUX R_{ON_MUX} and R_{ON_MUX} flatness. The recommended approach is to have an amplifier buffer the output of the MUX, as the preceding Figure 2 shows. The input impedance of a CMOS amplifier is very high and thus it eliminates any gain error and nonlinearity introduced by the MUX. However, be careful during the selecting process for the amplifier because it affects the settling and noise performance of the DAQ system (see Section 2.3.3 for further detail).

2.2.3 Signal Attenuation and Level Translation Requirements

To reduce system power, a low-voltage SAR ADC is usually selected in a DAQ system. The SAR ADC is configured in a single-supply configuration and the ADC inputs can take the input signal voltage up to the reference voltage (V_{REF}) provided on the reference pin of the ADC. However, the input signals from a PLC front end are high voltages and are bidirectional on dual supplies. So interfacing these signals to the ADC inputs requires an attenuation stage with level translation. The following Figure 8 shows this stage.

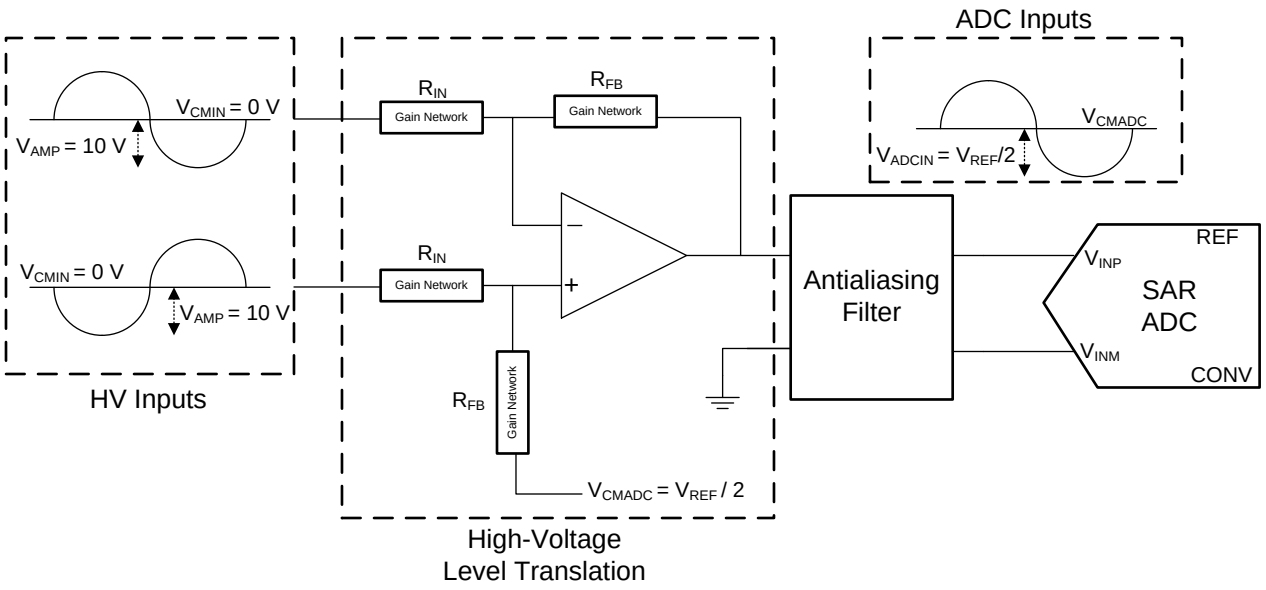

Figure 8. High-Voltage Level Translation Stage

The high-voltage, level-translation attenuation stage has been configured as a difference amplifier. The attenuation is set by the ratio of R_{IN} and R_{FB} (see Equation 8). The common-mode rejection for this stage is limited by a mismatch between the two R_{IN} resistors and the two R_{FB} resistors. TI recommends having a matched pair of resistors for R_{IN} resistors and R^{FB} resistors. The common-mode voltage level translation is achieved by providing a common-mode voltage at the V_{CMADC} node of the difference amplifier (see Equation 9). Section 2.2.4 explains this process in further detail.

$$\text{Attenuation} = \frac{R_{FB}}{R_{IN}} \tag{8}$$

$$V_{CMADC} = \frac{V_{REF}}{2} \tag{9}$$

To achieve the maximum dynamic range of the ADC, the input signal must swing from the ground to the V_{REF} voltage provided to the ADC. The common-mode voltage must be set as half of the V_{REF} voltage, as the preceding Equation 9 shows. All op amps have a defined output swing specification as provided in the respective data sheets. As the output swings closer to the op-amp power supply, it loses gain and thus the output distortion increases. For this reason, looking at the open-loop gain (A_{oL}) for the output swing condition specified is important. Selecting a high voltage amplifier and operating it on dual supplies ensures the maximum utilization of the dynamic range of an ADC.

2.2.4 Drive Requirements for V_{CM} of Difference Amplifier

As the previous subsection explains, the difference amplifier output requires level shifting to meet the input common-mode range of the ADC. This level shifting is accomplished by providing a voltage that is equal to half of the V_{REF} voltage of the ADC at the V_{CMADC} point, as derived in the preceding Equation 8. This voltage can be generated with a simple voltage divider from the reference voltage of the ADC. However, buffering the reference divider with an amplifier is extremely important, as Figure 9 shows.

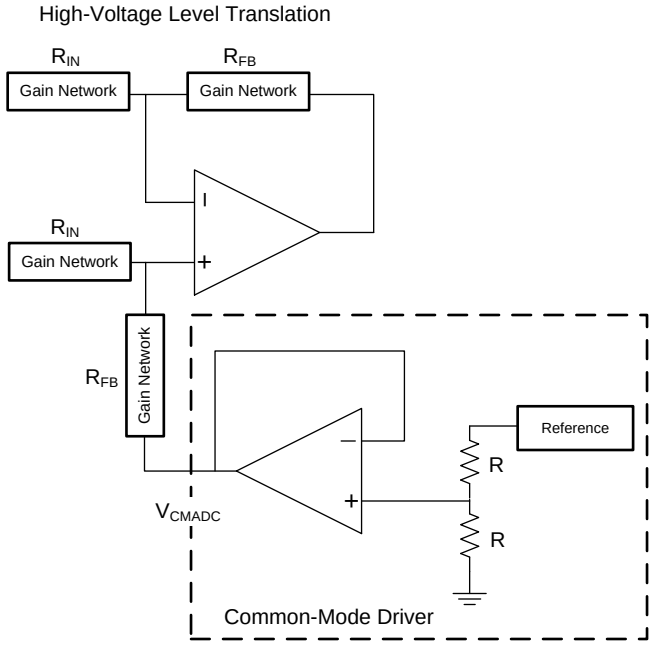

Figure 9. Difference Amplifier Common-Mode Driver

The V_{CMADC} is a lower impedance ($Z_{IN\_VCMADC} = R_{IN} \parallel R_{FB}$) node and thus requires to be driven by a very low impedance source to avoid gain error linearity at the output (see Equation 10). The buffer amplifier after the voltage divider provides low impedance. However, the closed-loop output impedance (R_{OUT}) of the amplifier is dependent on the frequency. At higher frequencies the output impedance increases for all amplifiers as the open-loop gain drops for the amplifier. Data sheets show the typical curve for open-loop output impedance (R_O) versus frequency.

$$R_{OUT}(\omega) = \frac{R_0(\omega)}{1 + A_{OL}(\omega)\beta} \tag{10}$$

Selecting an amplifier with sufficient bandwidth is important to keeping the output impedance low. Furthermore, any distortion introduced by the common driver amplifier is directly added to the signal chain. An amplifier with low distortion at the input signal frequency is thus important. The non-inverting node of the difference amplifier also experiences a signal swing of a couple volts. A sufficient bandwidth is required in the common-mode driver to settle the couple volts of signal swing. A general rule is to select an amplifier with the minimum bandwidth similar to the difference amplifier. Both the inverting and non-inverting node of the difference amplifier are driven with an attenuated signal at 10 kHz. The goal is to then achieve similar settling and AC performance between the non-inverting node and the inverting node (see Equation 11).

$$BWV_{CMBUFFER} \approx BW_{DIFFAMP} \tag{11}$$

Finally, the common-mode driver operates on a single supply, so the input common-mode range of the amplifier must support the REF / 2 common-mode voltage.

2.3 Understanding Multiplexed DAQ Settling Time Requirements

The design that the preceding Figure 2 shows merges the four-channel differential input signals into a time-division-multiplexed signal by the multiplexer after having been configured for continuous switching-mode operation. The multiplexed input signals in most PLC applications consist of large voltage steps when switching between channels. The worst-case scenario is when the previous channel is at a negative full-scale voltage and the next channel is at the positive full-scale voltage. In this scenario, the step can be as large as the input full scale range, 40 V. This ratio is an enormous challenge for the AFE; the output must settle to high precision from such large steps in a short time. Performing a careful timing analysis is important to understanding the amount of settling time required by all the blocks in the system to meet a required sampling rate (see Figure 10).

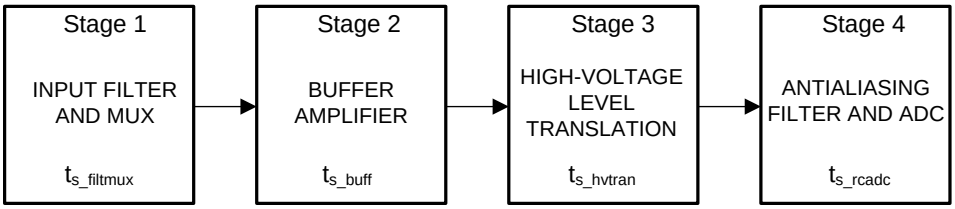

Figure 10. Multiplexed DAQ Settling Time Analysis

The total settling time is estimated to be the root sum square (RSS) of settling time of each stage (see Equation 12):

$$t_{s\_total} = \sqrt{t_{s\_filtmux}^{2} + t_{s\_buff}^{2} + t_{s\_hvtran}^{2} + t_{s\_rcadc}^{2}} \quad (12)$$

The total settling time (t_{s_total}) must be less than the acquisition time available for each channel (t_{acqn}) of the SAR ADC to avoid settling error during the conversion (see Equation 13).

$$t_{s\_total} \leq t_{acqn} \quad (13)$$

The following subsections systematically explain the design of each stage of the AFE (from the flow chart in Figure 10) for optimal settling performance.

2.3.1 Multiplexed DAQ Timing Design

The available settling time per channel in a multiplexed DAQ system can be optimized by understanding the ADC timing diagram. The ADC has two modes: acquire and conversion mode. In the acquire mode, the ADC samples the input voltage on its internal sampling capacitor. In the conversion mode, the ADC disconnects the input and starts the conversion of the sampled voltage. When the CONVST pin goes HIGH, the ADC starts the conversion process. Each ADC has a specified minimum acquire and conversion time in the respective data sheet.

The inputs of the ADC must be settled to the required resolution (16 bits) prior to the convert start pin going high. To operate the ADC at the maximum sampling rate, the inputs of the ADC must settle within the specified acquisition time of the ADC (t_{acq}). However, in a multiplexed application, this acquisition time can be longer by optimizing the MUX channel switching timing.

In a multiplexed application, when the CONVST pin goes HIGH, the ADC inputs disconnect from the circuit. Thus, at the rising edge of the CONVST pin, the MUX can be switched to the next channel. This switching allows the available acquiring time for a specified channel to be the sum of the acquisition time and conversion time of the ADC. However, take care to avoid switching channels prior to the rising edge of the CONVST pin. To avoid this switch, implement a small delay in the timing, as Figure 11 shows. Equation 14 expresses the available settling time for the channel.

$$t_{acqn} = t_{acqadc} + t_{convadc} - t_{delay} \quad (14)$$

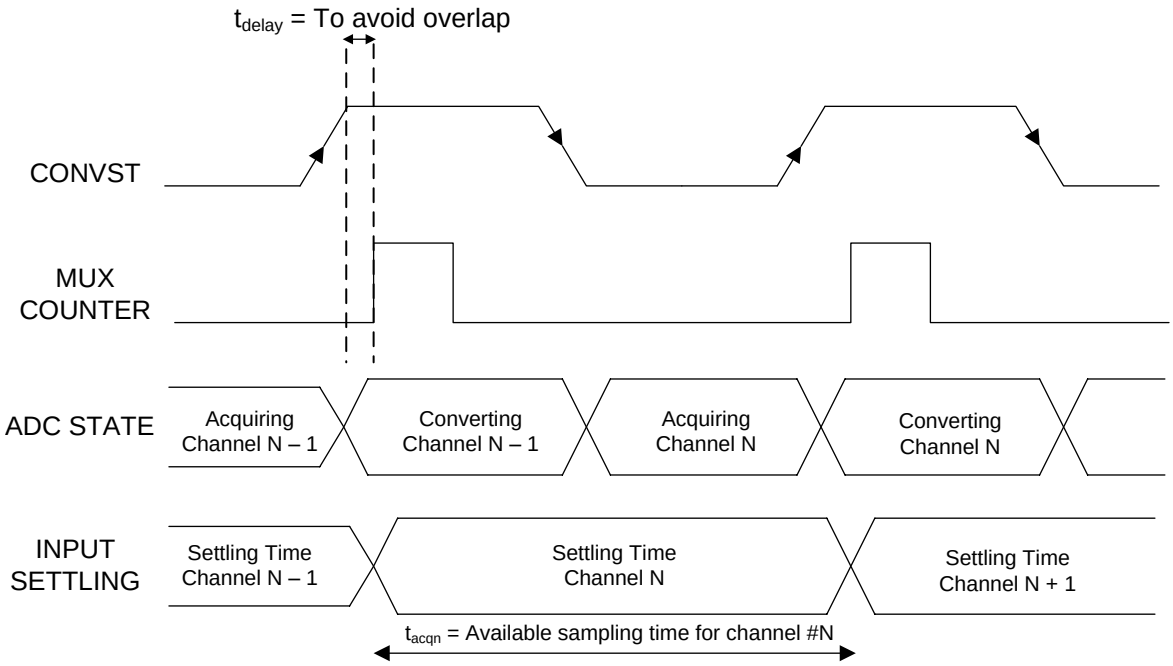

Figure 11. Multiplexed DAQ Timing Diagram

2.3.2 Input Low-Pass Filter and Multiplexer Settling Time

The input low-pass filter and the multiplexer (using the simplified model in Section 2.2.1) can be simplified as a cascaded RC network, as Figure 12 shows. The settling time for a cascaded network is then computed using the slower of the two time constants. The transition time of the MUX is then added to the total settling time for the input low-pass filter and multiplexer (see Equation 15).

$$t_{s\_filtmux} = \max\left(t_{s\_filt}, t_{s\_mux}\right) + t_{TRANSISTION} \quad (15)$$

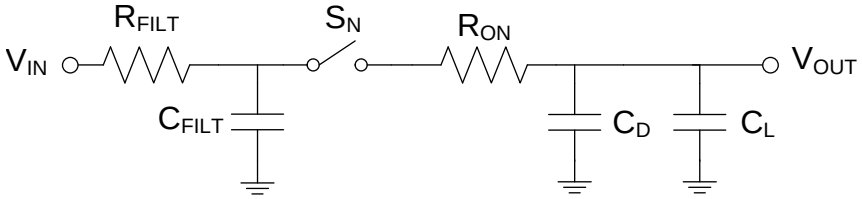

Figure 12. Simplified Model for Settling Time of Input Low-Pass Filter and MUX

2.3.2.1 Input Low-Pass Filter Settling Time

The input low-pass filter performs a dual function in a multiplexed DAQ time. The filter first provides low impedance at the input of the MUX. The second function of a low-pass filter is that it suppresses input noise. The C_{FILT} value must be chosen to meet the required accuracy based on the preceding Equation 3. The R_{FILT} value is selected to provide the 16-bit settling in the available acquisition time. The settling time of the low-pass filter can then be calculated using Equation 16. For a 16-bit settling requirement, the %Error = 0.0016%.

$$t_{s\_filt} = -\ln\left(\frac{\%Error}{100}\right) \times R_{FILT} \times C_{FILT} \quad (16)$$

2.3.2.2 Multiplexer Settling Time

The multiplexer can be simplified as a series resistor and capacitor, as Figure 13 shows. In a multiplexer the total settling time is a combination of the transition time ($t_{TRANSITION}$) and the settling at the output of the RC filter.

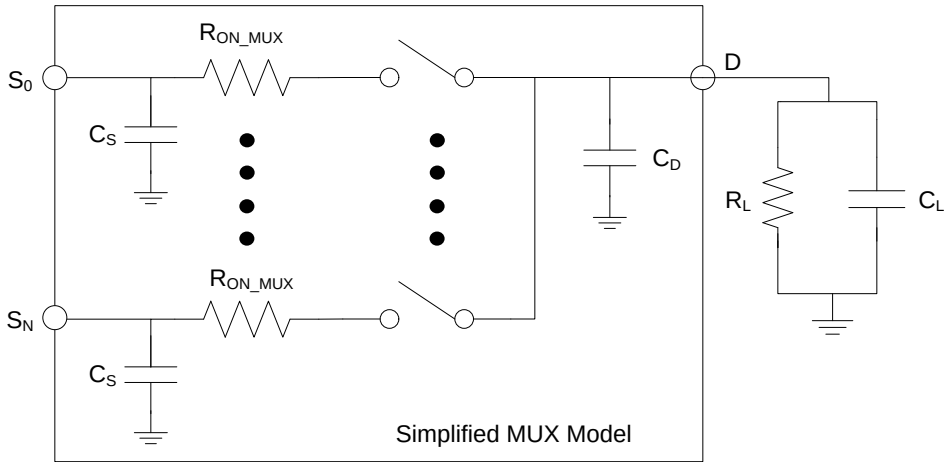

Figure 13. Simplified Model of a Multiplexer

The transition time of a multiplexer is the delay time between the 50% and 90% points of the digital input and the switch ON condition when switching between one channel to another. This specification is available in the respective multiplexer data sheets.

The settling time at the output of the MUX can be modeled as a simple RC circuit with a time constant of R_{ON_MUX} x C_D. The settling time is also impacted by the impedance at the output of the MUX. The settling time of the MUX (as the preceding Figure 13 shows) can be expressed as the following Equation 17:

$$t_{SETTLE\_RC} = -\ln\left(\frac{\%Error}{100}\right) \times \left(\frac{R_{ON\_MUX} \times R_L}{R_{ON\_MUX} + R_L}\right) \times (C_D + C_L) \quad (17)$$

As Section 2.2.2 explains, the impedance at the output (R_L) adds distortion to the DAQ system. Therefore, if the output of the MUX has been buffered, as the preceding Figure 5 and Figure 6 show, the settling time from Equation 17 can be simplified to Equation 18:

$$t_{SETTLE\_RC} = -\ln\left(\frac{\%Error}{100}\right) \times (R_{ON\_MUX} \times C_D) \quad (18)$$

2.3.3 Buffer Amplifier Settling Time

As Section 2.2.2 explains, buffering the output of the MUX with an op amp is important. This action eliminates any gain error and gain error nonlinearity introduced as a result of the MUX R_{ON_MUX} and R_{ON_MUX} flatness. The recommended approach is to have an amplifier buffer the output of the MUX. as the preceding Figure 2 shows. The transient and AC behavior of the buffer amplifier contributes to the total settling time of the amplifier.

An important concept to understand is the input structure of the buffer amplifier and its differential input impedance. Most high voltage amplifiers have back-to-back diodes connected between the inputs of the amplifier, as Figure 14 shows. The back-to-back diodes have been added for input front-end protection of the amplifier.

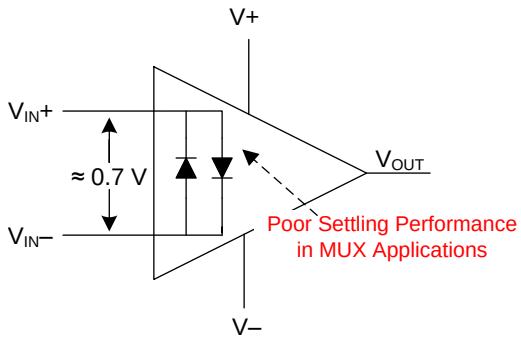

Figure 14. Back-to-Back Diodes at Inputs of High Voltage Amplifier

However, these protection diodes introduce significant settling time delay in a multiplexed application. The buffer amplifier at the output of the MUX observes a full-scale step change at its inputs. During this transition the input protection diodes turn ON and draw large currents, as the diagram in Figure 15 outlines.

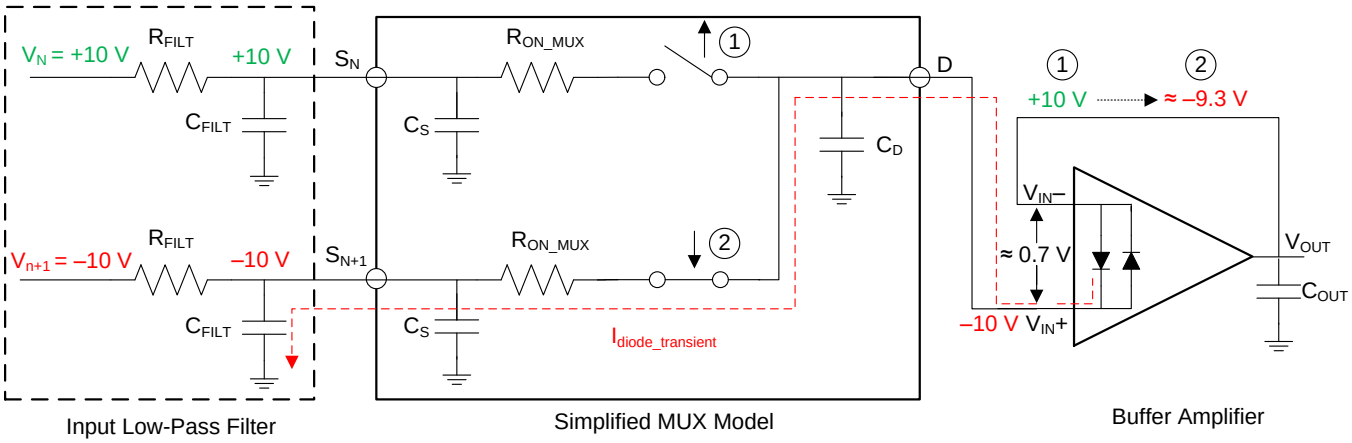

Figure 15. Back-to-Back Diode in Traditional Op Amp Introduces Settling Time Delay

Figure 15 shows the worst-case scenario from a settling perspective. In this example, the input channel V_N is connected to +10 V and the input channel V_{N+1} is connected to –10 V. Assume that channel S_N has been initially selected and then transitions to channel S_{N+1}. Because the amplifier has a finite slew rate, it cannot change instantaneously. When the multiplexer changes channels, the output of the amplifier is at +10 V, but the input is at –10 V. In this case, the input protection diodes turn and limit the input differential voltage to 0.7 V. The current through the diode in this condition is calculated in Equation 19.

$$I_{diode\_transient} = \frac{V_{fullscalepos} - V_{fullscaleneg} - 0.7}{R_{ON\_MUX}} \quad (19)$$

When the back-to-back diodes have been turned ON, the combined output capacitance of the amplifier and input capacitance of the following stage (C_{OUT}) is effectively in parallel with C_D. In most cases, the output capacitance of the amplifier itself can be at least ten times larger than C_D. When the MUX channel switches, charge redistribution occurs between C_{FILT} and [C_D + C_{OUT}], as Section 2.2.1 explains. As a result of the back-to-back diodes turning ON, a significant voltage droop occurs across C_{FILT}. This voltage droop takes a long time to recover because it has been low-pass filtered. The C_{FILT} capacitor can be made larger, but that impacts the settling time of the input signal frequency, and as previously explained, the COG capacitor size is physically limited.

Therefore, amplifiers with back-to-back input diodes create long settling tails in multiplexed applications and are not suitable. To mitigate the problem, a series resistor can be placed at the inputs to limit the current. However, this implementation introduces noise in the system and also creates a low-pass filter with the input capacitance of the amplifier. Further, when the input diodes are turned, the internal nodes of the amplifier are pulled apart. The internal, high-impedance nodes are driven close to supplies and consequently take a long time to recover to the desired voltage, which results in a long settling time in the amplifier.

To achieve the fastest settling performance, selecting an amplifier without back-to-back diodes at its inputs is important (see Figure 16).

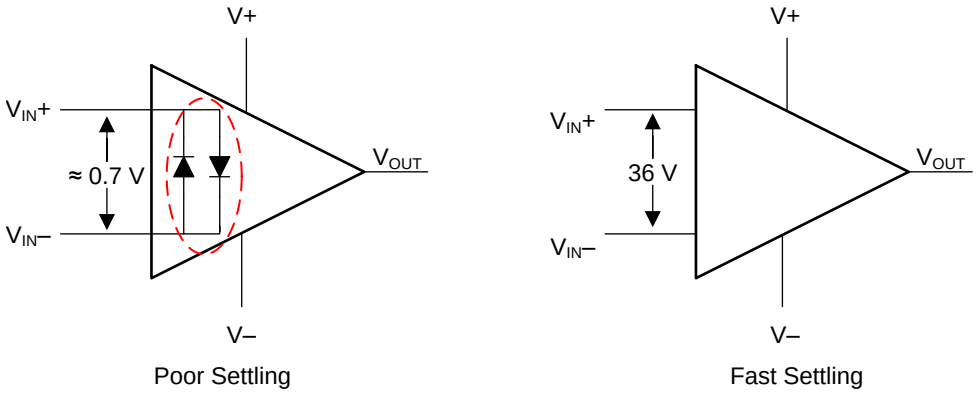

Figure 16. Selecting Amplifier for Fast Settling

After selecting an appropriate amplifier without back-to-back diodes, look up the settling time of the amplifier, which is usually provided in the data sheet for the amplifier. The settling time of the amplifier is defined as the duration of time that the output requires to respond to a step change at the input, come into, and remain within a defined error band. The error band is the specific percentage of the step, such as 0.1%, 0.01%, 0.001%, and so forth. An important thing to note is that the op amp settling time is nonlinear and it may take an amplifier much longer to settle to 0.001% compared to 0.1%. The thermal effects within the op amp can sometimes cause it to settle after a much longer time period.

For these reasons, the amplifier selected in this system must settle to 0.001% (16-bit) within an available acquisition time because the overall system must be settled to obtain the proper conversion results. Carefully read the op amp data sheet and select an amplifier with the sufficient settling time specifications for the required ADC resolution to help eliminate unknown settling time problems in the system.

2.3.4 Antialiasing Filter

An antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. The antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth has been optimized based on the application requirements. For the AC input signals, the filter bandwidth must be kept low to band-limit the noise fed into the ADC input, thereby increasing the SNR of the system.

In addition to filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor C_{FILT}, is connected across the ADC input, as Figure 17 shows. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor during the acquisition process.

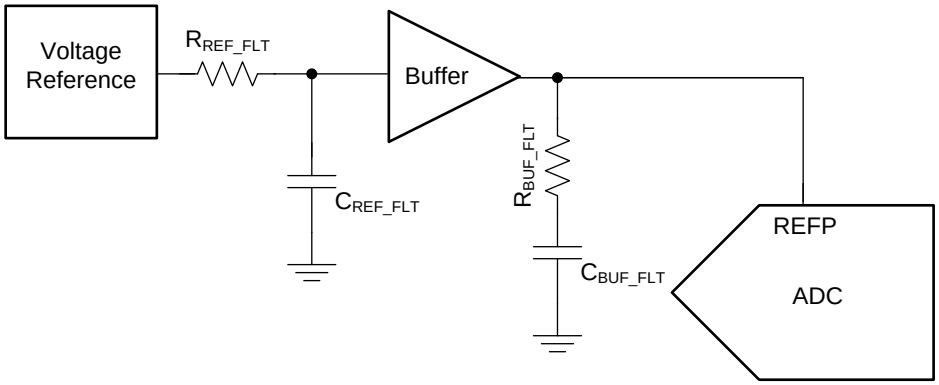

Figure 17. Simplified Schematic of Single-Ended Input Sampling Stage

The filter resistor must be selected appropriately to help stabilize the driver amplifier and filter noise from the previous stage. A higher value of R_{FILT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. A general guideline is usually provided in ADC data sheets for selecting the filter capacitor and resistor. Follow such guidelines to select the resistor and capacitor to stabilize the amplifier while meeting the required noise and settling performance. Section 3.6.2 further details this selection process. When the appropriate R_{FILT} and C_{FILT} have been selected, calculate the bandwidth of the antialiasing as Equation 20 shows:

$$BW_{AFILT} = \frac{1}{2 \times \pi \times R_{FILT} \times C_{FILT}} \quad (20)$$

2.3.5 High-Voltage Level-Translation Amplifier Settling

Obtain the time for the high-voltage level-translation amplifier settling by reading the amplifier data sheet. The output of the difference amplifier only acknowledges a step of the V_{REF}; therefore, the settling time requires calculation based on this step. The antialiasing filter limits the bandwidth of the amplifier and the C_{FILT} capacitor loads the output, which can also reduce the bandwidth of the amplifier. The settling performance of the level-translating amplifier can be simulated in the TINA-TI™ software to verify that it meets the required specification.

2.4 Understanding Multiplexed DAQ Noise and THD Requirements

2.4.1 Noise Analysis of Multiplexed DAQ System

The total noise in this multiplexed DAQ system is a result of the noise of each element in the signal chain, as the preceding Figure 2 shows. However, systematically analyzing the signal chain is important to better understand the major contributor of noise in the system. The total noise contributed by the AFE must be kept low to prevent the overall SNR of the system from significantly degrading.

With multiple noise sources, the total noise is the root sum of squares (RSS) of the individual noise contributors. The noise sources in the signal chain of this circuit are the thermal noise from the resistors and the voltage noise of the buffers and the attenuating level-translation amplifier. The ON resistance of the multiplexer is comparatively small to be a significant source of noise and thus the MUX is ignored in this analysis. Figure 18 shows the major noise contributors in the signal chain.

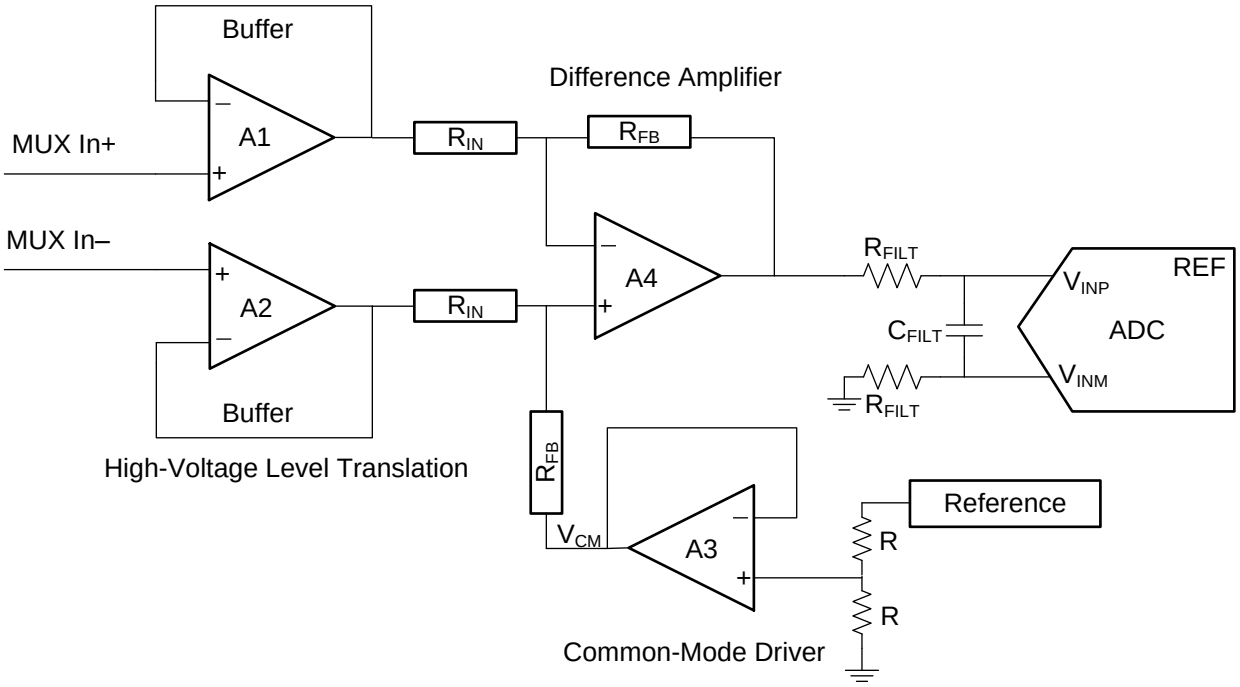

Figure 18. Major Noise Contributors in a Multiplexed DAQ System

The spectral noise density from the common-mode driver and difference amplifier can be calculated using Equation 21 and Equation 22. Refer to the *Noise Analysis in Operational Amplifier Circuits* application report for more details [2].

$$e_{rto\_diff\_amp} = \sqrt{\left(2In_{A4}R_{FB}\right)^2 + \left(en_{A4}\left(\frac{R_{IN} + R_{FB}}{R_{IN}}\right)\right)^2 + 8kTR_{FB}\left(\frac{R_{IN} + R_{FB}}{R_{IN}}\right)} \quad (21)$$

$$e_{rto\_vcmdriver} = \left(en_{A3}\left(\frac{R_{IN} + R_{FB}}{R_{IN}}\right)\right) \quad (22)$$

The noise from the buffers A1 and A2 are attenuated by the gain of the difference amplifier. In the system, the buffers are going to be the same amplifier, thus the total noise from both amplifiers referred to the output can be expressed as the following Equation 23 shows:

$$e_{rto\_buffer} = \left(2 \times en_{A1}\left(\frac{R_{FB}}{R_{IN}}\right)\right) \quad (23)$$

The total noise from the AFE can then be calculated using Equation 24:

$$e_{rto\_signalchan} = \sqrt{\left(e_{rto\_diff\_amp}\right)^2 + \left(e_{rto\_vcmdriver}\right)^2 + \left(e_{rto\_buffer}\right)^2}$$

$$e_{rto\_signalchan} \approx \sqrt{\left(e_{rto\_diff\_amp}\right)^2 + \left(e_{rto\_vcmdriver}\right)^2} \quad (24)$$

Analyzing the preceding equations, the designer can infer that the major source of noise is the difference amplifier and the common-mode driver for the difference amplifier. The noise of the buffer amplifiers is attenuated by the difference amplifier. The total RMS noise can be calculated by integrating the noise spectral density ($e_{rto\_signalchain}$) over the antialiasing bandwidth filter at the input of the ADC. Equation 25 expresses this calculation:

$$V_{n\_rto\_signalchan\_RMS} = e_{rto\_signalchan} \times \sqrt{1.57 \times BW_{AFILT}} \quad (25)$$

In a scenario with an ADC with an input dynamic range of V_{FSR}, the input referred noise can be calculated from the specified value of SNR in the data sheet by using the following Equation 26:

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\frac{SNR\ (dB)}{20}} \quad (26)$$

So the total noise contribution from the total multiplexed DAQ system can be calculated as the following Equation 27 shows:

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_rto\_signalchain\_RMS}^2 + V_{n\_ADC\_RMS}^2} \quad (27)$$

2.4.2 THD Analysis of Multiplexed DAQ System

The total distortion introduced in the multiplexed signal chain is contributed by the entire signal chain. For this reason, choosing a very low distortion difference amplifier is very important. Obtain the distortion of the amplifier from the applicable data sheet. The distortion of the amplifier is dependent on the amplitude and signal frequency. The amplifiers selected in this design have a 10-dB lower THD specification as compared to the ADC so that the ADC is the dominant source of error.

In this system, the difference amplifier and common-mode buffer amplifier are driving a 1-kΩ load and observe large, signal sine waves. Therefore, the THD specification must be verified for V_{IN} = 3.5 V_{RMS}, R_L = 1 kΩ, and f = 10-kHz input signal (see Equation 28). This specification is a very stringent condition for the difference amplifier. For the buffer amplifiers, the load is much larger at 10 kΩ.

$$THD_{DIFF\_AMP} = THD_{ADC} - 10\ dB \text{ at } V_{IN} = 3.5\ V_{RMS},\ f_{IN} = 10\ kHz,\ R_L = 1\ k\Omega$$

$$THD_{VCMDRIVER} = THD_{ADC} - 10\ dB \text{ at } V_{IN} = 3.5\ V_{RMS},\ f_{IN} = 10\ kHz,\ R_L = 1\ k\Omega$$

$$THD_{BUFFER} = THD_{ADC} - 10\ dB \text{ at } V_{IN} = 3.5\ V_{RMS},\ f_{IN} = 10\ kHz,\ R_L = 10\ k\Omega \quad (28)$$

2.5 Reference Driver Design

External voltage reference circuits are used with ADCs without internal references. These reference circuits provide low drift and very accurate voltages for the ADC reference input. However, the output broadband noise of the references is of the order of a few 100 μV_{RMS}, which degrades the noise and linearity performance of precision ADCs, for which the typical noise is of the order of tens of μV_{RMS}. So to optimize the ADC performance, appropriately filtering and buffering the output of the voltage reference is critical.

Figure 19 shows the basic circuit diagram for the reference driver circuit for precision ADCs. For details on designing the reference driver, refer to the *Data Acquisition Optimized for Lowest Distortion, Lowest Noise, 18-bit, 1-MSPS Reference Design* [1].

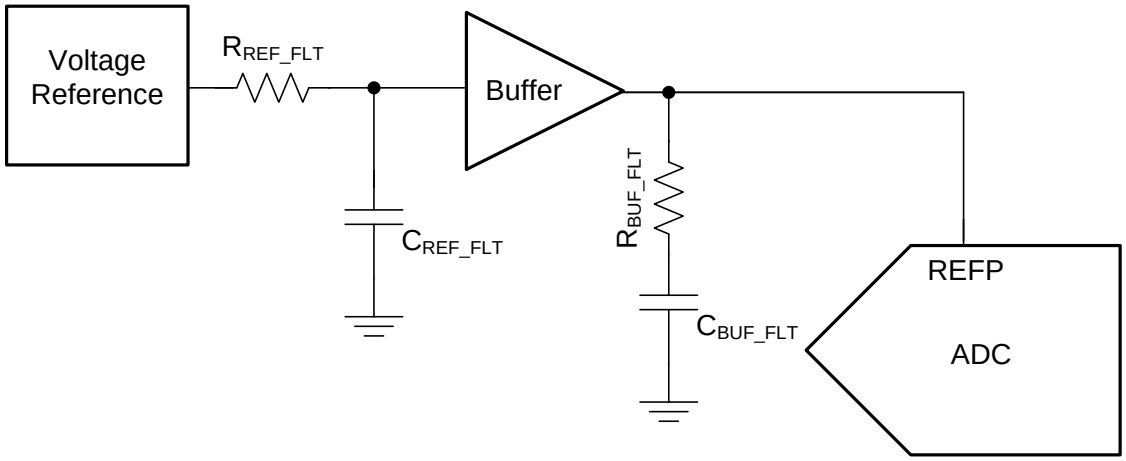

Figure 19. Simplified Schematic of Reference Driver Circuit

3 Component Selection

3.1 ADC Selection

This TI Design has been optimized for low distortion and noise using TI's high-resolution, 16-bit 400-KSPS SAR ADC ADS8864 at its maximum sampling rate for a full-scale differential sine wave input at 10 kHz. The ADS8864 is a single-ended SAR ADC designed for low-voltage operation from a 2.7- to 3.6-V AVDD and a 1.65- to 3.6-V DVDD. The ADS8864 has excellent dynamic performance while consuming very low power. The power dissipation is 2.6 mW (typical) at 400 kSPS and can be scaled down linearly for applications requiring a low throughput. Table 2 shows the key specifications when using the ADS8864 in this application.

Table 2. ADS8864 Key Specifications

SPECIFICATION	VALUE
Resolution	16 bit
Throughput	400 kSPS
INL	±2 LSB
SNR	93 dB
THD	–108 dB
$t_{acquisition}$	1200 ns
$t_{conversion}$	1300 ns

Based on Table 2, the available acquisition time per channel to operate at 400 kSPS can thus be calculated using Equation 29. The delay used in this design was 100 ns to ensure that the MUX channel does not switch until the ADC CONVST has gone high.

$$t_{acqn} = t_{acqadc} + t_{convadc} - t_{delay}$$

$$t_{acqn} = 1200 + 1300 - 100 = 2400 \text{ ns} \quad (29)$$

The entire multiplexed DAQ signal chain must settle to a 16-bit resolution for a worst-case signal step of ±20 V (40 V_{pk-pk}) within 2400 ns.

3.2 Multiplexer Selection

The multiplexer selected for this design is the TI MUX36D04. The MUX36D04 is a four-channel differential input multiplexer. The key specifications to ensure during the selection process is a low drain capacitance (C_D) and fast channel-switching time. A lower drain capacitance specification results in a smaller required capacitance for the input filter. Table 3 summarizes the key specifications for the MUX36D04 multiplexer.

Table 3. MUX36D04 Key Specifications

MUX36D04	VALUE
Drain capacitance: C_D	9 pF
Source capacitance: C_S	3 pF
Switch ON resistance: R_{ON_MUX}	150 Ω
Channel transition time: $t_{TRANSITION}$	100 ns

Based on Table 3 and Equation 30, the settling time of the MUX to 16 bit can be calculated as follows:

$$t_{SETTLE\_RC} = 15 \text{ ns}$$

$$t_{TRANSITION} = 145 \text{ ns} \quad (30)$$

3.3 Passive Component Selection for Input MUX RC Filter

The critical passive components for this design are the resistors (R_{FILT}) and capacitor (C_{FILT}) for the RC filter at the input of the MUX. The tolerance of the resistor was initially chosen to be 0.1%; however, this tolerance was not possible because of the high cost or limited availability; therefore, the tolerance has been set to 1%. Following the method described in Section 2.2.1, the component sizes can be calculated as Table 4 shows:

Table 4. RC Filter Component Selection

COMPONENT	EXPRESSION	VALUE
Filter capacitance: C_{FILT}	$C_{FILT} > \left\| \frac{C_D}{(0.05 \approx 0.1)} - C_D - C_S \right\|$	100 pF
Filter resistance: R_{FILT}	See Section 4.3 for settling simulation	400 Ω
Filter bandwidth: BW_{FILT}	$BW_{FILT} = \frac{1}{2\pi \times R_{FILT} \times C_{FILT}}$	4 MHz

Based on Table 4 and Equation 16, the settling time of the input filter to 16 bit can be calculated as Equation 31 shows:

$$t_{s\_filt} = 447 \text{ ns} \quad (31)$$

3.4 Input Low-Pass Filter and Multiplexer Settling Time

The total settling time from the input filter and multiplexer can now be calculated using Equation 32:

$$t_{s\_filtmux} = \max(447 \text{ ns}, 15 \text{ ns}) + 145 \text{ ns}$$

$$t_{s\_filtmux} = 592 \text{ ns} \quad (32)$$

3.5 Multiplexer Input and Output Buffer: Amplifier Selection

The selection of the input and output buffer amplifier in this multiplexed DAQ system has a significant impact on the overall linearity, settling time, and noise of the system. This TI Design uses the OPA192, which has very high precision and low noise with a unique input front end that allows for fast settling in multiplexed applications. Table 5 summarizes the key specifications for the OPA192 amplifier.

Table 5. OPA192 Key Specifications

SPECIFICATION	VALUE
V_{OS} (max)	25 µV
V_{OS} drift (max)	0.5 µV/°C
Bandwidth	10 MHz
Noise at 1 kHz	5.5 nV/√Hz
10-V step settling, 0.001%	2.1 µs
THD + N, f = 1 kHz, V_O = 3.5 V_{RMS}, R_L = 10 kΩ	0.00008% (≈ 121 dB)
Differential input voltage range	(V+) – (V–) + 0.2

The OPA192 is a CMOS high-precision amplifier with very low offset and drift, which is important in this 16-bit DAQ system. Furthermore, the OPA192 is an ideal choice for multiplexed DAQ because of its unique input front-end architecture, which does not have back-to-back diodes. Also, the OPA192 amplifier has the capability of withstanding a differential input range beyond the supplies. So, in a multiplexed system, the OPA192 device does not create any settling time issues as explained in Section 2.3.3. With a fast settling time and low distortion, the OPA192 amplifier provides excellent performance in this DAQ system.

3.6 High-Voltage Level Translation Difference Amplifier and Antialiasing Filter Design

3.6.1 Difference Amplifier Component Selection

The critical specifications for the difference amplifier are the THD and settling time specifications of the amplifier. The amplifier must have a low THD at the 10-kHz input frequency with a 1-kΩ feedback load. This specification requires an amplifier with low output impedance and a high current drive capability. The amplifier also must be capable of fast settling to a 16-bit resolution. The amplifier selected for this specification is the high-precision OPA140. The OPA140 is a junction gate field-effect transistor (JFET) input amplifier with excellent AC, noise specifications, and high current drives capability. Table 6 summarizes the key specifications of the OPA140 amplifier.

Table 6. OPA140 Key Specifications

SPECIFICATION	VALUE
Bandwidth	10 MHz
Noise at 1 kHz	5.1 nV/√Hz
THD + N, f = 10 kHz, V_O = 3.5 V_{RMS}, R_L = 600 Ω	0.003% (–110 dB)
10-V step settling, 0.001%	1.6 µs
Output impedance at 10 KHz	9 Ω

3.6.2 Common-Mode Driver Amplifier

As Section 2.3.5 details, the common-mode driver must be carefully selected to achieve fast settling and low distortion. The recommended amplifier must have an AC performance similar to the difference amplifier in addition to the input common-mode range supporting the V_{REF} / 2 voltage. The ideal preference is to use the same amplifier as the difference amplifier; however, the OPA140 input common-mode range does not support the V_{REF} / 2 voltage. Therefore, for the common-mode driver amplifier, the OPA350 has been selected. The OPA350 is already being used for the reference driver to the ADC, as Section 2.2.4 explains. The OPA350 amplifier can be reused for the common-mode driver of the V_{REF} / 2 signal. The OPA350 amplifier has excellent AC specifications, as summarized in Table 7.

Table 7. OPA350 Key Specifications

SPECIFICATION	VALUE
Bandwidth	38 MHz
Noise at 1 kHz	5 nV/√Hz
THD + N, f = 10 kHz, V_O = 0.8 V_{RMS}, R_L = 600 Ω	0.006%
2-V step settling, 0.01%	0.5 µs
Output impedance at 10 kHz	9 Ω

3.6.3 Antialiasing Filter Component Selection

The design of the low distortion, antialiasing filter is important to maintain the very low THD and noise requirement from the AFE. The ADS8864 datasheet recommends the use of the C_{FILT} capacitor to be greater than 590 pF. As explained earlier, the capacitor used in this application must also be of the COG- or NPO-type. The data sheet also recommends using an R_{FILT} resistor to be less than 22 Ω.

Keeping the above recommended requirements from the data sheet, the design uses component values as summarized in Table 8. The bandwidth of the filter was chosen to meet the settling and noise requirements. The resistor of 22 Ω allows sufficient isolation to meet the stability requirement.

Table 8. Bandwidth Calculation of the Antialiasing Filter

SPECIFICATION	VALUE
R_{FILT}	22 Ω
C_{FILT}	1.5 nF
BW_{AFILT}	2.41 MHz

3.6.4 Total Calculated Settling Time

The total estimated settling time based on the simplified Equation 11 can be calculated as the following Equation 33:

$$t_{s\_total} = \sqrt{0.59^2 + 2.1^2 + 1^2} = 2.4\ \mu s \tag{33}$$

Because the difference amplifier only observes a 4-V step at the output, the settling time is back-estimated from the specified 10-V settling in the data sheet. Thus the combined settling time of the difference amplifier and the antialiasing filter is estimated to be 1 µs. This quick estimation matches the simulated performance detailed in Section 4.3.

3.7 Noise Analysis of Multiplexed DAQ System

The total noise in the system can be estimated using Equation 34.

$$e_{rto\_diff\_amp} = \frac{8.24\ nV}{\sqrt{Hz}}$$

$$e_{rto\_vcmdriver} = \frac{5.5\ nV}{\sqrt{Hz}}$$

$$e_{rto\_buffer} = \frac{1.1\ nV}{\sqrt{Hz}}$$

$$e_{rto\_buffer} = \frac{9.97\ nV}{\sqrt{Hz}} \tag{34}$$

The integrated RMS noise can be then calculated over the antialiasing filter bandwidth. The following estimate in Equation 35 is very close to the simulated noise in Section 4.2:

$$V_{n\_rto\_signalchain\_RMS} = \left(10.6n \times \sqrt{2.41M \times 1.57}\right) = 19.5\ \mu V_{RMS} \tag{35}$$

The ADC RMS noise can be calculated using Equation 25 and Table 2, resulting in Equation 36:

$$V_{n\_ADC\_RMS} = 31\ \mu V_{RMS} \tag{36}$$

The total expected noise from the system can then be calculated as shown in Equation 37:

$$V_{n\_TOT\_RMS} = 50.5\ \mu V_{RMS} \tag{37}$$

3.8 Reference Driver: Passive Components Selection

The external reference used to drive the ADS8864 device in this design is the REF3240 from TI. This reference has been selected because it provides the required reference voltage of 4.096 V while consuming only 100 µA. As the REF3240 data sheet mentions, this external reference requires a capacitance of 1 µF (C_{REF_FILT}) at the VOUT pin for stability purposes. To limit the noise from the reference, a filter bandwidth of 160 Hz has been selected. Based on this decision, the value of R_{REF_FILT} has been selected as 1 kΩ for this design.

3.9 Reference Driver: Amplifier Selection

As Section 2.5 explains, the key amplifier specifications to consider when designing a reference buffer for a high-precision ADC are low offset, low drift, wide bandwidth, and low output impedance. The selected reference buffer that meets the above criteria is the OPA350. The OPA350 is a 38-MHz bandwidth amplifier with a maximum offset of 0.5 mV and low offset drift of 4 µV/ºC. The OPA350 amplifier achieves low offset and drift DC specifications while having high bandwidth, low output impedance, and a high capacitive drive capability.

With new and increased integration among available components, another option to drive the reference on the ADC is a reference with an integrated buffer. This option replaces the entire reference driver circuit with one major component, which avoids the long design process of choosing the correct amplifier for the best performance. Even when an amplifier does meet the necessary specifications, such as wide bandwidth, low output impedance, low offset, and lost drift, the power consumption must still be considered. The OPA350 used in the design meets all the criteria and performs exceptionally well, but it also consumes 5.2 mA of quiescent current. The REF60xx family, a high-performance line of reference drivers that TI offers, has an integrated low-output impedance buffer. Each reference driver is trimmed during production to achieve a max drift of only 5 ppm/°C for both the reference and integrated buffer combined. The device also consumes a low 820-µA quiescent current, while still being able to replenish a charge of 70 pC on a 47-µF capacitor in 1 µs. The REF6041 is specifically the ideal choice for this design, with an output of 4.096 V.

4 Simulation

The TINA-TI schematic in Figure 20 shows the final design and selected components as explained in the previous sections.

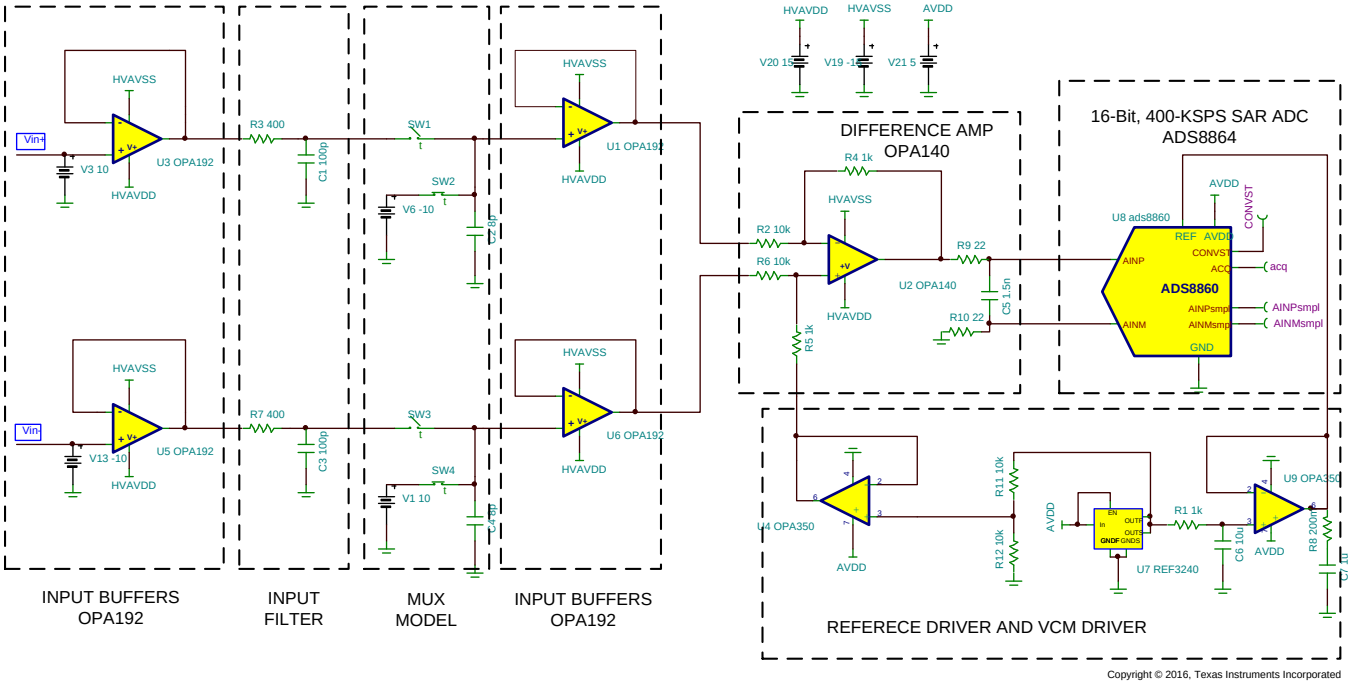

Figure 20. TINA-TI™—Schematic Showing Complete DAQ Block

The circuit in Figure 20 was simulated to perform a transient simulation using a 10-kHz sine wave signal to check that the ADC inputs are settling to the sufficient accuracy before the start of every conversion. View the simulation details and results in the following subsections.

4.1 Stability of Input Driver Amplifier

Figure 21 shows the TINA-TI schematic used to check the stability of the input drivers.

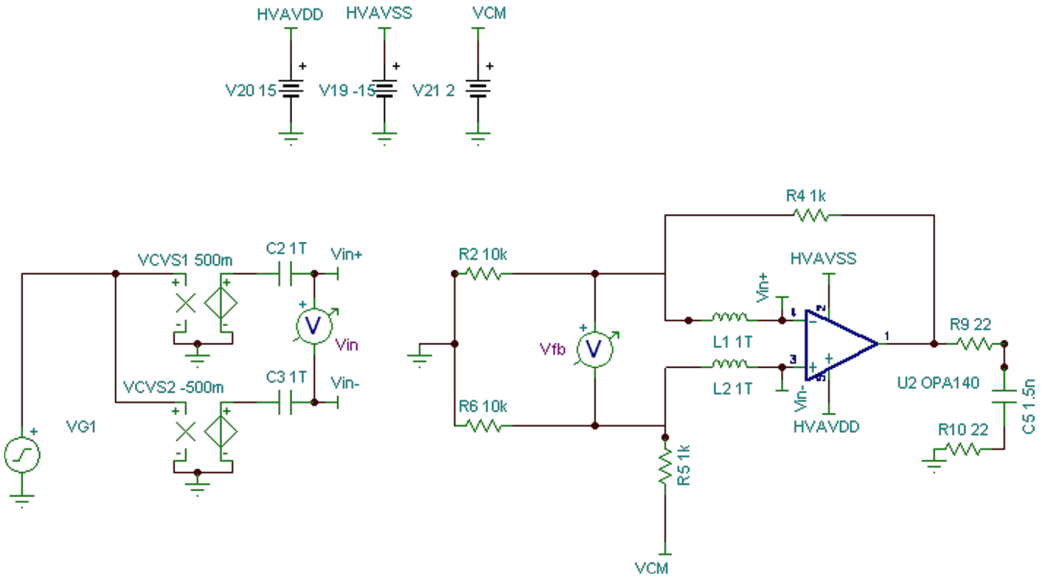

Figure 21. TINA-TI™—Schematic for Checking Input Driver Stability

A large inductor with a value of 1 TH is connected in the feedback loop of the amplifier, thus the circuits behave like an open-loop configuration at frequencies higher than the DC. The circuit has been simplified by only considering a half-circuit of the differential input structure [3]. To load the amplifier output appropriately, the ADC is connected with the CNV pin tie to GND so that the ADC is always sampling the input signal. Figure 22 shows the AC magnitude and phase response for this circuit.

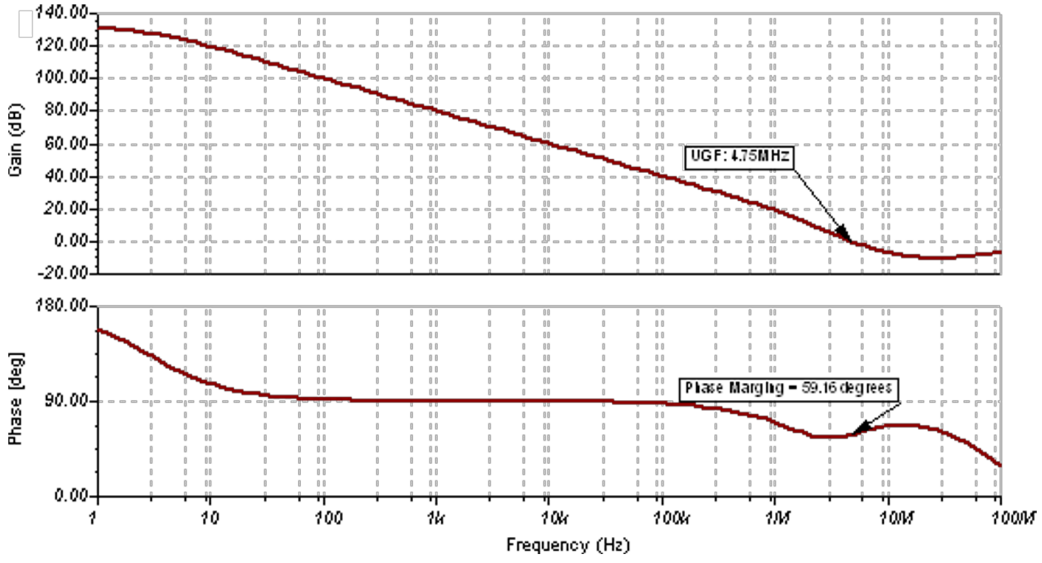

Figure 22. TINA-TI™ Schematic Result—AC Magnitude and Phase Plot for Input Drivers

The resulting phase margin of 59.16º at the 0-dB crossover frequency of 4.75 MHz validates the stability of the input drivers for this design.

4.2 Noise of Input Driver Amplifier

Figure 23 shows the TINA-TI schematic used to simulate the integrated RMS noise of the input driver. Ideally, to calculate the referred-to-output (RTO) noise from the input driver, the voltage noise density curve must be integrated to infinity. For a realistic approximation of the RTO RMS noise; integration to a decade beyond the bandwidth of the system is sufficient. Figure 24 shows that the simulated integrated noise from the fully-differential amplifier input driver referred to the output is 28.38 μV_{RMS}, which meets the design requirements. This simulation verifies the noise calculation made in Section 3.7.

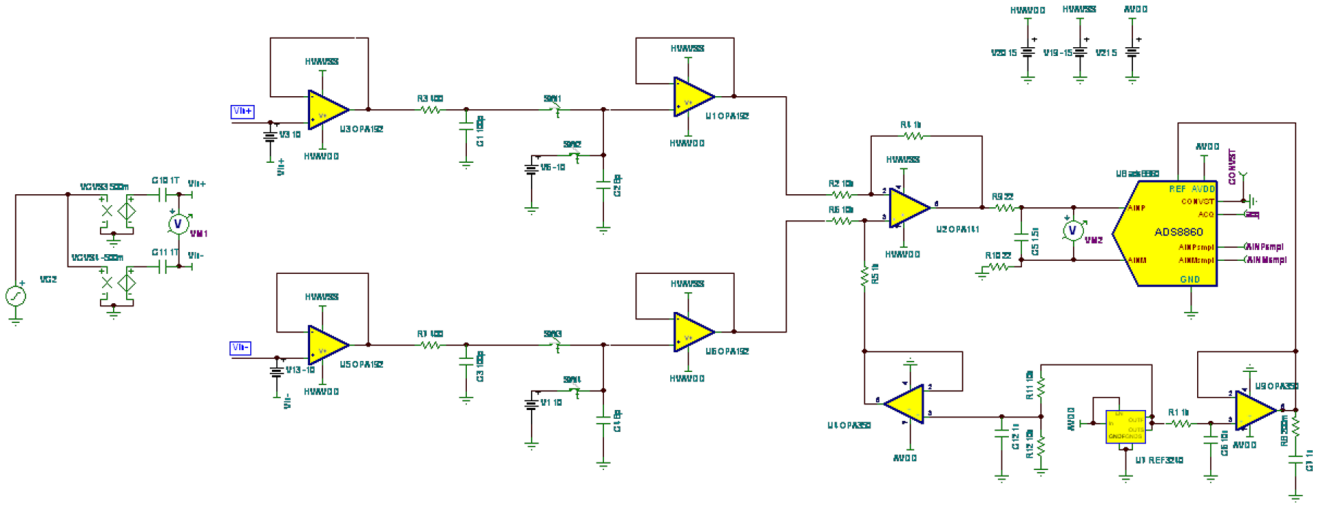

Figure 23. TINA-TI™—Schematic for Checking AFE Noise

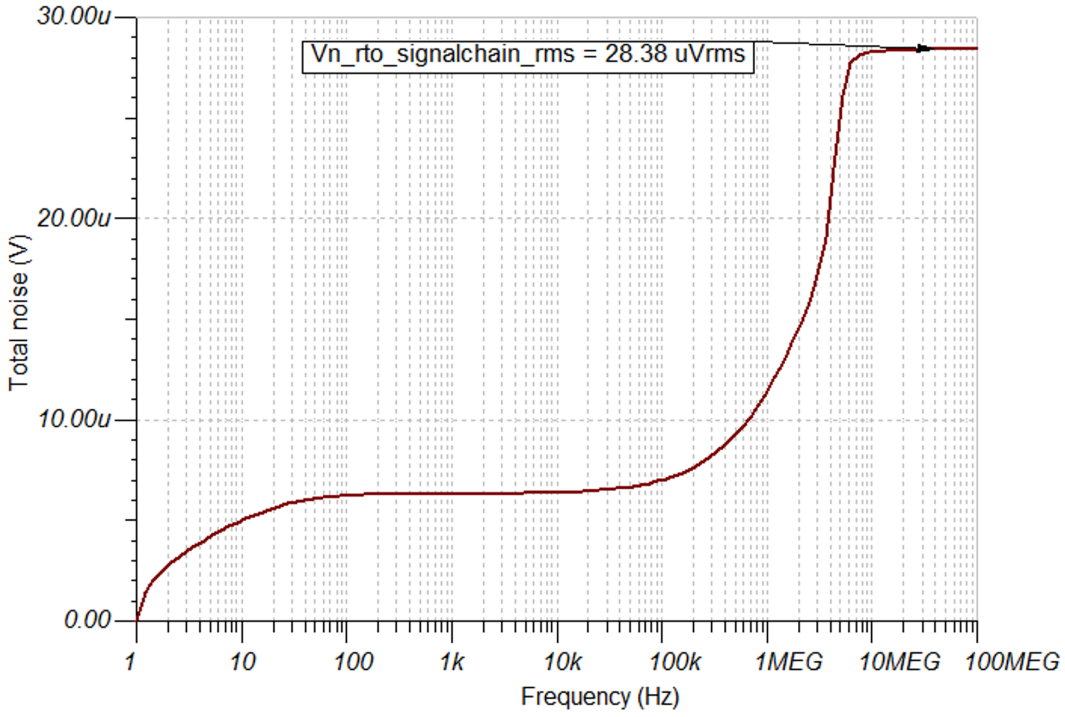

Figure 24. TINA-TI™ Schematic Result—Integrated AFE RMS Noise

Table 9 compares the calculated total noise and the simulated total noise.

Table 9. Total Noise in μV_{RMS}

SPECIFICATION	VALUE
Calculated total noise	19.5 μV_{RMS}
Simulated total noise	28.38 μV_{RMS}

The antialiasing filter creates gain peaking in the closed-loop response. Figure 22 shows this occurrence in the simulation: The unity gain frequency of the difference amplifier is 4.75 MHz as compared to the calculated filter frequency of 1.51 MHz. This difference results in additional noise integrating into the system and yields a mismatch between the calculated and simulated noise.

4.3 Settling Response of MUX Channel Switching

As previously explained, when in continuous switching mode operation, all four-channel differential input signals are merged into a time-division-multiplexed signal by the multiplexer. Simulating the full system settling when the MUX channel has switched to the next input signal is important. The worst-case scenario is when the previous channel is at the negative full-scale voltage and the next channel is at the positive full-scale voltage. In this scenario, the step can be as large as the input full-scale range, 40 V.

The TINA-TI schematic that Figure 25 shows is used to check the settling of an entire signal chain. The multiplexer has been modelled as a resistor and the capacitor has been based on the RON and CD of the MUX. The simulation has been designed such that the previous channel is at the negative full-scale (–20-V differential) and the next channel is at the positive full-scale (+20-V differential).

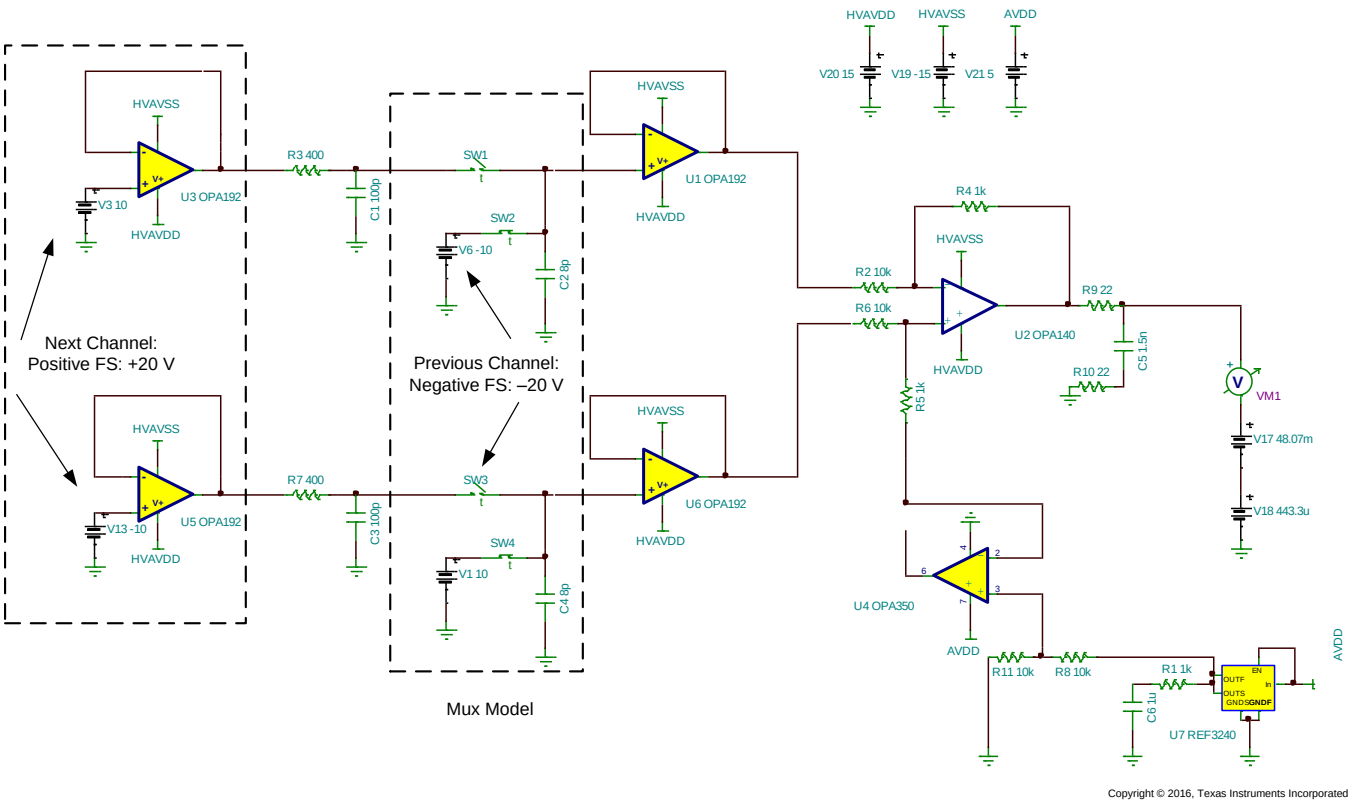

Figure 25. TINA-TI™ Schematic for Checking Settling Performance During Worst-Case Channel Switching

Figure 26 shows the full-scale step response observed at the inputs of the ADC. The entire signal chain settles within 2.14 µs, as in the plot in Figure 27 shows. This behavior meets the required settling time for an available acquisition time of 2.4 µs. The simulated settling time also matches closely with the calculated settling time in Section 3.6.4.

Table 10 compares the available, calculated, and simulated settling times for the design requirements.

Table 10. Settling Time Requirements in ns

SETTLING TIME	TIME
Available settling time: t_{aqn}	2300 ns
Calculated settling time	2400 ns
Simulated settling time	2140 ns

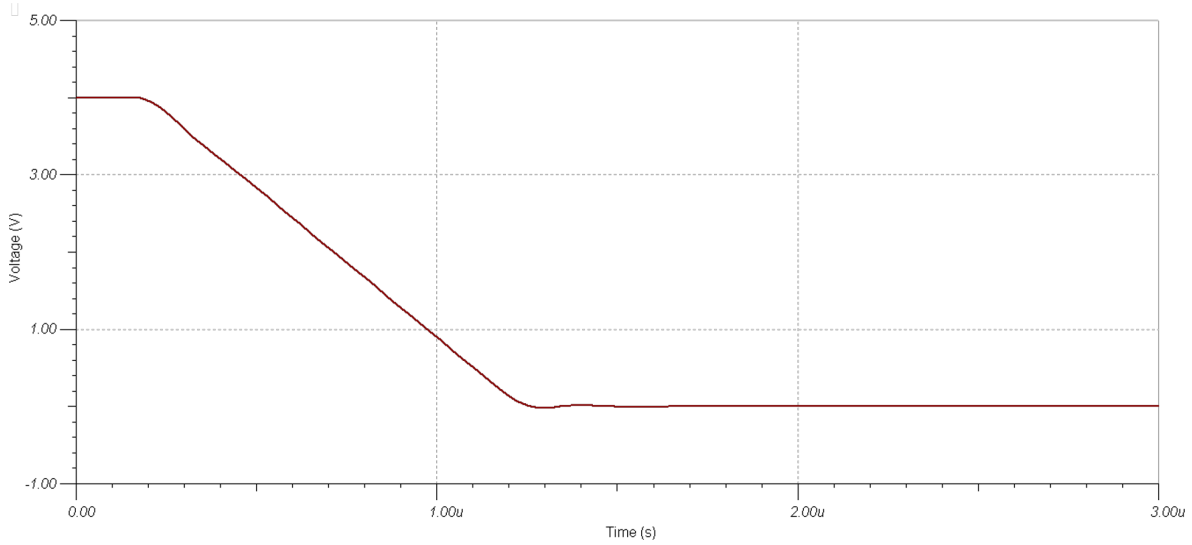

Figure 26. TINA-TI™ Schematic Result—Full-Scale Step Change at ADC Input (4.096 V)

Figure 27 shows the simulated settling time of 2.14 ms at the full-scale step change.

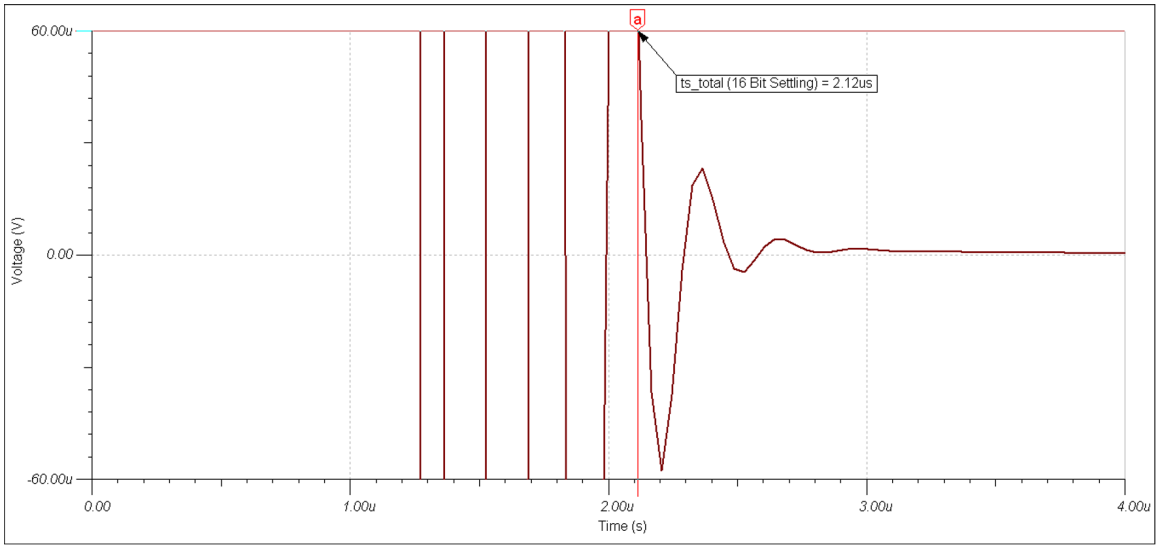

Figure 27. TINA-TI™ Schematic Result—Settling Time = 2.14 µs for Full-Scale MUX Step Change

4.4 PCB Layout

The following list details the most important considerations when designing the PCB layout for this DAQ block.

- The length of traces from the reference buffer circuit (REF3240 and OPA350) to the REFP input pin of the ADC must be kept as small as possible to minimize the trace inductance that can lead to instability and potential issues with the accurate settling of the reference voltage.
- The input driver circuit, which comprises the OPA140, must be placed as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust against electromagnetic interference (EMI) and radio frequency interference (RFI). Similarly, the resistors and capacitor of the antialiasing filter at the inputs of the ADC must be kept in close proximity and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC must be kept symmetrical without any sharp turns.

Figure 28 shows the complete PCB layout for this design.

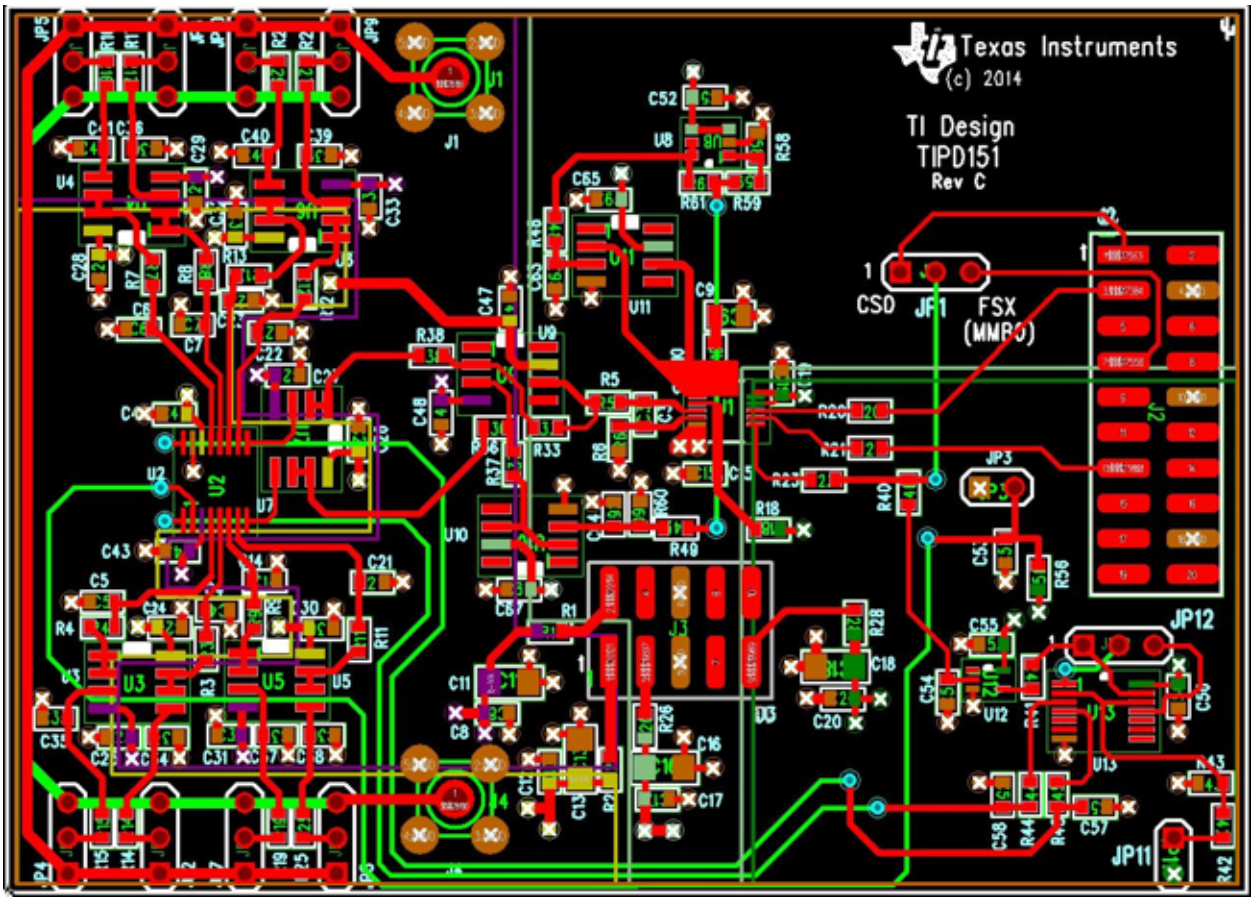

Figure 28. TI Design—16-Bit, 400-KSPS, Four-Channel Multiplexed DAQ System for HV Inputs

5 Verification and Measured Performance

This section provides the measurement results for the verification of this design.

5.1 DC Noise Measurement

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors and other circuitry, which is referred to the inputs of the ADC. The front end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often called as the *input-referred noise* of the ADC has significant impact on the overall system performance. The most common way to characterize this noise is by using a constant DC voltage as the input signal and collecting a large number of ADC output codes. A histogram can then be plotted to show the distribution of output codes, which can be used to show the impact of noise on the overall system performance. In this design, the DC noise for the system is measured by shorting the inputs of both input driving amplifiers to a common mode voltage, V_{CM} = 0 V, such that the differential voltage at the inputs of the ADC is equal to V_{DIFF} = 0 V. The resulting histogram of output codes is shown in Figure 29.

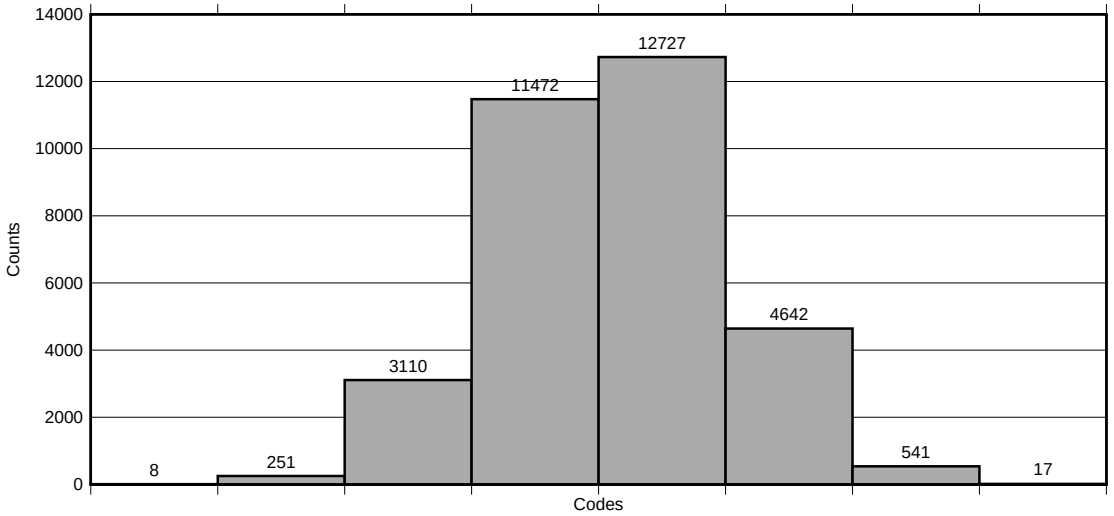

Figure 29. Measurement Result—Histogram Showing DC Noise (Mid-Scale)

The distribution of output codes looks like a Gaussian distribution, which indicates a properly designed system. However, if the output code distribution has large peaks and valleys that make it distinctly non-Gaussian, then this indicates significant DNL errors in the ADC or issues with the system design such as insufficient power supply decoupling, improper ground connections, other poor PCB layout effects. For a theoretically-perfect ADC system, the histogram of output codes are a single vertical bar because the ADC output is to always be the same for a DC input voltage. However, the noise contributions from the ADC and the front-end circuit lead to a distribution of output codes, which provides a measure of the overall system DC noise. The measured values of peak-to-peak difference between the codes (N_{PP}) and the standard deviation of codes (N_{σ}) are listed in Table 11.

The *noise-free resolution* of an ADC is defined as the number of steady output bits from the converter beyond which the system performance is dominated by noise and it is impossible to differentiate between individual code transitions. This is an extremely conservative measurement of the ADC performance because the formula for noise-free resolution is derived from the peak-to-peak code noise, which is extremely dependent on the total number of samples.

A more reliable approach is to use the standard deviation of output codes (N_{σ}) in calculating the *effective resolution* of the ADC. Note that the results that Table 11 shows do not assume a Gaussian-based formula in calculating the standard deviation from the peak-to-peak value because the overall DC noise is comparable to the size of the LSB. For the 16-bit ADC used in this design, the measured value of effective resolution is also equal to 16 bits, which indicates that there is no degradation in the performance of the converter performance as a result of the effects of DC noise.

Note that the effective resolution and effective number of bits (ENOB) shown in Section 5.4 are not to be confused with each other as they are two completely different entities. The ENOB for an ADC is measured with an AC sinusoidal input signal and includes the effects as a result of quantization noise and distortion terms, which have no impact on a DC measurement.

Table 11. Measurement Results for DC Noise

PARAMETER	FORMULA	MEASURED VALUE
Mean output code	—	32788.61
Peak-to-peak code noise (N_{PP})	—	8
Standard deviation (N_{σ})	—	0.93
Noise-free resolution (bits)	$\log_2\left(\frac{2^{18}}{N_{PP}}\right)$	13
Effective resolution (bits)	$\log_2\left(\frac{2^{18}}{N_{\sigma}}\right)$	16

5.2 Settling Time Performance

In a data acquisition system it is important to ensure that the input signal to the ADC is settled to within 1 LSB for the worst-case voltage step. In a multiplexed system like this, the worst-case voltage step is 40 V_{pk-pk}. To measure the settling performance of the system, use the approach in the following summarization.

Loop the following steps:

- Step to the highest code and take: sample 1
- Stay at the highest code and take: sample 2
- Step to the lowest code and take: sample 3
- Stay at the lowest code and take: sample 4

This loop is repeated in this test setup 50 times for each channel. The idea behind this methodology is to separate noise in the system from the settling time error in the sample. When stepping from the lowest code to the highest, in the first sample the user captures both the settling error and the noise in the system. However, after taking a second sample again, at this point no settling error is present in the measurement because the sample has had a long time to settle. Thus the second sample captures purely the noise. The difference in the average code measurement for sample 1 and sample 2 gives the settling time error in LSB for positive full-scale step. Similarly, the difference in the average code measurement for sample 3 and sample 4 gives the settling time error in LSB for a negative full-scale step.

- Positive full-scale settling error: (average code sample 2) – (average code sample 1)
- Negative-full scale settling error: (average code sample 4) – (average code sample 3)

In this measurement, the input signal step provided was –40.49 V_{pk-pk}. This measurement is slightly higher than the required step of 40 V_{pk-pk}. The larger step ensures that if the input settles then the user has enough margin in all cases for the 40-V_{pk-pk} signal to settle. Table 12 and Figure 30 provide a summary of the results for a single channel 0. Observe that for both the positive and negative full-scale step of –40.49 V_{pk-pk}, the system has excellent settling of less than 1 LSB for a rising step and 1.2 LSB for a falling step.

Table 12. Settling Time Performance for Full-Scale Step Change

AVERAGE CODE	SAMPLE 1	SAMPLE 2	POSITIVE FULL-SCALE SETTLING ERROR
50	65351.48	65352.18	0.7 LSB
AVERAGE CODE	**SAMPLE 3**	**SAMPLE 4**	**NEGATIVE FULL-SCALE SETTLING ERROR**
50	277.26	228.5	1.2 LSB

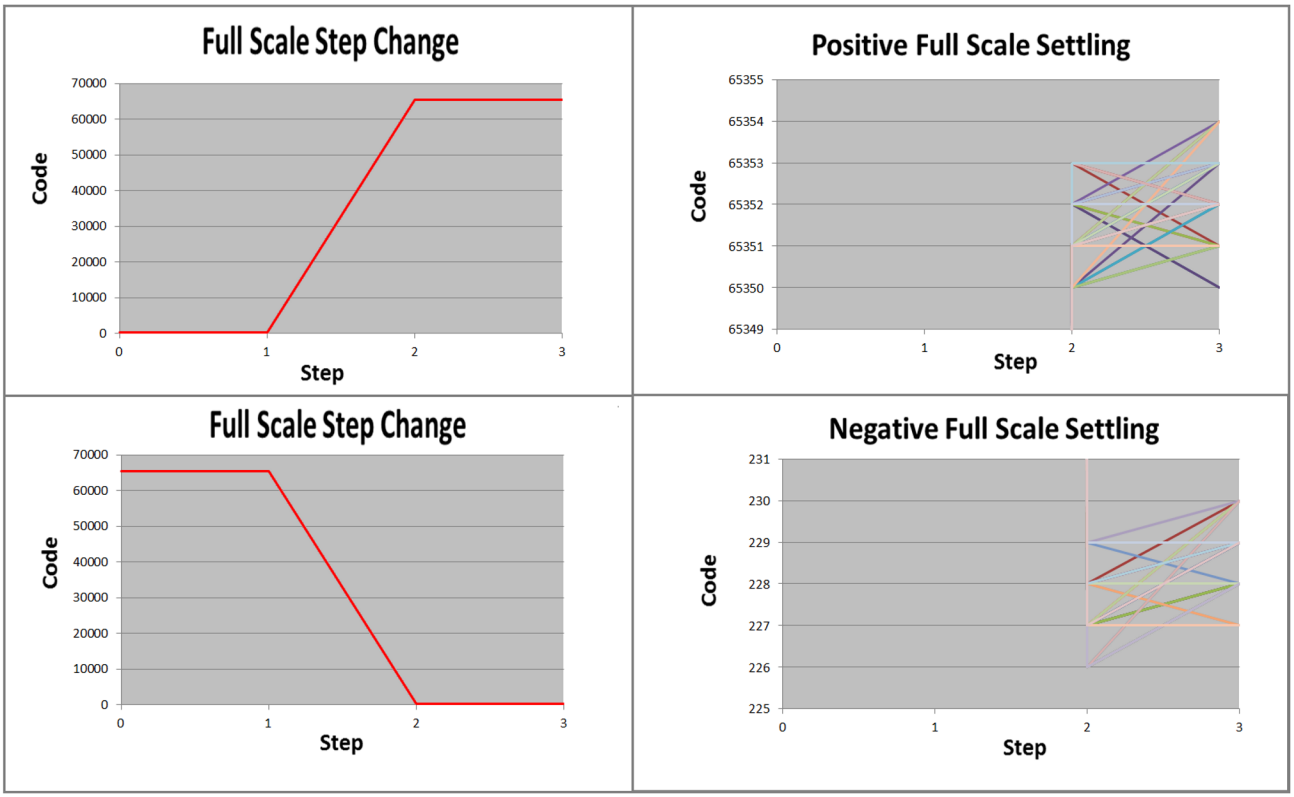

Figure 30. Measurement Result—Settling Time Performance for Full-Scale Step

5.3 ADC Linearity Measurement

The linearity of the system was measured by sweeping the differential input voltage from –20 V to 20 V in 11 voltage steps and the integral nonlinearity (INL) error is plotted after cancelling the offset and gain errors from the response. Figure 31 shows the 11-point INL plot. The DAQ block provides the *best linearity performance* of ±1 LSB, as the measurement result shows. The amplifiers used in the front-end driver (OPA140 and OPA192) have low output impedance, which results in extremely low distortion. The measured INL error from the entire system is within the specified INL of the ADC.

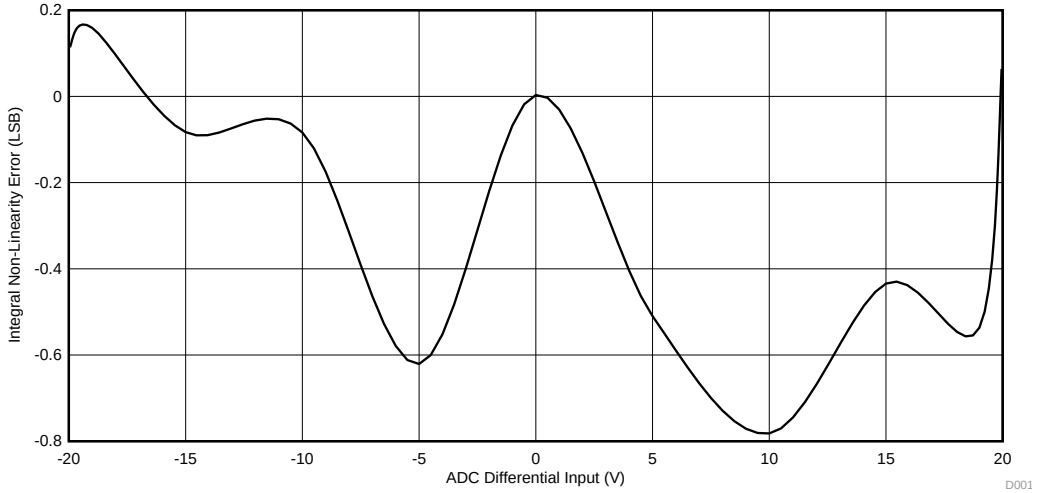

Figure 31. Measurement Result—ADC Integral Nonlinearity Error (INL) Plot (11 Points)

5.4 ADC Dynamic Performance Measurement

The design explained in this document has been optimized to achieve maximum performance out of an ADS8864 device at 400-kSPS throughput for a full-scale 10-kHz sine-wave input signal. The input signal to each channel is a ±20-V (40 V_{pk-pk}) sine wave. Each alternating channel is in opposite phase, thus the system observes a full-scale voltage swing of 40 V_{pk-pk} during channel switching. Figure 32 and Figure 33 show the input signal and Figure 34 shows the results.

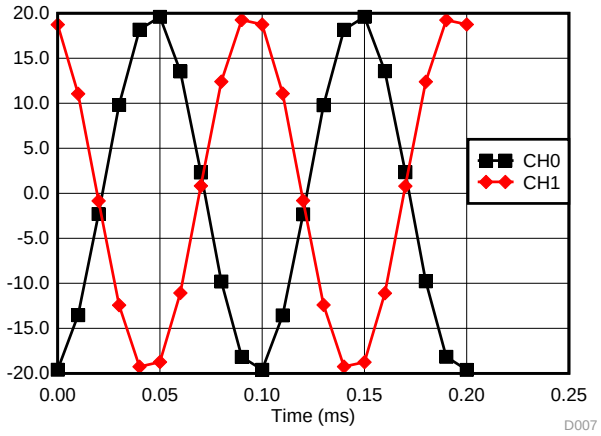

Figure 32. Input Signal of 40 V_{pk-pk} at 10 kHz—Alternating Channel 0 and Channel 1 Out of Phase For Worst-Case Scenario

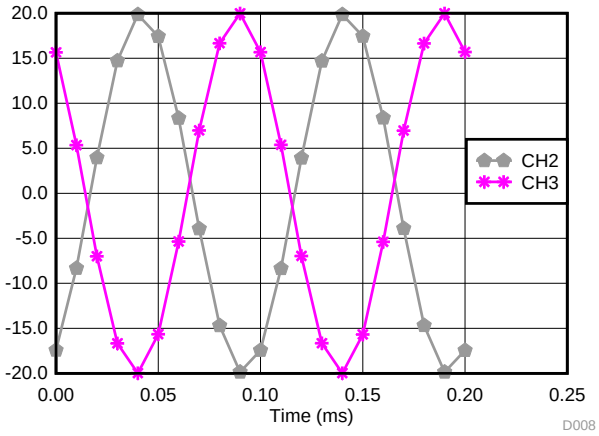

Figure 33. Input Signal of 40 V_{pk-pk} at 10 kHz—Alternating Channel 2 and Channel 3 Out of Phase For Worst-Case Scenario

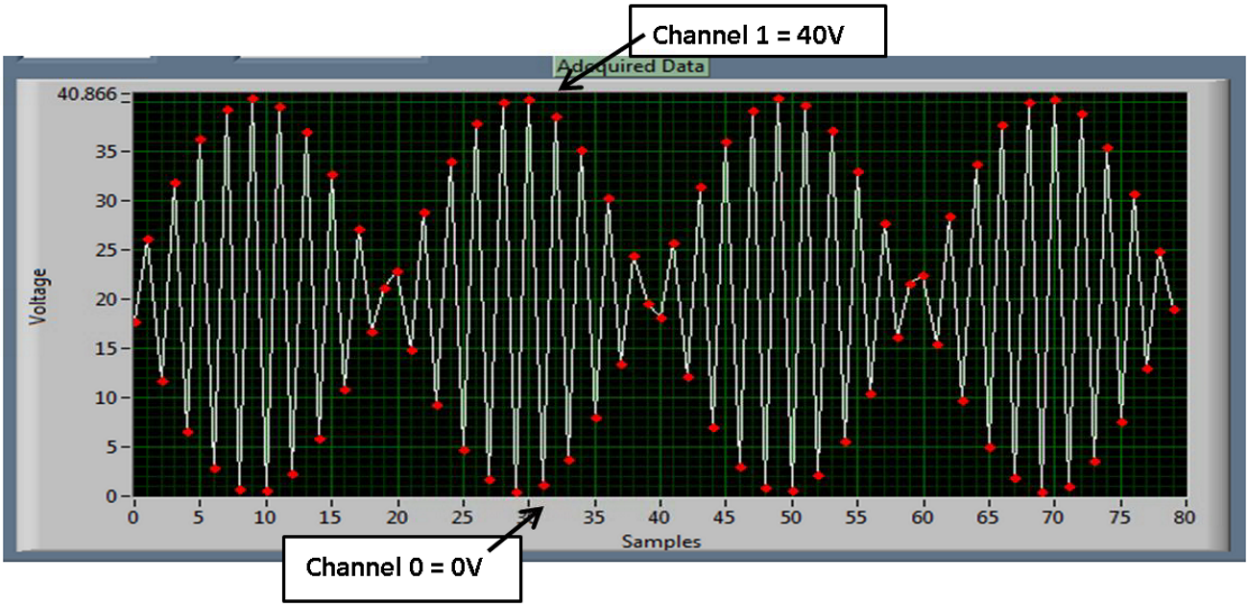

Figure 34. Measurement Result: Input Signal of 40 V_{pk-pk} at 10 kHz—Alternating Channels Out of Phase

Table 13 shows the AC performance of each channel of the DAQ block. The measurements have been performed using a 10-kHz sinusoidal input signal. Figure 35, Figure 36, Figure 37, and Figure 38 show the FFT of each channel of the data acquisition block. Observe how the overall system achieves an average SINAD per channel of 87.02 dB, which corresponds to an ENOB of 14.2 bits. The system achieves a high overall THD despite having a very large input sine wave of 40 V_{pk-pk} at a 10-kHz frequency. Furthermore, all channels are fairly symmetric in their performance.

Table 13. Measurement Results for ADC AC Performance

SPECIFICATION	CHANNEL 0	CHANNEL 1	CHANNEL 2	CHANNEL 3	AVERAGE
SNR (dB)	87.45	87.42	87.45	87.5	87.46
THD (dB)	–99.85	–97.45	–99.45	–97.9	–98.66
SINAD (dB)	87.21	87.0	87.19	87.12	87.13
ENOB (bits)	14.19	14.16	14.19	14.18	14.18

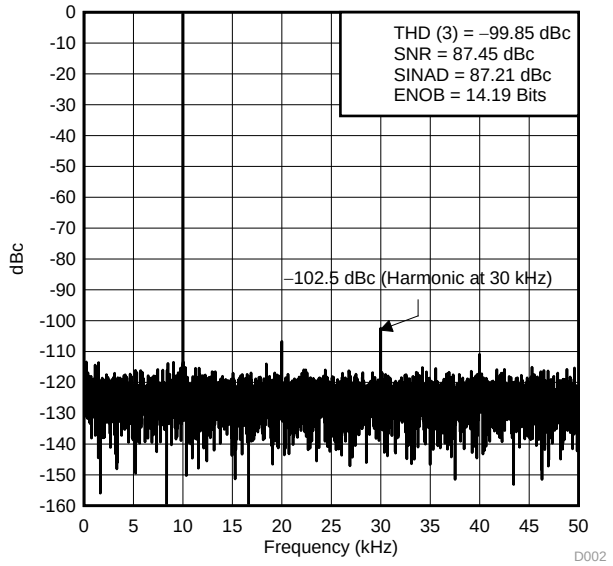

Figure 35. Measurement Result for FFT—Channel 0

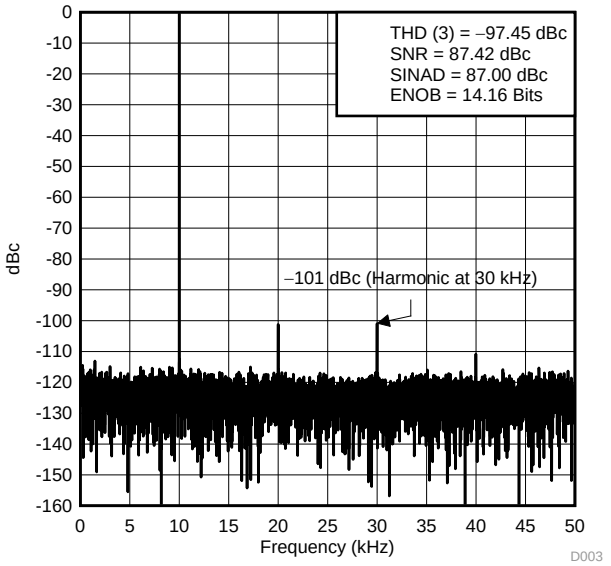

Figure 36. Measurement Result for FFT—Channel 1

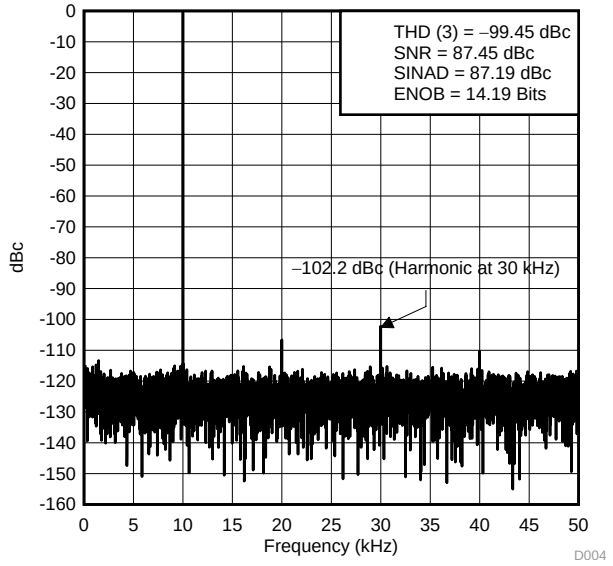

Figure 37. Measurement Result for FFT—Channel 2

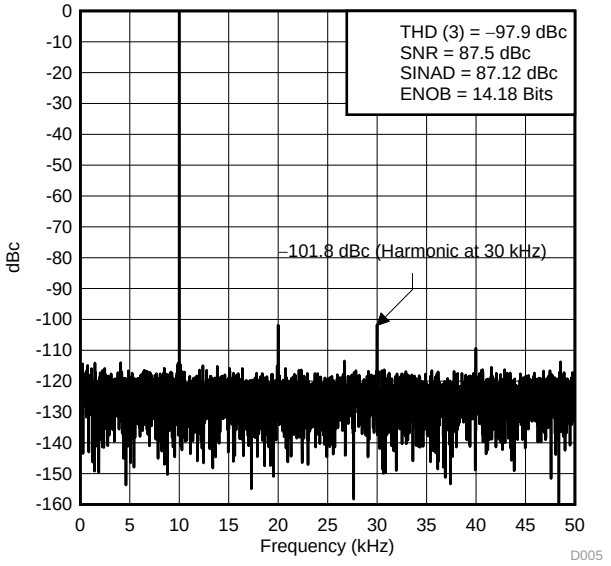

Figure 38. Measurement Result for FFT—Channel 3

6 Modifications

The DAQ system designed in this precision design is for a four-channel differential input. The design can be extended to an eight-channel differential input by merely replacing the input MUX to an 8:2 MUX and the ADC to a 16-bit, 1-MSPS ADS8860 device. The rest of the signal chain can remain identical. The new data acquisition still achieves 100 kSPS per channel at a 16-bit linearity.

The MUX508 and MUX509 devices are two other alternatives that can be used in this design but only if the output impedance of the signal source remains low. In this design, the OPA192 device provides a low enough source impedance such that the 10-pA leakage current of the MUX508 and MUX509 do not change the system performance. Table 14 shows two other low distortion and low noise amplifiers from TI's portfolio that have been considered for this design.

Table 14. Alternative Amplifiers Compared With OPA192 and OPA140

OP AMP	QUIESCENT CURRENT (mA)	NOISE DENSITY AT 10 kHz (nV/√Hz)	TOTAL HARMONIC DISTORTION (dB)	BANDWIDTH (MHz)
OPA172	1.6	6	–126	10
THS4031	7.9	1.6	–96	100

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIPD151.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIPD151.

7.3 PCB Layout Recommendations

7.3.1 Layout Prints

To download the layer plots, see the design files at TIPD151.

7.4 Altium Project

To download the Altium project files, see the design files at TIPD151.

7.5 Gerber Files

To download the Gerber files, see the design files at TIPD151.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIPD151.

8 Software Files

To download the software files, see the design files at TIPD151.

9 Acknowledgments

Thanks to Art Kay and Collin Wells for the many discussion during the design and help in reviewing this document.

10 References

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11 About the Author

VAIBHAV KUMAR is an Analog Design Manager in the Precision Linear group at Texas Instruments. He specializes in the IC design of precision amplifiers, references and mixed signal devices. Prior to joining Texas Instruments, Vaibhav received his MSEE and BSEE from Iowa State University. He has also authored in IEEE publications on design of precision amplifiers and data converters

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2016) to B Revision	Page
• Converted document to .xml	1
• Changed document title from *16-Bit, 400kSPS, 4-Channel Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion* to *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design*	1
• Deleted MUX509 from *Design Resources*	1
• Added paragraph to Section 2.2.1	6
• Added Equation 5	6
• Added paragraph to *Section 2.2.1*	6
• Added paragraph to *Section 3.9*	24

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