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Power-optimized 16-bit 1MSPS Data Acquisition Block for Lowest Distortion and Noise Reference Design

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Circuit Description

This circuit is the realization of a high precision, 16-bit 1MSPS data acquisition system suitable for applications such as digital audio that require front-ends with very low distortion and noise. The circuit uses a high performance Successive Approximation Register Analog to Digital Converter (SAR ADC) and has been optimized to provide superior dynamic performance, without excessive power consumption.

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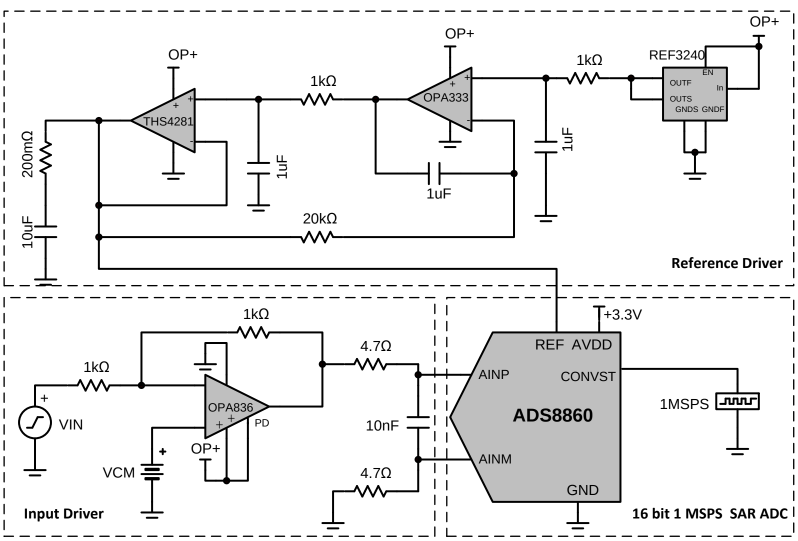

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1 Design Summary

The design requirements are as follows:

- ADC: 16 bit SAR ADC with 1MSPS sampling rate and full-scale input range (FSR) of 4.096V
- Input signal: 10 kHz sinusoid with peak-to-peak amplitude >3.87V
- Supply Voltage: 3.3V for ADC, 5V for other system components

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured output signal characteristics.

Table 1: Comparison of Design Goals and Measured Performance

	Goal	Measured
Total Harmonic Distortion (THD)	<-108dB	-110dB
Signal to Noise Ratio (SNR)	>91dB	91.6dB
Integral Non-Linearity (INL)	<±1.5LSB	<±0.5LSB
Dynamic Power Consumption	<40mW	30.75mW

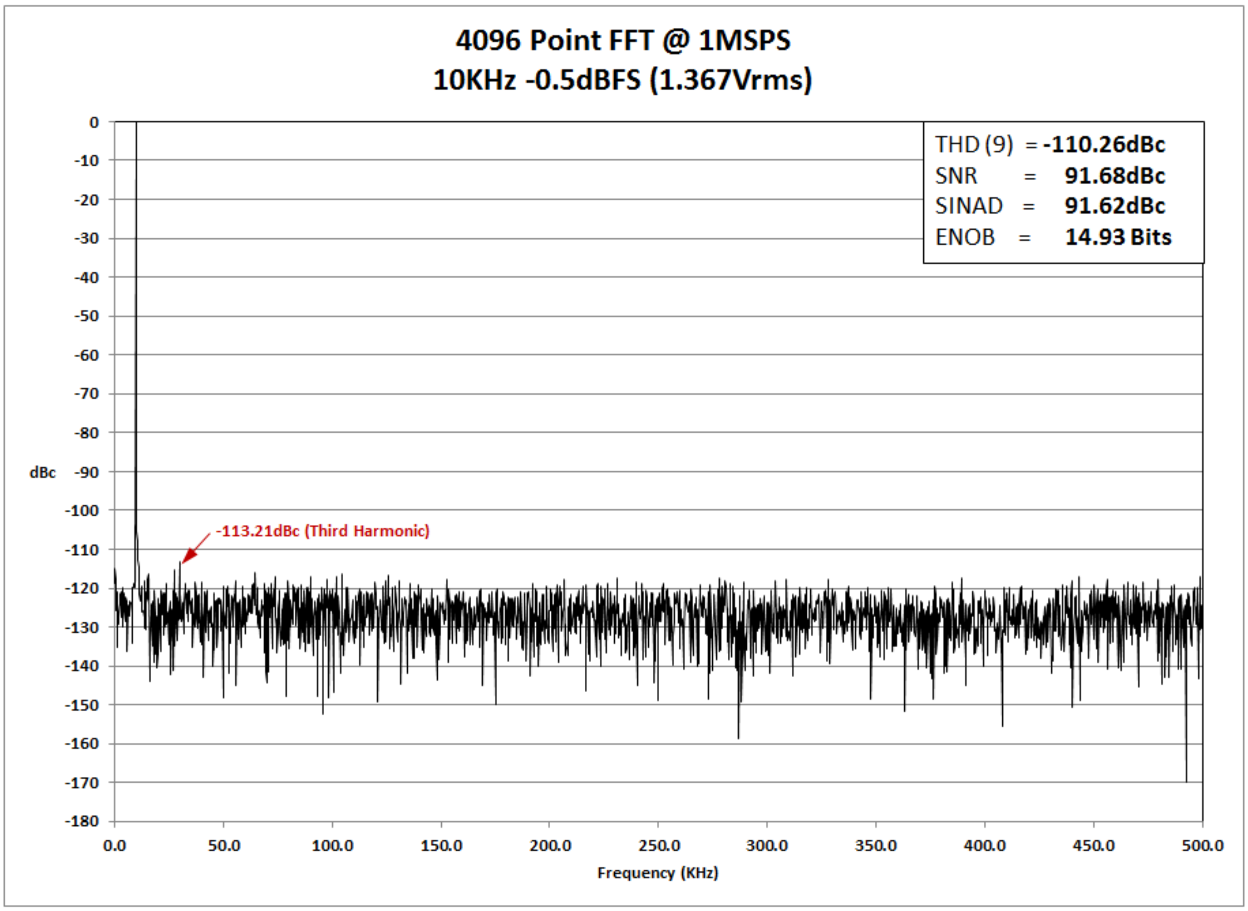


Figure 1: FFT of the ADC output

2 Theory of Operation

Figure 2 shows a block diagram highlighting the major blocks of this design.

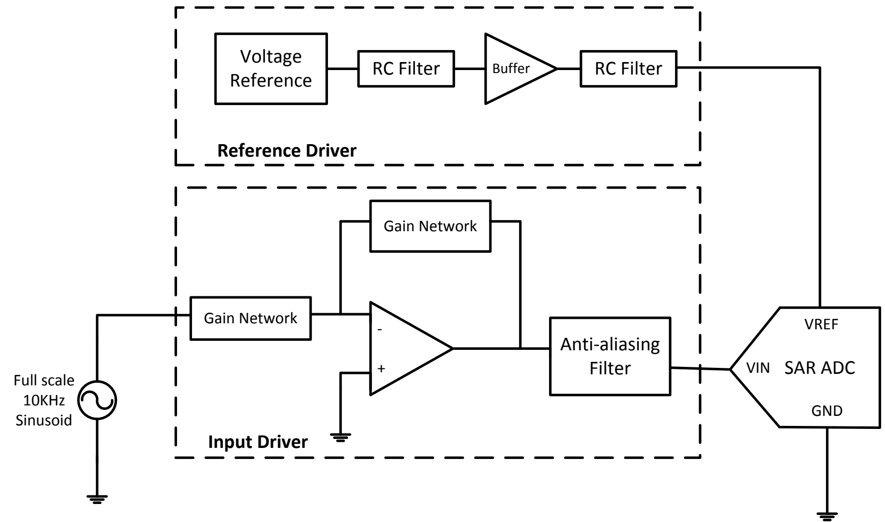


Figure 2: Block Diagram

The performance of the data acquisition system is limited primarily by the specifications of the SAR ADC. However, the input and reference drive circuits have certain non-ideal characteristics that further degrade the performance of the system. Therefore, the philosophy behind the design process is to identify the dominant sources of performance degradation external to the ADC, and either eliminate or minimize their effects through careful design.

2.1 Measuring distortion and noise

The distortion and noise content of the ADC output can be calculated from its Power Spectrum or FFT plot. Shown in Figure 3 is the normalized FFT plot of the output of an ADC for a 1 kHz sinusoidal input whose amplitude is about 0.5dB below the ADC's Full Scale Range (FSR).

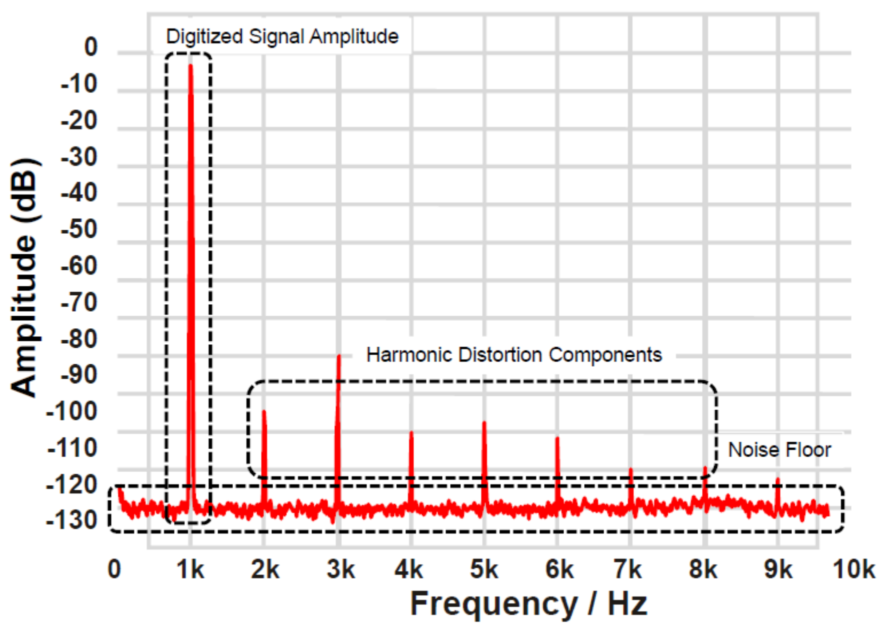


Figure 3: Typical FFT plot of ADC output signal

The distortion in the signal is computed by taking the root sum of squares (RSS) of the absolute amplitudes (in V for a voltage signal) of the harmonic components over the sampling bandwidth of the ADC. Harmonic frequencies are integral multiples of the input signal frequency (or “fundamental” frequency) and typically the first 9 harmonics are most significant. The power spectrum of the ADC output signal is generally specified in dB which is a fractional quantity of the fundamental power, and needs to be converted to absolute RMS amplitude (voltage) as follows:

$$V_{RMS} = V_{FSR} \times 10^{\frac{Amplitude_{dB}}{20}} \qquad (D1)$$

$$where\ V_{FSR}\ is\ the\ ADC\ full\ scale\ input\ range$$

The RSS combination of the harmonic components then becomes:

$$V_{HAR\_TOT\_RMS} = \sqrt{\sum_{i=1}^{9} V_{RMS}^2\big((i+1) \times f_{in}\big)} \qquad (D2)$$

$$where\ "f_{in}"\ is\ the\ input\ frequency$$

Likewise, the total output noise over the sampling bandwidth can be obtained by computing the RSS of the amplitudes of components other than the signal and its harmonics:

$$V_{n\_TOT\_RMS} = \sqrt{\int_0^{\frac{f_s}{2}} V_{RMS}^2(f)df - \sum_{i=0}^{9} V_{RMS}^2\big((i+1) \times f_{in}\big)} \qquad (D3)$$

$$where\ "f_s"\ is\ the\ ADC\ sampling\ frequency$$

The distortion and noise performance of the ADC are characterized by Total Harmonic Distortion (THD) and Signal to Noise Ratio (SNR) respectively. These quantities are simply relative measures of the output distortion and noise with respect to the fundamental signal amplitude (V_{SIG_RMS}). In other words:

$$THD = \frac{V_{HAR\_TOT\_RMS}}{V_{SIG\_RMS}} \qquad (D4)$$

$$SNR = \frac{V_{SIG\_RMS}}{V_{n\_TOT\_RMS}} \qquad (D5)$$

Note that for lowest distortion and noise performance THD should be minimized and SNR should be maximized.

2.2 Dominant sources of distortion and noise

As noted earlier, the design process involves minimizing the contributions of the major sources of distortion and noise in the system. The ADC and the input driver together produce most of the distortion, while the reference driver along with the ADC and the input driver contribute most of the noise. Therefore, in order to get lowest distortion and noise performance from the ADC the distortion contribution of the input drive circuit ($V_{HAR\_INP\_RMS}$) must be much lower than that of the ADC ($V_{HAR\_ADC\_RMS}$), and the noise contributions of the input ($V_{n\_INP\_RMS}$) and reference ($V_{n\_REF\_RMS}$) drive circuits must be much lower than that of the ADC ($V_{n\_REF\_RMS}$) as well:

$$V_{HAR\_INP\_RMS} \ll V_{HAR\_ADC\_RMS} \qquad (D6)$$

$$V_{n\_INP\_RMS} \ll V_{n\_ADC\_RMS} \qquad (D7)$$

$$V_{n\_REF\_RMS} \ll V_{n\_ADC\_RMS} \qquad (D8)$$

2.3 Input Driver Design

The purpose of the input driver in this design is to drive a full-scale 10 kHz sinusoidal signal across the SAR ADC input sampling capacitor, without introducing significant distortion or noise. In particular, the input driver must meet the following requirements:

1) Drive a capacitive load

2) Low distortion

3) Low noise

Requirement 1) translates into the need for a fast settling response. Each sample of the input signal must settle completely across the sampling capacitor before the end of the sampling window. This requires the input driver to have low output impedance over a wide frequency range. The signal source itself may serve as the input driver as long as its output impedance is sufficiently low, but this cannot be guaranteed for every source. Therefore, it is necessary to decouple the signal source from the ADC input by way of a buffering element that is guaranteed to provide low impedance drive to the ADC input. So an op amp buffer must be present in the signal path, between the signal source and the ADC input.

One of the problems with using an op amp to drive a capacitive load is that depending on the magnitude of the voltage change across the sampling capacitor, the transient load current can be large enough to cause the op amp output to current limit and slew. Slewing not only distorts the op amp output but also increases its settling time. To prevent op amp slew, there must be an alternate input source that is capable of regulating the ADC input voltage by supplying the fast transient load currents. For this purpose, a sufficiently large (so-called "charge bucket") capacitor, which functions as a near-ideal voltage source, is placed across the ADC input.

The value of the charge bucket capacitor (C_{FLT}) is chosen so that there is a less than 5% voltage drop across the ADC input (V_{IN}) after the required charge (Q_{SH}) has been transferred to the sampling capacitor (C_{SH}) during the acquisition phase. Therefore:

$$Q_{SH} = C_{FLT} \times \Delta V_{IN} \quad where \quad \Delta V_{IN} \leq 0.05 \times V_{IN} \quad (1a)$$

$$Q_{SH} = C_{SH} \times V_{IN} \leq C_{FLT} \times 0.05 \times V_{IN} \quad (1b)$$

$$\boldsymbol{C_{FLT} \geq 20 \times C_{SH}} \qquad \mathbf{(1)}$$

C_{SH} is a datasheet parameter and therefore C_{FLT} can be suitably chosen.

The issue with connecting a large capacitor directly at the output of an op amp is that it causes the op amp to become unstable and therefore non-linear. In this case, C_{FLT} combines with the open-loop output resistance (R_O) of the op amp and introduces a second pole (f_P) in the op amp's gain bandwidth. Since each pole contributes -90˚ of phase shift to the op amp output, the phase shift of the op amp output relative to its input approaches -180˚, for frequencies above $f_{P,}$ at which point the op amp becomes unstable. The proximity of the input-output phase difference to 180˚ over the closed-loop bandwidth of the circuit is called "phase margin". So in other words, the second dominant pole causes a degradation of the op amp's phase margin, as a result of which the op amp becomes less stable.

To overcome closed-loop instability, a sufficiently large resistor (R_{FLT}) must be placed in series with the op amp output to isolate it from C_{FLT}. The resistor introduces a zero at a frequency (f_Z) above f_P. The zero contributes +90˚ phase shift to the op amp output, essentially nullifying the phase lag introduced by the second pole. Consequently, the op amp's phase margin improves and it becomes more stable.

The effects of these phase changes due to f_P and f_Z on the op amp's open-loop gain response (A_{OL}) are depicted in Figure 5.

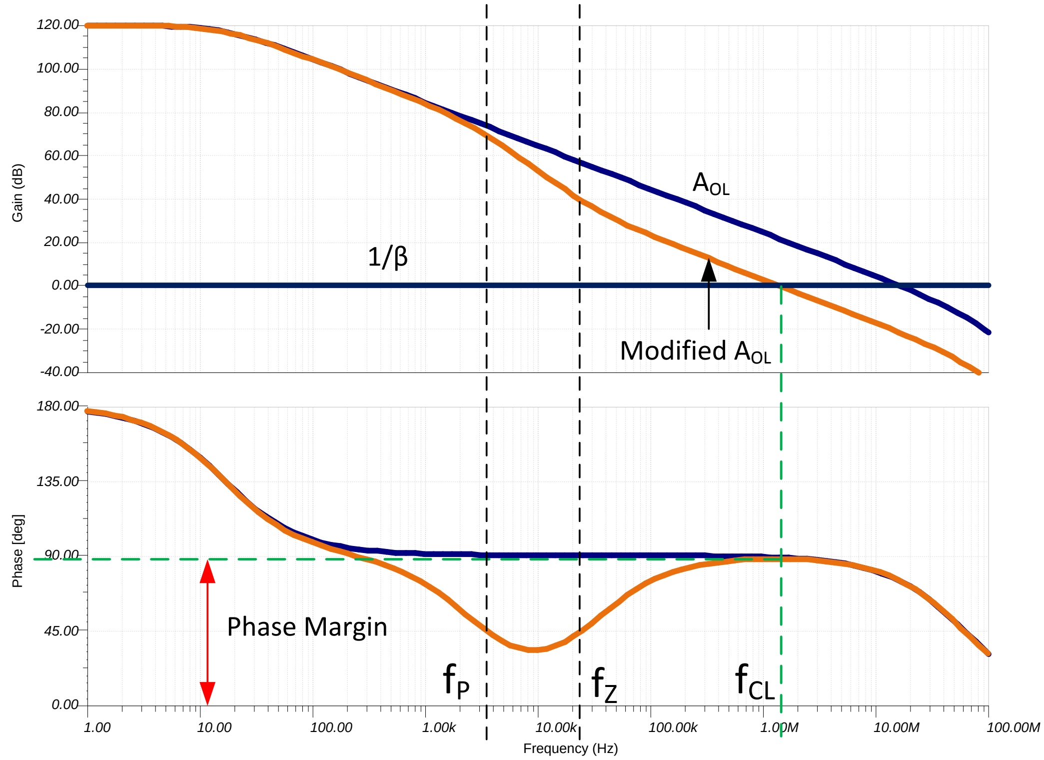


Figure 5: Introducing fz restores AOL phase and stabilizes the op amp

The pole and zero frequencies are given by:

$$f_P = \frac{1}{2\pi R_{FLT} C_{FLT}} \quad (2a)$$

$$f_Z = \frac{1}{2\pi (R_{FLT} + R_O) C_{FLT}} \quad (2b)$$

To ensure that the op amp will have sufficient phase margin when loaded by C_{FLT}, the value of R_{FLT} must be chosen so that f_Z occurs within a decade above f_P. In other words,

$$f_z \leq 10 \times f_p \quad (2c)$$

$$\frac{1}{2\pi R_{FLT} C_{FLT}} \leq 10 \times \frac{1}{2\pi (R_o + R_{FLT}) C_{FLT}} \quad (2d)$$

$$\boldsymbol{R_{FLT} \geq \frac{R_o}{9}} \quad (\mathbf{2})$$

R_O is typically derived from the op amp datasheet and thus the minimum required value of R_{FLT} can be calculated.

The isolation resistor forms a low-pass filter in combination with the reservoir capacitor which is critical for meeting requirement 3). By picking suitable values for R_{FLT} and C_{FLT} the bandwidth of the input signal path can be set to a suitable value within $f_S/2 < BW_{FLT} < f_S$ (f_S is the ADC sampling rate) to suppress aliased noise.

Shown in Figure 6 is the general structure of the input drive circuit that emerges:

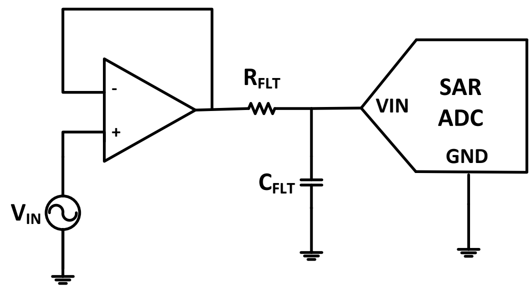


Figure 6: General structure of ADC input path

2.3.1 Optimizing Input Driver for Low Distortion

Now that the general topology of the input drive circuit is known, the circuit may be optimized for distortion and noise performance. With regard to distortion, there are at least three significant sources of distortion in the input signal path, apart from op amp slew and instability. These distortion sources are modeled in Figure 7:

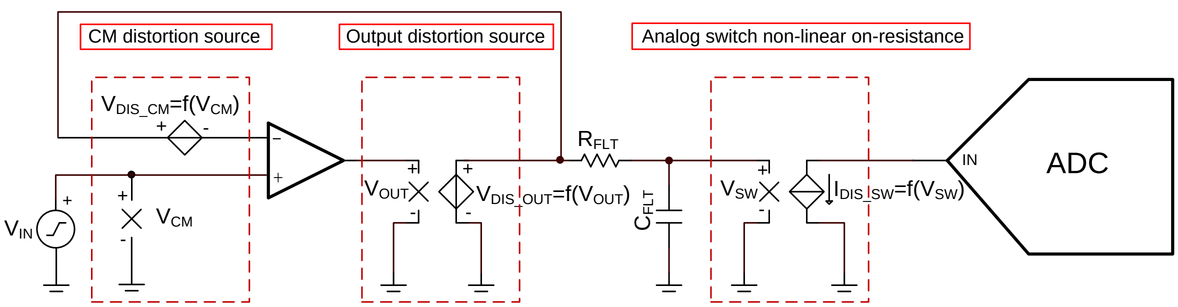


Figure 7: Major sources of distortion in input signal path

Common mode distortion is the result of the input offset voltage not being constant. In many op amps the input offset voltage varies with the input common mode voltage. This makes the op amp’s input-output relationship non-linear and thus the op amp output is distorted.

Common mode distortion (V_{DIS_CM}) is an issue when the op amp is configured for non-inverting gain because the input common-mode voltage follows the dc input signal in this configuration. On the other hand, the inverting gain configuration keeps the input CM voltage fixed. As a result the input offset voltage remains constant and the op amp output is free of CM distortion. So for lowest distortion, it is best to use the input op amp in an inverting gain configuration.

Output distortion (V_{DIS_OUT}) is due to non-linearity in the op amp’s output stage transfer function. Push-pull output stages use complementary transistors to conduct the output current. Each transistor conducts over a different range of output voltage, and there is a so-called “crossover” region in which the output current crosses over from one transistor to the other, where both transistors are in cut-off. The gain of the op amp output stage over this crossover region is zero and consequently the output voltage does not respond to changes in the input voltage, thus creating a non-linear region in the output stage transfer function.

Negative feedback minimizes op amp output distortion. Figure 8 depicts a block diagram representation of the input buffer circuit with the op amp output stage distortion modeled as “NL”. The closed loop response of the system is given by Equation (3a), which shows that the effect of NL on the output of the closed loop system is minimized by a factor of 1/(1+Aβ). “A” represents the op amp’s A_{OL}, “β” is called the “feedback factor” and “Aβ” is known as “loop gain”. So negative feedback minimizes op amp output distortion as long as loop gain is large enough (>>1).

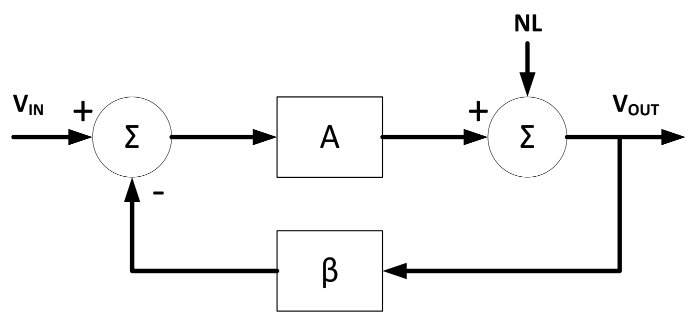


Figure 8: Closed loop model of input drive circuit showing output stage distortion

$$V_{OUT}(f) = \frac{V_{IN}(f)}{1 + A(f)\beta(f)} + \frac{NL}{1 + A(f)\beta(f)} \quad (3a)$$

However, note that loop gain is a frequency dependent quantity. As shown in Figure 9, loop gain is high at low frequencies and degrades at higher frequencies. Consequently, distortion increases at higher frequencies.

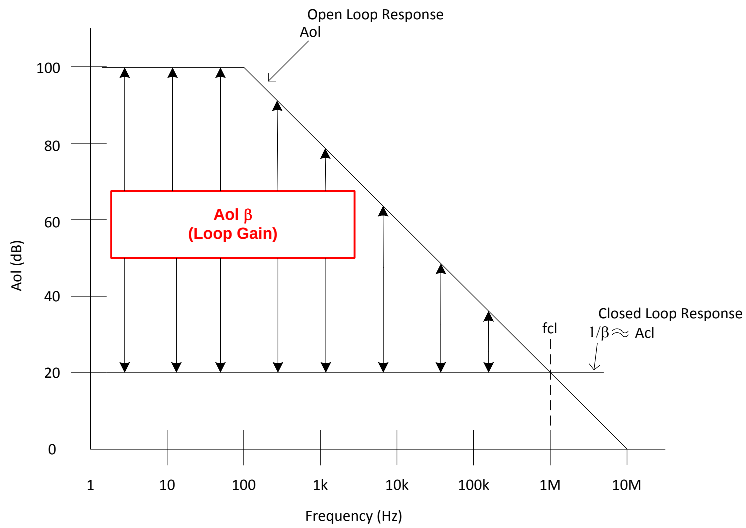


Figure 9: Loop gain vs. Frequency

In order to minimize distortion, sufficient loop gain must be available at the frequencies of interest to provide the required attenuation. Preserving loop gain over frequency requires selecting an op amp with sufficient gain-bandwidth (GBW).

From section 2.2 recall the requirement $V_{HAR\_INP\_RMS}$ << $V_{HAR\_ADC\_RMS}$. This requirement can be made more specific by restating it as follows:

$$\boldsymbol{THD_{AMP} < THD_{ADC} - 10dB} \quad (\mathbf{3})$$

$$THD_{ADC} = -108dB \implies THD_{AMP} < -118dB \quad (4a)$$

Assuming the output stage distortion is at least 0.1% (or >-60dBc), the required attenuation over the frequency range of interest is:

$$Required\ A\beta > -60dB - (-118dB) \approx\ 60dB \quad (4b)$$

Since the first and second harmonics typically contain the majority of the distortion content, the loop gain must be > 60dB over at least 3x the input frequency. From Figure 9, it is evident that loop gain decreases at the rate of -20dB/decade. So the number of decades above 3x input frequency before the loop gain diminishes from 60dB to 0dB is:

$$decades\ to\ f_{CL} = \frac{(0dB - 60dB)}{-20dB/decade} = 3\ decades \quad (4c)$$

Therefore the GBW of the input driver op amp should be 3 decades above $3f_{IN}$ or in other words:

$$\boldsymbol{GBW \geq 10^{3\ decades} \times (3f_{IN}) = 3000 \times f_{IN} \quad (4)}$$

The third major source of distortion in the input signal path is the on-resistance of the analog sampling switch inside the ADC (modeled as I_{DIS_SW} in Figure 7) that has a non-linear dependence on input voltage. Figure 10 shows the typical Ron vs. input voltage curve of a CMOS analog switch.

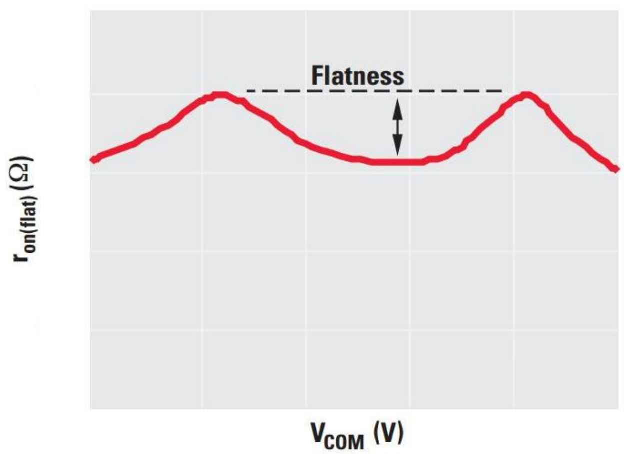


Figure 10: Typical Ron vs. input voltage characteristic of CMOS analog switch

When the sampling phase begins, the sampling switch is closed and the non-linear switch resistance forms a voltage divider in combination with the isolation resistor R_{FLT} at the output of the op amp and distorts the input signal.

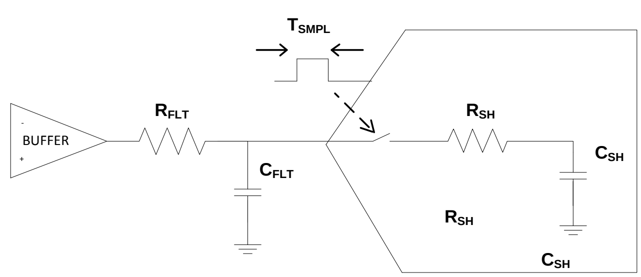


Figure 11: ADC input during sampling phase

Using smaller values of R_{FLT} ensures that the input signal attenuation, although non-linear, is as small as possible. As a rule of thumb R_{FLT} is chosen such that:

$$\boldsymbol{R_{FLT} \leq \frac{R_{SH}}{10} \quad (5)}$$

2.3.2 Optimizing Input Driver for Low Noise

As stated in section 2.2, achieving good noise performance requires the noise contribution of the input driver to be much less than that of the ADC. More specifically, this requirement may be restated as follows:

$$\boldsymbol{V_{n\_INP\_RMS} \leq \frac{1}{3} \times V_{n\_ADC\_RMS}} \quad \mathbf{(6)}$$

The total noise present at the ADC input is dominated by the output-referred (RTO for "Referred To Output") noise of the op amp buffer circuit. Figure 12 shows the various noise sources.

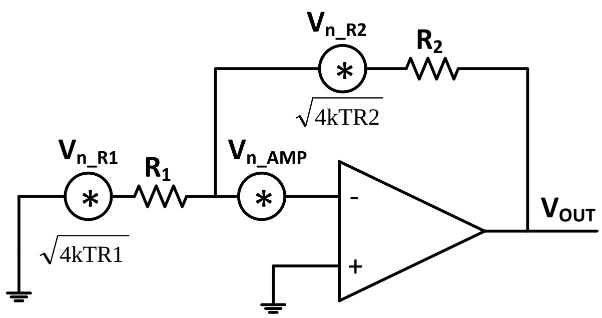


Figure 12: Noise sources in inverting op amp buffer circuit

The RTO noise of the buffer circuit is the product of the total input-referred noise (RTI for "Referred To Input") and the Noise Gain (NG).

$$V_{n\_INP\_RMS} \approx V_{n\_RTO\_AMP\_RMS} = NG \times V_{n\_RTI\_AMP\_RMS} \quad (7a)$$

The noise gain is the reciprocal of the output-to-input gain seen by the noise source present at the op amp output, with all other sources removed.

$$NG = \left[\frac{R1}{R1 + R2}\right]^{-1} = 1 + \frac{R2}{R1} \qquad (7b)$$

The total input referred noise is the RSS of the RMS noise contributions of the op amp and resistors at the op amp input. The noise contribution of each individual source is calculated by integrating the noise spectral density of the source over the effective bandwidth of the input path.

$$V_{n\_RTI\_AMP\_RMS} = \sqrt{\frac{\pi}{2} \times BW_{FLT}} \times \sqrt{e_{n\_AMP\_RMS}^2 + 4kTR1\left(\frac{R2}{R1 + R2}\right)^2 + 4kTR2\left(\frac{R1}{R1 + R2}\right)^2} \quad (7c)$$

The equation can be used to establish a minimum requirement on $e_{n\_AMP\_RMS}$ and this serves as a second criterion in addition to GBW for selecting the right op amp for the input drive circuit.

$$Equation\ (6) \Longrightarrow V_{n\_RTI\_AMP\_RMS} \leq \frac{V_{n\_ADC\_RMS}}{3 \times NG} \qquad (7d)$$

$$\sqrt{\frac{\pi}{2} \times BW_{FLT}} \times \sqrt{e_{n\_AMP\_RMS}^2 + \frac{4kTR1R2}{R1 + R2}} \leq \frac{V_{FSR} \times 10^{\left(\frac{-SNR\_dB}{20}\right)}}{3 \times 2\sqrt{2} \times NG} \quad (7e)$$

$$\boldsymbol{e_{n\_AMP\_RMS} \leq \sqrt{\left(\frac{V_{FSR} \times 10^{\left(\frac{-SNR\_dB}{20}\right)}}{3 \times 2\sqrt{2} \times NG}\right)^2 \times \frac{2}{\pi \times BW_{FLT}} - \frac{4kTR1R2}{R1 + R2}}} \quad \mathbf{(7)}$$

2.4 Reference Driver Design

The function of the reference drive circuit is to provide and maintain a constant dc voltage at the ADC reference input. The dc voltage must be accurate over time and precisely regulated against the large, fast load transients that occur at the ADC reference input during conversion. In particular, the reference driver must provide:

1) Low offset, low offset drift and low noise
2) Sufficient bandwidth and low output impedance for load regulation

Satisfying requirement 1) requires a high-precision voltage reference IC that can provide the required output voltage.

Voltage references are typically too noisy to be used for directly driving the input of a high resolution SAR ADC. Since the reference voltage is a dc signal, the voltage reference output needs to be band-limited to a narrow range near dc to minimize output noise. An RC low pass filter is typically used for this purpose.

The filter resistor increases the output impedance of the voltage reference and limits the amount of current the driver can provide to the load. Load currents at the REF input of a SAR ADC during conversion are characterized by spikes that are only a few nanoseconds in duration and have magnitudes of several milliamps, as switch-capacitor loads internal to the ADC are switched on and off the REF pin. Figure 13 shows the reference current transients measured on a typical 12-bit SAR ADC during conversion.

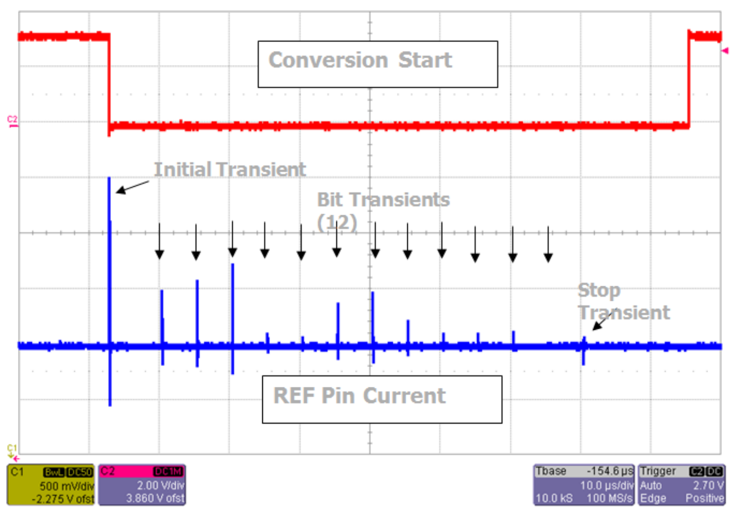


Figure 13: ADC reference input current during conversion

Each current transient occurs at the beginning of a period when the ADC makes a bit decision. As the source impedance of the reference driver is greater than 0Ω these current pulses cause the reference voltage to drop. The reference driver must be able to correct the voltage drop to < 1LSB error before the bit decision is made. Otherwise, the bit decision is incorrect and the ADC output will have errors. For low initial error and fast recovery of the reference voltage signal, the reference driver must have low output impedance over a wide range of frequencies.

Therefore, an op amp buffer is required to minimize the output impedance of the reference signal path. However, since loop gain decreases with A_{OL} over the bandwidth of the op amp, the closed loop output impedance of the op amp increases over frequency. Figure 14 shows the inductive characteristic of the buffer output impedance over frequency.

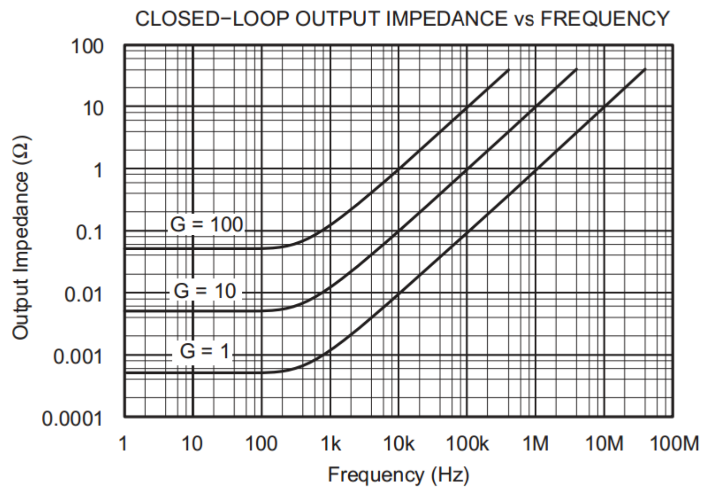


Figure 14: R_{OUT} of op amp buffer vs. frequency

Thus, whenever there is a high frequency change, such as when there is an instantaneous change in load current during the ADC conversion phase, the op amp presents high impedance to the load. The larger source impedance lowers the op amp's current limit, and increases the time required for the reference voltage to recover. To improve the reference voltage settling behavior, a bypass (or charge bucket) capacitor is required at the output of the reference buffer. The capacitor emulates an ideal voltage source (low ESR, very high bandwidth) and instantly supplies almost all the load current at high frequencies. The charge loss causes the voltage across the capacitor to decrease exponentially. This is a more gradual change so that the output impedance of the buffer decreases, and the buffer is able to correct the reference voltage error more quickly.

Shown in Figure 15 is the general structure of the reference drive circuit that follows from the discussion:

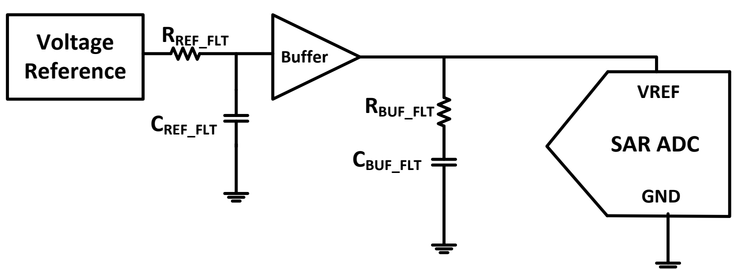


Figure 15: General structure of ADC reference drive circuit

An isolation resistor, R_{BUF_FLT} is required for stabilizing the op amp buffer. Placing the isolation resistor in series with the charge bucket capacitor maintains a low impedance path between the op amp output and the ADC reference input. The value of this resistor is chosen through simulation once the buffer op amp and charge bucket capacitor have been selected (see section 4).

The value of the C_{BUF_FLT} is selected to restrict the voltage drop across the capacitor after an ADC conversion phase to less than 1LSB. The ADC datasheet specifies the average current (I_{REF}) measured over many conversion cycles under the worst case input condition. At a sampling rate f_{samp}, the total charge transferred into the reference pin is given by:

$$Q_{REF} = \frac{I_{REF}}{f_{samp}} \quad (9a)$$

The charge bucket capacitor provides virtually all of this charge and the voltage across the capacitor droops by ΔV such that:

$$Q_{REF} = C_{BUF\_FLT} \times \Delta V \quad (9b)$$

As noted earlier, ΔV must be less than 1LSB for ADC output accuracy:

$$\Delta V < 1LSB = \frac{V_{FSR}}{2^N} \implies Q_{REF} < C_{BUF\_FLT} \times \frac{V_{FSR}}{2^N} \quad (9c)$$

Hence the minimum required value of the charge bucket capacitor can be calculated as follows:

$$\frac{I_{REF}}{f_{samp}} < C_{BUF\_FLT} \times \frac{V_{FSR}}{2^N} \quad (9d)$$

$$\boldsymbol{C_{BUF\_FLT} > \frac{I_{REF} \times 2^N}{V_{FSR} \times f_{samp}}} \quad (\mathbf{9})$$

For a fast, stable settling response of the voltage error across C_{BUF_FLT}, the closed loop output impedance (Z_{OUT}) of the op amp buffer must be as low as possible. This requires an op amp that has low open loop output impedance and wide GBW to preserve loop gain over frequency. However, in addition to these high speed characteristics, the op amp buffer must have low drift and low power consumption. Achieving high speed, high precision and low power consumption simultaneously is non-trivial and careful tradeoffs must be made to design a reference buffer that optimally meets these criteria. Section 3.3, presents a robust reference buffer circuit that has been thoroughly tested and verified for proper operation.

2.4.1 Optimizing Reference Driver for Low Noise

To minimize the noise contribution of the reference driver relative to that of the ADC, the following design requirement is imposed:

$$\boldsymbol{V_{n\_REF\_RMS} < \frac{V_{n\_ADC\_RMS}}{2}} \quad (\mathbf{10})$$

The most significant source of noise in the reference signal path is the voltage reference. The output noise of the voltage reference has two components – 1/f (or flicker) noise that dominates at low frequencies (0.1Hz to 10Hz) and broadband (or thermal) noise that dominates at higher frequencies. The total noise is the RSS of the two components. Therefore:

$$\sqrt{V^2{}_{1/f\_REF\_RMS} + V^2{}_{BB\_REF\_RMS}} < \frac{1}{2} \times \frac{FSR}{2\sqrt{2}} \times 10^{\frac{-SNR(dB)}{20}} \quad (11a)$$

The peak-to-peak value of the 1/f component (V_{1/f_REF_pp}) is generally specified in the voltage reference datasheet and can be used to compute the corresponding RMS value. The broadband component is obtained by integrating the noise spectral density of the broadband noise (e_{n_REF}) over the effective bandwidth of the voltage reference (f_{REF_3dB} * π/2). Therefore,

$$\boldsymbol{\sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + \left(e_{n\_REF}\sqrt{f_{REF\_3dB} \times \frac{\pi}{2}}\right)^2} < \frac{1}{2} \times \frac{FSR}{2\sqrt{2}} \times 10^{\frac{-SNR(dB)}{20}}} \quad (\mathbf{11})$$

The broadband noise spectral density of the voltage reference, e_{n_REF} is generally not a datasheet parameter. Instead, the quiescent supply current can be used as an indicator of noise performance. Measurements from multiple TI voltage references indicate an inverse square root relationship between quiescent supply current and broadband noise density. The empirical relationship is modeled by equation (12) which is plotted in Figure 16.

$$e_{n\_REF} \approx \frac{10000nV}{\sqrt{Hz}} \times \frac{1}{\sqrt{2 \times I_{Q\_REF}(in\ \mu A)}} \quad (12)$$

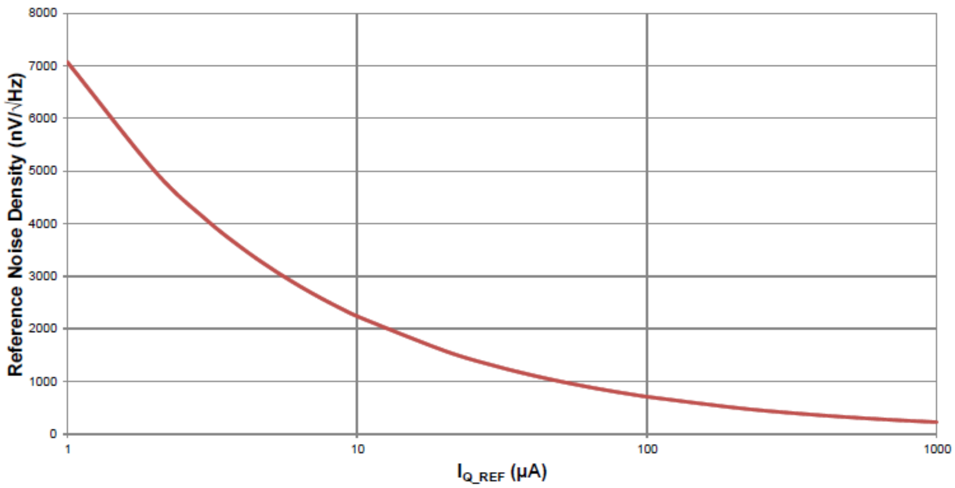


Figure 16: Voltage Reference noise spectral density vs. IQ

The parameter of interest in (11) is f_{REF_3dB}, which needs to be optimized not just for achieving low noise but also for reasonable N-bit settling time, in the interest of minimizing wasteful power dissipation. Solving constraints (11) and (12) for f_{REF_3dB} requires the knowledge of I_{Q_REF} and V_{1/f_REF_pp}. Both parameters are datasheet specifications and can be determined only after selecting a suitable voltage reference IC.

A suitable voltage reference must provide a nominal output voltage to properly set the ADC full-scale input range to the required value. In addition, the temperature drift of the voltage reference output must be as low as possible to preserve the long-term gain accuracy of the ADC.

Once a suitable voltage reference IC has been identified, f_{REF_3dB} can be calculated using (11) and (12).

3 Component Selection

The constraints derived in Section 2 can now be used to select suitable components for this design.

3.1 *SAR ADC*

The ADS8860 is a 16-bit 1MSPS SAR ADC that supports a 5V full-scale input range. The ADS8860 has typical THD and SNR specifications of -108dB and 93dB respectively for a near-full-scale pseudo-differential input sinusoid. Thus, the ADS8860 is a suitable ADC for this design.

3.2 *Input Driver*

3.2.1 *Op amp*

Equations (4) and (7) from section 2.3 set the following constraints on the op amp:

1. $GBW \geq 3000 \times f_{IN} = 3000 \times 10KHz = 30MHz$
2. $e_{n\_AMP\_RMS} \leq \sqrt{\left(\frac{V_{FSR} \times 10^{\left(\frac{-SNR\_dB}{20}\right)}}{3 \times 2\sqrt{2} \times NG}\right)^2 \times \frac{2}{\pi \times BW_{FLT}} - \frac{4kTR1R2}{R1+R2}}$

   Using typical values of R1 = R2 = 1kΩ, NG = 2 (inverting gain configuration), BW_{FLT} = 1MHz, V_{FSR} = 5V (nominal test condition), SNR_{dB} = 91dB yields:

$$e_{n\_AMP\_RMS} \leq 5.8nV/\sqrt{Hz}$$

   The op amp must also operate on a single +5V supply, have reasonably low IQ and support rail-to-rail output (RRO) swing.

   Shown in Table 2 are suitable voltage feedback amplifiers that consume less than 10mA of IQ:

Compare Parts	OPA836	THS4521	LMH6654	OPA690	OPA820	LMH6609	OPA380
Architecture	Voltage Feedback	Fully Differential Voltage Feedback	Voltage Feedback	Voltage Feedback	Voltage Feedback	Voltage Feedback	Voltage Feedback
GBW (Typ) (MHz)	118	95	260	300	280	900	90
Vn at Flatband (Typ) (nV/rtHz)	4.6	4.6	4.5	5.5	2.5	3.1	3
Iq per channel (Max) (mA)	1	1	6	6.2	6.4	8.5	8.8
Vs (Max) (V)	5.5	5.5	12	12	12	12	5.5
Vs (Min) (V)	2.5	2.5	4.5	4.5	5	6	2.7
Number of Channels (#)	1	1	1	1	1	1	1

Table 2: List of possible op amps for input driver

Based on the requirements of this design the OPA836 is an optimal fit.

3.2.2 Anti-aliasing RC filter components

The value of the charge bucket capacitor is given by (1):

$$C_{FLT} \geq 20 \times C_{SH} = 20 \times 59pF = 1.18nF$$

For low distortion, the filter capacitor must be a C0G/NP0 type. C0G type capacitors exhibit minimal change in capacitance over input voltage, frequency, temperature, etc., and are typically available in values of 10nF or less.

Thus, a C0G type capacitor with a value of C_{FLT} = 10nF is selected for this design.

The value of filter resistor has the following constraint that is obtained by combining (2) and (5):

$$\frac{R_o}{9} \leq R_{FLT} \leq \frac{R_{SH}}{10}$$

The nominal value of R_O is derived from the closed loop output impedance vs. frequency plot shown in the OPA836 datasheet (Figure 18)

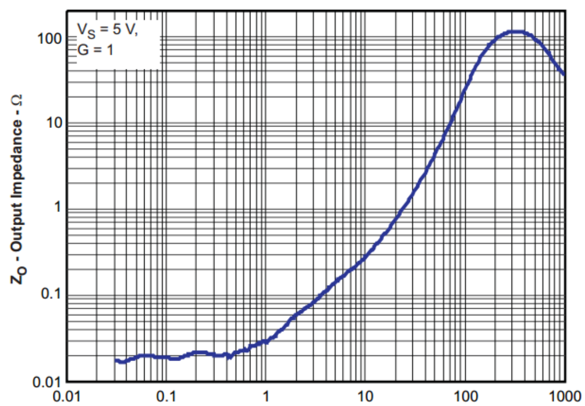


Figure 18: OPA836 closed loop output impedance vs. frequency

The magnitude of the op amp's closed loop output impedance (R_{OUT}) is a function of the op amp's open loop output impedance (R_O) and loop gain (Aβ):

$$R_{OUT}(f) = \frac{R_o}{1 + A\beta(f)} \implies R_o = R_{OUT}(f) \times \left(1 + A\beta(f)\right)$$

At f = GBW, A(f) = 1 and 1/β = 1 so loop gain A(f)β = 1 and thus

$$R_o = R_{OUT}(f = GBW = 118MHz) \times (1 + 1) = 21\Omega \times 2 = 42\Omega$$

From the ADS8860 datasheet, R_{SH} = 96Ω

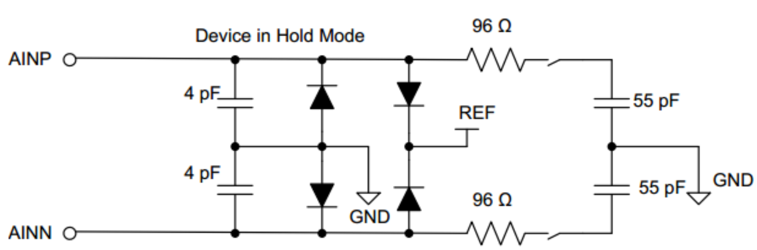


Figure 19: Structure of ADS8860 input stage

So the constraint on R_{FLT} becomes 4.6Ω ≤ R_{FLT} ≤ 9.6Ω, and a standard value of R_{FLT} = 4.7Ω can be used.

3.3 Reference Driver

3.3.1 Voltage Reference and output RC low-pass filter

The selection of the voltage reference is governed by nominal output voltage and temperature drift specifications. Shown in Table 3 is a list of low drift voltage references that provide between 4V and 5V output:

Compare Parts	REF5045	REF5040	REF3240	REF3140
VO (V)	4.5	4.096	4.096	4.096
Temp Coeff (Typ) (ppm/ degree C)	2.5	2.5	4	5
Initial Accuracy @ 25/deg C (%)	0.05	0.05	0.2	0.2
Iq (Typ) (uA)	800	800	100	100
0.1-10Hz Noise (Max) (µVpp)	13.5	12	53	53
Vin (Min) (V)	4.7	4.296	4.146	4.146
Vin (Max) (V)	18	18	5.5	5.5

Table 3: Search results for suitable Series Voltage References

The REF3240 provides a good balance between low drift and low power consumption, and is therefore the most appropriate choice for this design.

Using the typical IQ and flicker noise parameters for the REF3240 from Figure 20, the inequality in (11) can be solved for f_{REF_3dB}, yielding

$$f_{REF\_3dB} < 423\ Hz$$

Assuming R_{REF_FLT} = 1kΩ, C_{REF_FLT} becomes

$$C_{REF\_FLT} > \frac{1}{2\pi \times R_{REF\_FLT} \times f_{REF\_3dB}} \approx 0.38\ uF$$

A value of C_{REF_FLT} = 1µF can be selected so that f_{REF_3dB} = 159Hz and both requirements are satisfied.

3.3.2 Charge bucket capacitor and buffer amplifier

The charge bucket must be selected so that the voltage droop across the capacitor after each ADC conversion phase is less than 1LSB. Solving equation (9), using I_{REF} = 300µA, T_{CONV_MAX} = 710ns, V_{FSR} = 4.096 and N = 16, yields:

$$C_{BUF\_FLT} > \frac{I_{REF} \times 2^N}{V_{FSR} \times f_{samp}} = 4.8\mu F$$

A value of 10µF, which is about 2x the minimum required value, is chosen so that the capacitor only discharges by about 0.48LSB each conversion phase.

Now the selection of a suitable op amp for the reference buffer can be considered. Figure 21 shows a list of high speed op amps that support RRO swing on a single +5V supply:

Compare Parts	LMP7731	OPA320	OPA350	LM8261	OPA835	THS4281
Status	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	ACTIVE
Architecture						Voltage Feedback Rail-to-Rail
Rail-Rail	In Out	In Out	In Out	In Out		In Out
Acl, min stable gain (V/V)					1	1
Iq per channel (Max) (mA)	3	1.75	7.5	1.25	0.25	1
GBW (Typ) (MHz)	22	20	38	21	31	
BW @ Acl (MHz)					56	90
Offset Drift (Typ) (uV/C)	1	1.5	4	2		
Vn at 1kHz (Typ) (nV/rtHz)	2.9	8.5	18	15		
Total Supply Voltage (Max) (+5V=5, +/-5V=10)	5.5	5.5	5.5	30		
Total Supply Voltage (Min) (+5V=5, +/-5V=10)	2.5	1.8	2.7	2.5		

Table 4: Prospective op amps for reference buffer

The THS4281 is the best candidate for this design because it provides the highest bandwidth and consumes the lowest quiescent current relative to the other options featuring RRIO (OPA835 does not support RRI swing). The THS4281 also has <100mΩ of closed-loop output resistance at low frequencies (up to 100 kHz) in a buffer configuration (see Figure 22).

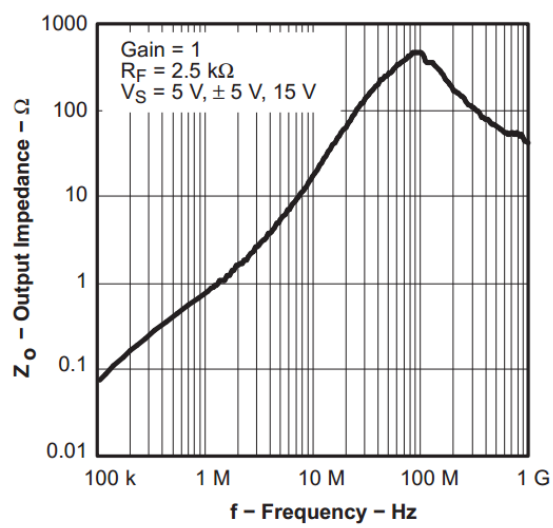


Figure 22: THS4281 closed-loop output impedance in buffer configuration

The only drawback of the THS4281 as it relates to this application is that it suffers from excessive offset drift (7µV/˚C). This adds to the 4ppm/˚C * 4.096V ≈ 16.4µV/˚C drift of the voltage reference, making Vref inaccurate over time. To limit the drift contribution of the THS4281, it can be used in a composite amplifier configuration as shown in Figure 28 with the OPA333, an ultralow power zero drift (0.05µV/˚C) amplifier, in the feedback loop of the THS4281.

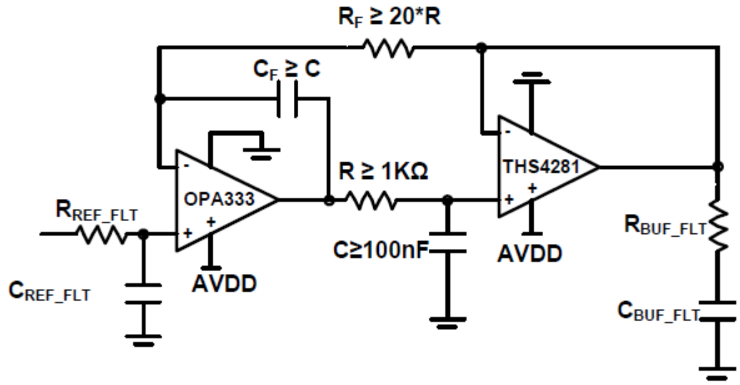


Figure 23: Reference buffer circuit

For high frequency operation, C_F behaves as a short and R_F is open. The OPA333 simply buffers the voltage reference output and the THS4281 buffer regulates the dynamic load. The noise contribution of the OPA333 is limited by heavy low pass filtering of its output using an RC filter.

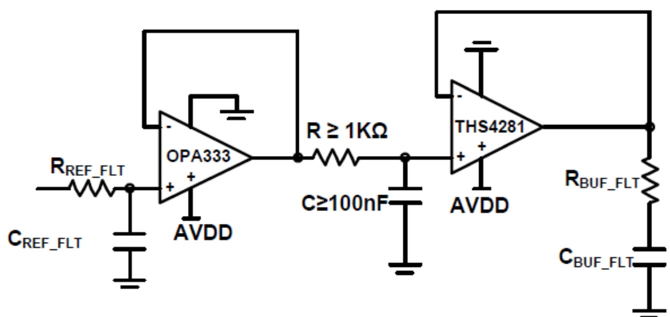


Figure 24: Reference buffer high frequency model

At dc however, C_F is open. The OPA333 senses any difference between the THS4281 output and the voltage reference output, and corrects it to within the margin allowed by its own offset error which is over two orders of magnitude lower than that of the THS4281. Thus, the composite amplifier limits the dc error in reference voltage to just the error introduced by the voltage reference.

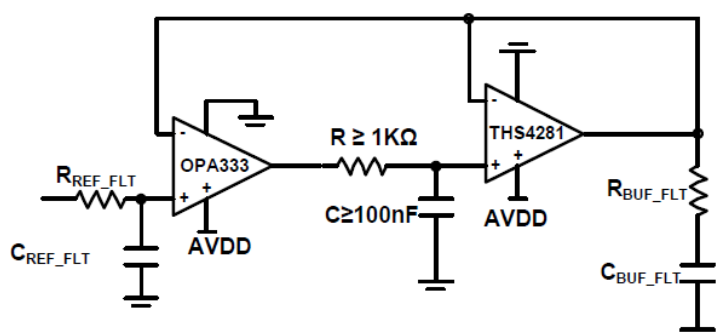


Figure 25: Reference buffer dc model

4 Simulation

With component selection complete, the stability, noise performance and transient behavior of the input and reference drive circuits can now be simulated using the TINA-TI™ Spice Simulator. Figure 26 depicts the schematic of this design.

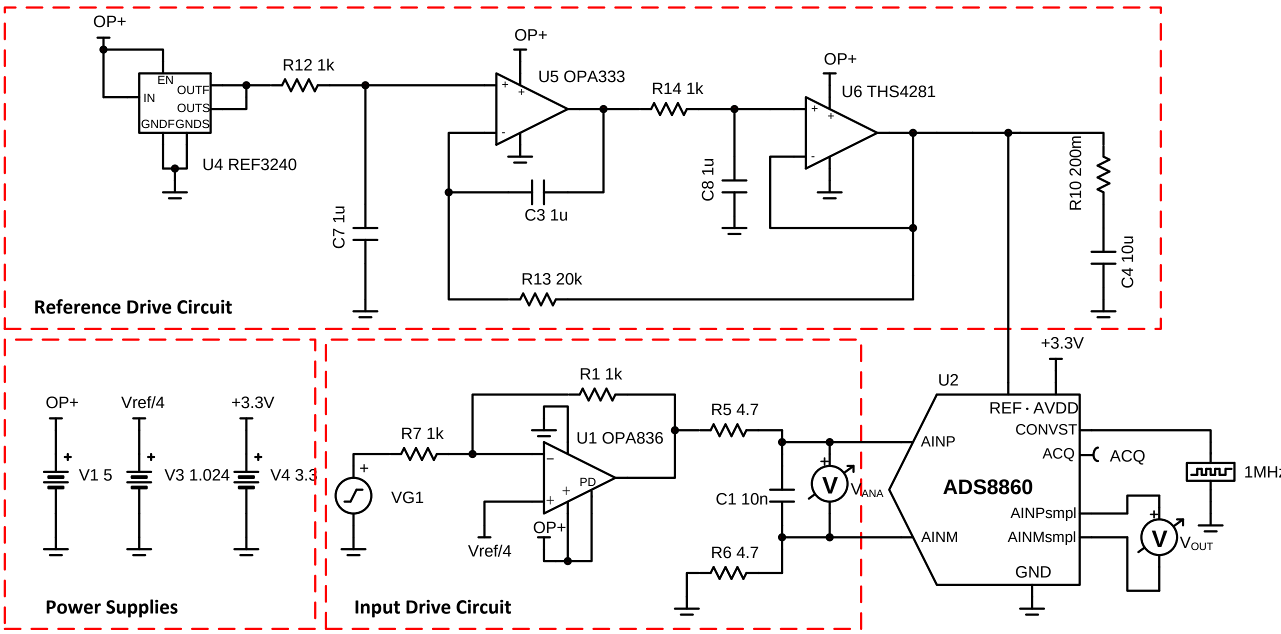


Figure 26: Top level TINA-TI™ schematic of DAQ block

4.1 *Input driver stability*

To ascertain input driver stability, it is necessary to determine the phase margin of the loaded circuit from the Bode plot of its Loop Gain function (Vy(f)/Vx(f)). To this end, the feedback loop must first be "broken" for ac small-signal analysis as shown in Figure 27. Only the dominant 10nF load is shown.

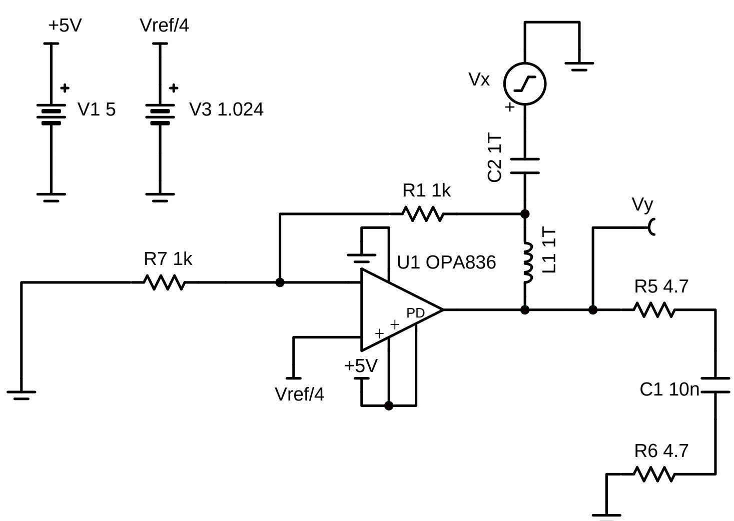


Figure 27: Schematic for simulating input driver stability

The op amp must operate in open-loop configuration for ac (stability) analysis and in closed-loop configuration for the dc operating point to be computed. The large inductor is precisely for this purpose. For frequencies just above dc, the large (1TH) inductor behaves as an open-circuit connection and the op amp is in open loop configuration. The ac signal is injected through the large (1TF) capacitor which acts as a short just above dc. On the other hand, for dc analysis, the inductor is shorted and the capacitor is open so that the circuit is in a closed-loop configuration.

With the dc operating point computed and the ac analysis completed, the phase margin can be calculated by examining the magnitude and phase plots of the loop gain.

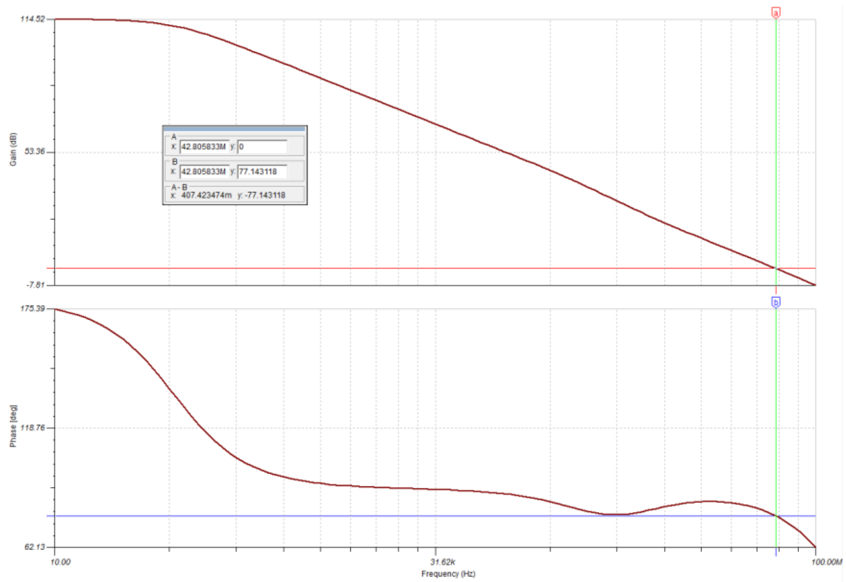


Figure 28: Bode plot of input driver Loop Gain function

At the frequency where loop gain goes to 0dB, the phase margin is about 77˚, which confirms that the input driver is stable and therefore that the output of the closed-loop circuit will not oscillate.

4.2 Input driver noise

The RMS output noise of the input drive circuit can be determined by running a noise simulation on the schematic shown in Figure 29.

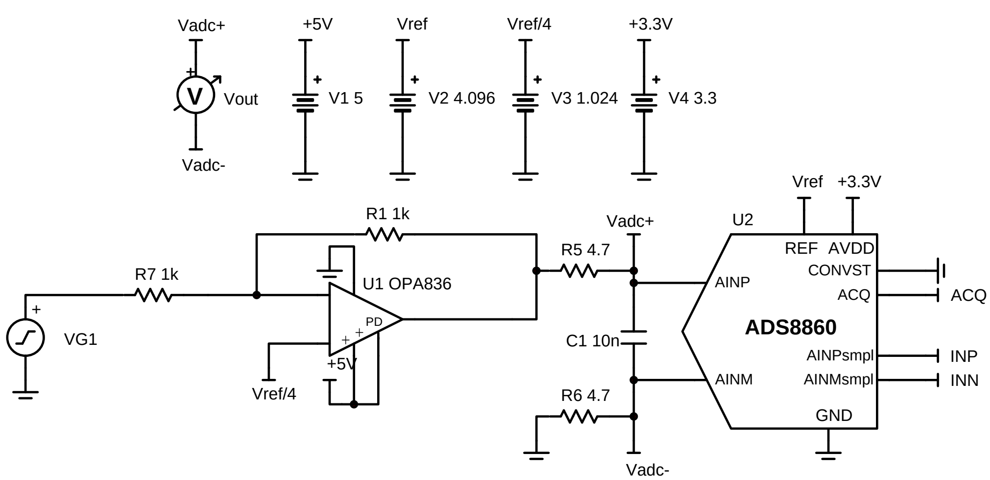


Figure 29: Schematic for input driver noise simulation

To compute the RMS noise contribution of the op amp, the noise spectral density of the op amp must be integrated over approximately 10x the bandwidth of the input driver which is about 1.7MHz.

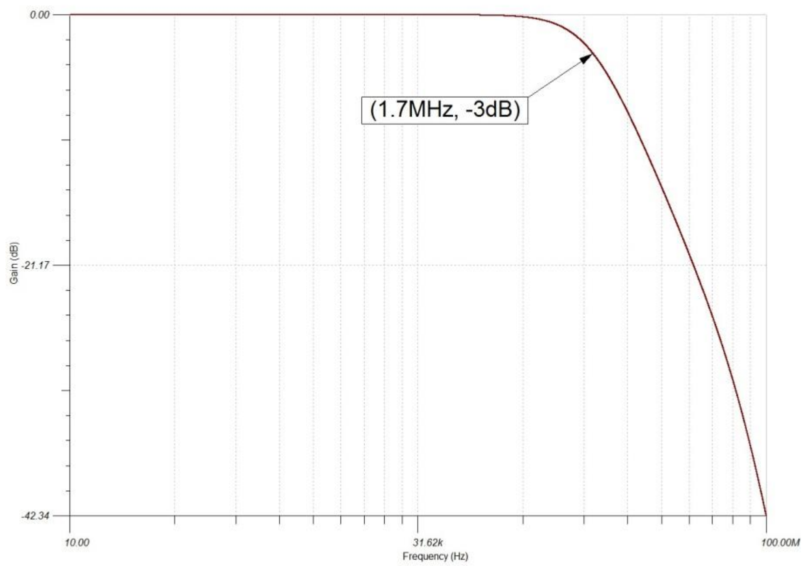


Figure 30: Input driver bandwidth

The integrated RMS output noise of the input drive circuit over a 20MHz bandwidth is shown in Figure 31.

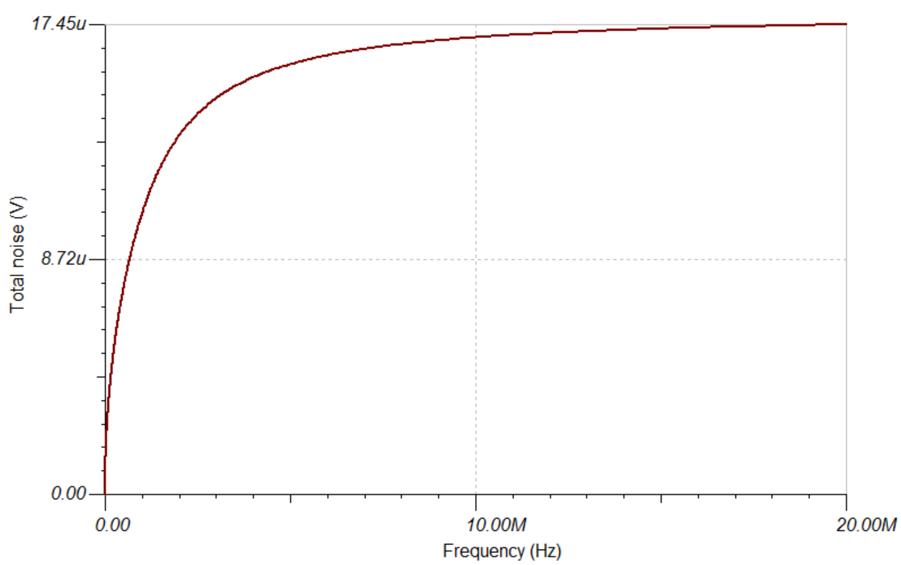


Figure 31: RMS output noise of ADC input drive circuit

In relation to the total ADC noise of about 43uVrms, the input driver produces about 1/2.5x the noise which more or less satisfies the noise requirement specified in equation (6).

4.3 Input driver dynamic behavior

The TINA-TI™ schematic shown in Figure 26 is used to check the accurate settling of the sine-wave signal at the inputs of the ADC during sampling phase. The simulated time-domain response for the circuit is shown in Figure 32. The transient plot on the top shows one cycle of a 10 kHz sine-wave with amplitude 1.98V is applied at the input of the ADS8860. The signal "Vana" represents the actual input signal at the input terminals of the ADC and the signal "Vout" shows the output of the ADC's input sample-and-hold circuit. The lower plot shows the same waveform zoomed in on time scale for more details. The curves are collated together to show that the sampled signal accurately tracks the input signals during sampling and stays on hold when the ADC is converting.

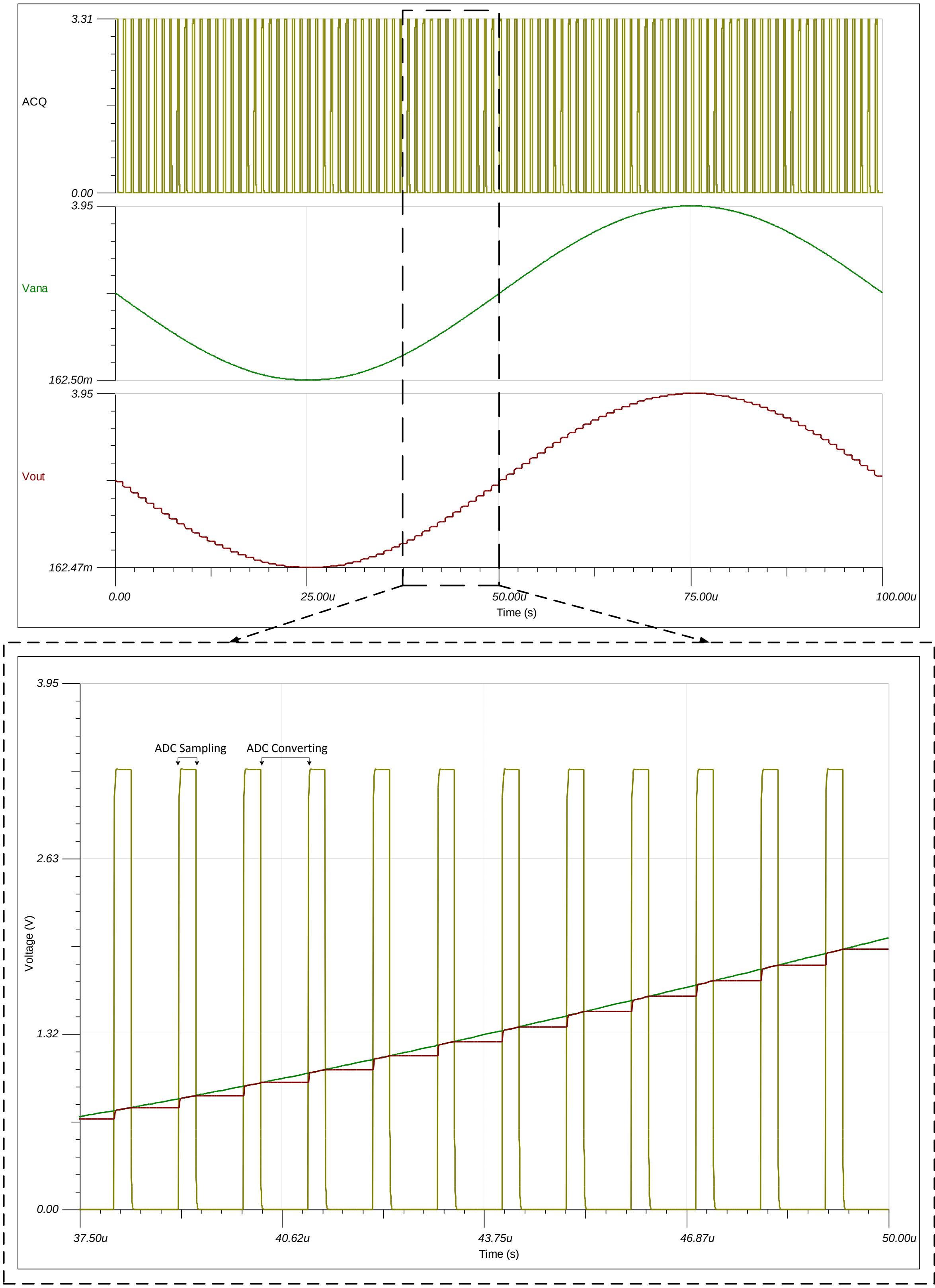


Figure 32: Simulated digitization of Input sine signal showing ADC sample and hold

4.4 Reference driver stability and isolation resistor selection

The stability of the reference driver is highly dependent on the value of the resistor that isolates the output of the reference buffer from the large charge bucket capacitor. The value of the resistor is determined in an iterative fashion so that the closed loop gain peaking is less than 1dB. The schematic is shown in Figure 33.

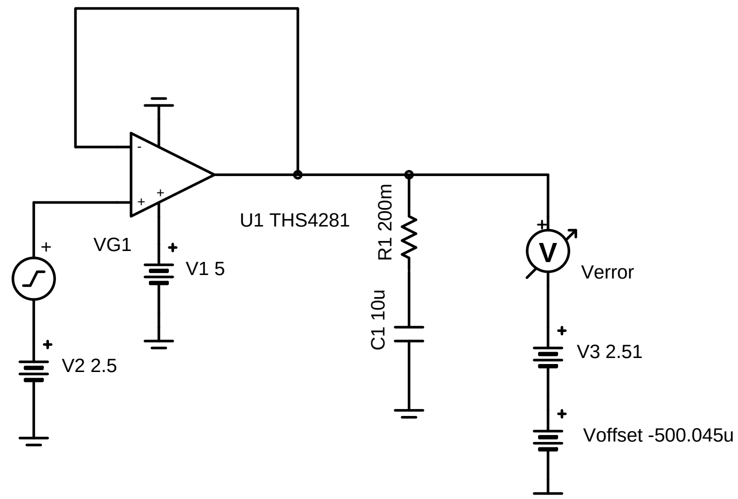


Figure 33: Schematic for reference buffer stability

The closed loop gain of the buffer is shown in Figure 34 for various values of the isolation resistor.

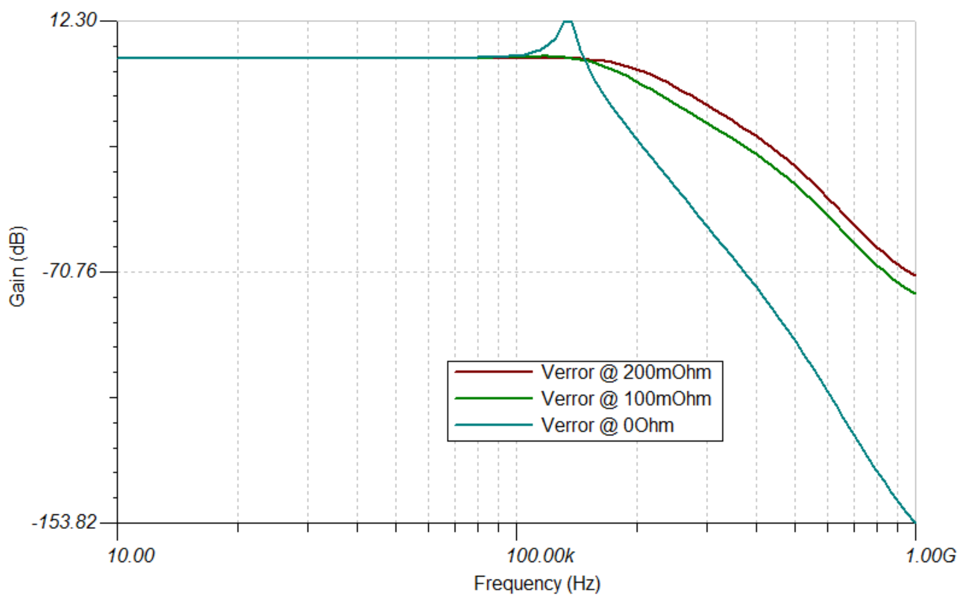


Figure 34: Closed loop gain for multiple ESR values

Figure 35 shows the association between gain peaking and phase margin. An optimal value of phase margin that would produce a fast underdamped response is between 50˚ and 60˚. From Figure 34, this corresponds to less than +1dB of gain peaking. Among the values that were tried, the 200mΩ ESR produced the lowest gain peaking, and was thus the value chosen.

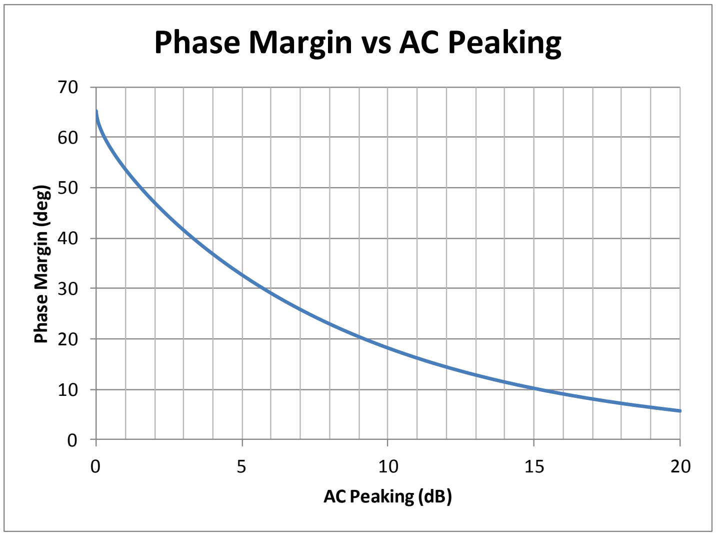


Figure 35: Closed loop gain peaking vs. phase margin

4.5 Reference driver dynamic behavior

Now the dynamic behavior of the ADC reference driver can be simulated over multiple conversion cycles to verify that the reference voltage error is less than 1LSB during the ADC conversion phase.

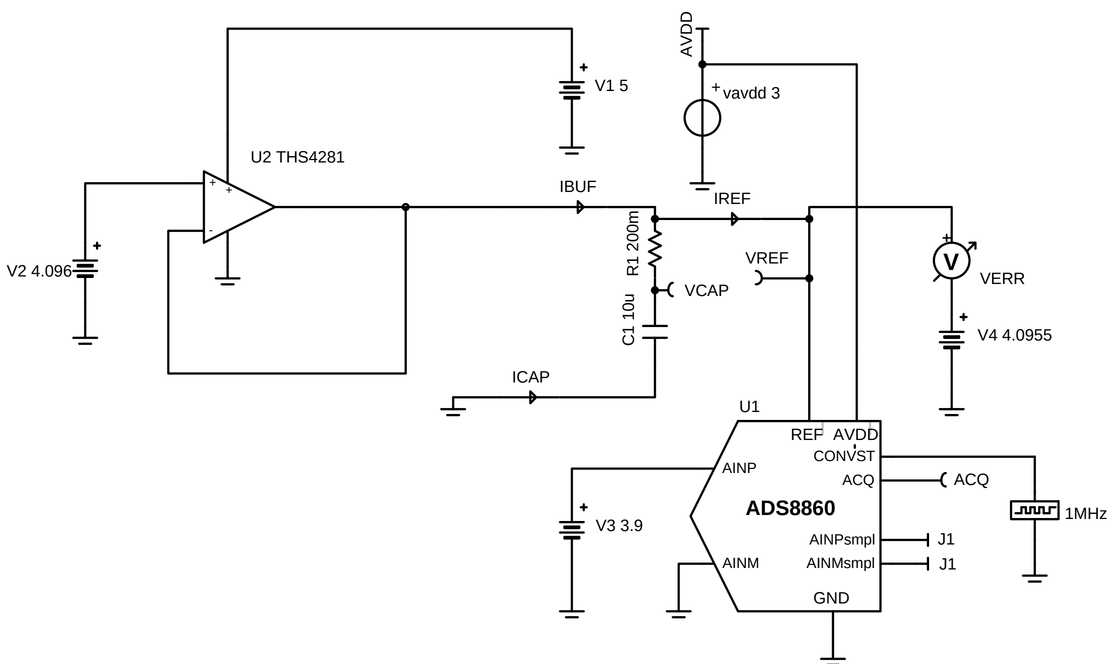


Figure 36: Schematic to simulate dynamic behavior of ADC reference driver

Figure 37 shows the results of the transient simulation of the schematic in Figure 36.

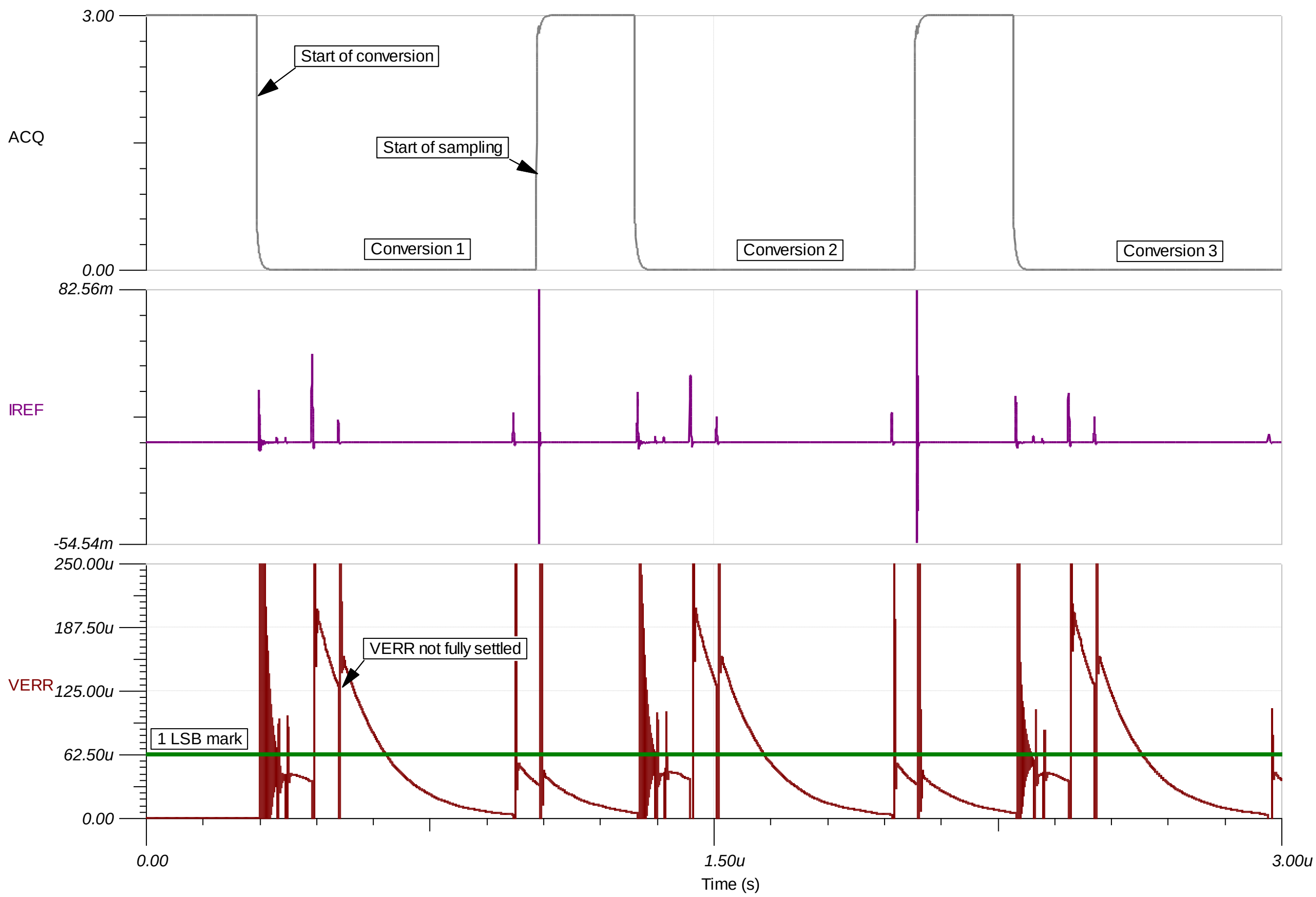


Figure 37: Reference driver transients over three ADC conversion cycles

The ACQ signal indicates when the ADC is converting and when it is acquiring – ACQ high implies acquisition or sampling. IREF shows the load current into the ADC reference pin. Note that IREF is zero during sampling. The VERR signal shows that the reference error settles to within 1LSB between current pulses in all but one case where it settles to within 3 LSB. This deviation from the ideal behavior is quite possibly due to the conservative nature of the ADC reference load model. Nevertheless the settling behavior of the reference error signal does indicate that the reference driver has good load regulation.

4.6 Reference driver noise

Lastly, the noise contribution of the reference driver can be estimated using the schematic shown in Figure 38. The voltage reference and the OPA333 buffer are not included because their outputs are heavily low-filtered and as such their noise contributions are not significant.

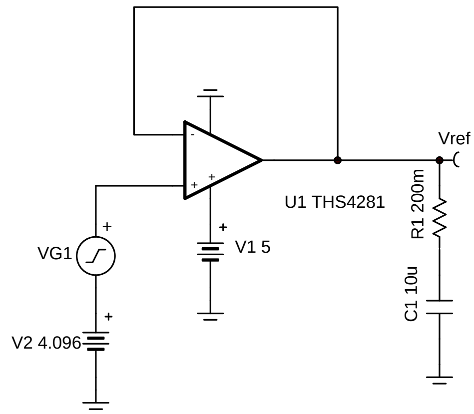


Figure 38: Schematic for estimating reference driver noise

Recall from section 2 that the RMS output noise is calculated by integrating the noise spectral density of the op amp over approximately 10x the bandwidth of the circuit. Since the buffer output has a capacitive load, the bandwidth is substantially lower than the GBW of the THS4281. The closed loop gain magnitude curve of the loaded op amp buffer is shown in Figure 39:

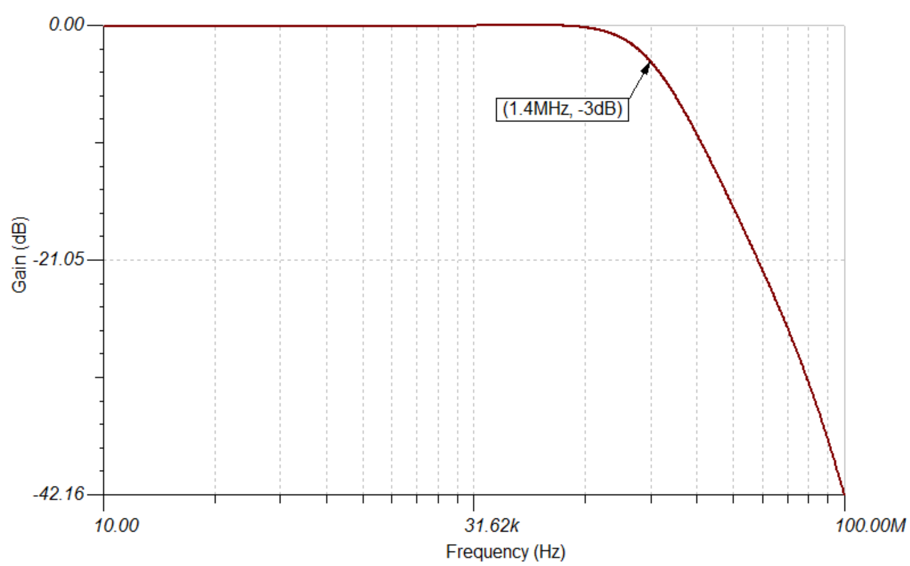


Figure 39: Gain magnitude of loaded op amp buffer

Integrating the noise spectral density over a 14MHz bandwidth, the RMS output noise of the reference driver is about 22µVrms which is about half the RMS noise contribution of the ADC (43 µVrms) and nearly meets the design requirement of <21µVrms.

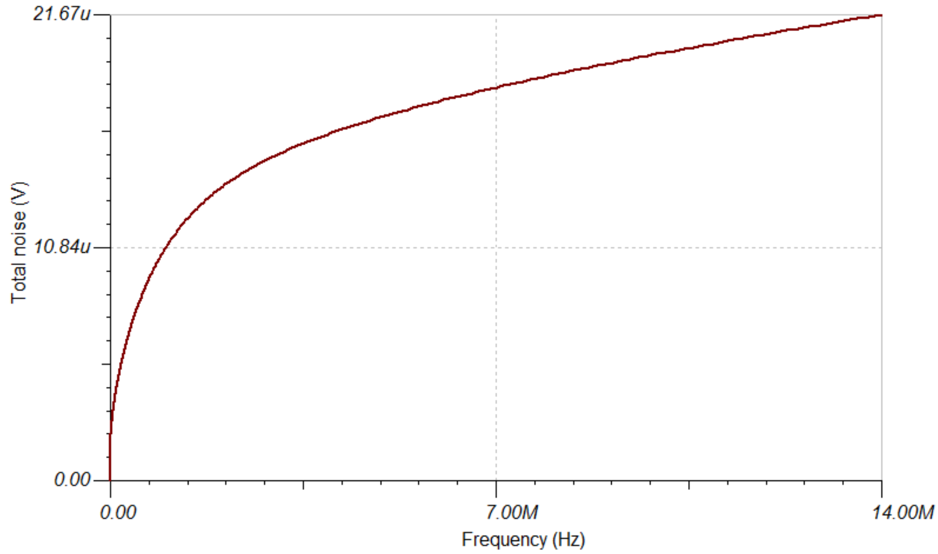


Figure 40: Reference buffer RMS output noise

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The most important PCB layout considerations for this design are discussed below:

- The analog and digital routing must be kept physically separated on the board in order to minimize cross-talk
- The trace between the reference driver output the ADC reference input must be kept as short as possible to minimize trace inductance that can potentially cause instability or settling issues with the reference voltage
- The input driver block must be located as close to the ADC input as possible to minimize loop area and improve EMI/RFI rejection. Similarly, the components of the input driver must be placed close to one another to minimize loop area.

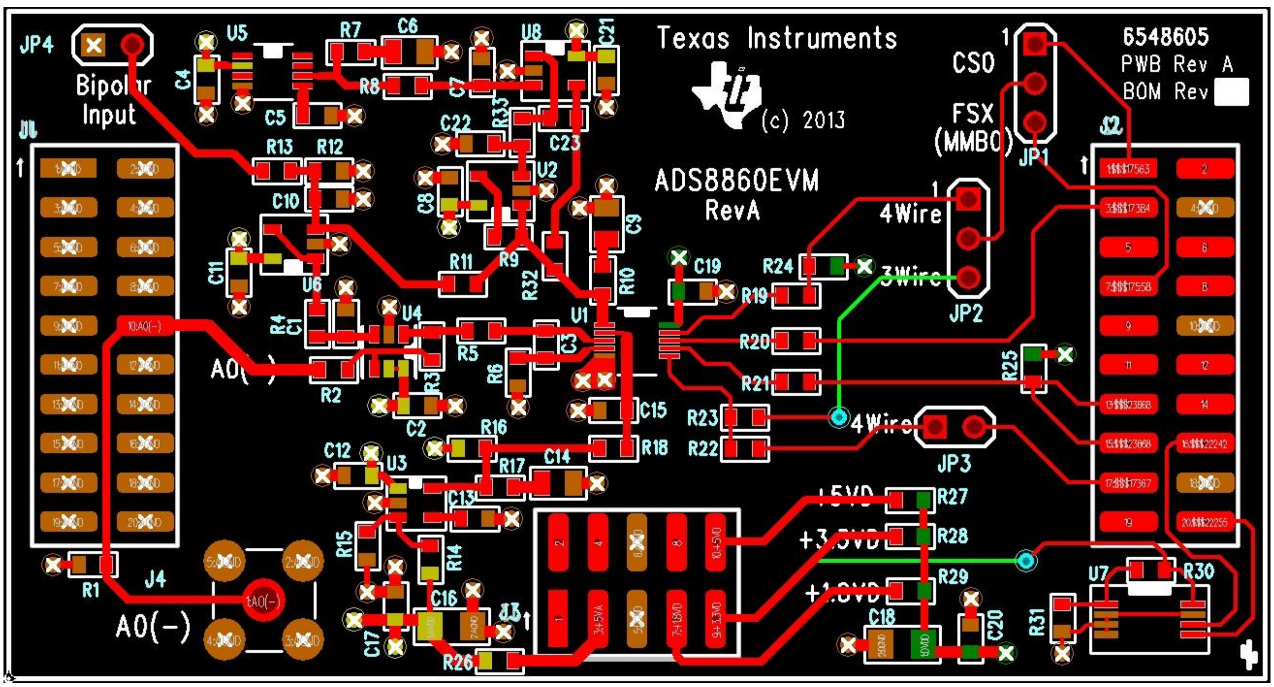


Figure 41: PCB Layout

6 Verification & Measured Performance

6.1 DC Noise Measurement

The dc noise measurement provides a gross estimate of the system's overall performance. The goal is to obtain a histogram of ADC output codes for multiple conversions performed on a constant dc input signal, and use histogram data to estimate the Effective Resolution of the DAQ system. Effective Resolution, like ENOB, is a measure of the dynamic range lost due to noise and linearity errors in the system, relative to the ideal case. However, unlike ENOB, Effective Resolution only considers static or dc errors that are inherent to the system components, i.e. ADC DNL errors, ADC thermal or transition noise and thermal noise from the input and reference drive circuits.

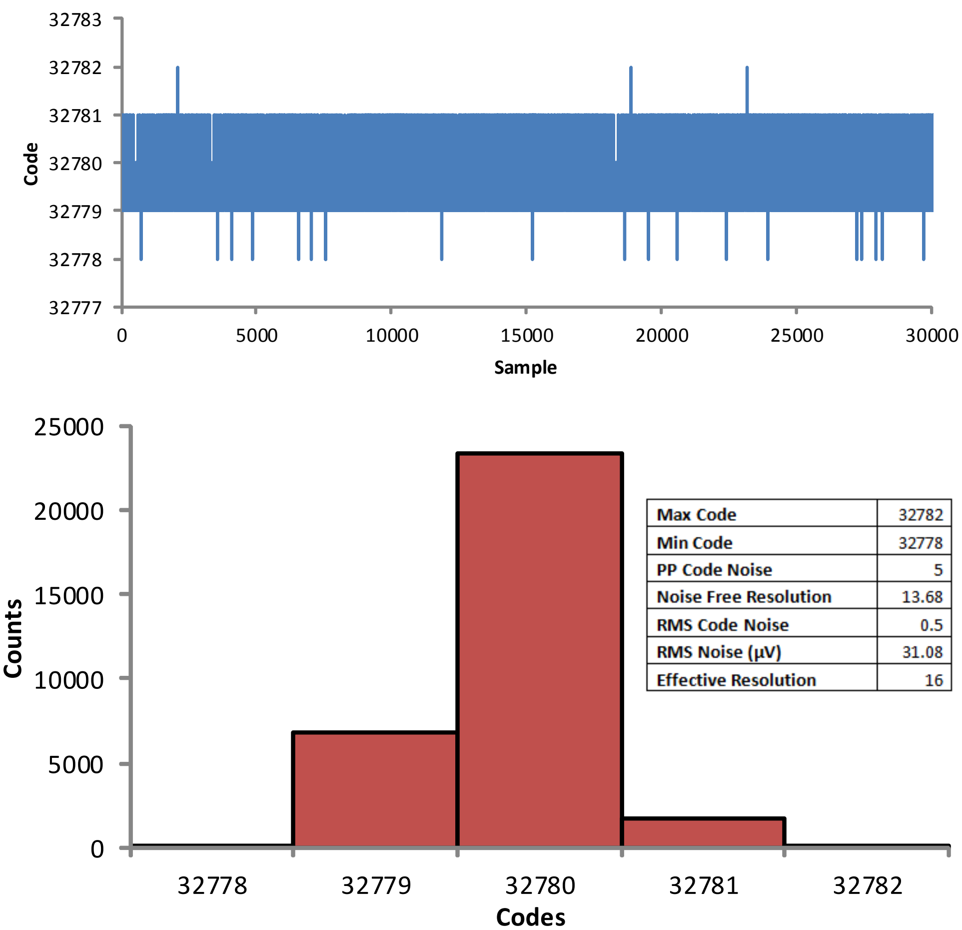
The histogram in Figure 42 was generated from 32000 conversions performed on a 2.048V (mid-scale) dc input signal. The parameters of interest are also defined:

$$Effective\ Resolution = 16 - \log_2(RMS\ Code\ Noise)$$

$$RMS\ Code\ Noise = stdev\big(code(1){:}\, code(32000)\big)$$

$$RMS\ Noise = RMS\ Code\ Noise \times LSB\ size = RMS\ Code\ Noise \times \frac{4.096}{2^{16}} \times 10^6\ \mu V$$

$$Noise\ Free\ Resolution = 16 - \log_2(PP\ Code\ Noise)$$



Max Code	32782
Min Code	32778
PP Code Noise	5
Noise Free Resolution	13.68
RMS Code Noise	0.5
RMS Noise (µV)	31.08
Effective Resolution	16

Figure 42: Code histogram of 32K conversions on mid-scale dc input

Two important observations can be made:

1) The dc code distribution has a Gaussian characteristic, which indicates that there are no gross issues with the board. A non-Gaussian characteristic (such as a bi-modal distribution) is typically the result of issues such as large DNL errors in the ADC, insufficient power supply decoupling, improper ground connections or poor layout.

2) The Effective Resolution of the system is the same as the ideal resolution which means that the RMS noise of the system under dc conditions is very low (< 1LSB).

Note that Effective Resolution neglects dynamic errors, namely quantization noise and distortion. As a result it is a good estimate of system performance only for dc inputs. On the other hand, ENOB takes dynamic errors into consideration and as such, it is a much better indicator of system performance for time-varying inputs.

6.2 ADC Dynamic Performance Measurement

Figure 43 depicts the FFT of the samples of a full-scale sinusoidal input signal digitized by the ADC:

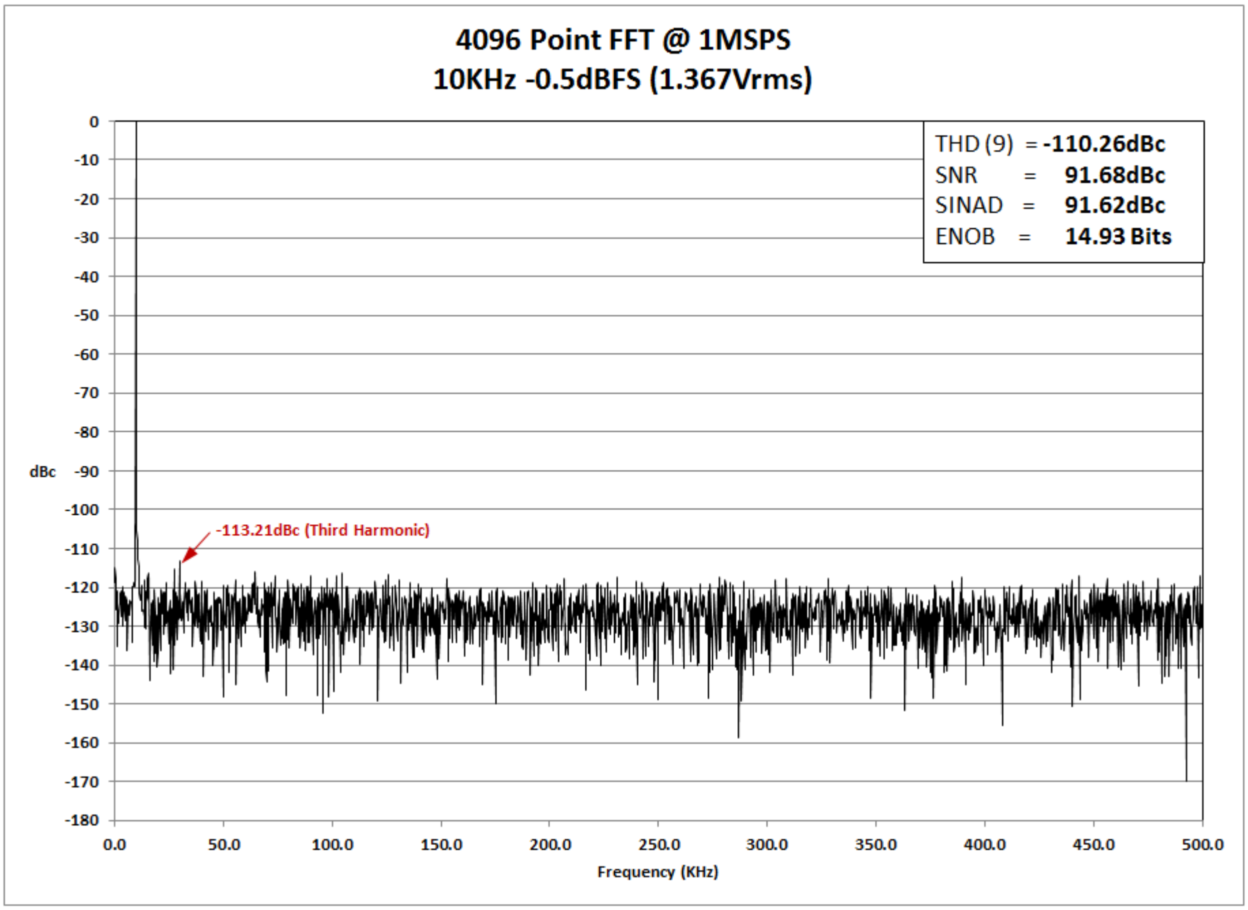


Figure 43: FFT and dc performance of the Data Acquisition System

The plot confirms that this design delivers THD < -108dB and SNR > 91dB and fulfills the stipulated performance goals.

6.3 ADC Linearity Measurement

Since linearity is correlated with distortion and the circuit meets the THD requirement, it would be reasonable to expect the system to have excellent INL (Integral Non-Linearity) which is the dc error remaining at each code after removing the offset and gain errors. Figure 44 shows an estimated INL curve generated from a sample set of INL measurements of 41 strategic codes in the ADC output range that are known to have extreme INL values.

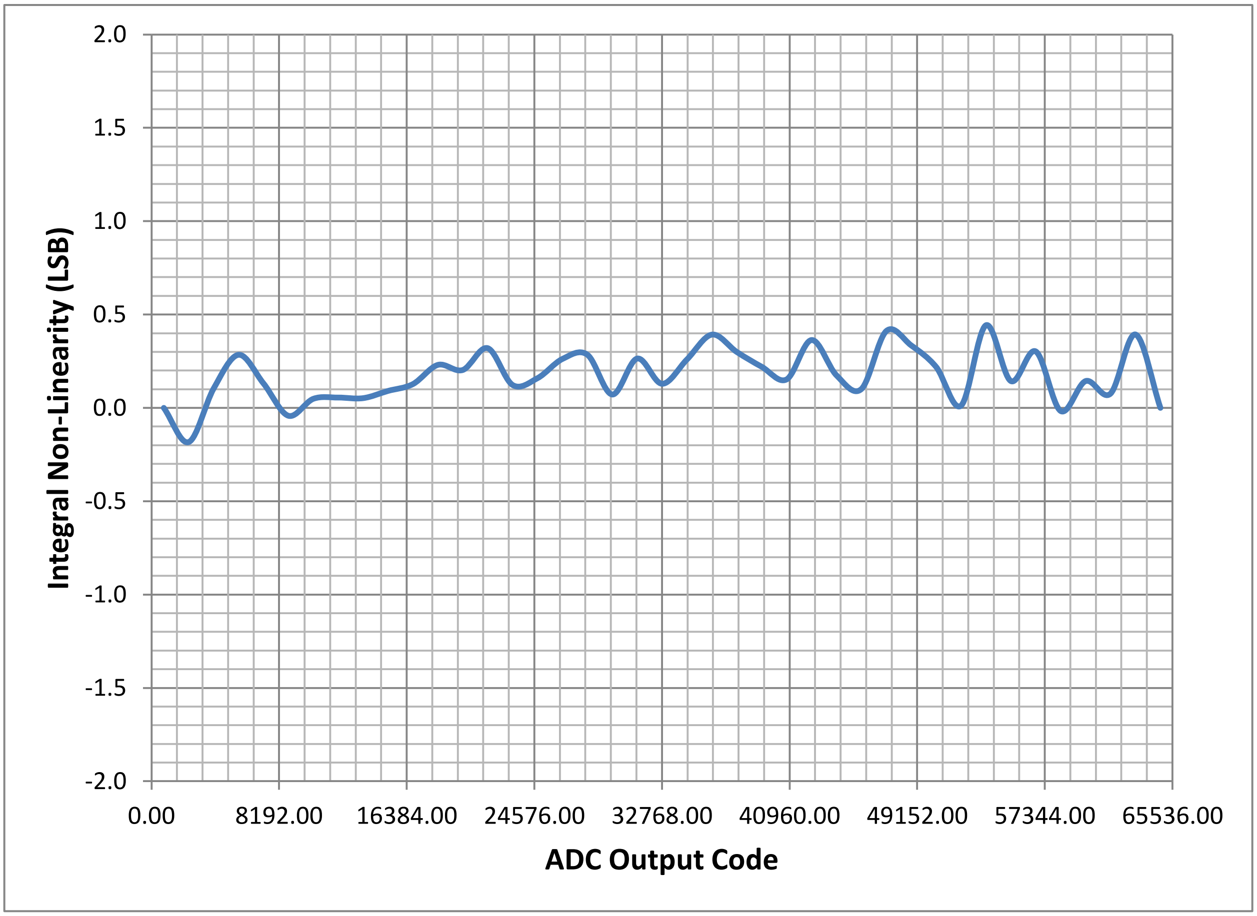


Figure 44: 41 point INL curve

According to the INL plot of Figure 44, the data acquisition system is accurate to within ±0.5LSB which exceeds the design goal of ±1.5LSB.

7 Modifications

The THS4281 is a great choice for the reference driver in terms of its high bandwidth (>40MHz) and low power consumption (750uA typical). However, it is possible to extract additional power savings using the OPA835 (55MHz GBW and 250uA typical IQ). The only issue is that the input range of the OPA835 on a +5V supply is limited to 3.9V, which is lower than the application requirement of 4.096V. This means that the op amp must be used in a gain of >+1 which requires gain setting resistors. The resistors not only consume board space but also generate a current in the feedback loop which leads to an increase in power consumption. The additional power consumption can be mitigated using resistors of larger value. Using 10kΩ resistors in a gain of +2 configuration produces 4.096/(2*10kΩ) = 204.8µA, bringing the total supply current consumed by the OPA835 reference buffer to about 550µA, which is lower than the current consumption of the THS4281 buffer.

8 About the Author

Harsha Munikoti is an Applications Engineer in the Precision Analog SAR ADC team at Texas Instruments. Prior to joining the Applications team, Harsha was a Product and Test Engineer developing final test solutions for many of TI’s precision data converter products. Harsha has a MSEE degree from the University of Florida, Gainesville.

Rafael Ordonez is an applications engineer in Precision Analog, SAR ADC team at Texas Instruments based in Tucson, Arizona. Rafael earned his Master and Bachelor degrees of Science from the University of Texas at El Paso co-inventing a patent in solar cell fabrication technology.

9 Acknowledgements & References

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6. *A. Kumbasi, R. Ordonez, H. Munikoti. (2013, June). 18-bit 10KSPS Data Acquisition Block for Ultra Low Power. (TIPD114)*

7. *Analog Switch Guide (SLYB125D)*

Appendix A.

A.1 Electrical Schematic

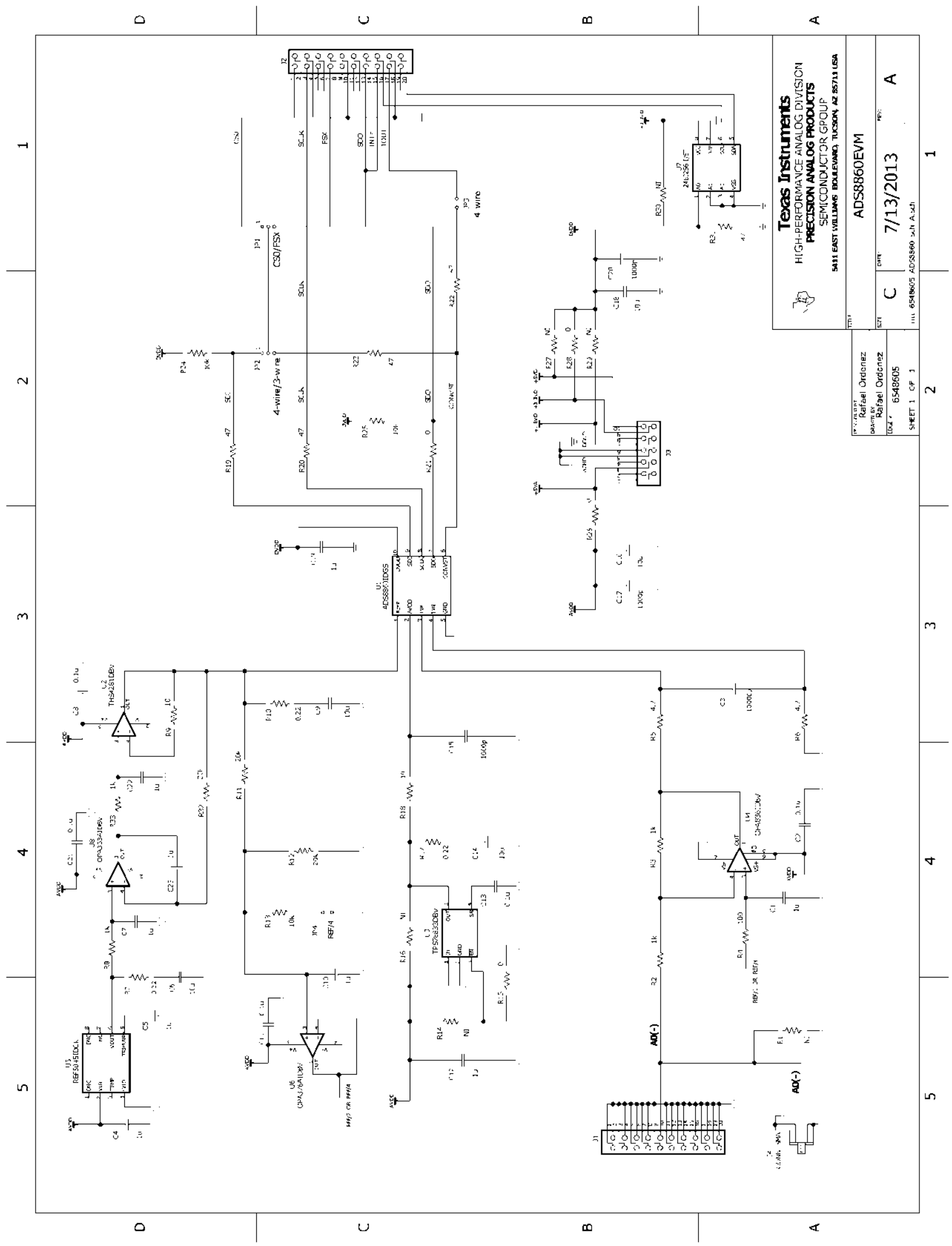

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Item	QTY	Value	Ref Des	Description	Manufacturer	Part Number
1	1		N/A	Printed Circuit Board	Texas Instruments	6548605
2	9	1u	C1, C4, C5, C7, C10, C12, C19, C22, C23	Capacitor, X7R Ceramic +/- 10%, 25WV, 0603	Murata	GRM188R71E105KA12D
3	5	0.1u	C2, C8, C11, C13, C21	Capacitor, X7R Ceramic +/- 10%, 25WV, 0603	Murata	GRM188R71E104KA01D
4	1	10000p	C3	Capacitor, C0G Ceramic +/- 5%, 25WV, 0603	TDK	C1608C0G1H103J
5	3	10u	C6, C9, C14	Capacitor, X7R Ceramic +/- 10%, 10WV, 0805	Murata	GRM21BR71A106KE51L
6	3	1000p	C15, C17, C20	Capacitor, C0G Ceramic +/- 5%, 50WV, 0603	Murata	GRM1885C1H102JA01D
7	2	10u	C16, C18	Capacitor, X7R Ceramic +/- 10%, 16WV, 1206	TDK	C3216X7R1C106K
8	2		J1, J2 (Top)	Header 20 Pin SMT Plug, .100" Gold (2x10)	Samtec	TSM-110-01-L-DV-P
9	2		J1, J2 (Bottom)	Header 20 Pin SMT Socket, .100" Gold (2x10)	Samtec	SSW-110-22-F-D-VS-K
10	1		J3 (Top)	Header 10 Pin SMT Plug, .100" Gold (2x5)	Samtec	TSM-105-01-L-DV-P
11	1		J3 (Bottom)	Header 10 Pin SMT Socket, .100" Gold (2x5)	Samtec	SSW-105-22-F-D-VS-K
12	1		J4	CONN SMA JACK STRAIGHT PCB	Amphenol Emerson	132134 142-0701-201
13	2		JP1, JP2	Header Strip, 3 pin .100" Gold (1x3)	Samtec	TSW-103-07-L-S
14	2		JP3, JP4	Header Strip, 2 pin .100" Gold (1x2)	Samtec	TSW-102-07-L-S
15	6		R1, R14, R16, R27, R29, R30	Not Installed		
16	2	1k	R2, R3	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB102V
17	1	100	R4	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1000V
18	2	4.7	R5, R6	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW06034R70FKEA
19	3	0.22	R7, R10, R17	Resistor, Thin Film Chip, 1%, 1/5W, 0603	Susumu	RL0816S-R22-F
20	2	1k	R8, R33	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1001V
21	2	10	R9, R18	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Vishay/Dale	CRCW060310R0FKEA
22	3	20k	R11, R12, R32	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB203V
23	1	10k	R13	Resistor, Metal Film Chip, 0.1%, 1/10W, 0603	Panasonic	ERA-3AEB103V
24	4	0	R15, R21, R26, R28	Resistor, Thick Film Chip, 1/10W, 0603	Panasonic	ERJ-3GEY0R00V
25	5	47	R19, R20, R22, R23, R31	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF47R0V
26	2	10k	R24, R25	Resistor, Thick Film Chip, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1002V
27	1		U1	IC ADC 16bit 1MSPS Pseudo-Diff 10-MSOP	TI	ADS8860IDGS
28	1		U2	IC OP AMP VFB R-R 95MHZ SOT23-5	TI	THS4281DBV
29	1		U3	IC LDO RGLTR 3.3V LN SOT-23-5	TI	TPS78833DBV
30	1		U4	IC OP AMP VFB RRO 205MHZ SOT23-6	TI	OPA836IDBV
31	1		U5	IC VREF SERIES PREC 4.5V 8-MSOP	TI	REF5045IDGK
32	1		U6	IC OP AMP GP 5.5MHZ SGL SOT23-5	TI	OPA376AIDBV
33	1		U7	IC EEPROM 256KBIT 400KHZ 8TSSOP	Microchip	24LC256-I/ST
34	1		U8	IC OP AMP CHOP R-R 350KHZ SOT23-5	TI	OPA333AIDBV
35	3		N/A	0.100 Shunt - Black Shunts	3M	969102-0000-DA

Figure A-2: Bill of Materials

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