TEXAS INSTRUMENTS INC.
HIGH PERFORMANCE ANALOG

HIGH SPEED AMPLIFIERS

Design Guide

Considerations for High-Gain Multistage Designs

Pavol Balaz

Contents

List of Figures

List of Tables

1 Introduction

Amplifying a voltage signal by more than 100 $\frac{V}{V}$ using a single operational amplifier while maintaining several MHz, or even tens of MHz of bandwidth, can prove difficult to both design and to implement. The goal of this paper is to describe the development and the physical implementation of a high-gain, multi-stage design featuring a voltage gain well above 100 $\frac{V}{V}$. The first part of the paper discusses the general factors to be considered during the design phase while the second part focuses on physical implementation.

2 Signal-Chain Considerations

2.1 First Stage - Input Noise

Since the noise of the first stage is the limiting factor from a noise perspective, input noise is one of the most important factors to be considered when selecting the amplifier for the first stage. Another key factor is the available bandwidth. Starting with the traditional gain-bandwidth product (GBWP) where the product of the gain and the bandwidth is constant for a voltage-feedback amplifier (see 2.1), a quick survey of non-unity gain stable amplifiers combining the highest possible GBWP and low noise yields the results as shown in table 2.1.

$$Gain \times Bandwidth = GBWP \tag{2.1}$$

Table 2.1: Devices combining high GBWP and low input noise

Part Number	**Input Voltage Noise Density [nV/$\sqrt{Hz}$]**	**GBWP [MHz]**
OPA847	0.85	3900
OPA846	1.1	1800
LMH6629	0.69	3900

Note that FET input devices have not been considered here because the input voltage noise tends to be high, while input current noise is low. Because low value resistors are used to

minimize noise contribution, the low input bias current of a FET amplifier is not needed here. Only relatively low input impedance voltage sources are considered.

2.2 Noise Considerations

Consider using a non-inverting amplifier architecture, allowing its input impedance to be matched to any source impedance as well as minimizing system noise. Also, at high gain, the output voltage noise density can be approximated as shown in equation 2.2.

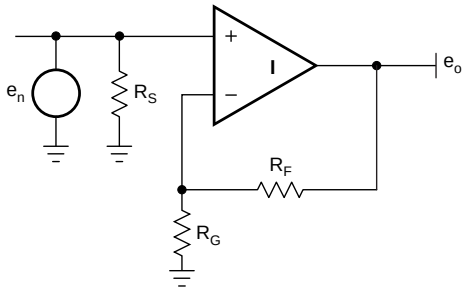
$$e_o \cong (e_n + \sqrt{4kTR_S}) \times \left(1 + \frac{R_F}{R_G}\right) \tag{2.2}$$

where

- k = 1.3806488 $\times 10^{-23}$ $m^2kgs^{-2}K^{-1}$
- T = temperature in Kelvins

Note that in this model, both the current noise and the resistor noise are considered to be negligible.

Figure 2.1: Simplified Noise Model



The SNR for a such a configuration is shown in equation 2.3.

$$SNR_{(dB)} = 20 \times \log\left(\frac{V_{orms}}{e_o \times \sqrt{NPWB}}\right) \tag{2.3}$$

where NPBW = the noise power bandwidth of the stage. Each stage amplifies the noise from the previous stage and adds its own noise. For two stages, the result is shown in equation 2.4.

$$e_o^2 = e_{o1}^2 + \left(e_{o1}^2 \times G_2^2\right) + e_{o2}^2 \tag{2.4}$$

$$e_o^2 = e_{o1}^2 \times (1 + G_2^2) + e_{o2}^2 \tag{2.5}$$

where e_o, e_{o1} and e_{o2} are the output voltage noise densities in $\frac{nV}{\sqrt{Hz}}$ of the total system, the first stage and the second stage, respectively.

Also, in order to maximize SNR, additional RC filters can be added between the stages.

The total gain equals the sum (in dB) or product (in $\frac{V}{V}$) of the gain of each stage as shown in

$$G_{tot}\left[\frac{V}{V}\right] = G_1\left[\frac{V}{V}\right] \times G_2\left[\frac{V}{V}\right] \times ... \times G_n\left[\frac{V}{V}\right] \tag{2.6}$$

$$G_{tot}\left[dB\right] = G_1\left[dB\right] + G_2\left[dB\right] + ... + G_n\left[dB\right] \tag{2.7}$$

2.3 Following Stages

Since the noise of the first stage is the limiting factor from a noise perspective, any stage other than the first stage does not require very low noise. The entire current-feedback amplifier portfolio is now available for selection. Table 2.2 provides a selection of amplifiers suited for both high gain and high bandwidth applications.

Table 2.2: Current Feedback OP-Amps combining high gain with high BW

Part Number	**Gain at BW [V/V]**	**BW [MHz]**	**Comment**
OPA683	100	35	Lowest power solution
OPA684	100	70	Highest equivalent GBWP
OPA695	16	350	Highest BW solution

Note that either inverting or non-inverting gain circuits can be considered, depending on the amplifier and the desired bandwidth. The OPA695 achieves lower noise in an inverting configuration whereas the OPA683 and OPA684 achieve lower noise in the non-inverting configuration. Because we are set to achieve high gain on a single stage, the gain resistor can be as low as 10 Ω. In an inverting topology, this setting can place an additional constraint on the driving stage. In practice, keep the gain resistor between 10 Ω and 50 Ω and do not exceed 1.5 kΩ for the feedback resistor. Remember that the frequency response is limited by the feedback resistor (R_F) and the feedback capacitor (C_F) pole - there always will be a parasitic capacitor as a result of the component layout, and so forth.

The following sections of this design guide focus on output offset voltage and stability issues.

3 Output Offset Voltage and Stability Considerations

In the previous sections, this design guide discussed signal chain considerations to match required gain and bandwidth while maintaining sufficient SNR. Two issues remain to make this circuit easily implementable:

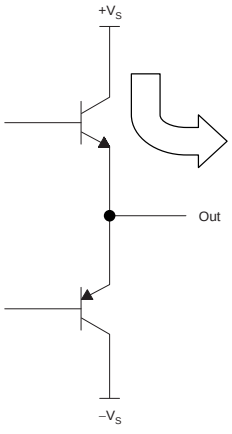
1. DC accuracy requirements
2. Amplifier power supply rejection ratio (PSRR)

3.1 Output Offset Voltage

Since very high gains are targeted, any DC error in the first or even the second stage can prove fatal to any implementation. The simplest way to circumvent the output offset voltage is to make sure that the DC gain of each stage is unity. Adding an AC coupling capacitor in series with the gain resistor solves this issue. Care must be taken when specifying the capacitor value. This will be discussed later in the simulation section.

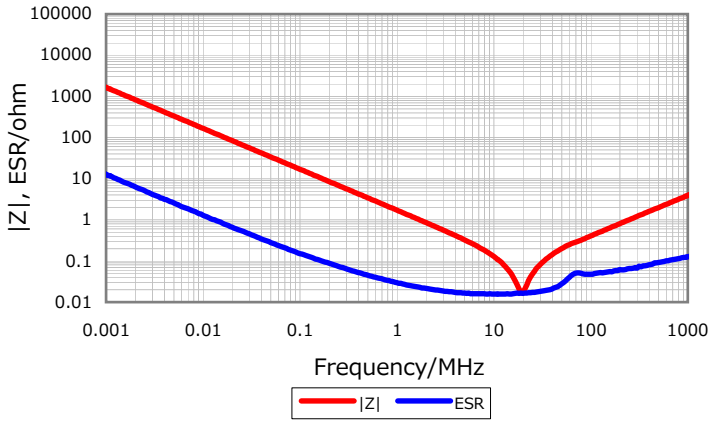
3.2 Power Supply Rejection Ratio (PSRR)

Figure 3.1: Operational Amplifier Emitter Output Stage



The output current flows through the output stage transistor and is originating from the power supply, as expected. If the supply is ideal and has constant low impedance over frequency,

Figure 3.2: Impedance vs. Frequency for a 100 nF multilayer ceramic chip capacitor [TDK13]



no disturbance will appear. However, the impedance of the supply will vary over frequency, either due to the limited bandwidth of a supply such as a LDO or due to the limitations of the bypass capacitor maintaining constant impedance over frequency. Figure 3.2 shows the impedance over frequency plot for a 100 nF multilayer ceramic chip capacitor.

It is possible to minimize such effect over frequency by putting capacitors of different technology and values in parallel. However, no matter how good the power supply regulator or the bypassing implementation, the impedance of the supply will have ripples upon which the load current will create a small signal riding on the power supply. This signal is referred to as disturbance in the following discussion.

However, this disturbance does not appear in the simulation unless the line regulation of a non-ideal power supply is implemented.

Such disturbance is seen by the first stage and if the PSRR of the first amplifier is insufficient at the frequency of interest, the disturbance finds its way into the signal path and will be amplified by the high gain of the following stages, eventually resulting in oscillations.

Preventing these oscillations requires careful planning in regards to the power supply. The power supply is connected directly to the last amplifier of the high gain signal chain. From this last amplifier to the previous one, an inductor is placed in series in the power supply path. This inductor combined with the local bypass capacitor forms a low pass filter that attenuates the disturbance. A positive feedback loop created in the supply can happen on both positive and negative supplies. Therefore, this needs to be implemented on both supplies.

Additionally, a single operational amplifier package must be used. Since dual, triple or quad amplifier packages share the power supplies internally, oscillations may occur since no filtering can be done externally.

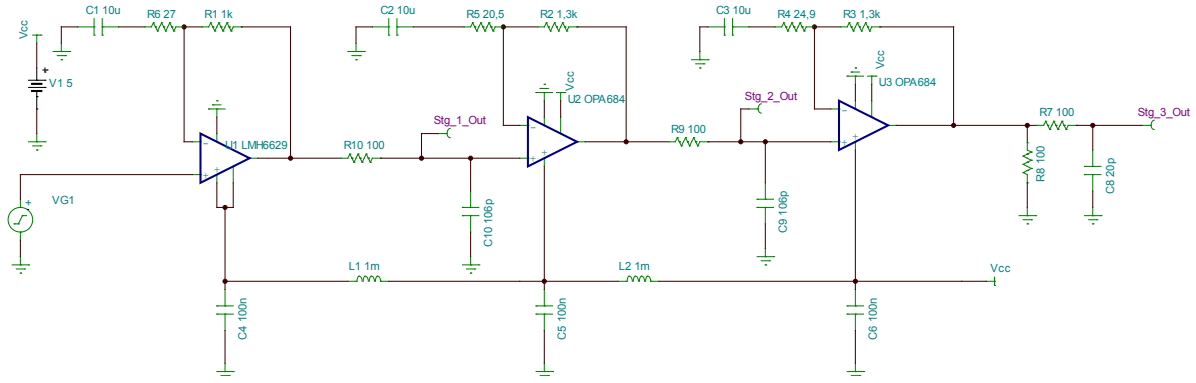
4 Simulations

The schematic shown in figure 4.1 reflects all the items discussed in the previous sections and shows a possible implementation for a +5V single supply, providing a voltage gain of approx. **120,000 V/V**. Please note that a single +5V supply was used in simulation, therefore no inductors are present on the negative supply side.

Following is a short summary of the items discussed in the previous sections:

- Very low input voltage noise density amplifier on the first stage (LMH6629)
- High gain, high bandwidth amplifiers on the following stages (OPA684)
- AC coupling capacitors in series with the gain resistors to ensure DC gain equals unity (C1,C2,C3)
- Inductors in the power supply line between the stages to implement LC filters using the bypass capacitor, creating low pass filters to attenuate the disturbances in the power supply line
- RC filters between the stages to increase SNR

Figure 4.1: Final Simulation Schematic



Figures 4.2 and 4.3 show simulated frequency responses with different gain AC coupling capacitor values. To ensure that the flat band is as wide as possible, select high capacitor values. On the stages featuring the current feedback OPA684 amplifier, the gain resistor shields the capacitor from the low impedance non-inverting input of the amplifier.

Figure 4.4 shows the simulated SNR.

Figure 4.2: Simulated Frequency Response, $C_{AC-GAIN} = 10nF$

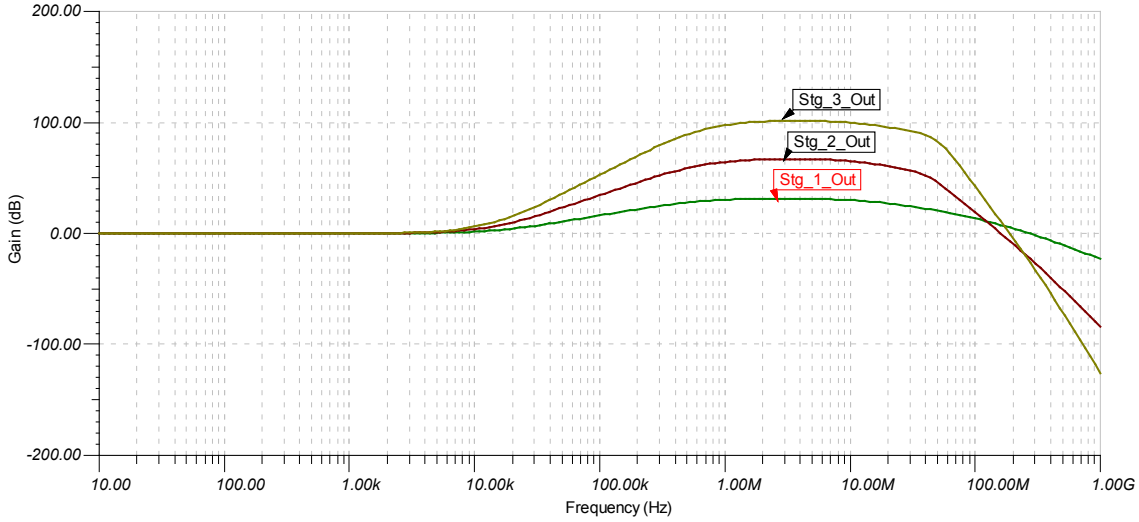


Figure 4.3: Simulated Frequency Response, $C_{AC-GAIN} = 10\mu F$

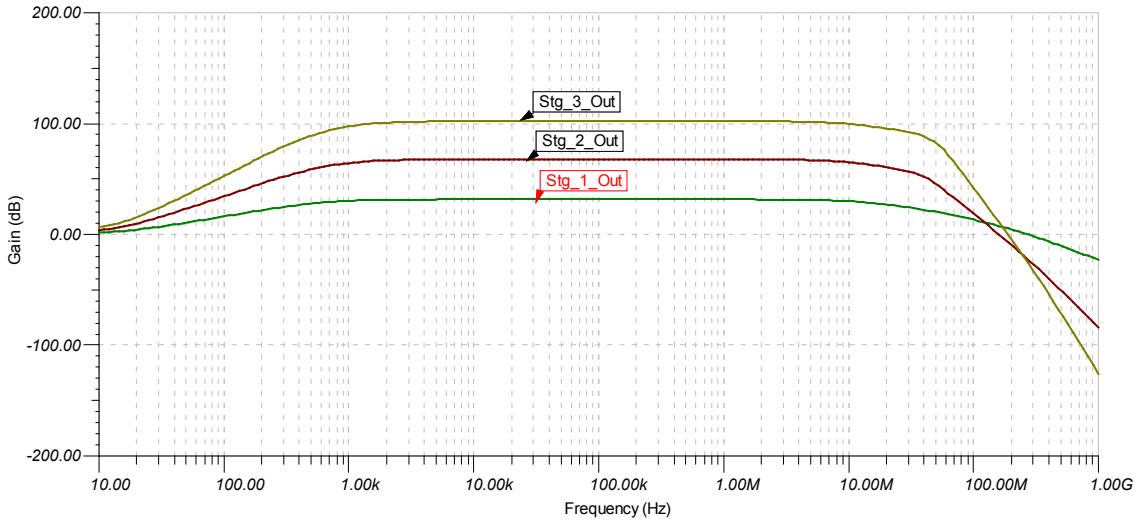


Figure 4.4: Simulated SNR, $C_{AC-GAIN} = 10\mu F$

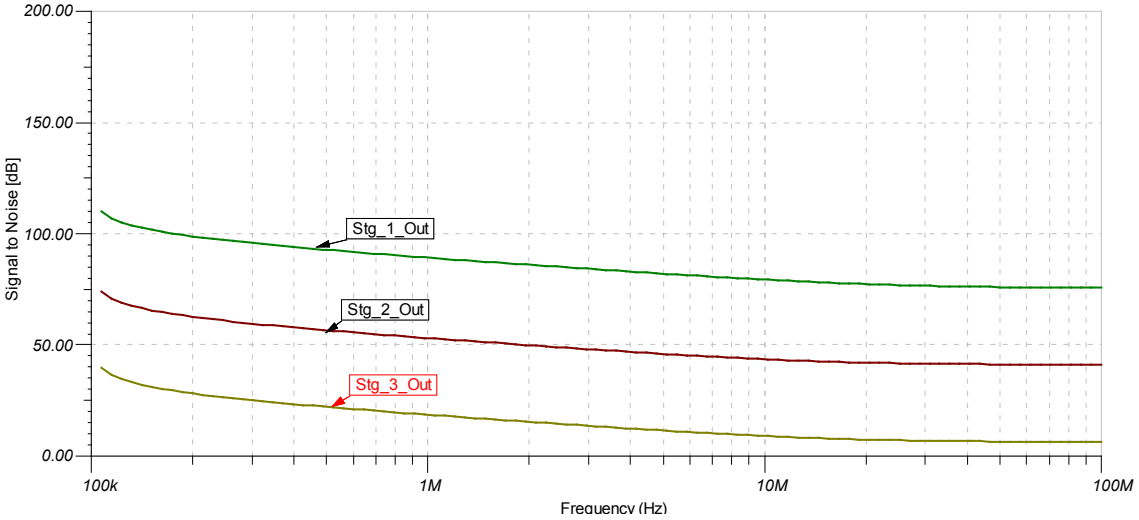
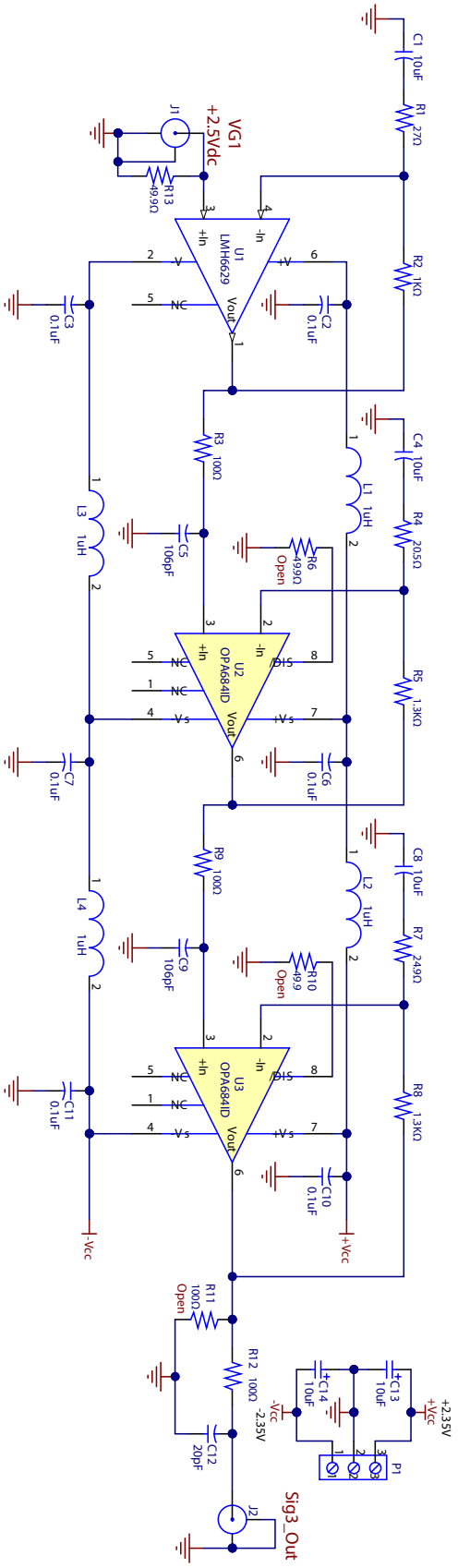


Figure 4.5: Schematic of the implemented High-Gain, High-Bandwidth Circuit



5 Circuit Implementation and Board Design

Simulations are only proof of concepts and should be considered with caution. Therefore, a dedicated board for this circuit was designed to verify functionality.

The board circuit is shown in figure 4.5. Note there are two principal distinctions between the schematic simulated and its implementation:

1. The power supplies are bipolar
2. The inductors on the negative supply are explicitly shown here

The layout has three layers. The top layer has most of the circuitry, the middle layer contains the power supplies and the bottom layer is used for the ground plane as well as component placement.

In order to minimize stray capacitance, no plane was present on the inverting input pins of any amplifier or at the output. The OPA684, a current feedback amplifier with very low output impedance on its inverting pin, is very sensitive to stray capacitance on that node.

The figures 5.1 through 5.3 show the three layers of the board.

Figure 5.1: PCB - Top Layer

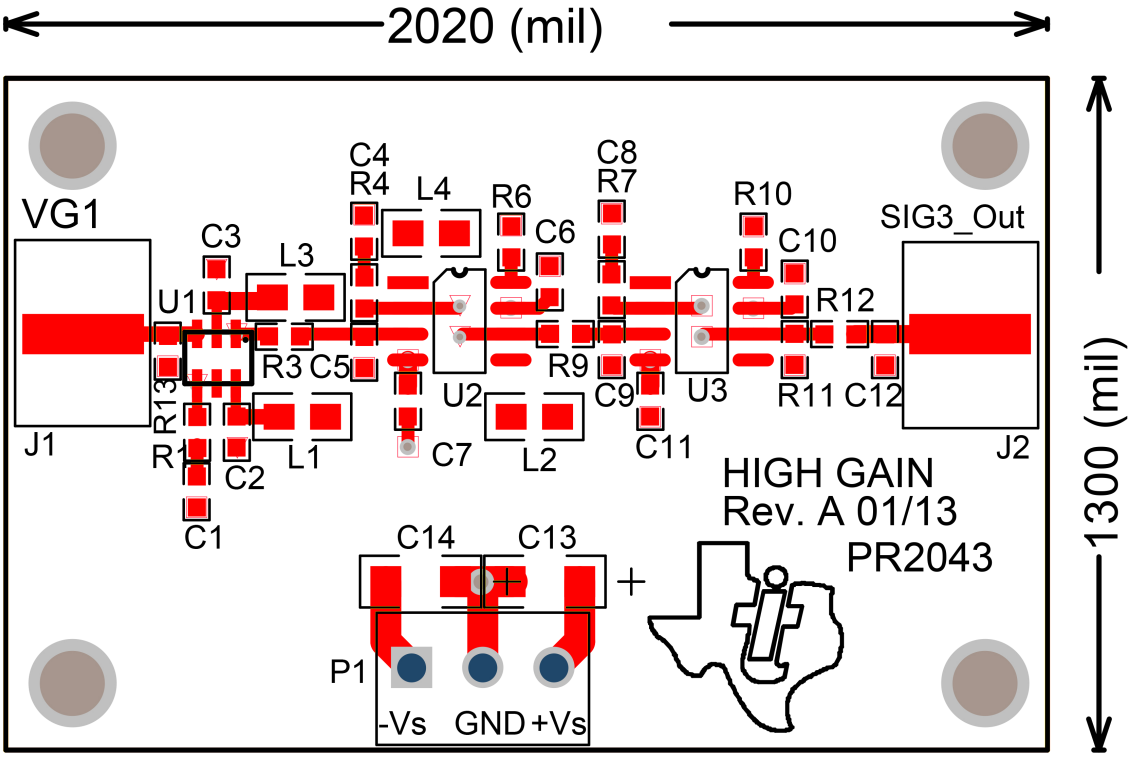


Figure 5.2: PCB - Mid Layer

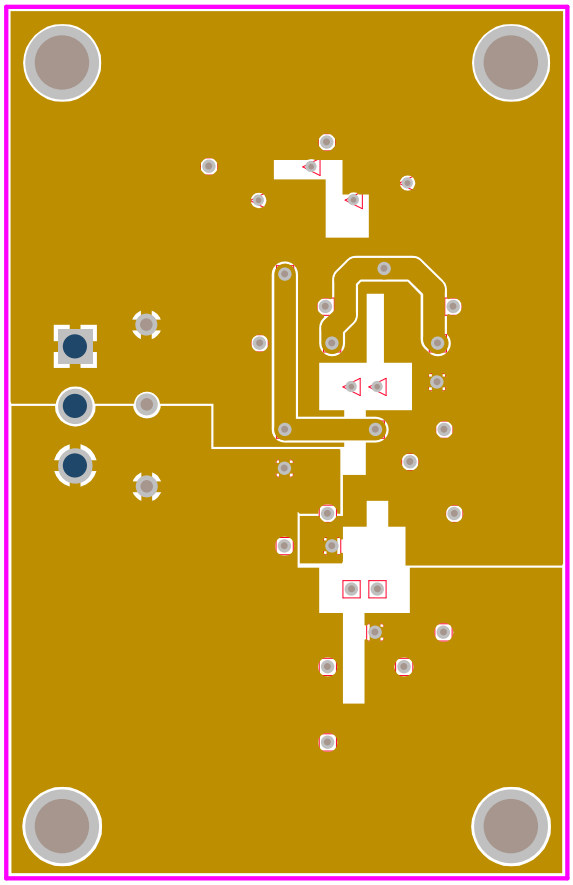
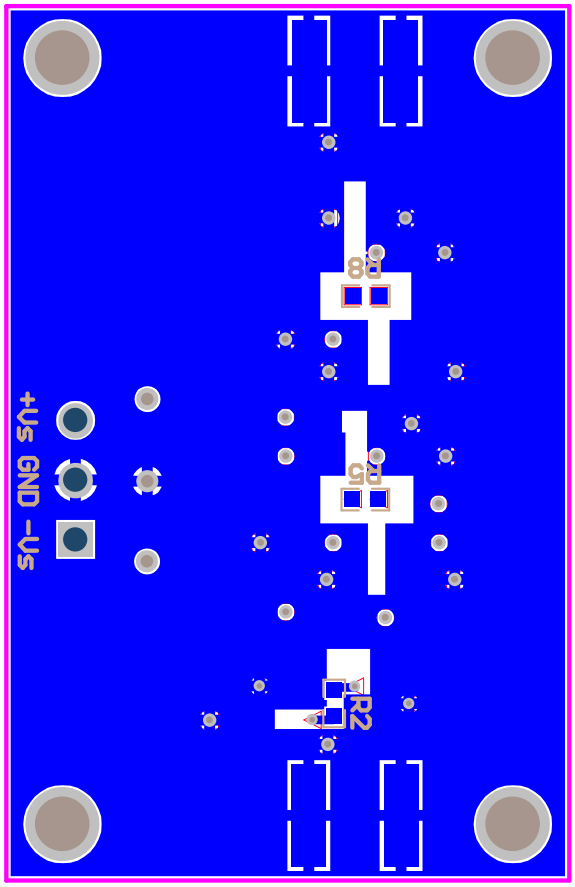


Figure 5.3: PCB - Bottom Layer



6 Evaluation

Evaluating the board required finding an arbitrary waveform generator (ARB) with sufficiently low signal amplitude control and noise (please keep in mind the very high voltage gain of **120,000 V/V**). A suitable ARB could not be found in the lab. Therefore, a steep band-pass filter eighth order) was connected to the ARB followed by two 40-dB attenuation pads to achieve the desired 20 μV_{PP} signal generation.

The output was evaluated using a standard oscilloscope. Averaging was used to extract the signal from the noise floor. Figures 6.1 through 6.3 show the output signal for a 1, 5 and 10 MHz sine wave input, respectively. The input signal amplitude was 20 μV_{PP} for all measurements. Looking at the 1MHz output signal plot, one can clearly see the distortion, whereas the 5 MHz and 10 MHz output plots look much cleaner. This can be explained by looking at the frequency response (figure 6.5). For the 1 MHz signal, HD2 and HD3 are still within the flat band. For 5 and 10 MHz, HD2 and HD3 are attenuated by the frequency response of the circuit and thus filtered out.

Please also note that equipment limitations due to signal generation (ARB) as well as signal evaluation (scope, network analyser) were experienced during evaluation. Noise issues in combination with the 20 μV_{PP} input signal and the very high gain (120,000 V/V) represented the main difficulty. Extracting the output signal from the noise floor presented a challenge to the scope's ADC-s, especially in respect to resolution. Please take the amplitude values in the following figures with a grain of salt. When it comes to amplitude values, the frequency response measured by the network analyser should be more accurate (see figures 6.4 and 6.5). However, even though averaging was used on the network analyser too, noise was still an issue.

The frequency response was measured using a network analyser. Using its internal attenuator, it was possible to set the test signal amplitude to a suitable level (no clipping / compression at the output). Figures 6.4 and 6.5 show the frequency response for 10 nF and 10 μF gain AC-coupling caps, respectively.

7 Conclusion

This design guide described the process and factors of developing a very high voltage gain, multi-stage design and explained its functionality and limitations. Knowing the important factors and the limitations, it should be possible to adjust this circuit to a given application while keeping in mind the limitations (especially the limited SNR).

Figure 6.1: Measured Output Signal, Sine Input, $f_{IN} = 1MHz$, $V_{IN} = 20\mu V_{PP}$, $C_{AC-GAIN} = 10\mu F$

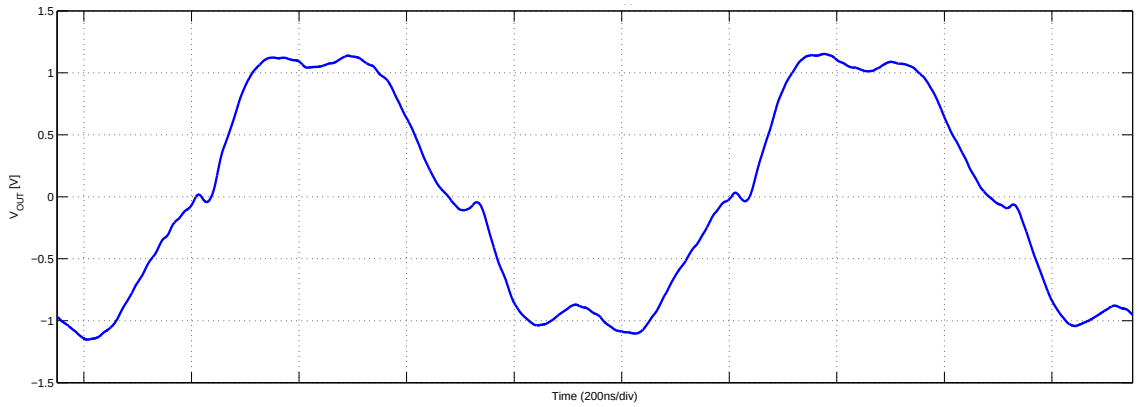


Figure 6.2: Measured Output Signal, Sine Input, $f_{IN} = 5MHz$, $V_{IN} = 20\mu V_{PP}$, $C_{AC-GAIN} = 10\mu F$

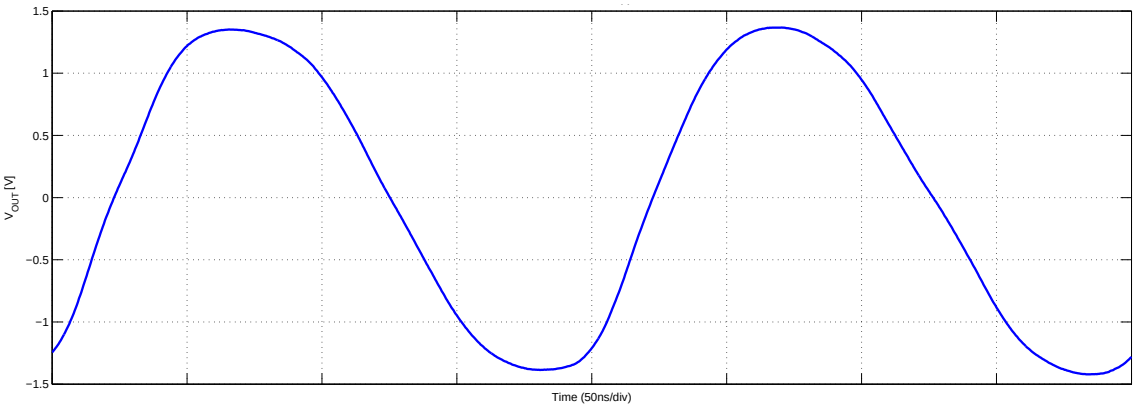


Figure 6.3: Measured Output Signal, Sine Input, $f_{IN} = 10MHz$, $V_{IN} = 20\mu V_{PP}$, $C_{AC-GAIN} = 10\mu F$

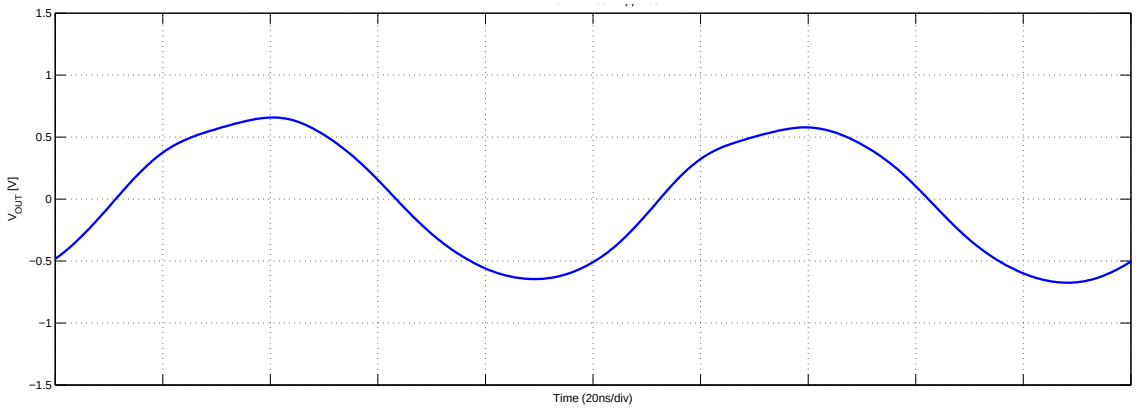


Figure 6.4: Measured Frequency Response, 10kHz-100MHz, $C_{AC-GAIN} = 10nF$

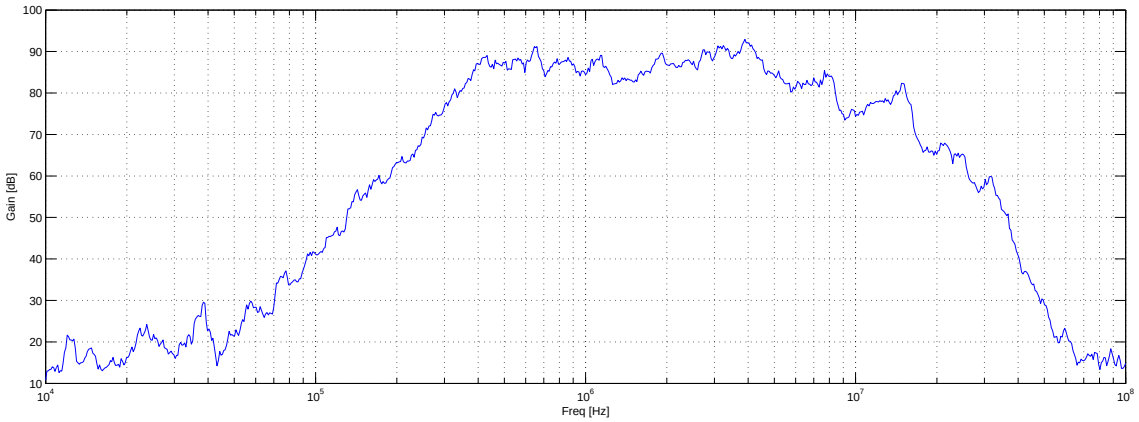
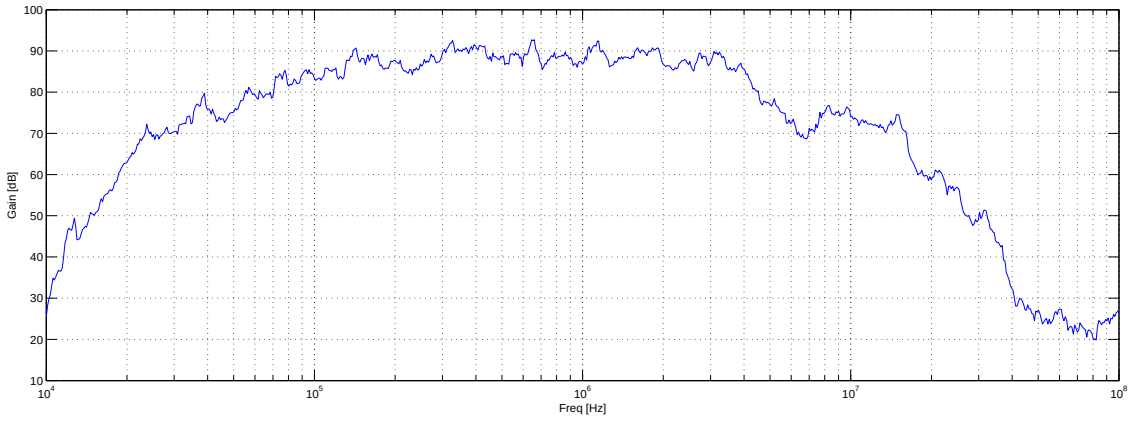


Figure 6.5: Measured Frequency Response, 10kHz-100MHz, $C_{AC-GAIN} = 10\mu F$



References

[TDK13] TDK: *C1608X7R1E104K080AA 100 nF, 0603, Multilayer Ceramic Chip Capacitor Datasheet.* September 2013. http://product.tdk.com/capacitor/mlcc/en/documents/C1608X7R1E104K080AA.pdf.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265