Test Report: PMP23552

50V_{IN} to 150V_{IN}, 28V 12A Synchronous Buck Converter Reference Design for Range of Space Missions

Description

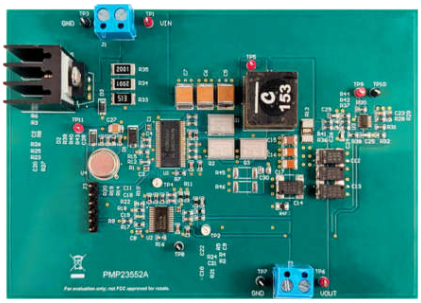
This reference design is a 28V output, 12A synchronous buck converter for space missions operating from a 50V to 150V input range. Primary applications include stepping down voltages from solar panels and 120VDC power distribution buses. The TPS7H5006-SEP pulse width modulation (PWM) controller controls the power stage using voltage-mode control. The OPA4H199-SEP senses the sense resistor voltage which enables the output short-circuit protection. The adjustable dead time of the TPS7H6005-SEP allows the timing of the switching MOSFETs to be optimized and results in over 95% efficiency with a 100V input and over 96% efficiency with a 50V input. A 12V self-biasing circuit is included to power the control circuits directly from the output. If an external 12V bias is provided, the self-biasing circuit can be removed, and results in higher efficiency.

Features

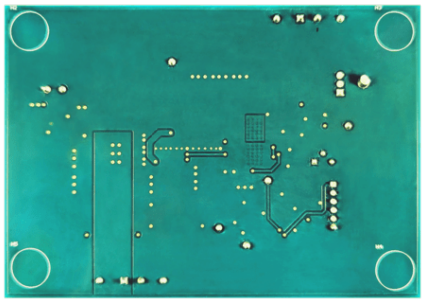
- Rad-tolerant: TPS7H5006-SEP TID 50krad (Si), TPS7H6005-SEP 50krad (Si), OPA4H199-SEP 30krad (Si) SEL, SEB, SEGR immune up to 43MeV-cm^2/mg
- Pin-to-pin radiation hardened options: TPS7H5002-SP TID 100krad (Si), TPS7H6005-SP 100krad (Si), OPA4H199-SP 100krad (Si) SEL, SEB, SEGR immune up to 75MeV-cm^2/mg
- Space-grade Gallium nitride field effect transistor (GaN FET) based
- > 95% efficiency at 100V_{IN}
- Overcurrent and short-circuit protection
- Synchronizable
- Optional self-bias circuit (higher efficiency with external bias)

Applications

- Satellite electrical power system (EPS)



Top of Board



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	50VDC to 150VDC
Output Voltage	28V
Maximum Load Current *Current was limited to 10A at 150V_{IN} due to thermal performance*	12A
Switching Frequency	245kHz

1.2 Required Equipment

- Programmable DC Power Supply (Chroma Model 62024P-600-8)
- Electronic Load (Kikusui Model PLZ334WL)
- Electronic Load (Kikusui Model PLZ152WA)

1.3 Dimensions

Board XY dimensions: 125mm × 87mm.

Approximate circuit size: 90mm × 50mm.

1.4 Test Setup

The unit under test (UUT) was enclosed in an 18in × 11.5in × 7.5in Plexiglas box, including a fan for forced airflow at 25ºC ambient. A 220uF 450V Rubycon ZL Series capacitor was used at the circuit input.

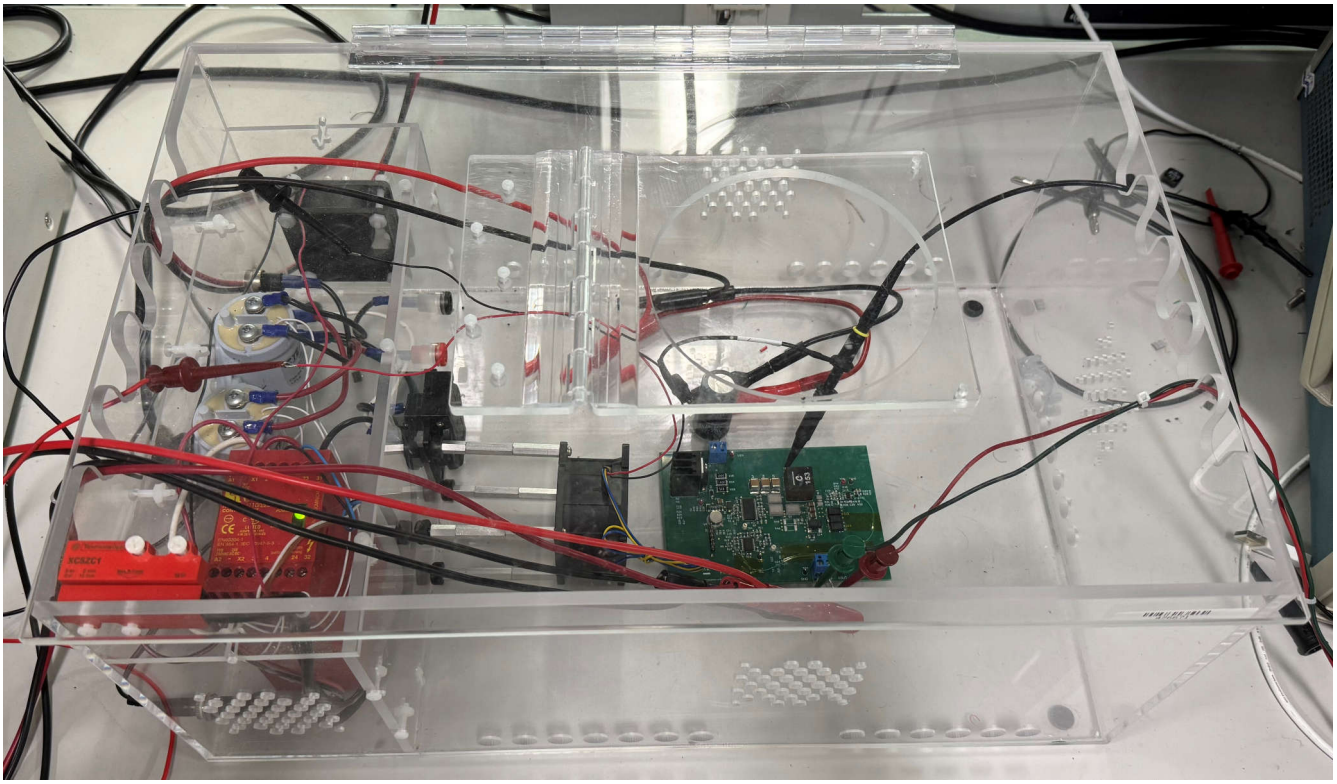

Figure 1-1. Test Setup

2 Testing and Results

2.1 Efficiency Graphs

Efficiency and power loss at various input voltages are shown in Figure 2-1 and Figure 2-2.

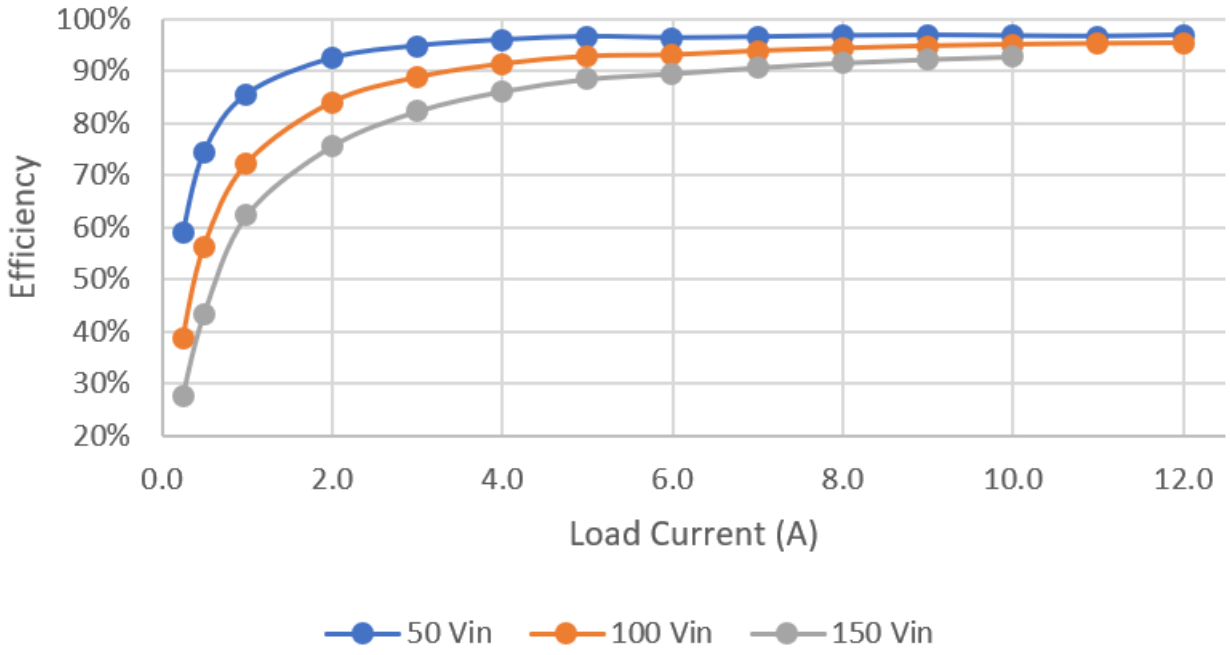

Figure 2-1. Efficiency Graph

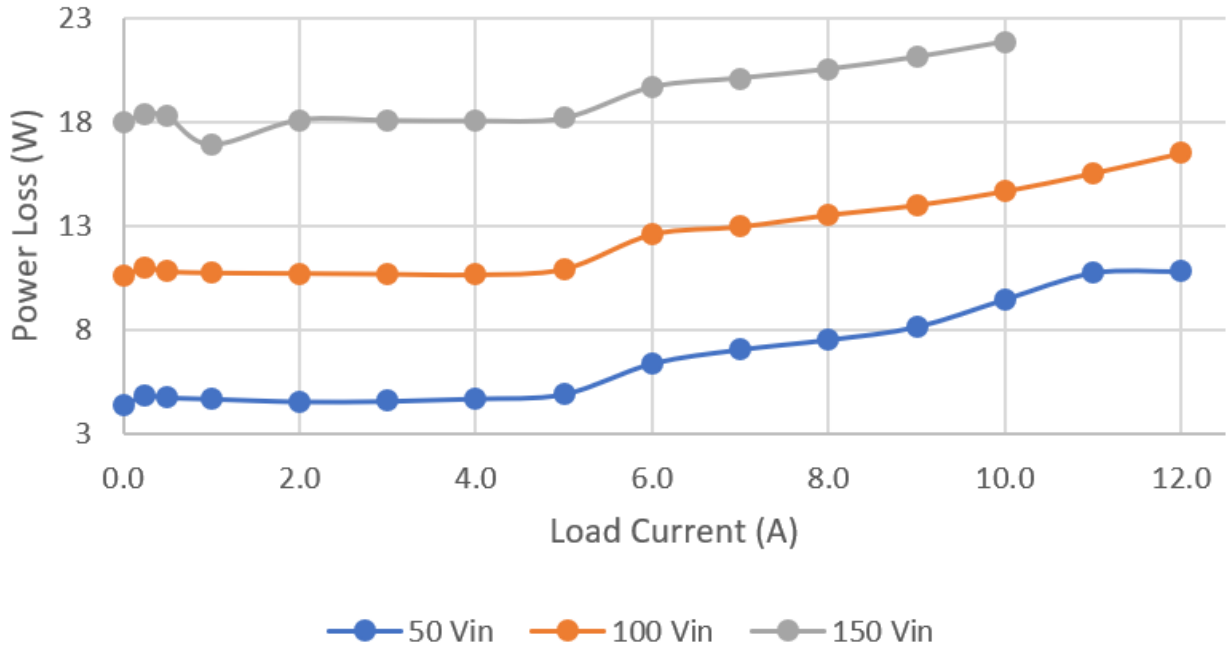

Figure 2-2. Power Loss Graph

2.2 Efficiency Data

Efficiency data is shown in Table 2-1 through Table 2-3.

Table 2-1. Efficiency Data for 50V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
50	0.088	27.93	0.00	4.40	0.00	4.40	0.0
50	0.237	27.93	0.25	11.9	7.0	4.87	58.9
50	0.375	27.93	0.50	18.8	14.0	4.79	74.5
50	0.653	27.93	1.00	32.7	27.9	4.72	85.5
50	1.209	27.93	2.00	60.5	55.9	4.59	92.4
50	1.768	27.93	3.00	88.4	83.8	4.61	94.8
50	2.329	27.93	4.00	116.5	112	4.73	95.9
50	2.892	27.93	5.00	145	140	4.95	96.6
50	3.48	27.93	6.00	174	168	6.42	96.3
50	4.052	27.93	7.00	203	196	7.09	96.5
50	4.62	27.93	8.00	231	223	7.56	96.7
50	5.191	27.93	9.00	260	251	8.18	96.8
50	5.776	27.93	10.0	289	279	9.5	96.7
50	6.36	27.93	11.0	318	307	10.77	96.6
50	6.92	27.93	12.0	346	335	10.84	96.9

Table 2-2. Efficiency Data for 100V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
100	0.106	27.93	0	10.6	0	10.60	0.0%
100	0.18	27.93	0.25	18.0	7.0	11.02	38.8%
100	0.248	27.93	0.50	24.8	14.0	10.84	56.3%
100	0.387	27.93	1.00	38.7	27.9	10.77	72.2%
100	0.666	27.93	2.00	66.6	55.9	10.74	83.9%
100	0.945	27.93	3.00	94.5	83.8	10.71	88.7%
100	1.224	27.93	4.00	122.4	111.7	10.68	91.3%
100	1.506	27.93	5.00	150.6	139.7	10.95	92.7%
100	1.802	27.93	6.00	180.2	167.6	12.62	93.0%
100	2.085	27.93	7.00	208.5	195.5	12.99	93.8%
100	2.37	27.93	8.00	237.0	223.4	13.56	94.3%
100	2.654	27.93	9.00	265.4	251.4	14.03	94.7%
100	2.94	27.93	10.0	294.0	279.3	14.70	95.0%
100	3.228	27.93	11.0	322.8	307.2	15.57	95.2%
100	3.517	27.93	12.0	351.7	335.2	16.54	95.3%

Table 2-3. Efficiency Data for 150V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
150	0.12	27.92	0	18.0	0	18.00	0.0%
150	0.169	27.92	0.25	25.4	7.0	18.37	27.5%
150	0.215	27.92	0.5	32.3	14.0	18.29	43.3%
150	0.299	27.92	1.00	44.9	27.9	16.93	62.3%
150	0.493	27.92	2.00	74.0	55.8	18.11	75.5%
150	0.679	27.92	3.00	101.9	83.8	18.09	82.2%
150	0.865	27.92	4.00	129.8	111.7	18.07	86.1%
150	1.052	27.92	5.00	157.8	139.6	18.20	88.5%
150	1.248	27.92	6.00	187.2	167.5	19.68	89.5%
150	1.437	27.92	7.00	215.6	195.4	20.11	90.7%
150	1.626	27.92	8.00	243.9	223.4	20.54	91.6%
150	1.816	27.92	9.00	272.4	251.3	21.12	92.2%
150	2.007	27.92	10.0	301.1	279.2	21.85	92.7%

2.3 Thermal Images

All images were captured with the unit under test (UUT) enclosed in an 18in × 11.5in × 7.5in Plexiglas box, 25ºC ambient, after a 30-minute warm up, and with forced airflow. The unit was tested with up to 12A load and at various input voltages. The high-side GaN FET became the hottest component on the board when operating at 150V_{IN} at 10A loading with a recorded temperature of 96.6C°.

Table 2-4. Component Legend

Measurement	Component
Sp1	Inductor (L1)
Sp2	High-Side GaN FET (Q1)
Sp3	Half-Bridge Gate Driver (U1)
Sp4	Low-Side GaN FET (Q2)
Sp5	Low-Side GaN FET (Q3)
Sp6	Fault Sense Resistor (R14)
Sp7	Op-amp (U3)
Sp8	PWM Controller (U2)

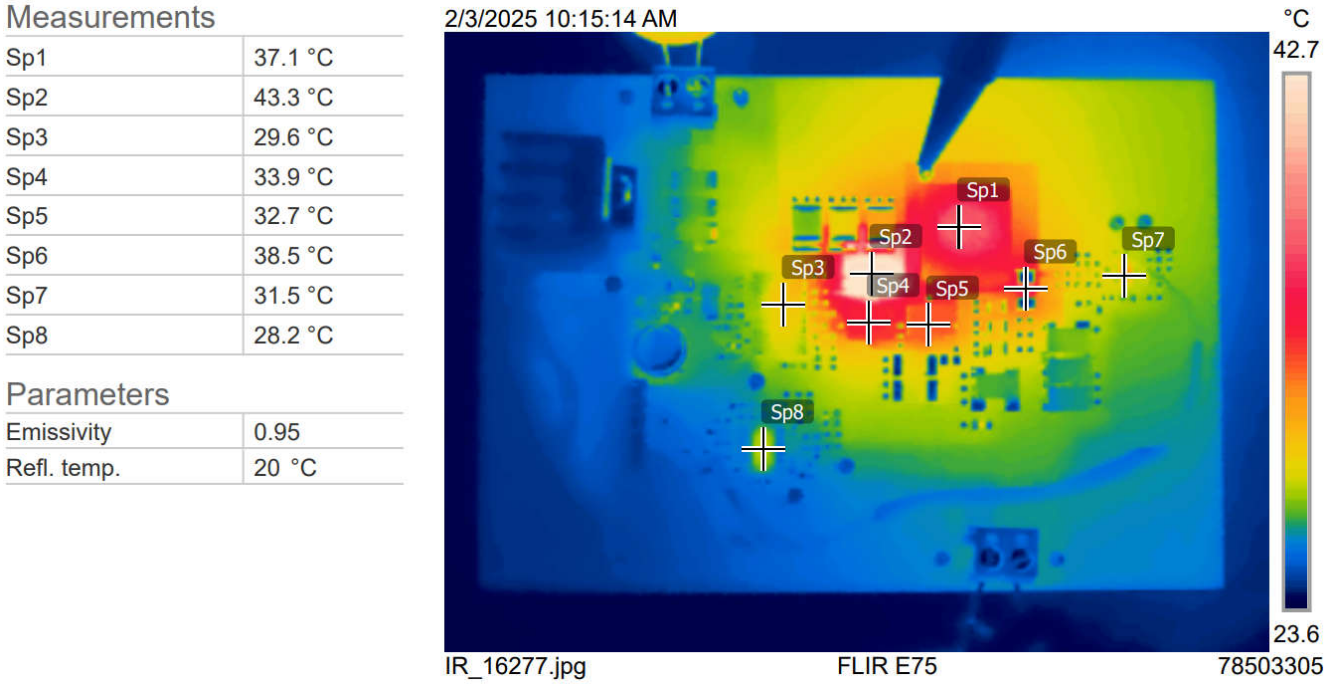

Figure 2-3. Thermal Image, 50V_{IN}, 12A Load

Measurements	
Sp1	52.0 °C
Sp2	66.2 °C
Sp3	34.6 °C
Sp4	44.3 °C
Sp5	41.8 °C
Sp6	44.0 °C
Sp7	34.9 °C
Sp8	30.1 °C

Parameters	
Emissivity	0.95
Refl. temp.	20 °C

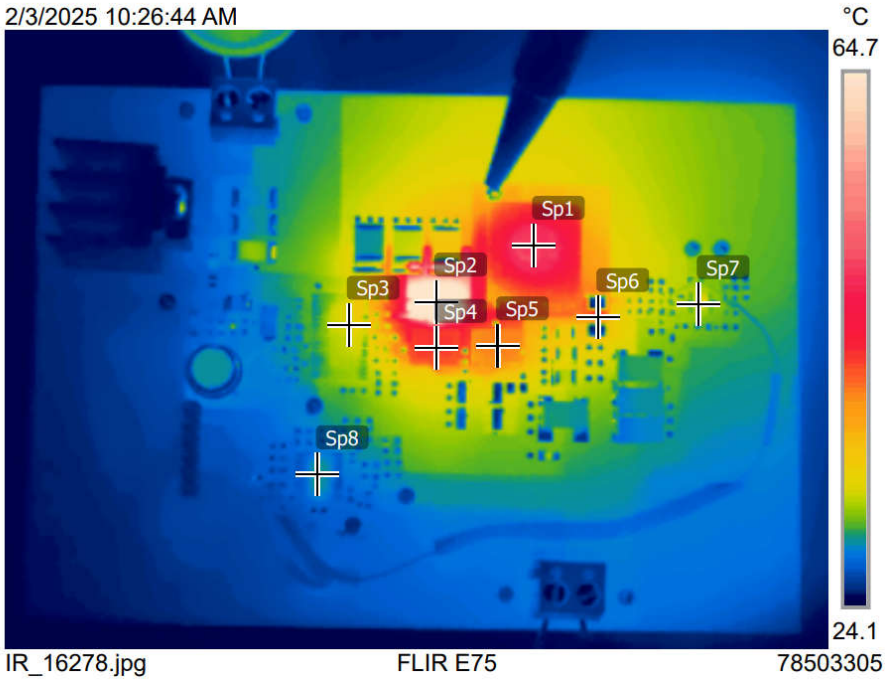

Figure 2-4. Thermal Image, 100V_{IN}, 12A Load

Measurements	
Sp1	62.2 °C
Sp2	96.6 °C
Sp3	40.3 °C
Sp4	61.0 °C
Sp5	54.7 °C
Sp6	47.6 °C
Sp7	38.7 °C
Sp8	32.2 °C

Parameters	
Emissivity	0.95
Refl. temp.	20 °C

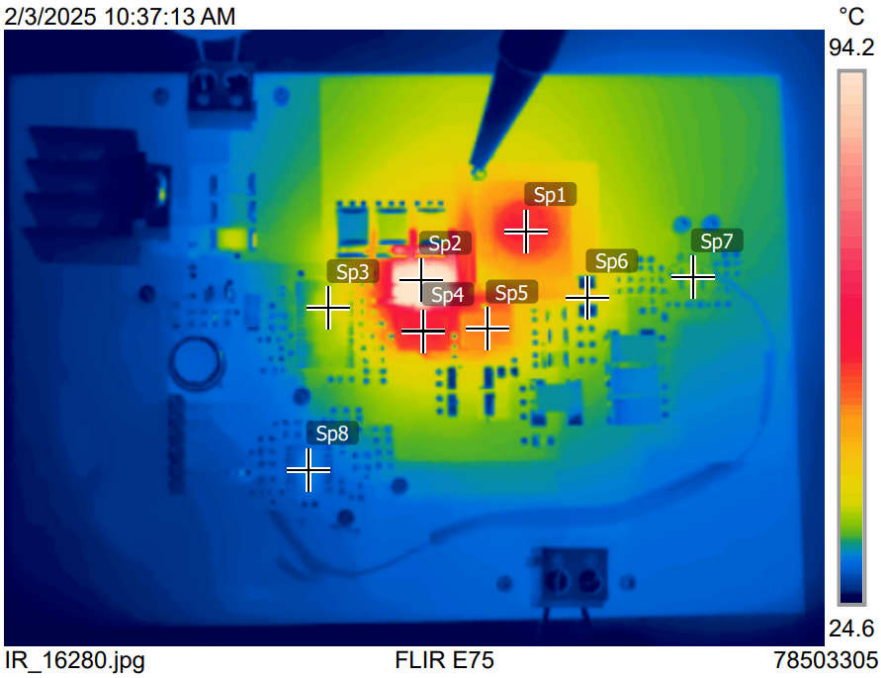

Figure 2-5. Thermal Image, 150V_{IN}, 10A Load

2.4 Bode Plots

The feedback loop frequency response was measured with a 10A load at various input voltage conditions and is shown in Figure 2-6 through Figure 2-8.

Table 2-5. Feedback Loop Frequency Response

Condition	Unity Gain Bandwidth (kHz)	Phase Margin (°)	Gain Margin (dB)
$50V_{IN}$, 10A load	14.7	65	28.97
$100V_{IN}$, 10A load	22.5	67	23.98
$150V_{IN}$, 10A load	31.9	66	19.57

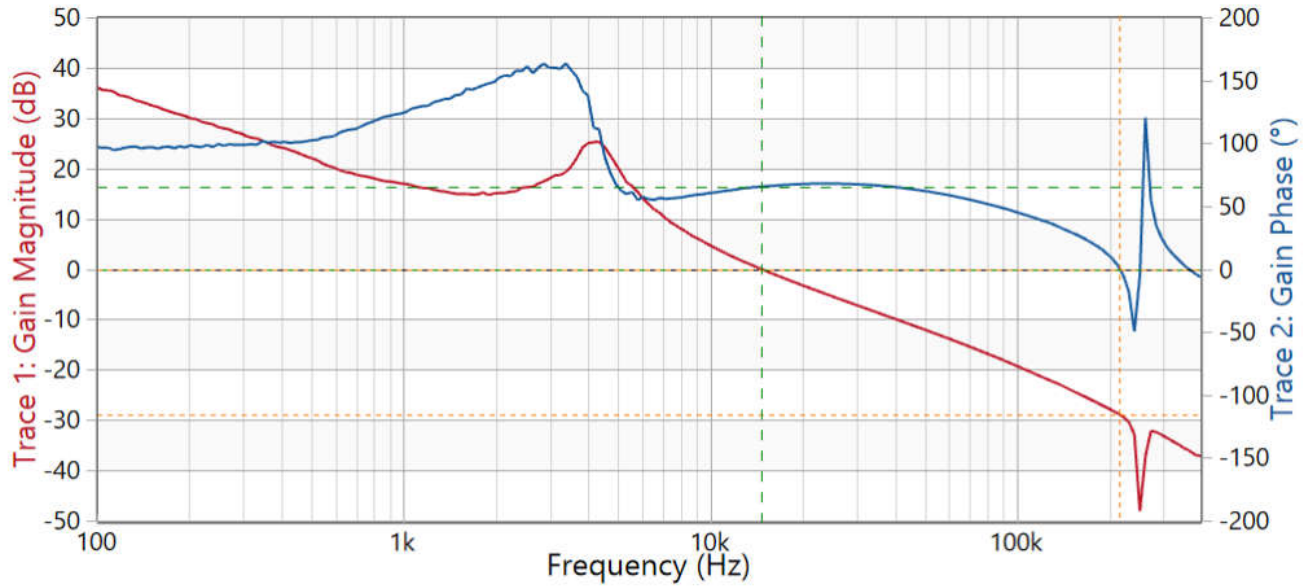

Figure 2-6. Bode Plot, $50V_{IN}$, 10A Load

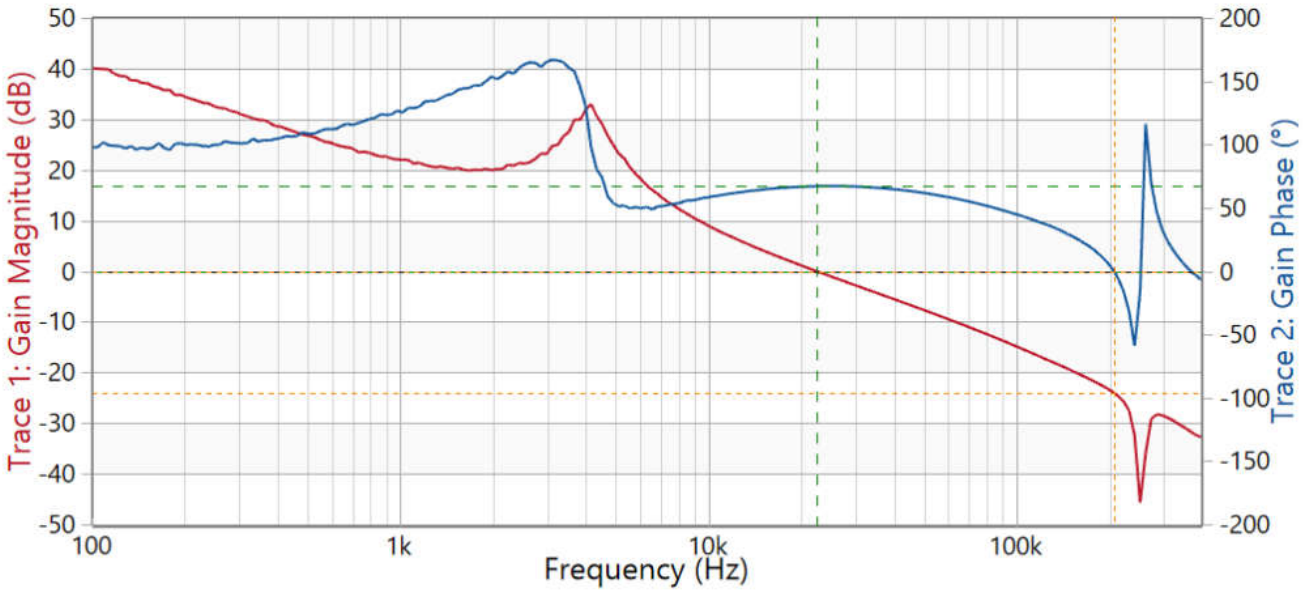

Figure 2-7. Bode Plot, $100V_{IN}$, 10A Load

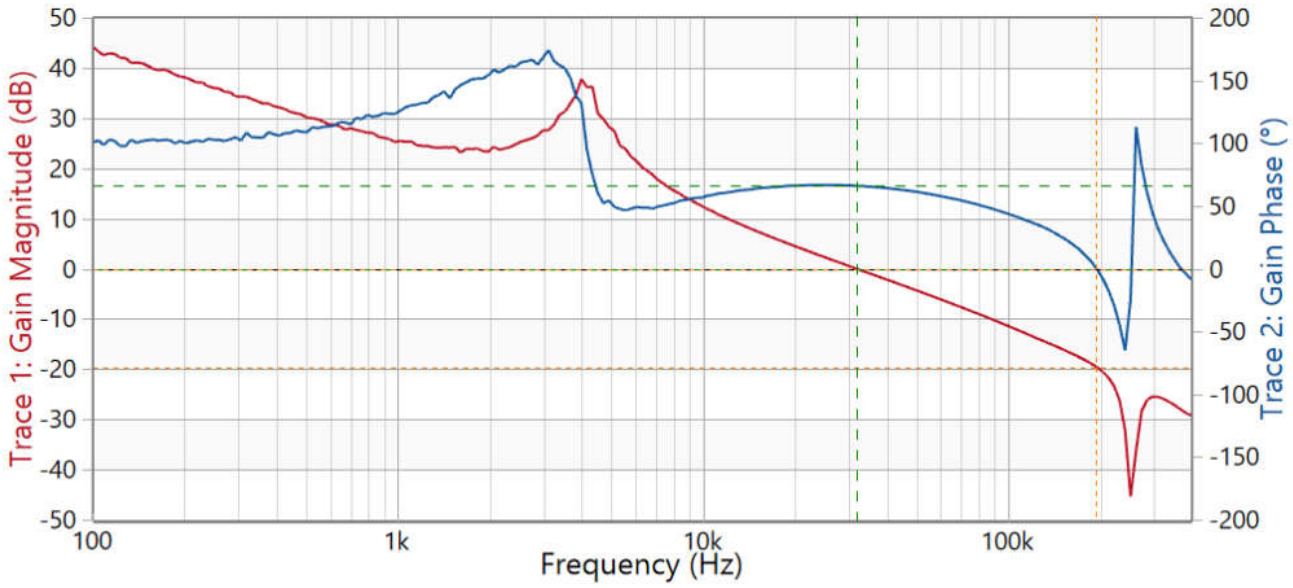

Figure 2-8. Bode Plot, 150V_{IN}, 10A Load

3 Waveforms

3.1 Switching

The maximum voltage stress on the drain of the low-side FETs (Q2 and Q3) occurs with 150V input and 10A load. This was recorded as 170Vpk, as shown in Figure 3-1 and Figure 3-2.

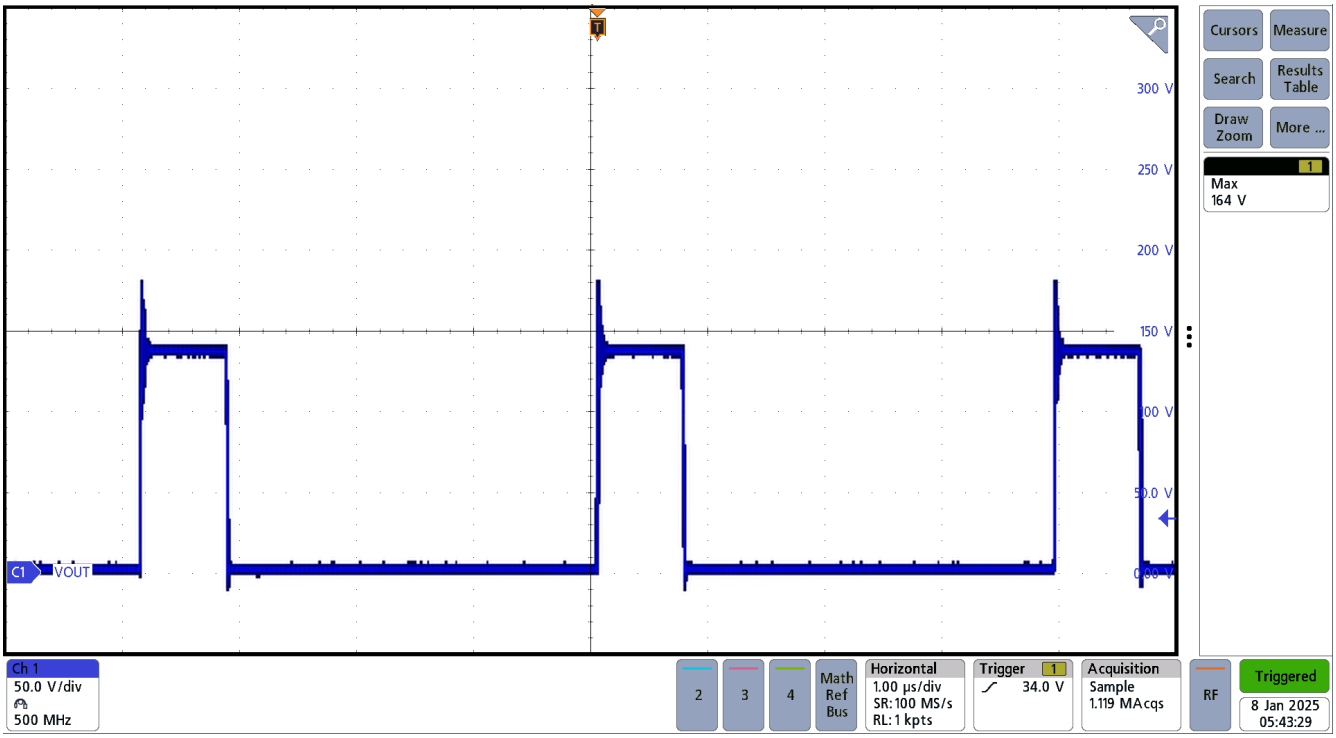

Figure 3-1. Maximum Voltage Stress, 150V_{IN}, 10A Load

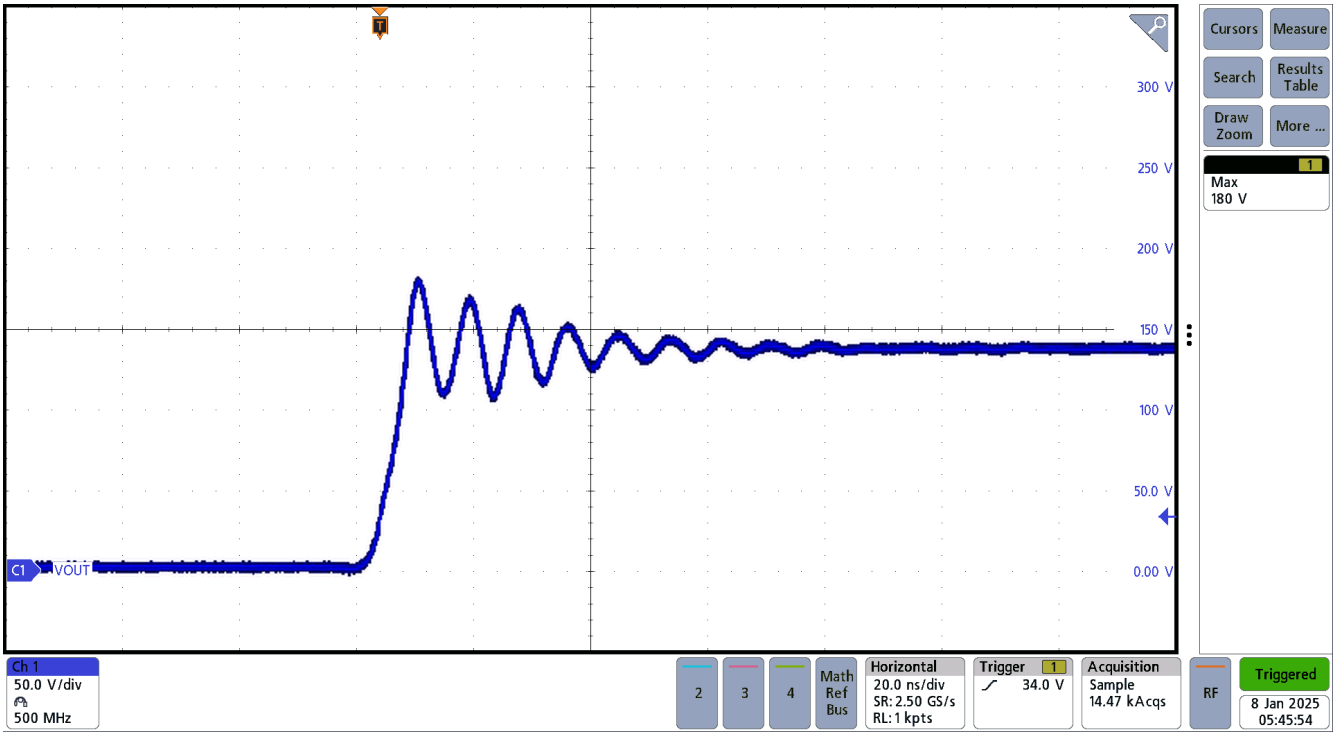

Figure 3-2. Switch Node, 150V_{IN}, 10A Load

3.2 Output Voltage Ripple

The output ripple voltage was measured using a tip-and-barrel technique across output capacitor C18. Figure 3-3 through Figure 3-5 show the output ripple with a 10A load at various input voltages.

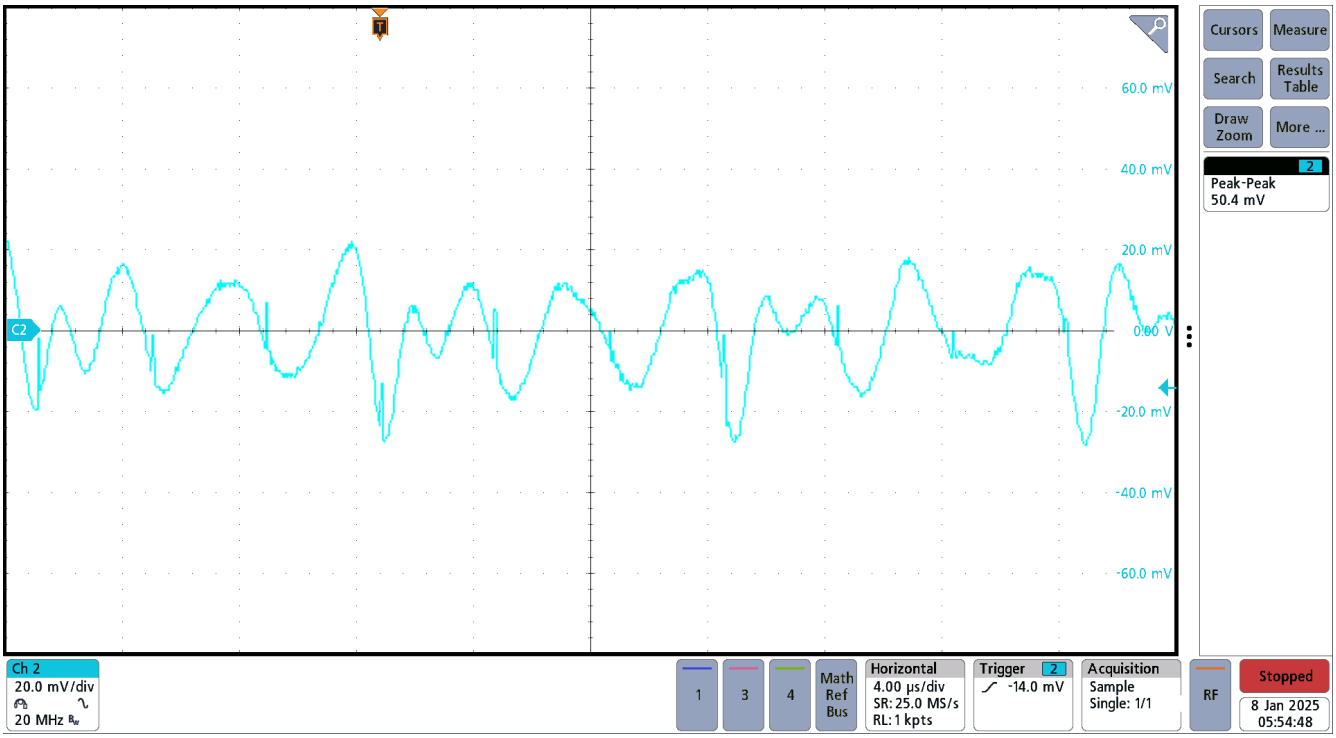

Figure 3-3. Output Voltage Ripple, $50V_{IN}$, 10A Load

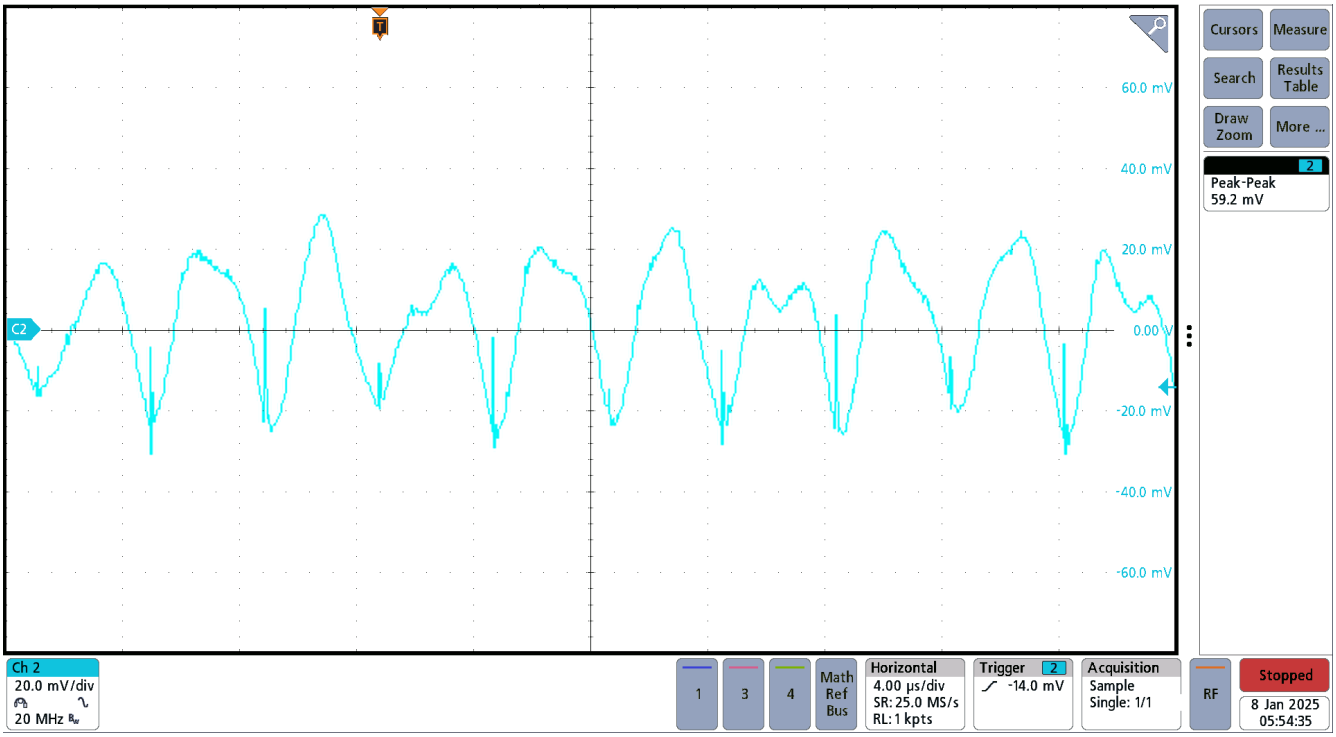

Figure 3-4. Output Voltage Ripple, $100V_{IN}$, 10A Load

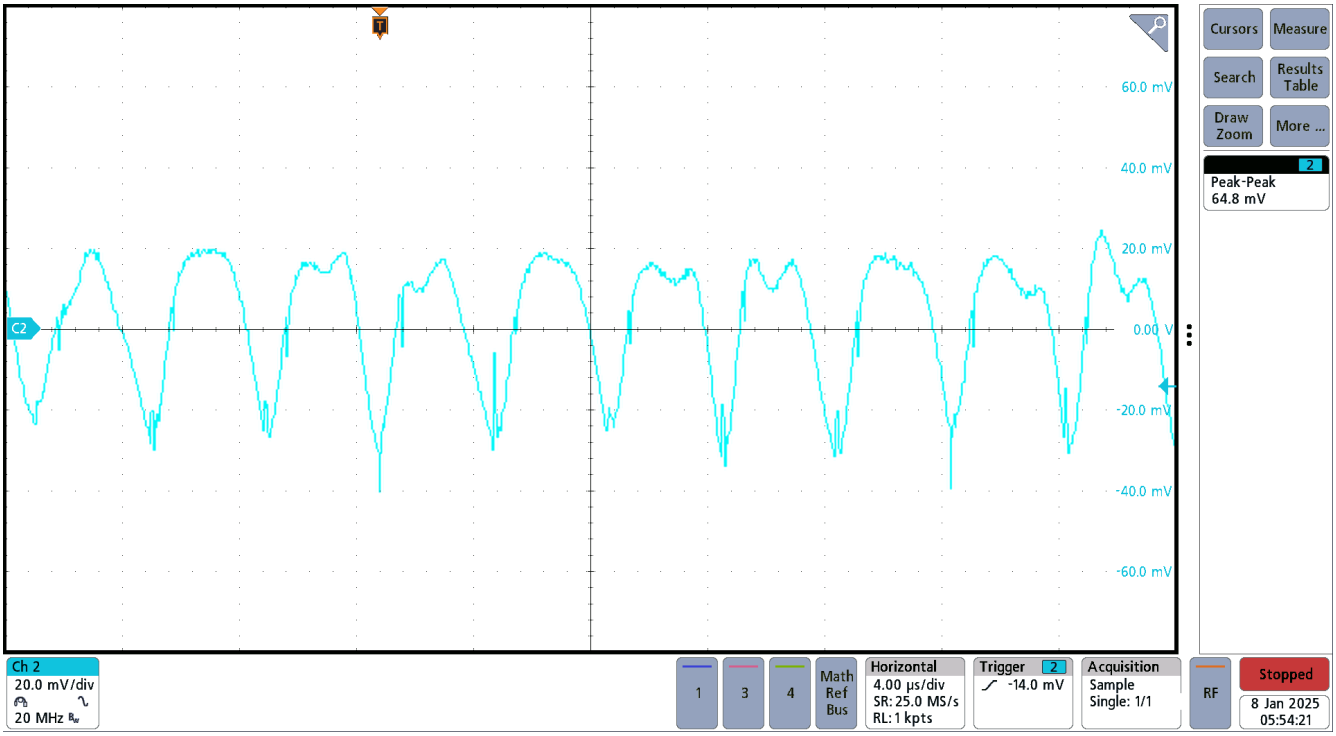

Figure 3-5. Output Voltage Ripple, 150V_{IN}, 10A Load

3.3 Short-Circuit Protection

Figure 3-6 and Figure 3-7 show the switch node, output voltage, and current during a short-circuit event. The input voltage was 100V for both figures. Channel 1 shows the switch node, channel 2 shows the output voltage, and channel 4 shows the output current.

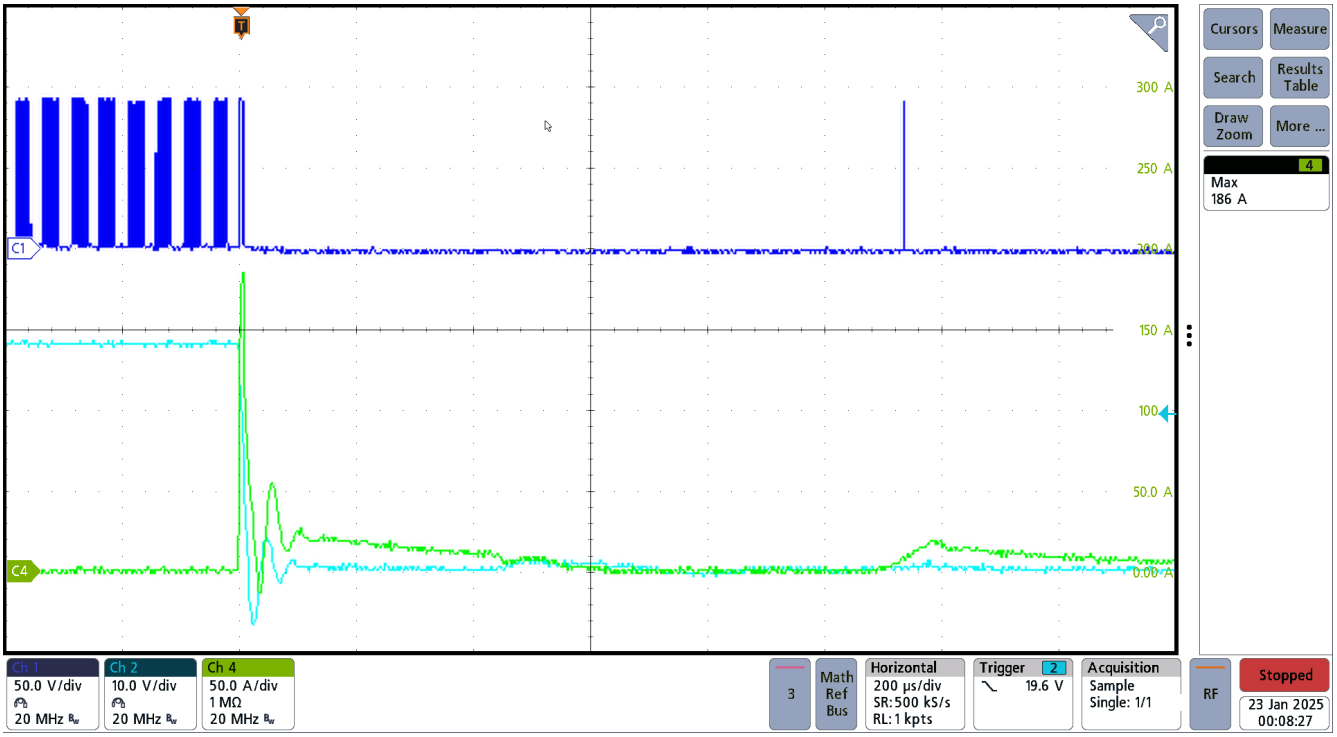

Figure 3-6. Operation Upon Application of Short Circuit, 100V_{IN}

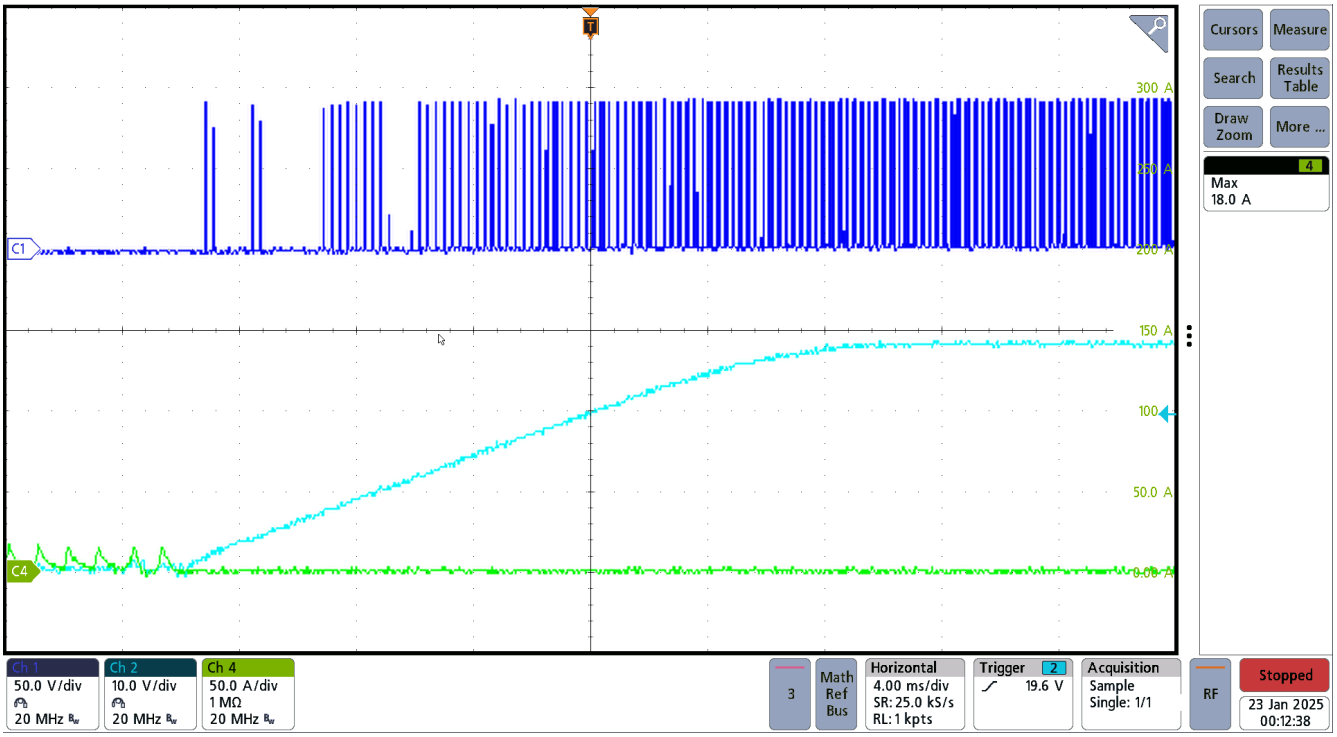

Figure 3-7. Operation During Sustained Short Circuit, 100V_{IN}

3.4 Load Transients

Load transient response is shown in Figure 3-8 and Figure 3-10. The load was stepped between 1A and 10A at various input voltages.

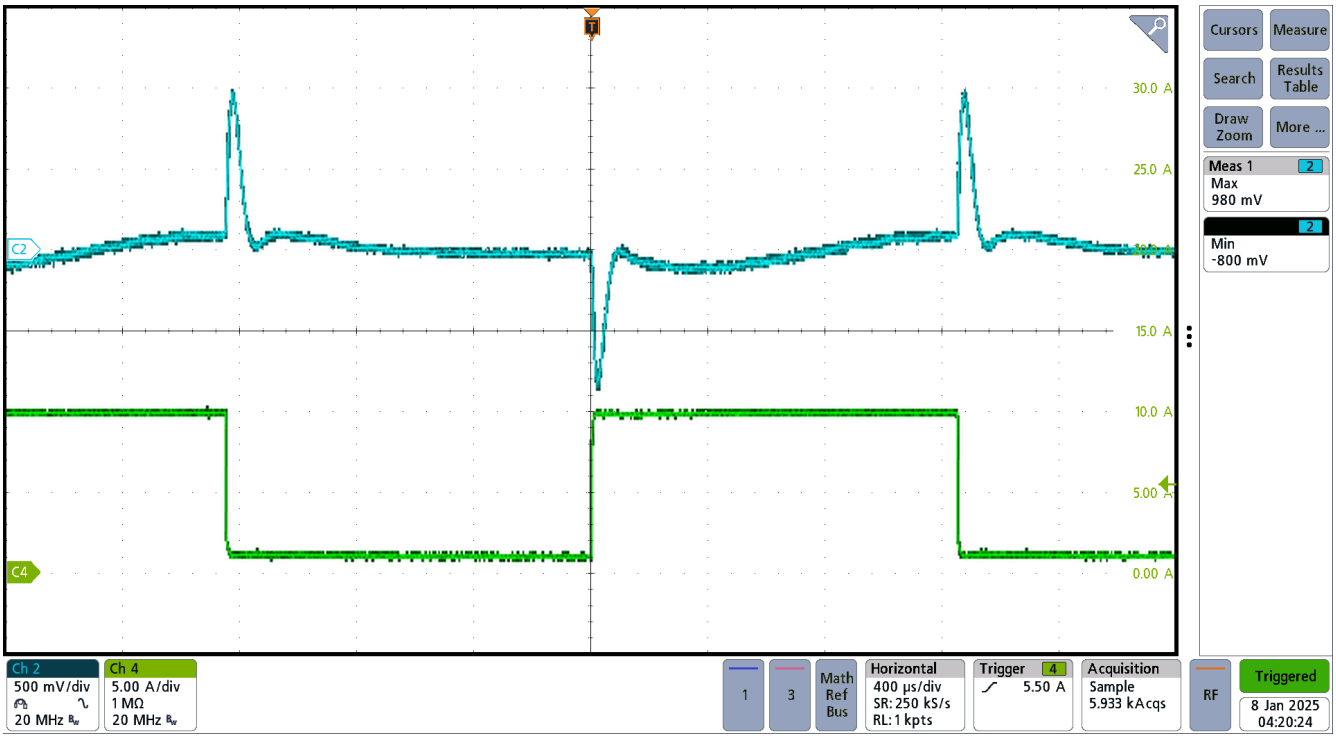

Figure 3-8. Load Transient, $50V_{IN}$, 1A to 10A

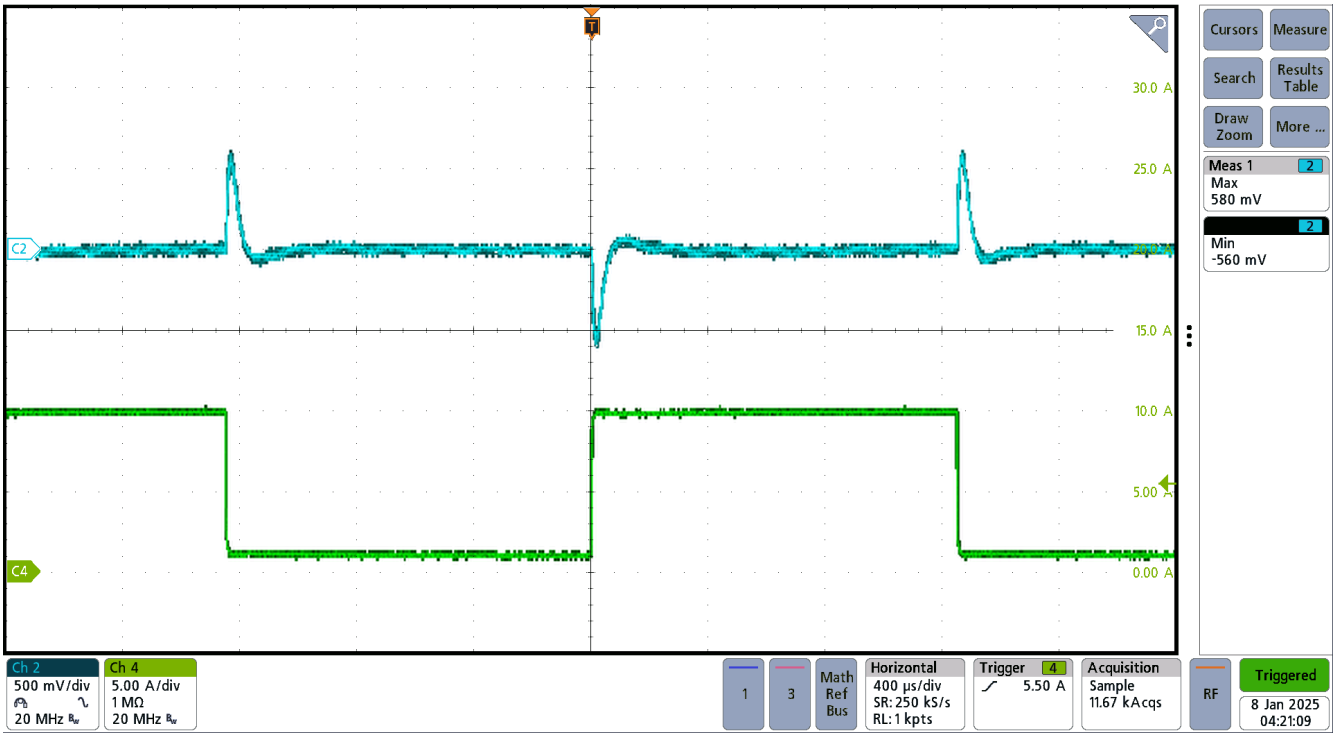

Figure 3-9. Load Transient, $100V_{IN}$, 1A to 10A

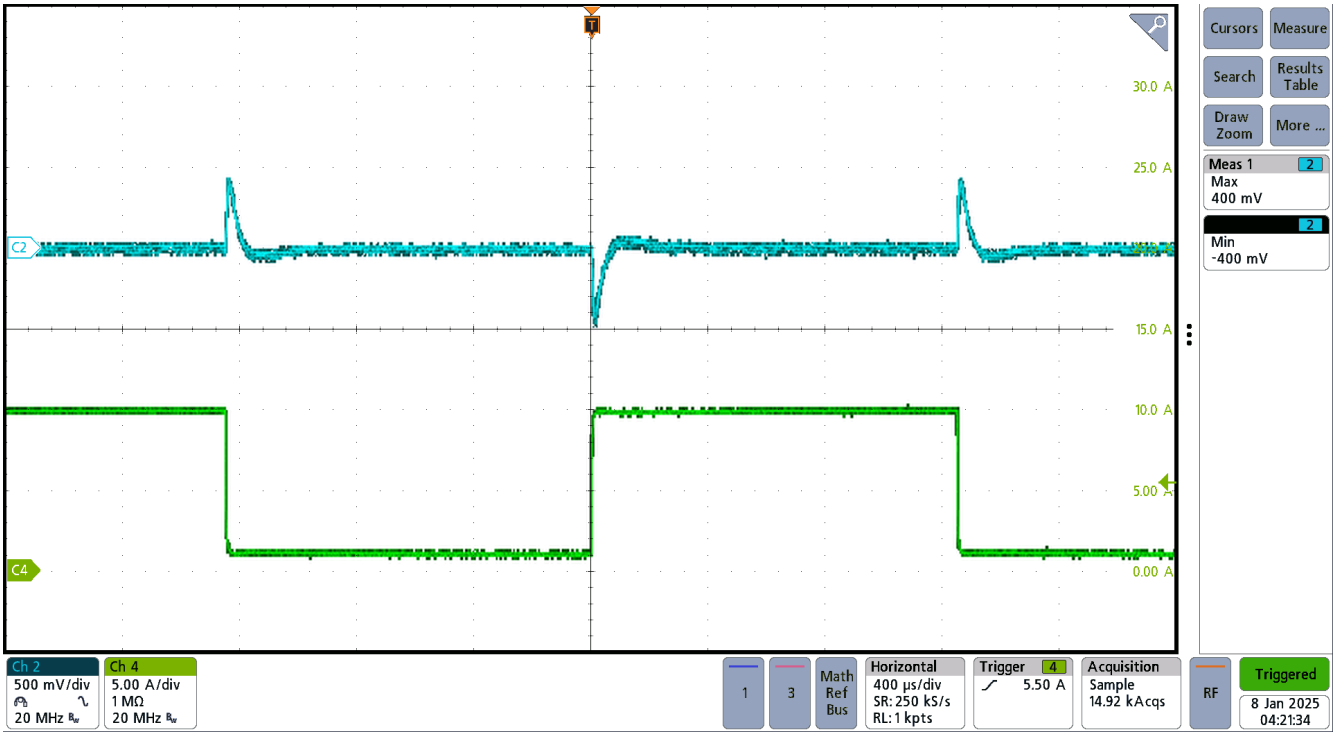

Figure 3-10. Load Transient, 150V_{IN}, 1A to 10A

3.5 Start-up Sequence

Start-up behavior at 100V input with no load and a 10A load is shown in Figure 3-11 and Figure 3-12.

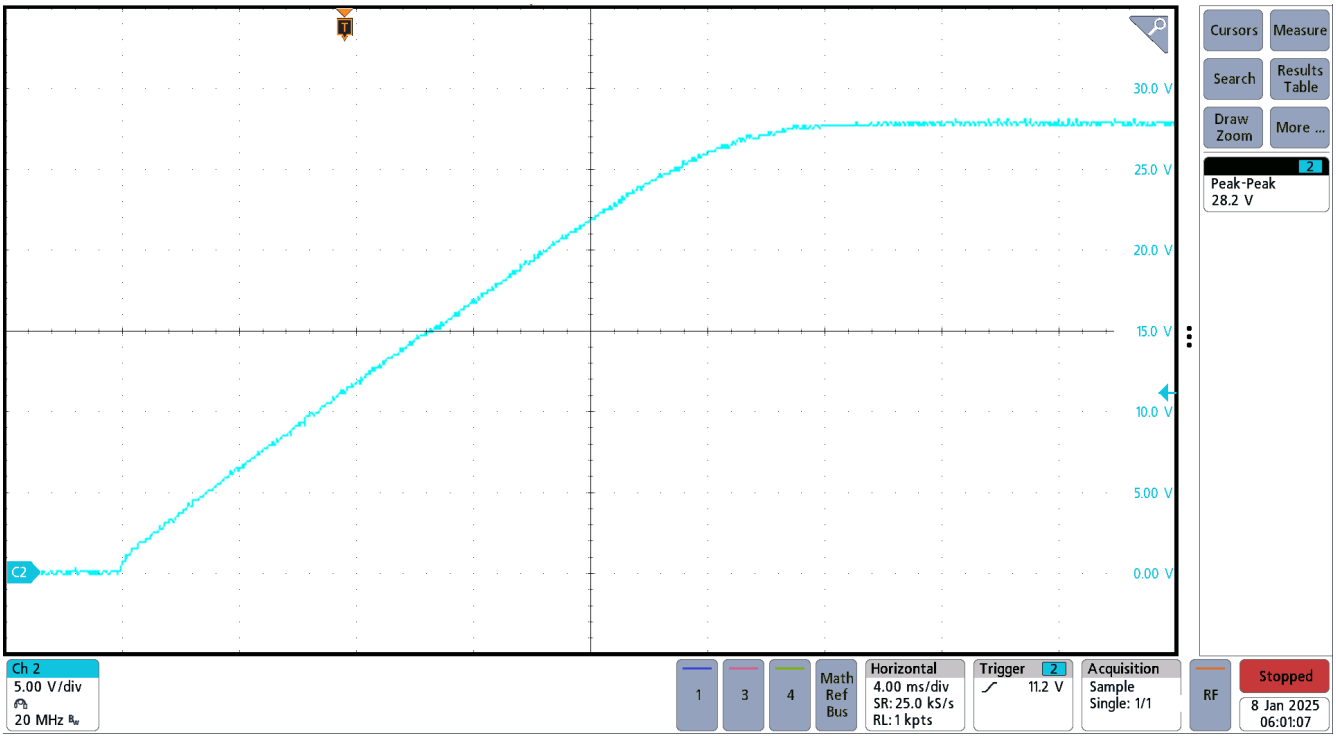

Figure 3-11. Start-Up, 100V_{IN}, No Load

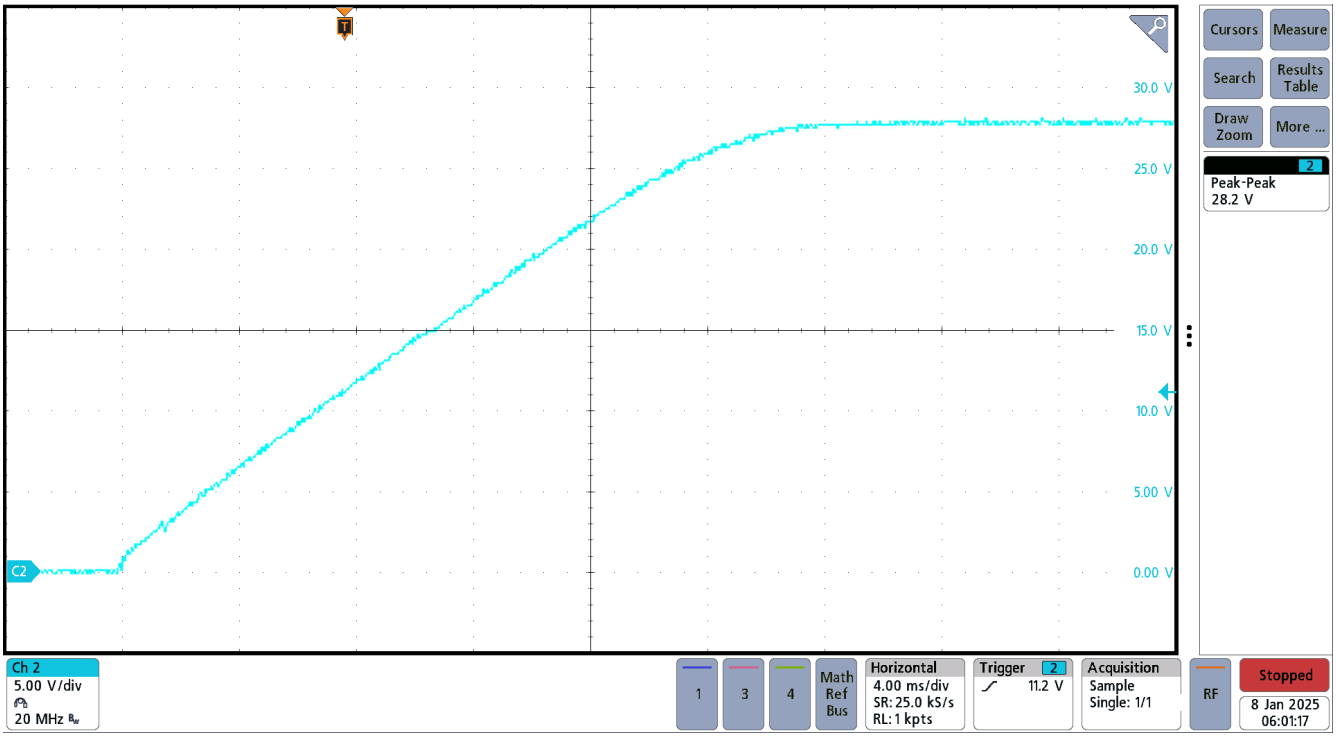

Figure 3-12. Start-Up, 100V_{IN}, 10A Load

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