Test Report: PMP22822

2.2-W Multi-Output Flybuck Reference Design

Description

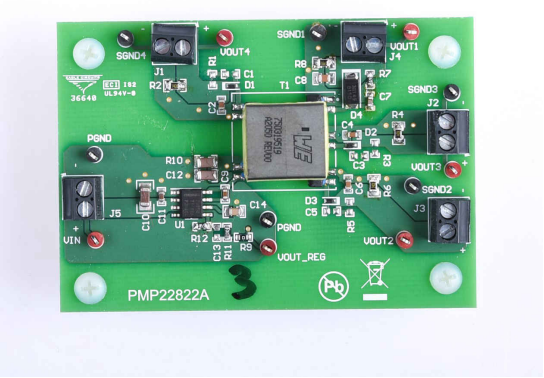
This reference design is a 2.2-W multi-output flybuck design for isolated gate-drive bias supplies. The supply is designed to accept an input from 24-V systems. This design uses the LM36520 synchronous buck converter to generate four isolated outputs. Primary-side regulation maintains each of the four 17-V outputs within ±10%.

Features

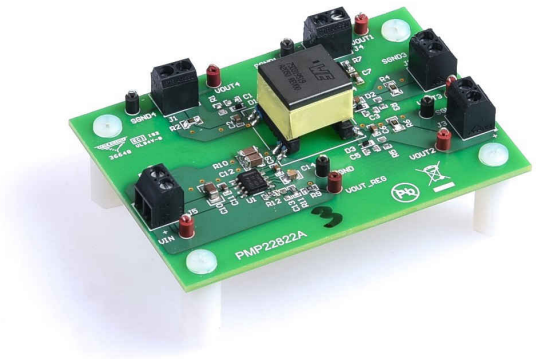
- Four 17-V isolated outputs
- Achieves ±10% output voltage accuracy on non-regulated outputs
- PSR eliminates need for an optocoupler
- Transformer designed to comply with: IEC61800-5-1

Applications

- Servo drive power supply module



Board Top Photo



Bottom Side Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications	Units
Input Voltage	21.6–26.4	V
Output Voltage 1	17	V
Output Current 1	0.1	A
Output Voltage 2	17	V
Output Current 2	0.01	A
Output Voltage 3	17	V
Output Current 3	0.01	A
Output Voltage 4	17	V
Output Current 4	0.01	A

2 Testing and Results

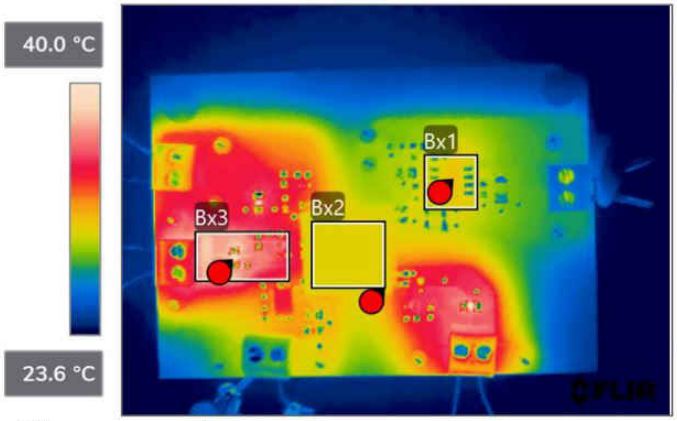
2.1 Efficiency Data

Table 2-1. Efficiency Data

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT1} (V)	V_{OUT2} (V)	V_{OUT3} (V)	V_{OUT4} (V)	I_{OUT1} (A)	I_{OUT2} (A)	I_{OUT3} (A)	I_{OUT4} (A)	P_{OUT} (W)	Efficiency	Loss (W)
24.00	0.12	2.78	**16.85**	**17.11**	**17.05**	**17.14**	0.10	0.01	0.01	0.01	2.20	0.79	0.58
24.00	0.02	0.53	**18.27**	**17.65**	**17.74**	**17.58**	0.00	0.00	0.00	0.00	0.00	0.00	0.53
21.61	0.12	2.66	**16.02**	**16.58**	**16.38**	**16.72**	0.10	0.01	0.01	0.01	2.09	0.79	0.57
21.60	0.02	0.50	**18.14**	**17.61**	**17.68**	**17.55**	0.00	0.00	0.00	0.00	0.00	0.00	0.50
26.39	0.11	2.85	**17.13**	**17.29**	**17.27**	**17.30**	0.10	0.01	0.01	0.01	2.24	0.79	0.61
26.40	0.02	0.58	**18.34**	**17.69**	**17.79**	**17.60**	0.00	0.00	0.00	0.00	0.00	0.00	0.58

2.2 Thermal Images

Thermal image is shown in the following figure.



Measurements	
Bx1	
Max	31.7 °C
Bx2	
Max	30.7 °C
Bx3	
Max	41.8 °C

Bx1 = U1

Bx2 = T1

Bx3 = R4

Figure 2-1. Thermal Image

2.3 Bode Plots

Bode plot is shown in the following figure.

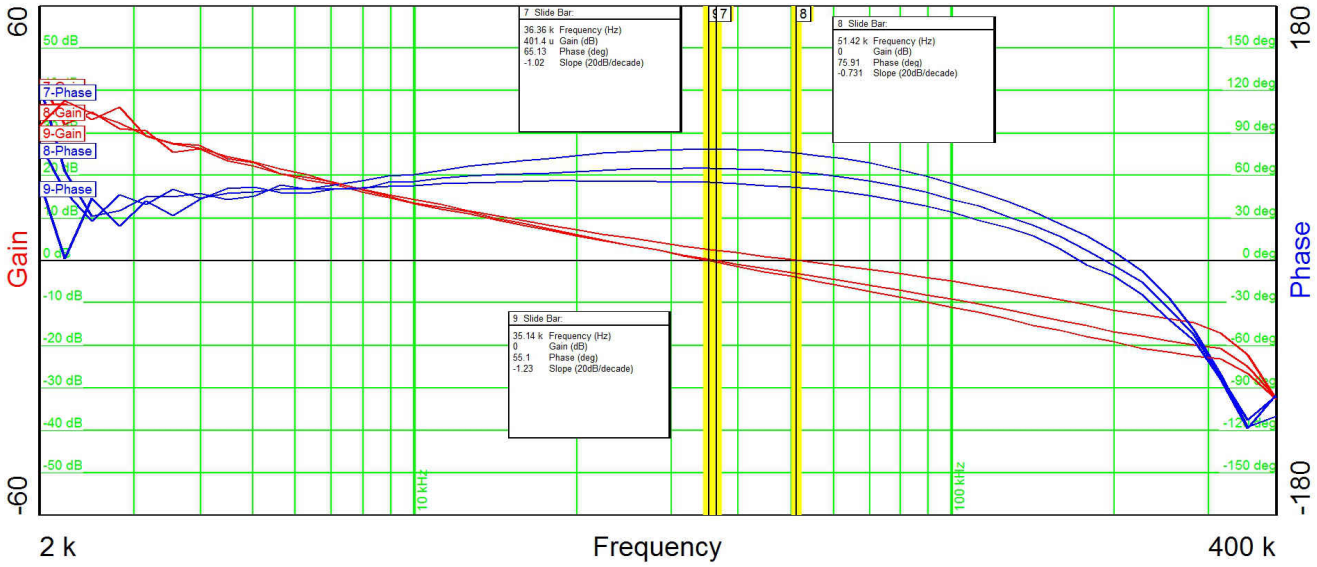


Figure 2-2. Bode Plot

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures.

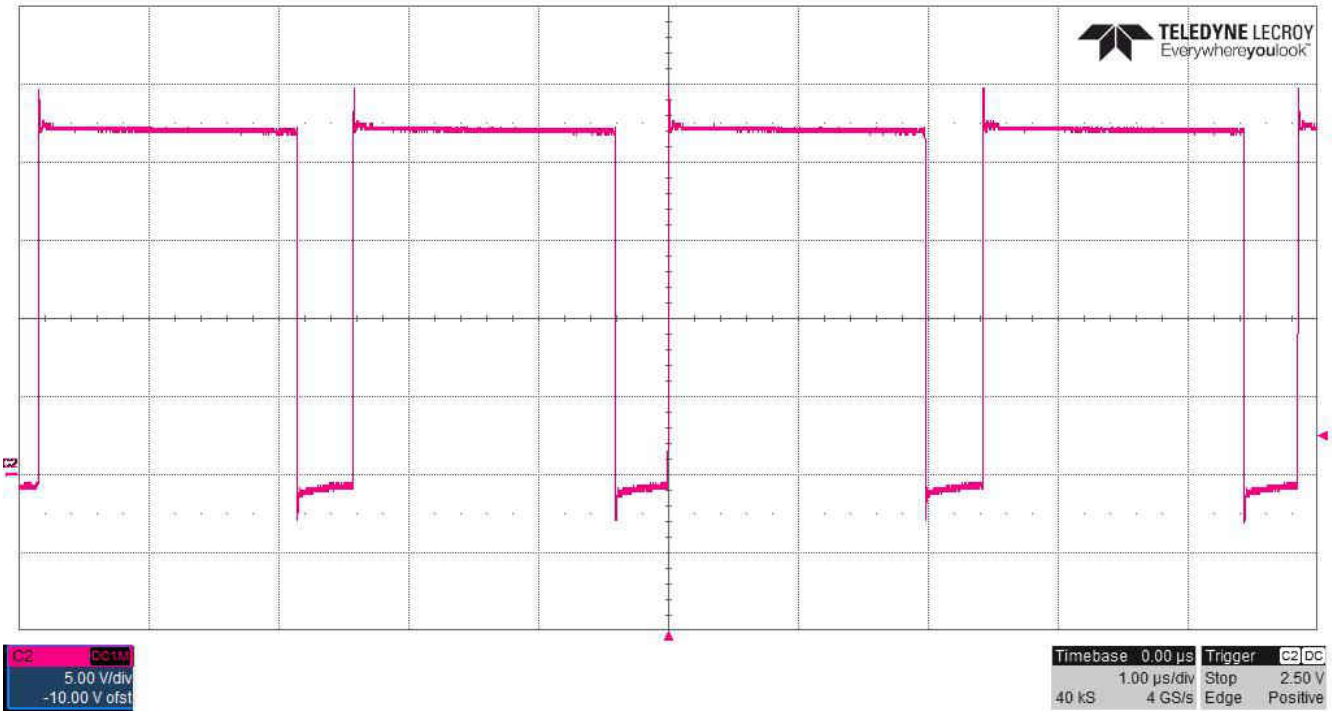


Figure 3-1. Primary FET Vds (U1 Pin 8) – 21.6 V_{IN}, Full Load

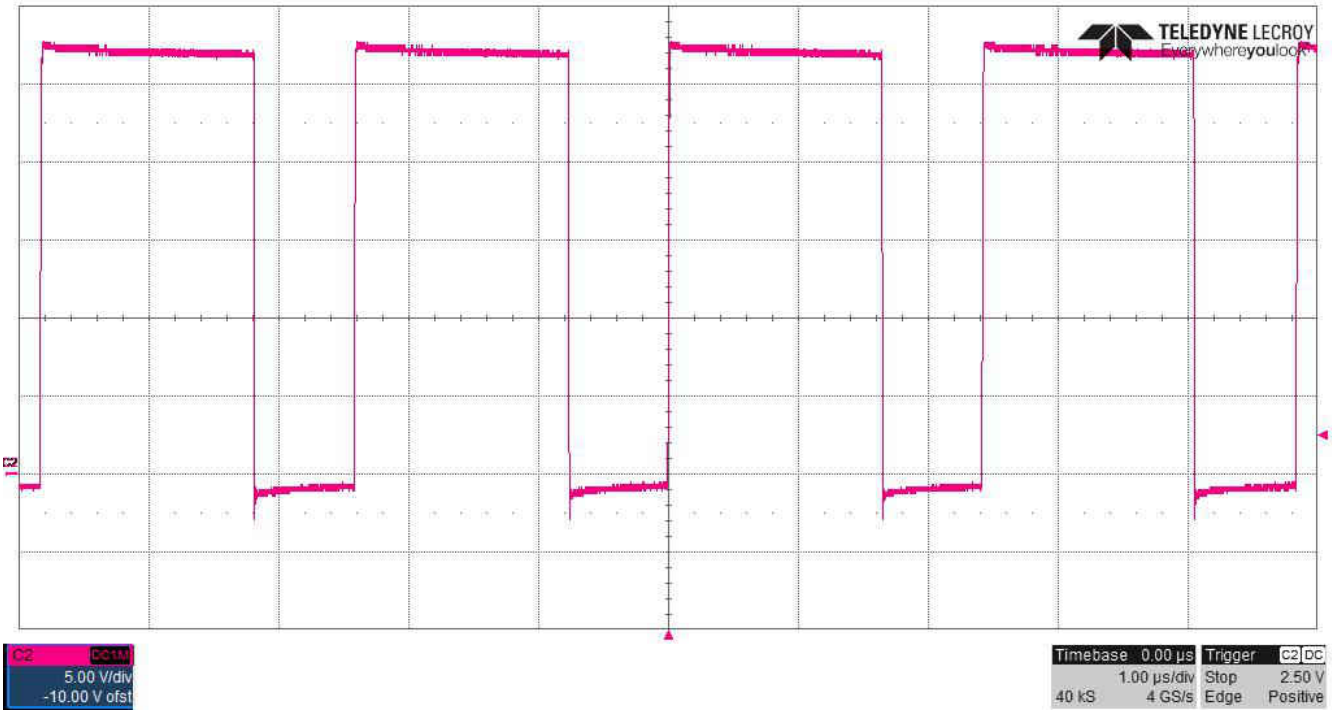


Figure 3-2. Primary FET Vds (U1 Pin 8) – 26.4 V_{IN}, Full Load

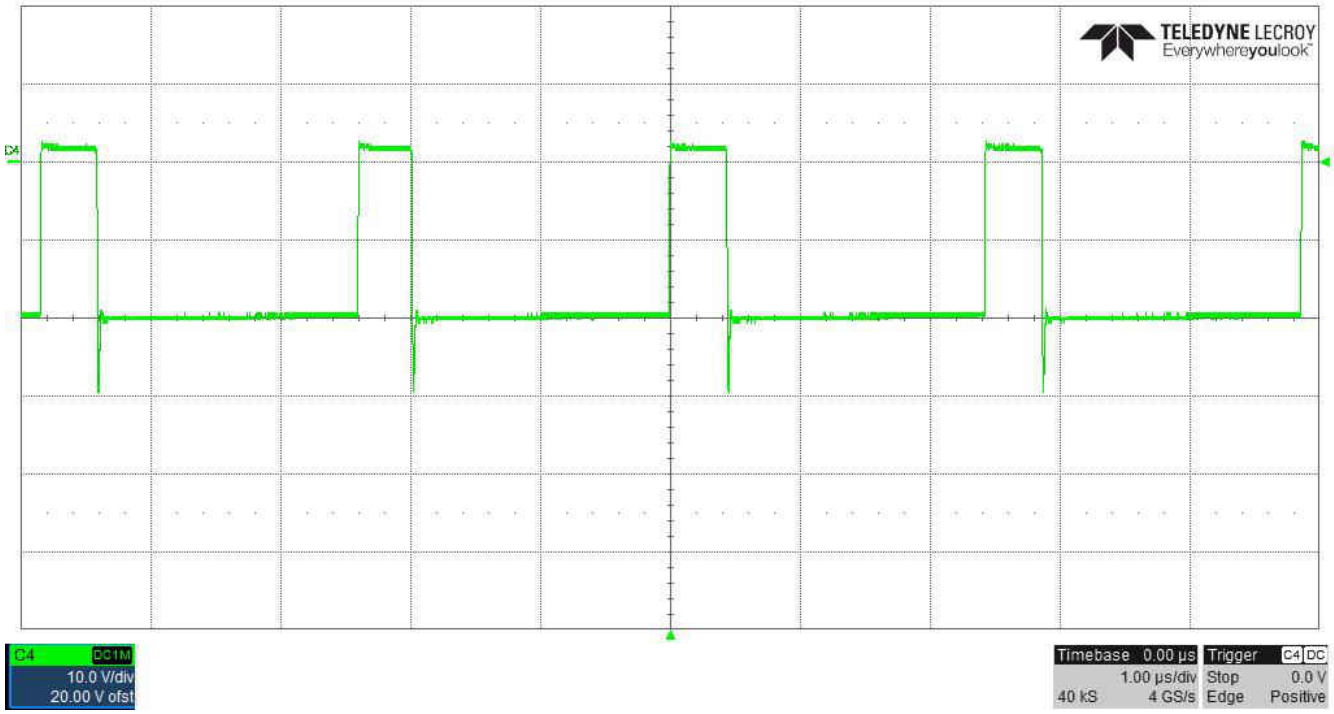


Figure 3-3. Diode (D4) – 21.6 V_{IN}, Full Load

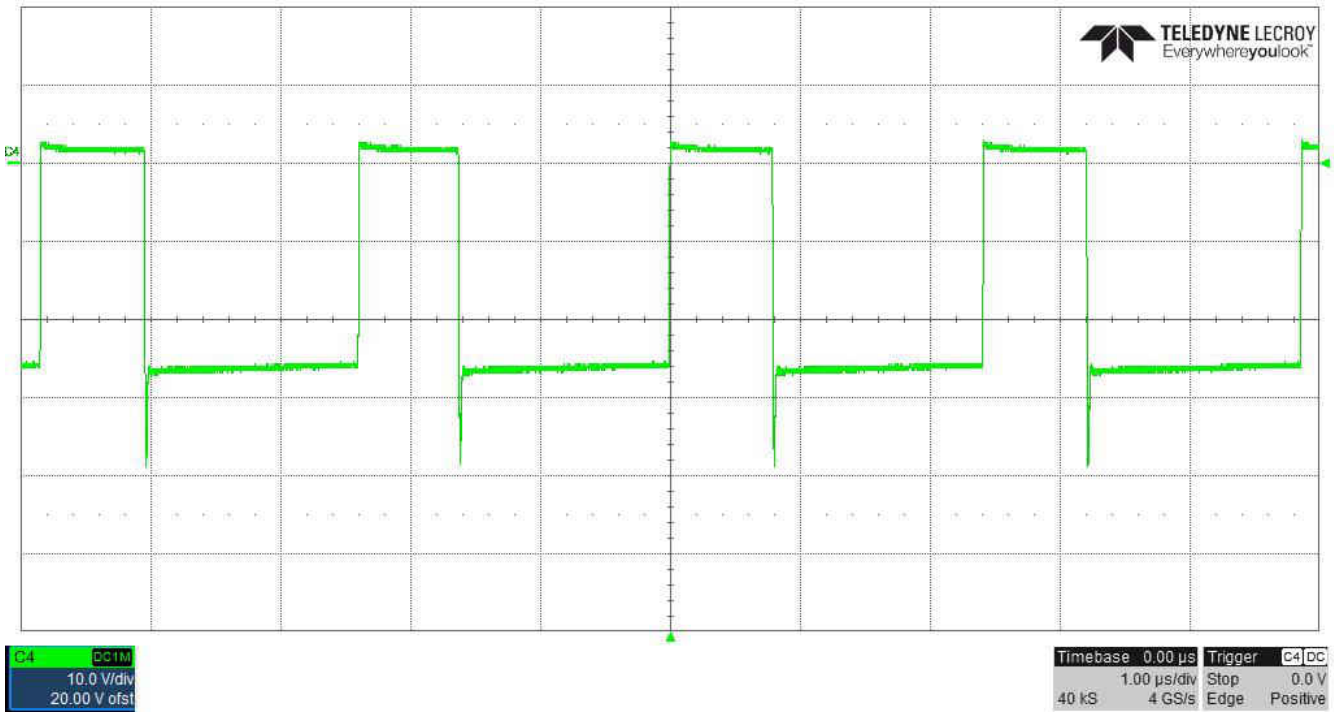


Figure 3-4. Diode (D4) – 26.4 V_{IN}, Full Load

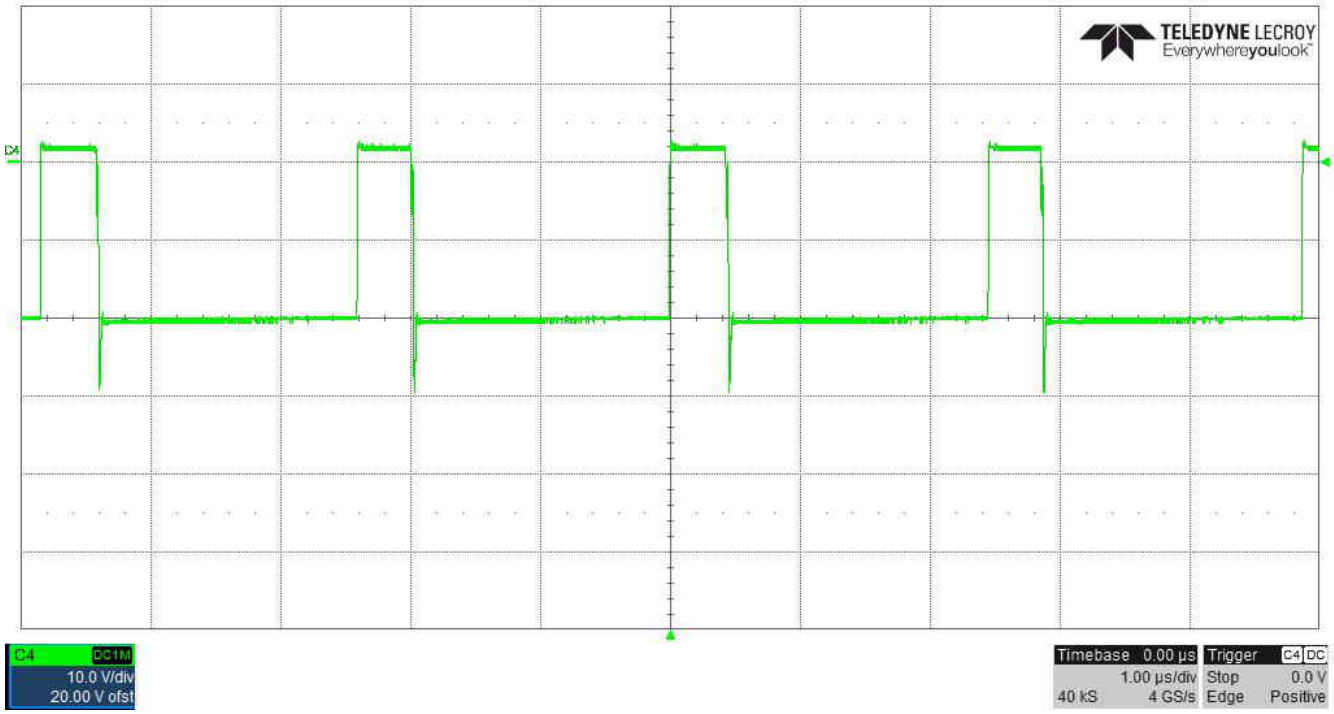


Figure 3-5. Diode (D2) – 21.6 V_{IN}, Full Load

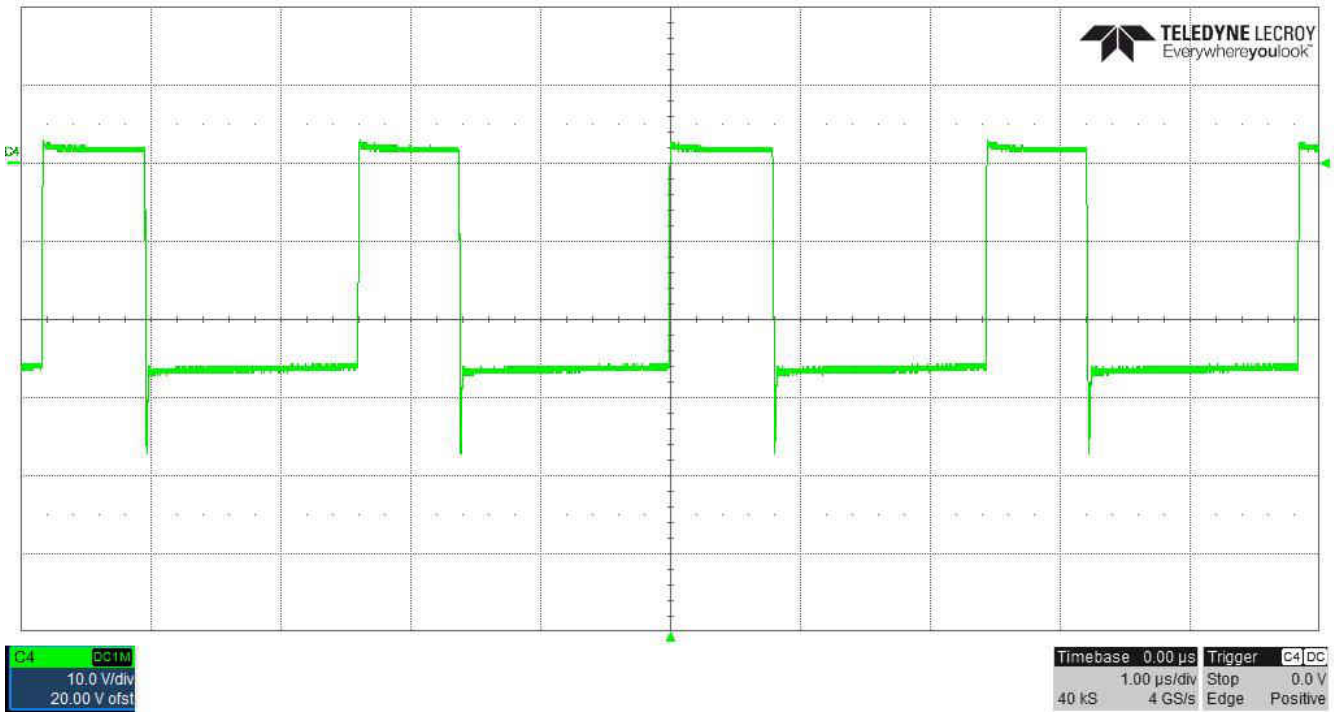


Figure 3-6. Diode (D2) – 26.4 V_{IN}, Full Load

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

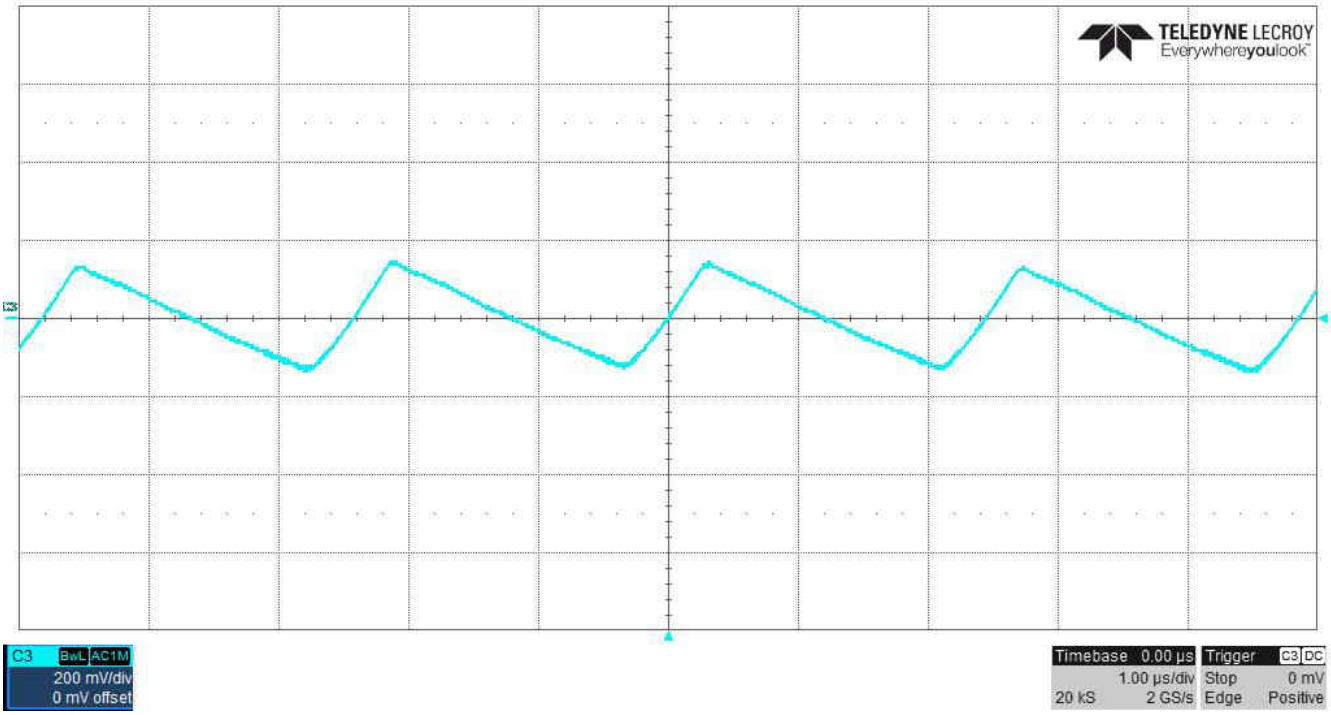


Figure 3-7. 24-V Input, V_{OUT1}, Maximum Load

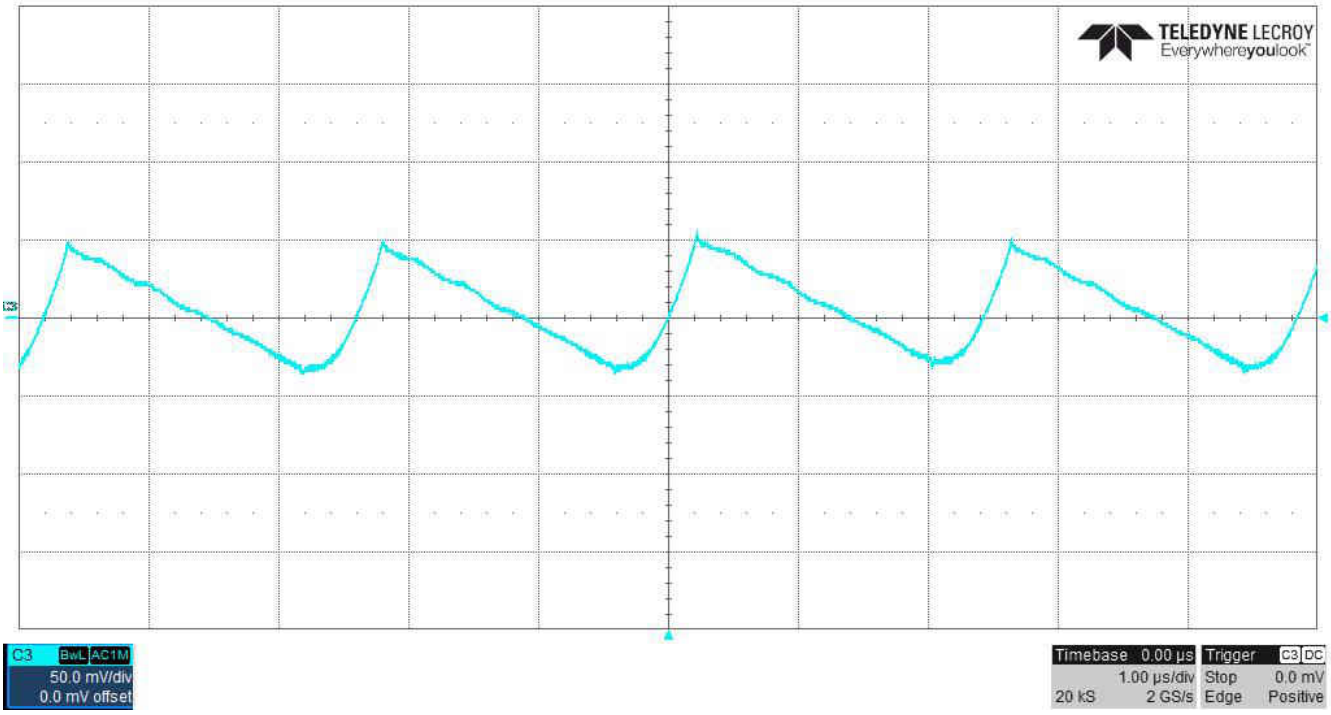


Figure 3-8. 24-V Input, V_{OUT2}, Maximum Load

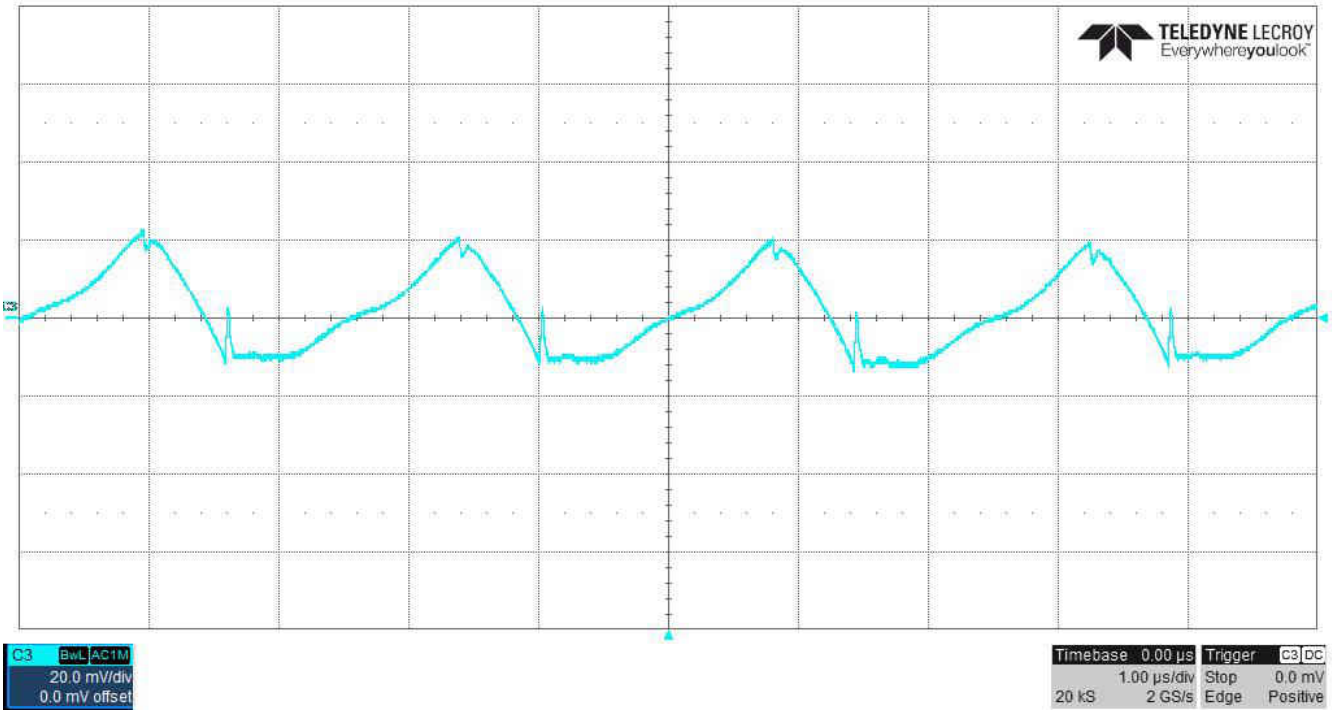
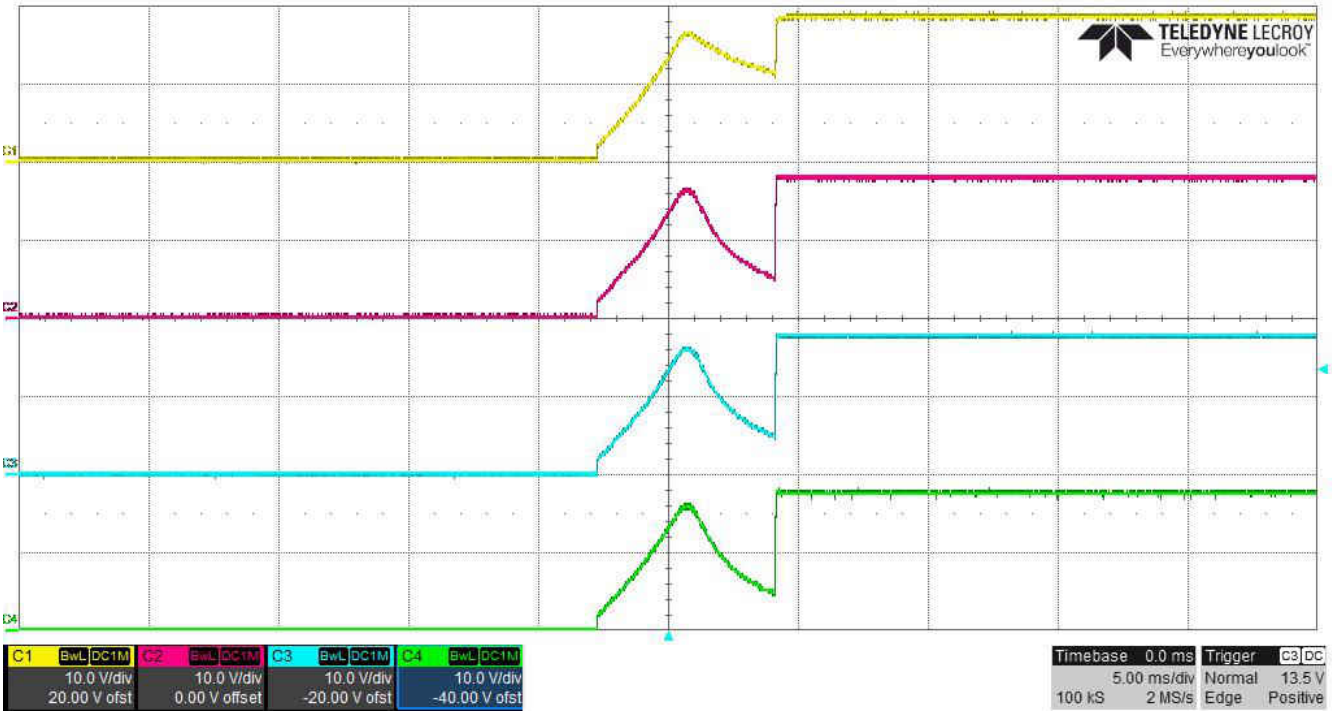


Figure 3-9. 24-V Input, V_{REG}, Maximum Load

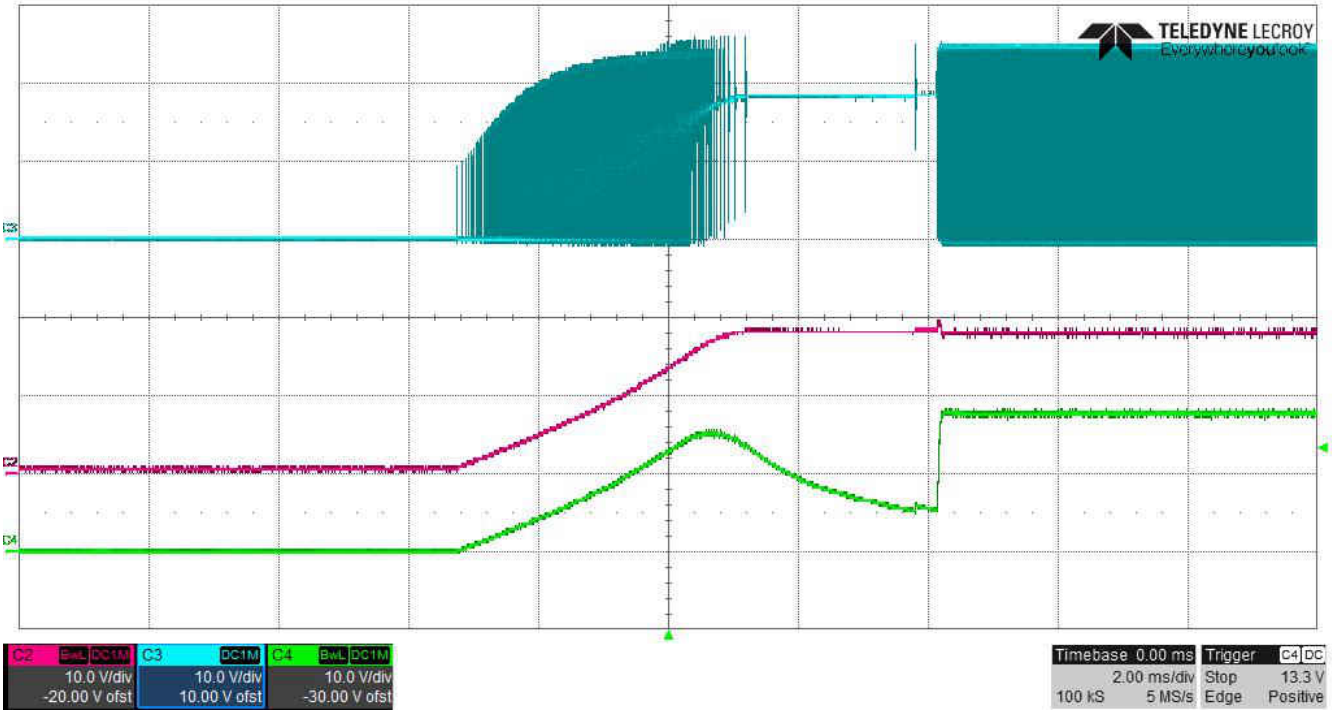
3.3 Start-Up Sequence

Start-up behavior is shown in the following figures.



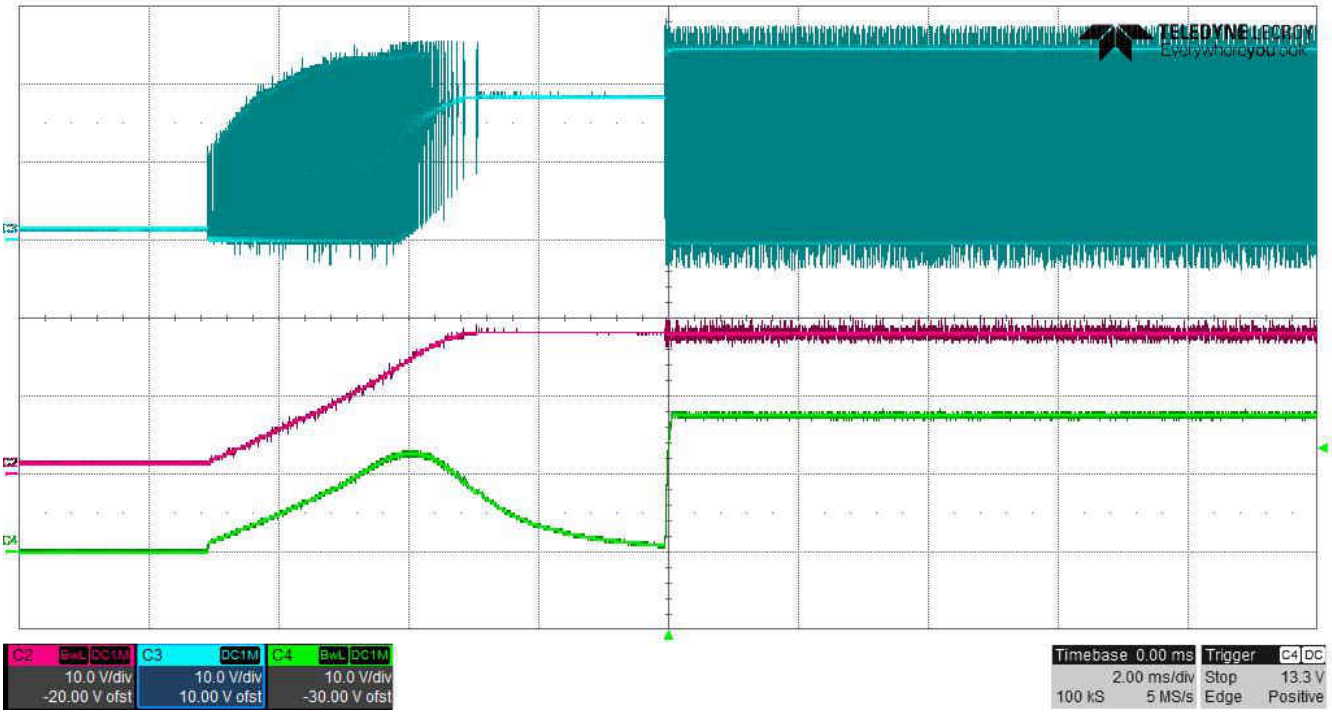
Yellow (C1) = V_{OUT1}; Pink (C2) = V_{OUT2}; Blue (C3) = V_{OUT3}; Green (C4) = V_{OUT4}

Figure 3-10. 24-V Input, No Load



Blue (C3) = Vds; Pink (C2) = V_{REG}; Green (C4) = V_{OUT4}

Figure 3-11. 24-V Input, No Load



Blue (C3) = Vds; Pink (C2) = V_{REG}; Green (C4) = V_{OUT4}

Figure 3-12. 24-V Input, Full Load

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