Test Report: PMP31139

Tiny Auxiliary SEPIC Converter Reference Design

Description

This reference design is a small SEPIC converter using the LM5158 device with integrated FET. The main design concern is using the smallest possible board space – setting the switching frequency to 2-MHz which means accepting some switching losses, accepting some magnetizing losses, but maintaining efficiency up to 400 mA at ≥ 80%.

Though the design has been tested up to 800-mA peak load, be aware that the continuous output is limited to 400 mA by thermal interface. Due to a pulsed load, the loop has been squeezed to the maximum bandwidth to enable the lowest output capacitance.

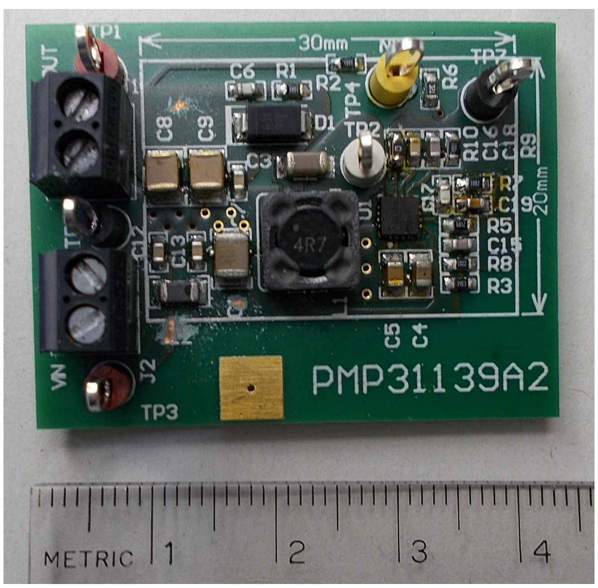
A small RF filter to prevent FM band noise is included, with a total solution size of 30 mm × 20 mm by using a two layer board, single side assembly, and a solid ground plane.

Features

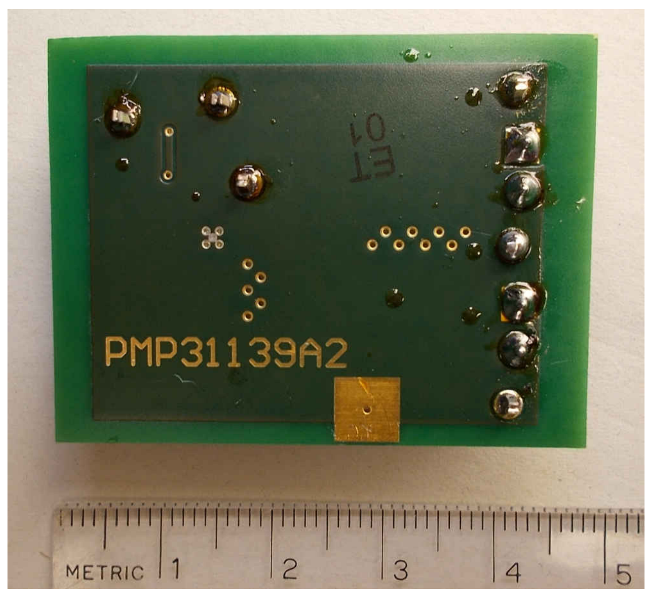
- Tiny footprint, highly-integrated, ideal for space-constrained applications
- Small FM filter and dual random spectrum are for EMI mitigation
- The design is thoroughly tested

Applications

- Intelligent antenna module
- Aftermarket telematics
- Telematics control unit
- Smart telematics gateway



Top Photo



Bottom Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	8 V to 18 V (36-V load dump)
Output Voltage	12 V at < 800 mA_{pk}, < 400 A_{avg}
Switching Frequency	2-MHz
Topology	SEPIC with LM5158-Q1

1.2 Considerations

When working with this design, remember the following conditions:

- The measured switching frequency is 1.95 MHz.
- The circuit starts to switch around 9.0 V and stops with switching around 7.3 V.
- Unless otherwise indicated, a variable resistor was used as pure resistive load.
- Measurements were done without random spread spectrum (R10 = 0R) to check switching waveforms at drain properly.

1.3 Dimensions

The outline of the board is 41.9 mm × 31.7 mm, including bulky jacks and some test points; the converter itself is 30 mm × 20 mm.

2 Testing and Results

2.1 Efficiency Graphs

Figure 2-1 shows the efficiency graph and Figure 2-2 shows the loss graph.

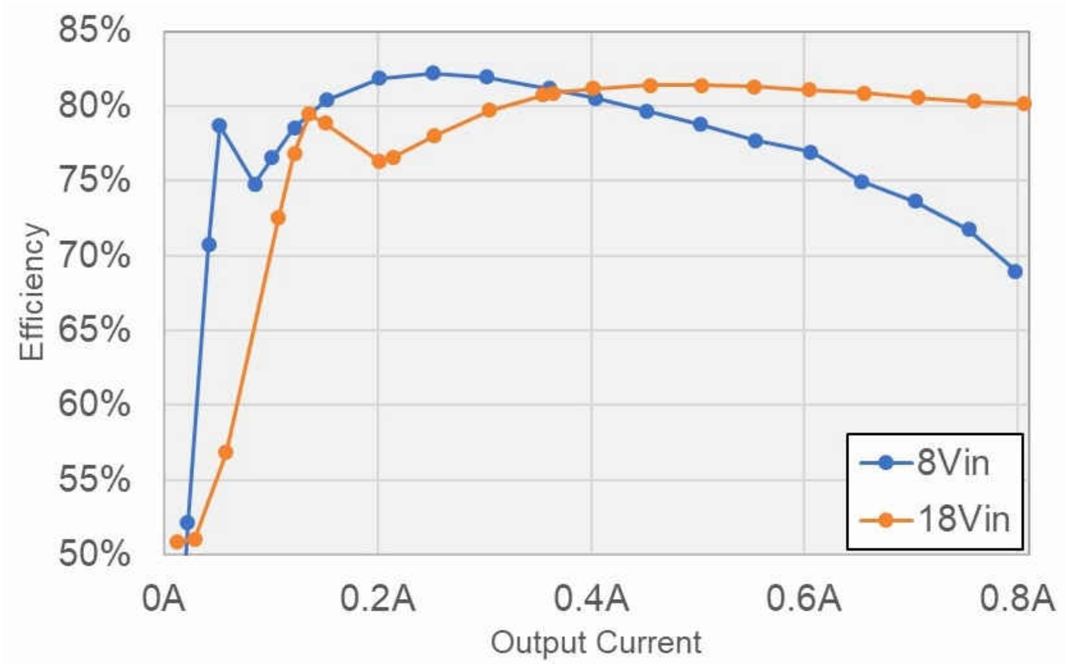


Figure 2-1. Efficiency Graph

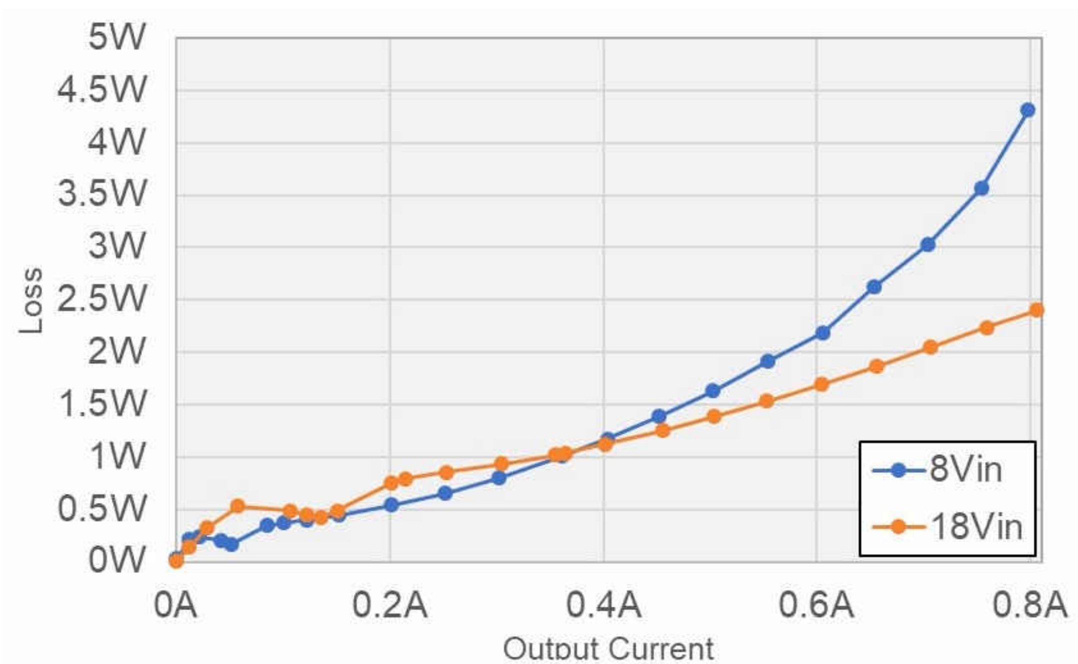


Figure 2-2. Loss Graph

2.2 Load Regulation

Figure 2-3 shows the output voltage versus output current load regulation graph.

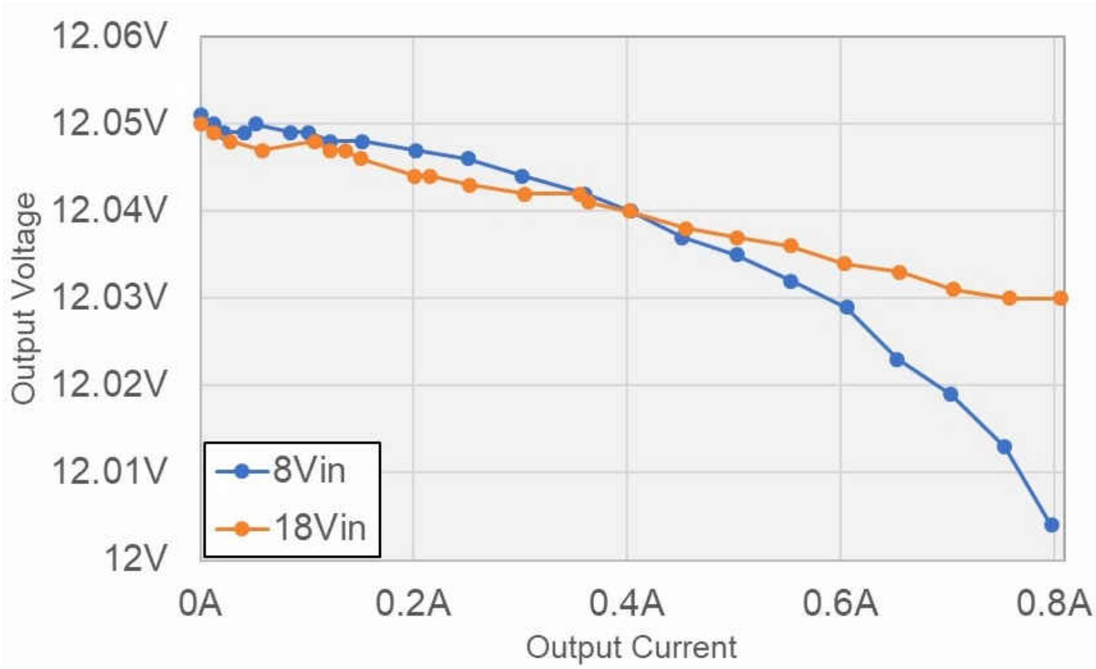


Figure 2-3. Output Voltage vs Output Current

2.3 Line Regulation

Figure 2-4 shows the line regulation output versus input voltage graph. Figure 2-5 shows the input voltage versus full load efficiency and loss graph.

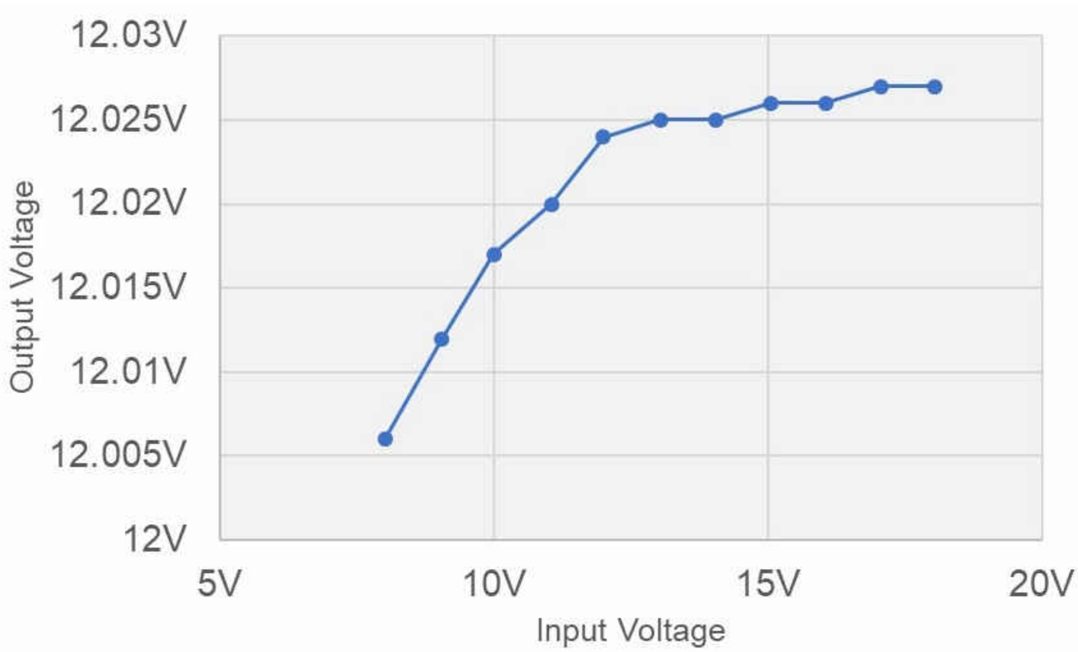


Figure 2-4. Output Voltage vs Input Voltage

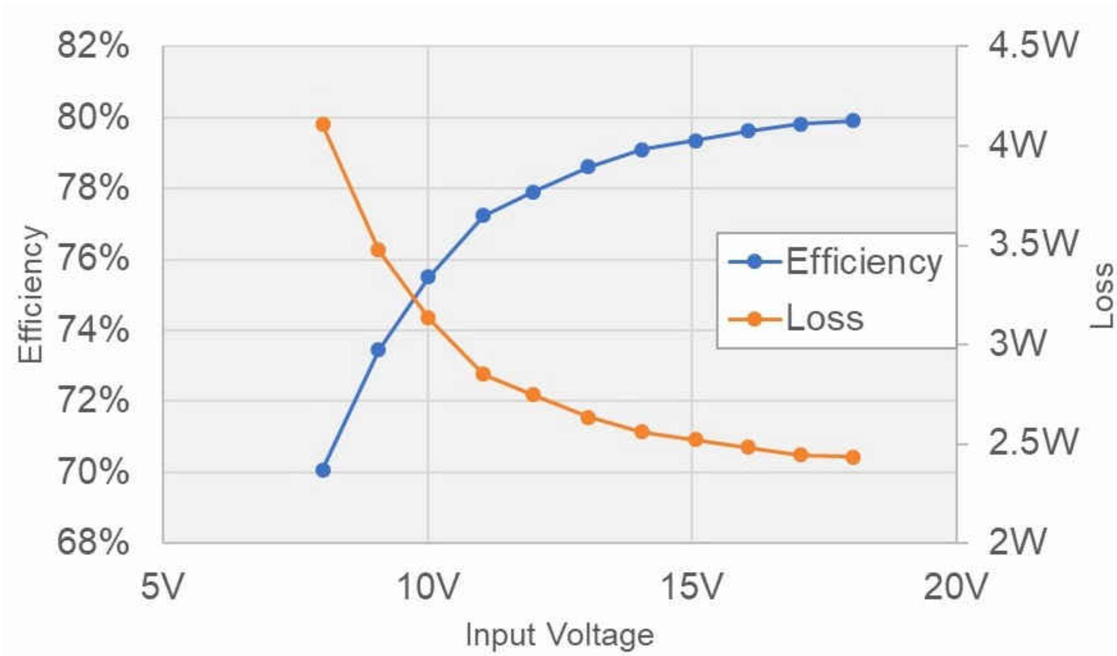


Figure 2-5. Efficiency and Loss vs Input Voltage

2.4 Thermal Images

2.4.1 8-V Input Voltage

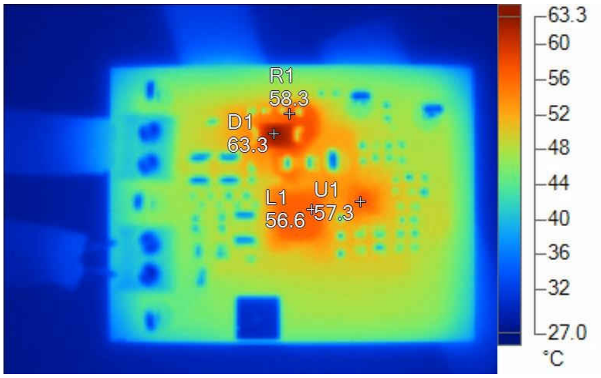


Figure 2-6. 0.4-A Output Current

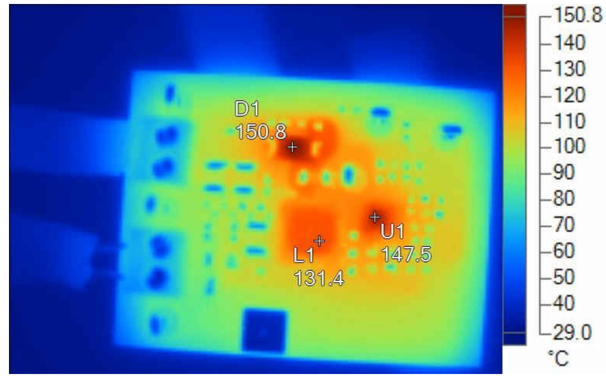


Figure 2-7. 0.8-A Output Current

Name	0.4 A Out	0.8 A Out
D1	63.3°C	150.8°C
L1	56.6°C	131.4°C
R1	58.3°C	
U1	57.3°C	147.5°C

2.4.2 18-V Input Voltage

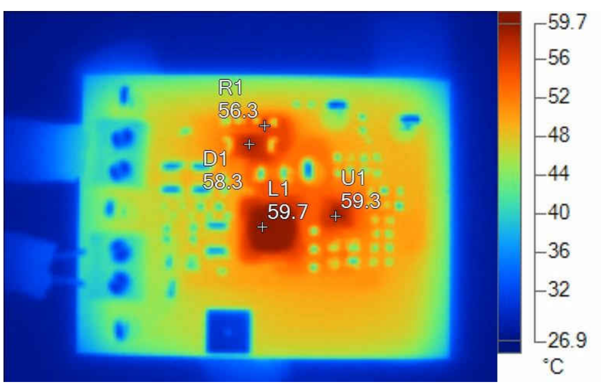


Figure 2-8. 0.4-A Output Current

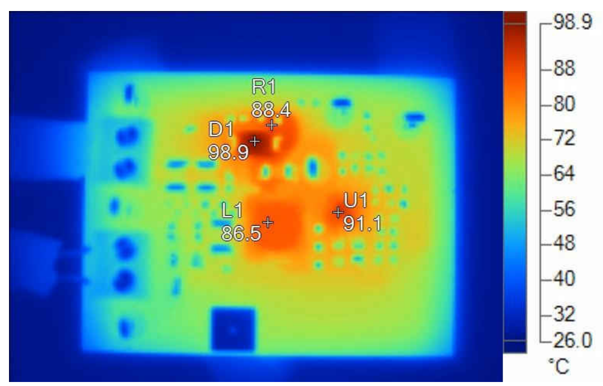


Figure 2-9. 0.8-A Output Current

Name	0.4 A Out	0.8 A Out
D1	58.3°C	98.9°C
L1	59.7°C	86.5°C
R1	56.3°C	88.4°C
U1	59.3°C	91.1°C

2.5 Bode Plots

Figure 2-10 and Figure 2-11 show the PMP31139 bode plots. R7 is reduced to 10 kΩ, C19 is increased to 22 nF – maximum loop bandwidth.

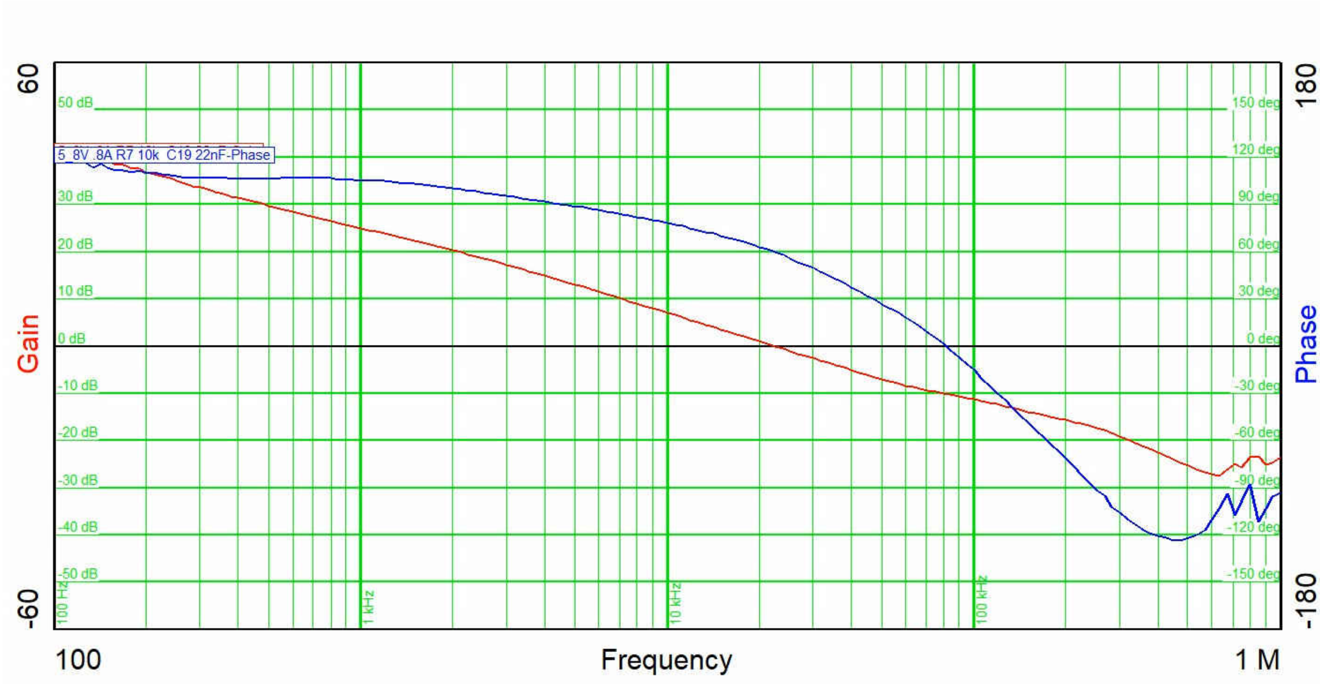


Figure 2-10. Bode Plot at 8-V_{IN} 0.8-A_{OUT}

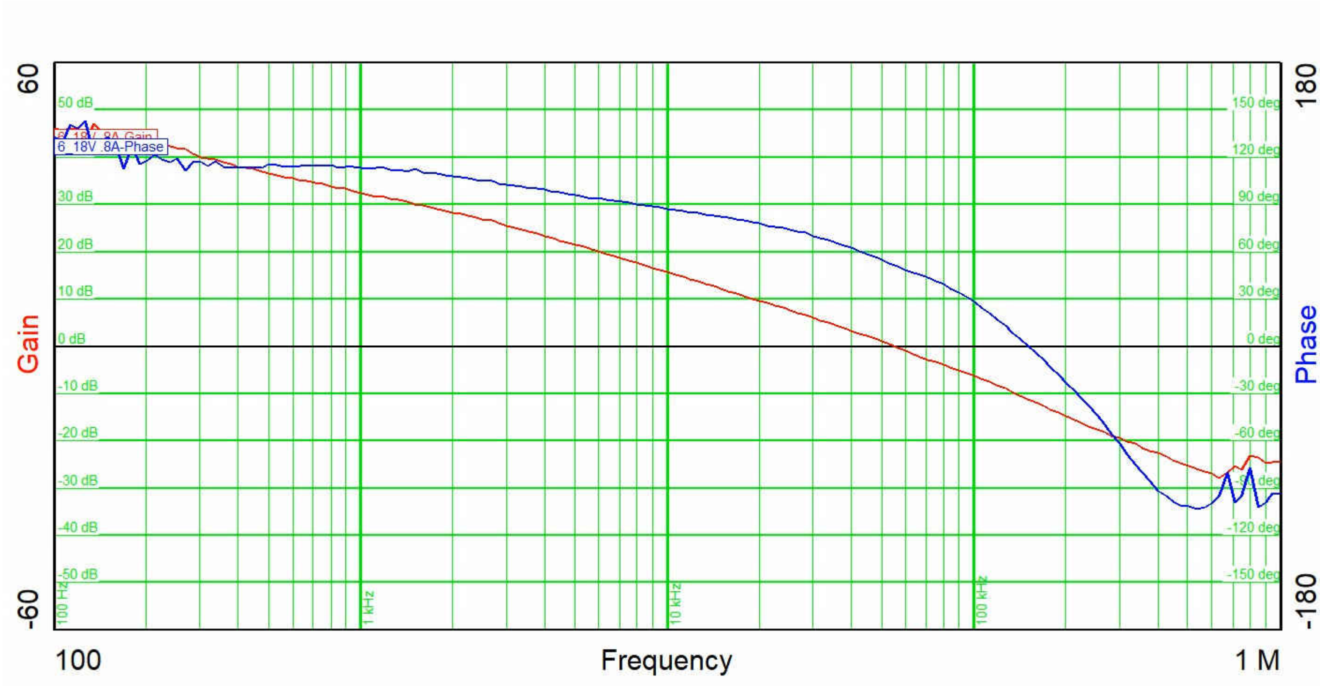


Figure 2-11. Bode Plot at 18 V_{IN}, 0.8 A_{OUT}

V_{IN}	8 V	18 V
Bandwidth (kHz)	22	55
Phase Margin	59.8°	51.5°
Slope (20 dB/decade)	–1	–1.5
Gain Margin (dB)	–10	–11
Slope (20 dB/decade)	–0.63	–1.5
Freq (kHz)	81	150

A loop modification is made, tuning the poles.

The gain of LM5158 increases at bigger input voltage, crossover frequency Fco = 55 kHz at 18-V input. To keep the loop bandwidth around 20 kHz at 8-V input voltage the two poles have been adjusted, RC corner frequency is set around 500 kHz, C17 = 33 pF and C18 = 4.7 pF.

The roll off of the phase has been stretched, achieving a better phase margin of 55 degrees,

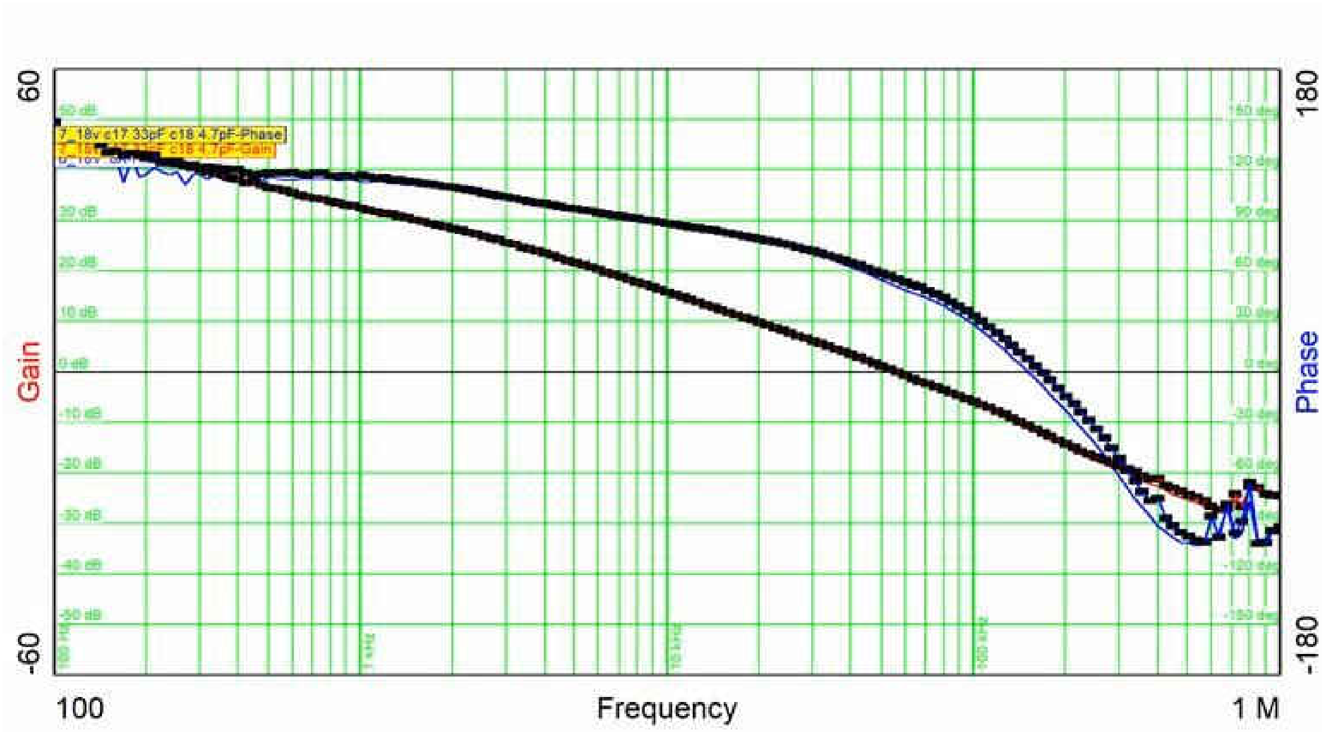


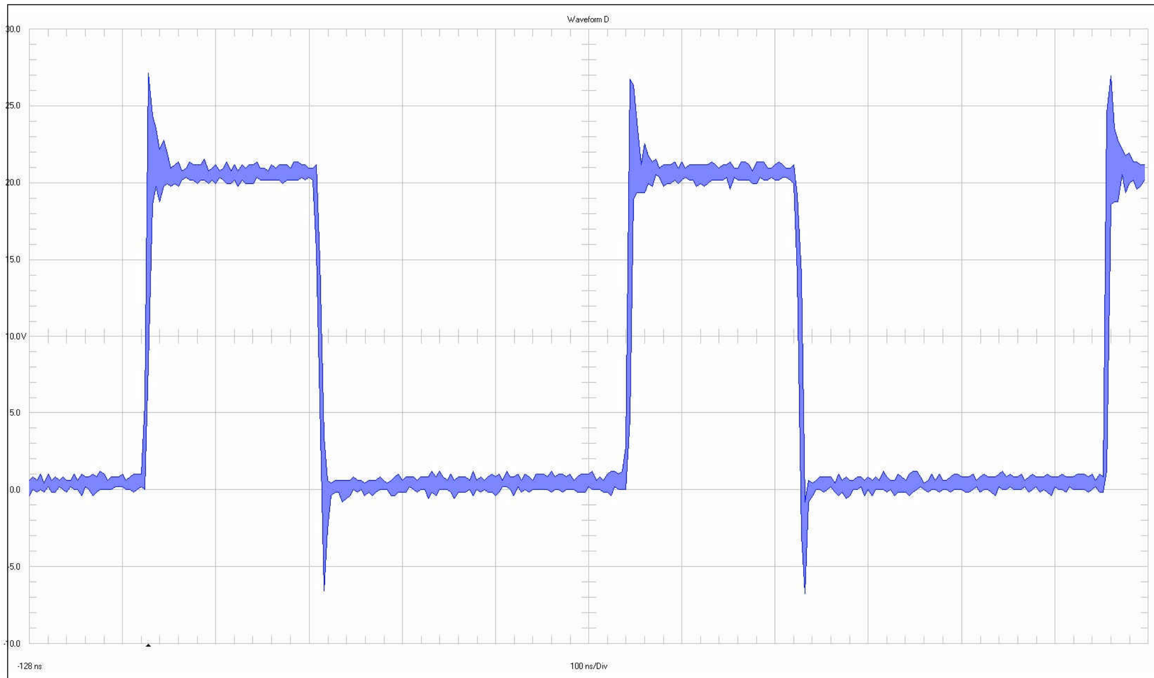
Figure 2-12. Bode Plot

	18 V_{IN}	**18 V_{IN} New**
Bandwidth (kHz)	55.0	55.9
Phase Margin	**51.5°**	**55.4°**
Slope (20 dB/decade)	–1.5	–1.2
Gain Margin (dB)	–11.0	–11.9
Slope (20 dB/decade)	–1.50	–1.44
Freq (kHz)	150	167

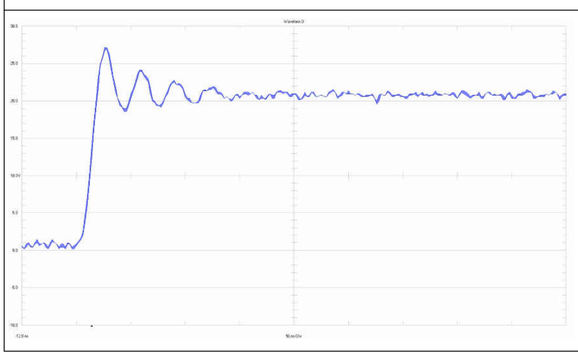
3 Waveforms

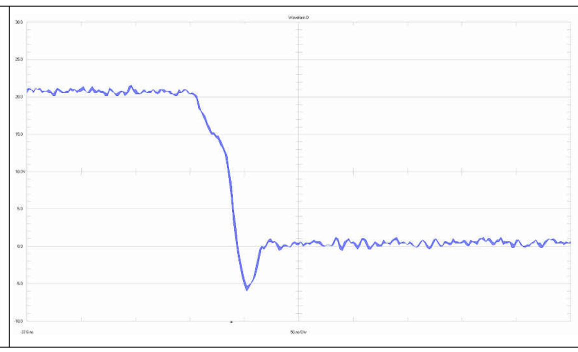
3.1 Switching

The switching waveforms are illustrated in the following images.



CH1 ⇒ 5-V / div,
100-ns / div,
full bandwidth





CH1 ⇒ 100-ns
full scale

Figure 3-1. Switch Node (TP2 to GND), 8-V Input Voltage

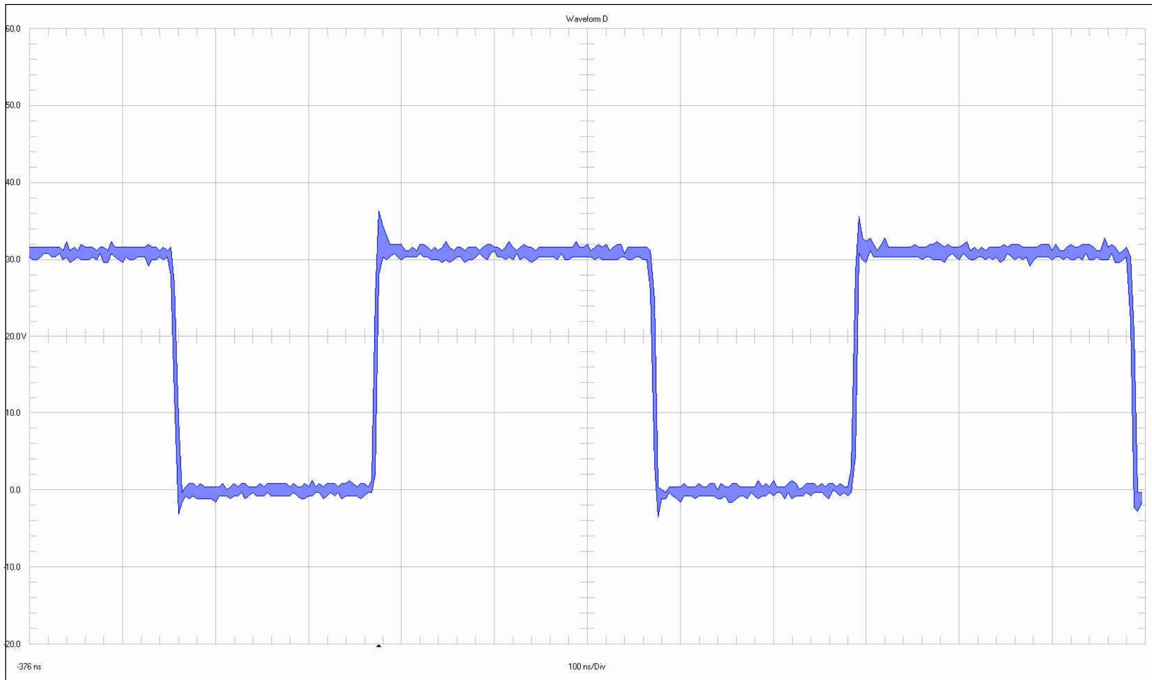
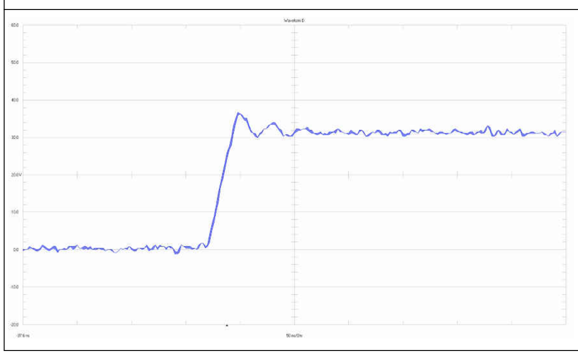
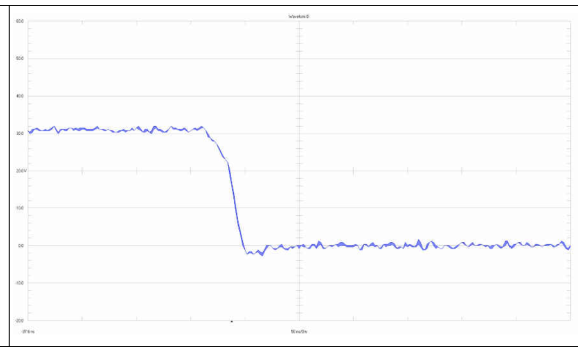
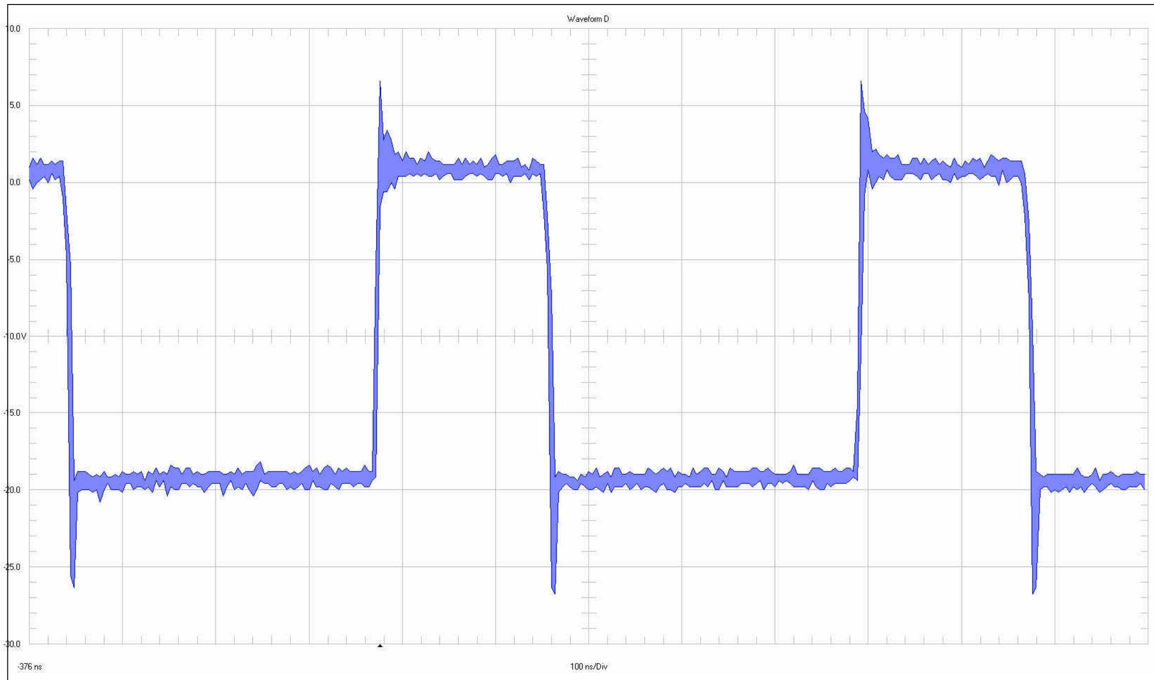
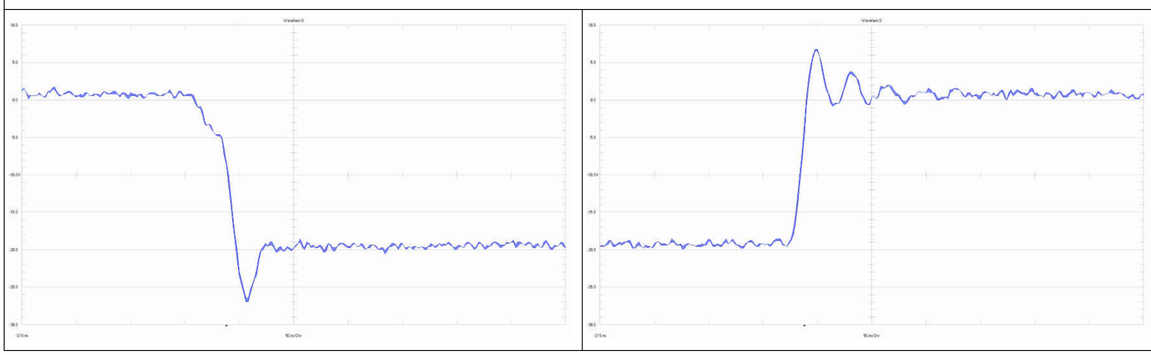
<table>
<tr><td>
</td><td colspan="1">CH1 ⇒ 10 V / div
100-ns / div
full bandwidth</td></tr>
<tr><td> </td><td>CH1 ⇒ 100-ns
full scale</td></tr>
</table>

Figure 3-2. Switch Node (TP2 to GND), 18-V Input Voltage



CH1 ⇒ 5 V / div
100 ns /div
full bandwidth



CH1 ⇒ 100-ns
full scale

Figure 3-3. D1 to V_{OUT}, 8-V Input Voltage

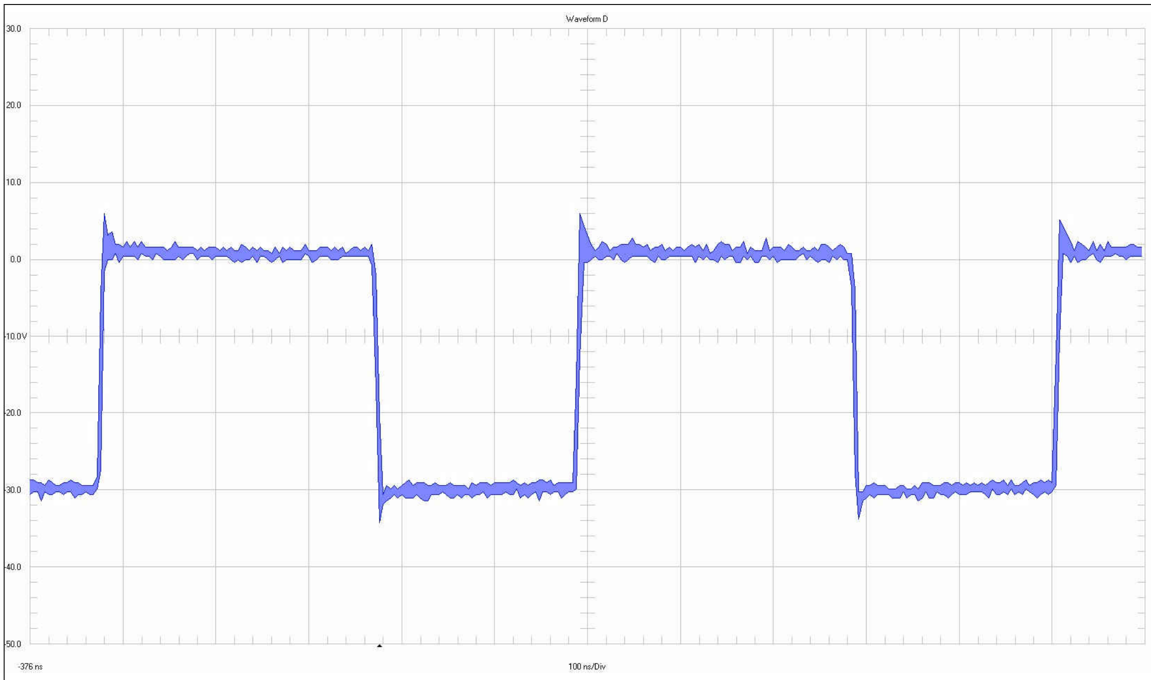
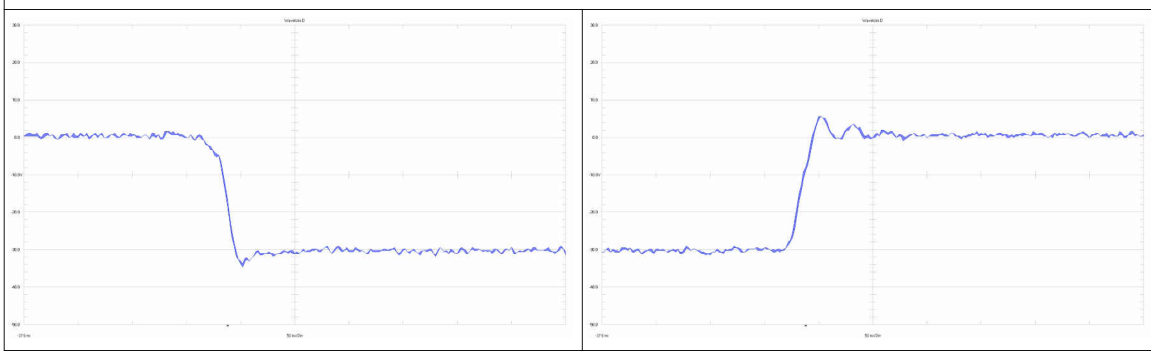
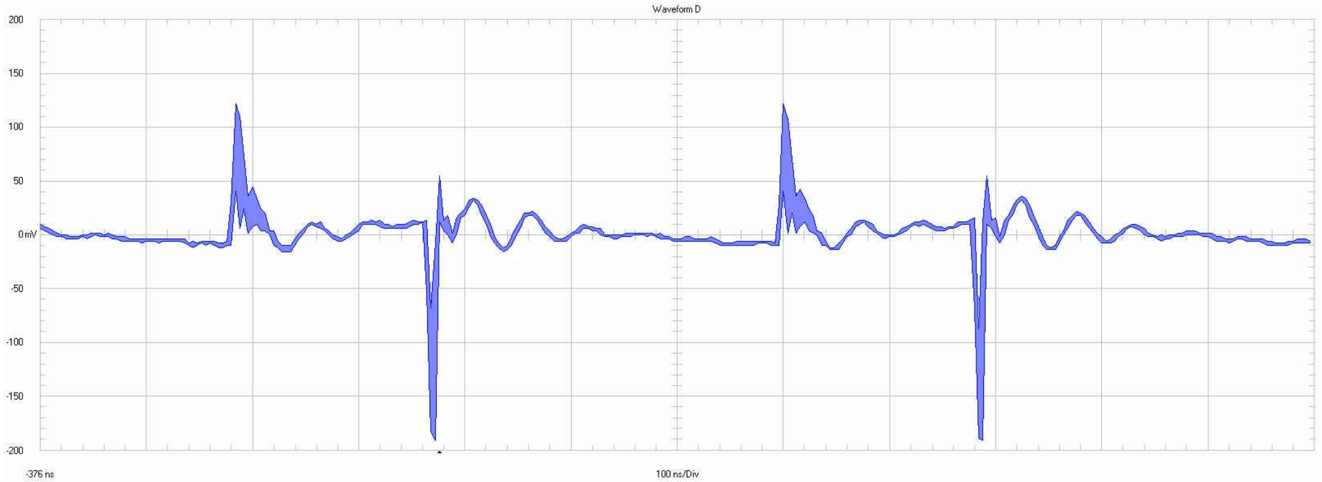
	CH1 ⇒ 10 V / div 100 ns /div full bandwidth
	CH1 ⇒ 100-ns full scale

Figure 3-4. D1 to V_{OUT}, 18-V Input Voltage

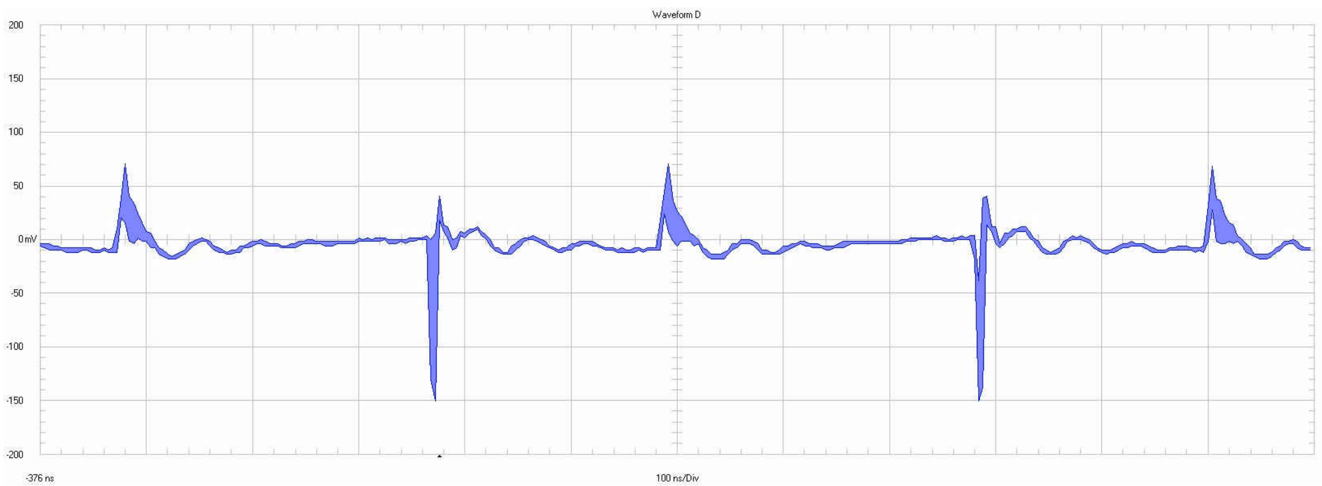
3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.



50 mV / div, 100 ns / div, 20-MHz bandwidth

Figure 3-5. Output Voltage Ripple at 8-V Input Voltage

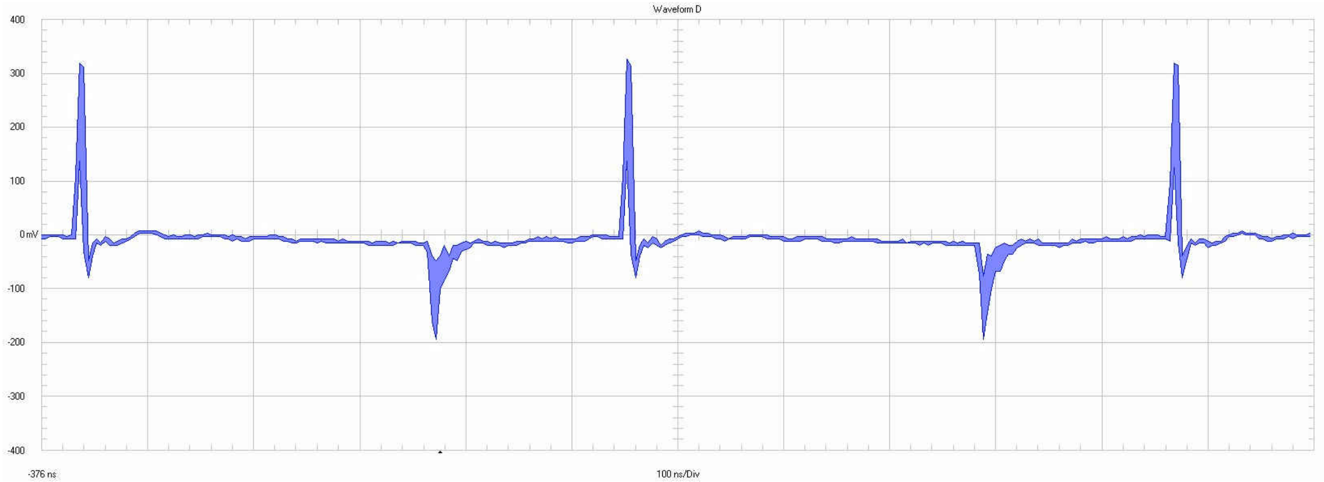


50 mV / div, 100 ns / div, 20 MHz bandwidth

Figure 3-6. Output Voltage Ripple at 18-V Input Voltage

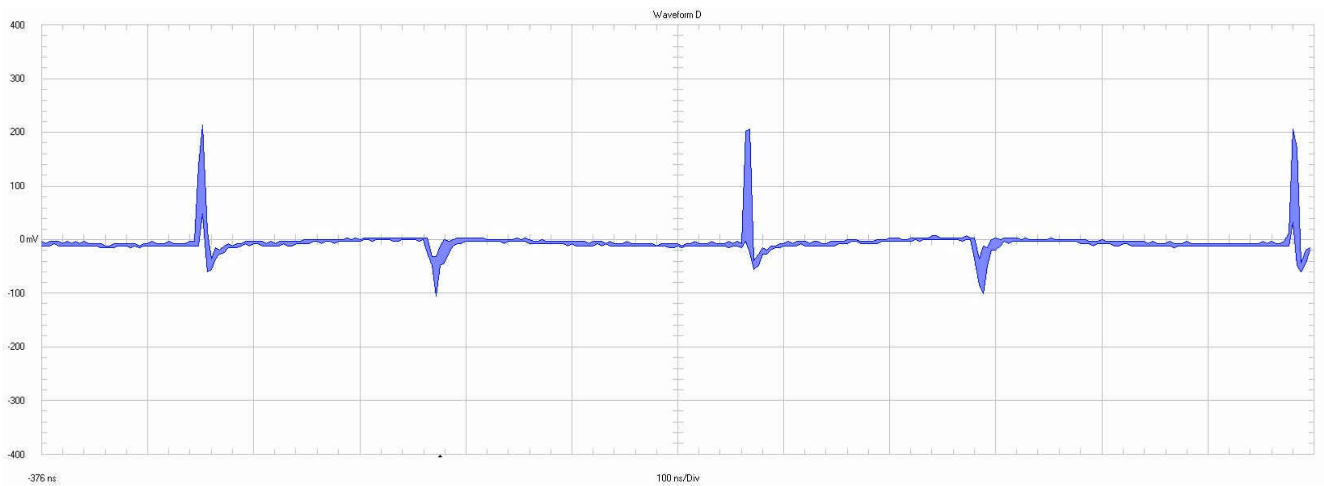
3.3 Input Voltage Ripple

Input voltage ripple is shown in the following figures.



100 mV / div, 100 ns / div, 20-MHz bandwidth

Figure 3-7. Input Voltage Ripple at 8-V_{IN}



100 mV / div, 100 ns / div, 20-MHz bandwidth

Figure 3-8. Input Voltage Ripple at 18-V_{IN}

3.4 Load Transients

Load transient response is shown in the following figures.

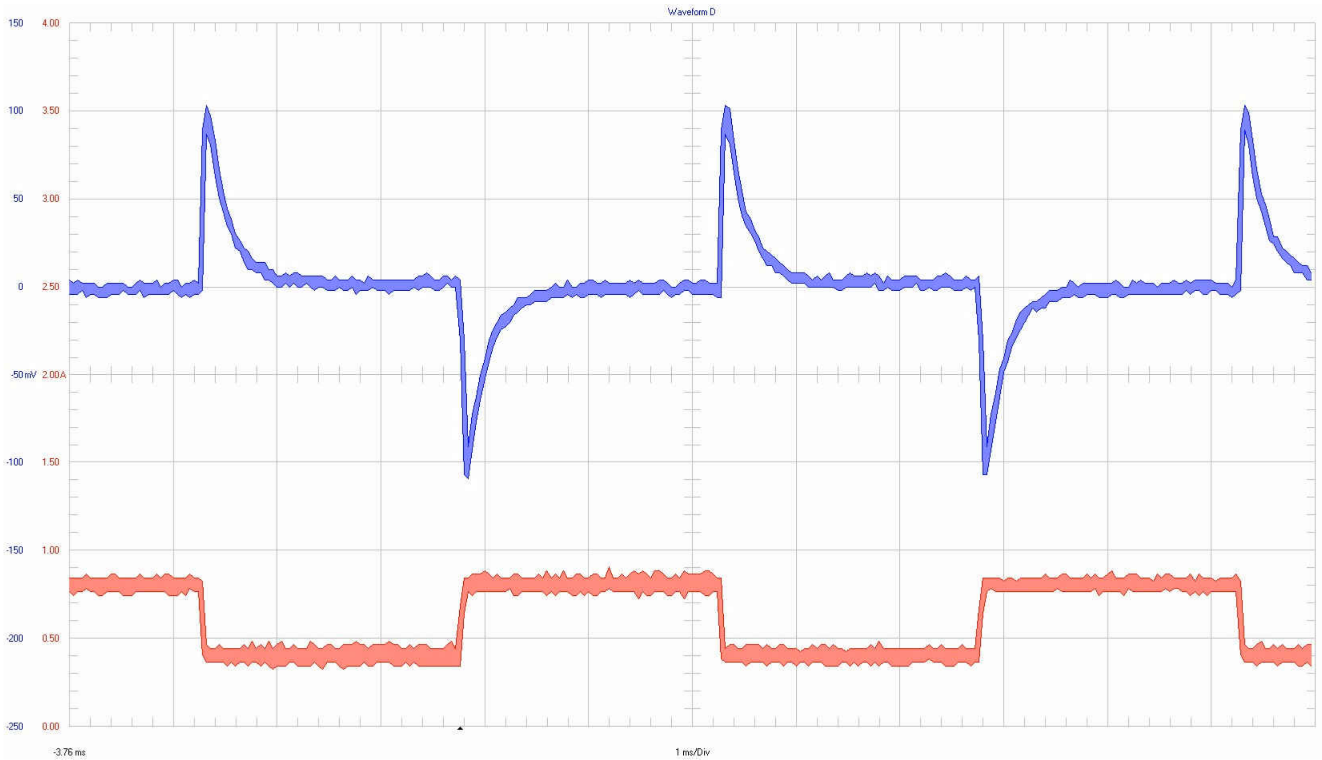


Figure 3-9. Transient 0.4 A to 0.8 A at 8-V Input Voltage

V_{OUT}

- 50 mV / div
- 10-kHz bandwidth

I_{OUT}

- 0.5 A / div
- full bandwidth

1 ms / div

- excellent transient response 1% of output voltage

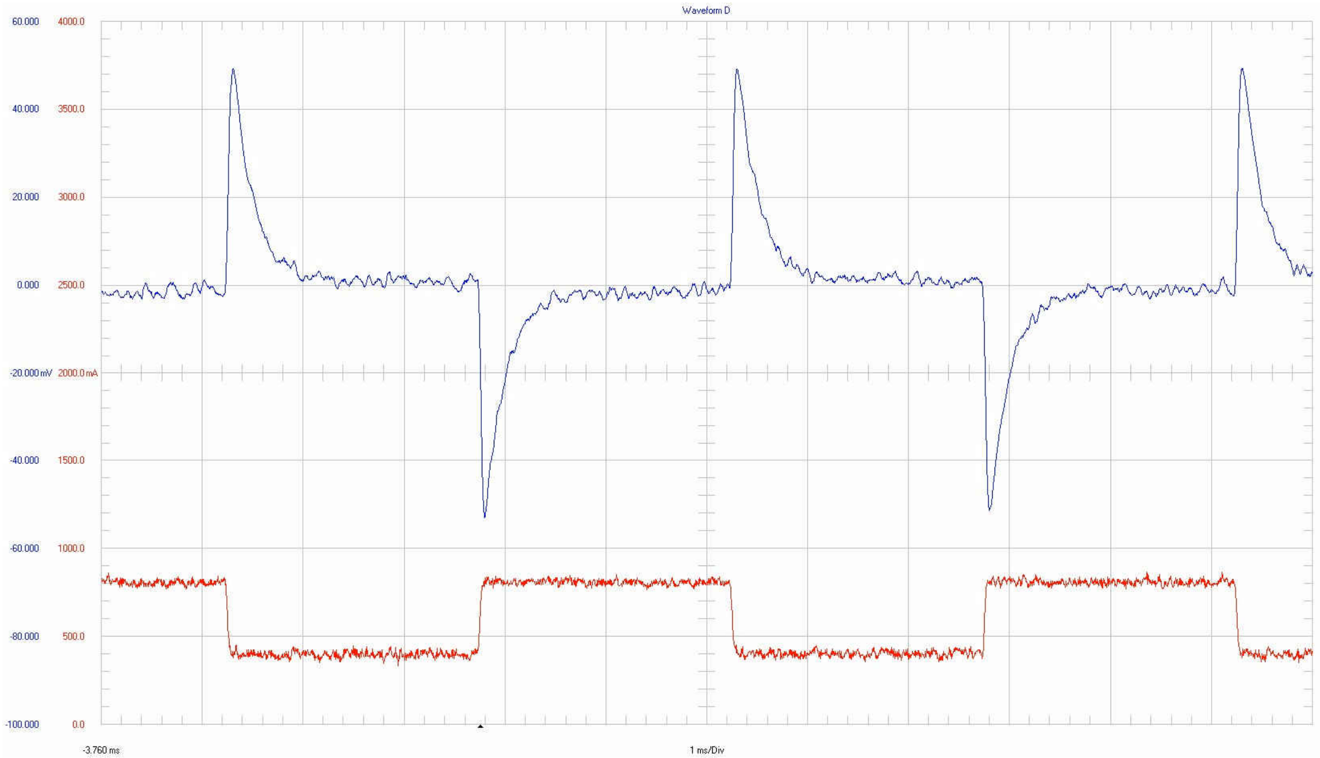


Figure 3-10. Transient 0.4 A to 0.8 A at 18-V Input Voltage

V_{OUT}

- 20 mV / div
- 10-kHz bandwidth

I_{OUT}

- 0.5 A / div
- full bandwidth

1 ms / div

3.5 Start-Up Sequence

Start-up behavior is shown in the following figures.

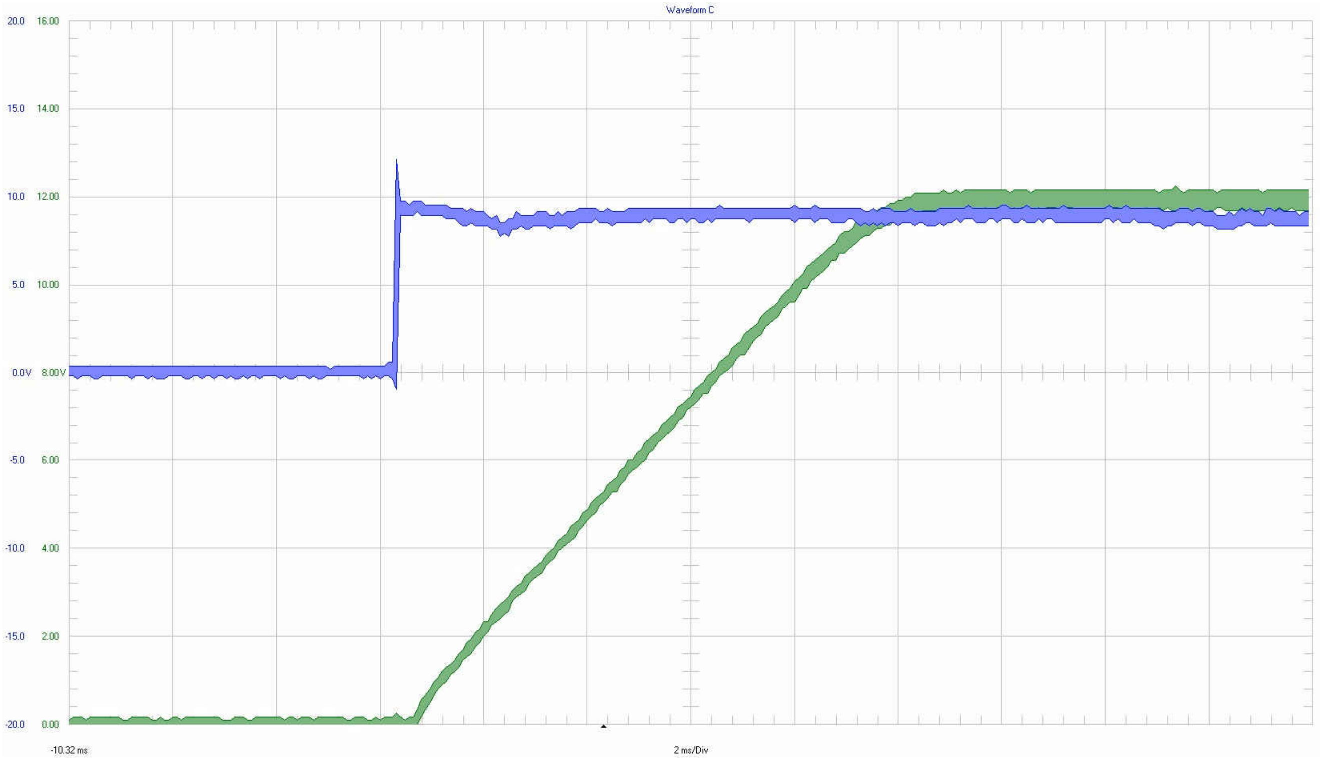


Figure 3-11. 9-V Input Voltage (UVLO set to 9.0 V ON and 7.3 V OFF)

V_{IN} (blue curve)

- 5-V / div
- 20-MHz bandwidth

V_{OUT}

- 2 V / div
- 20-MHz bandwidth

2 ms / div

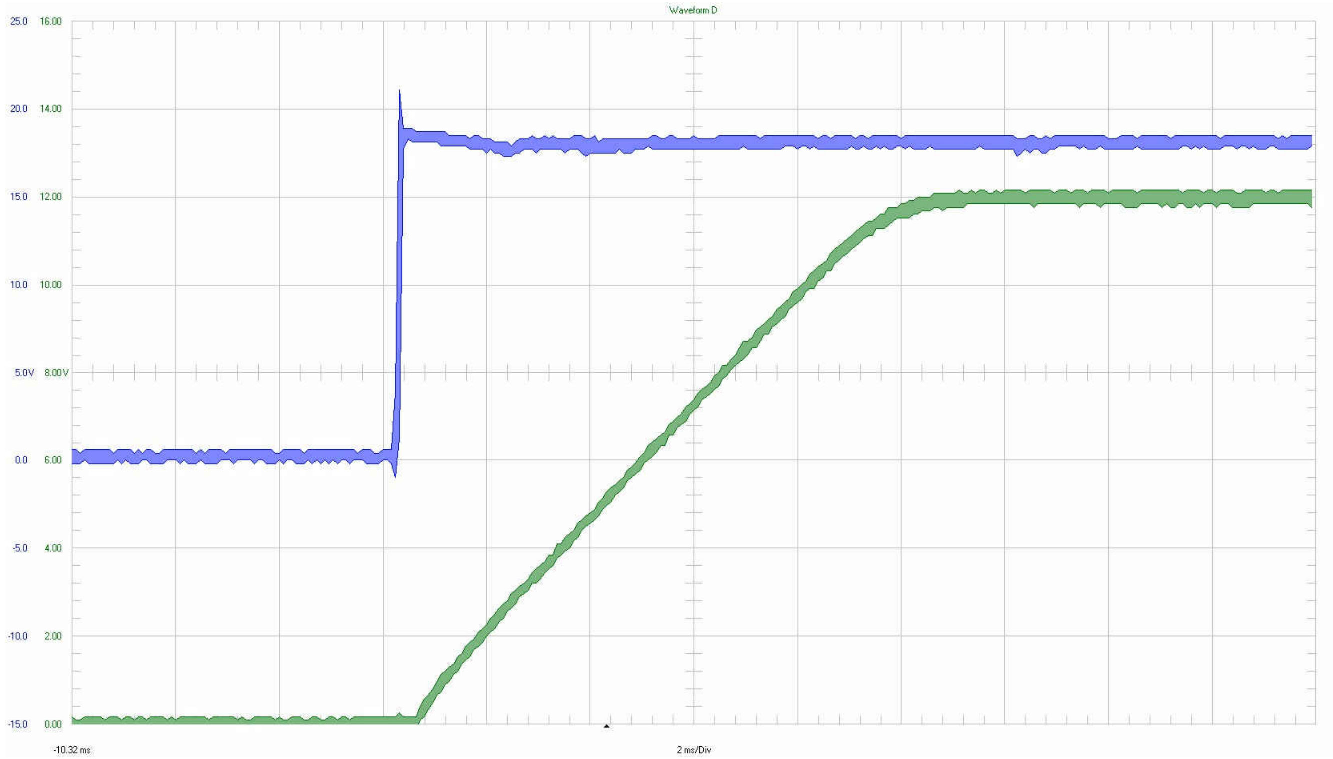


Figure 3-12. Start-up at 18-V Input Voltage

V_{IN} (blue curve)

- 5-V / div
- 20-MHz bandwidth

V_{OUT}

- 2 V / div
- 20-MHz bandwidth

2 ms / div

3.6 Shutdown Sequence

The following waveforms shows the shutdown sequence for this reference design.

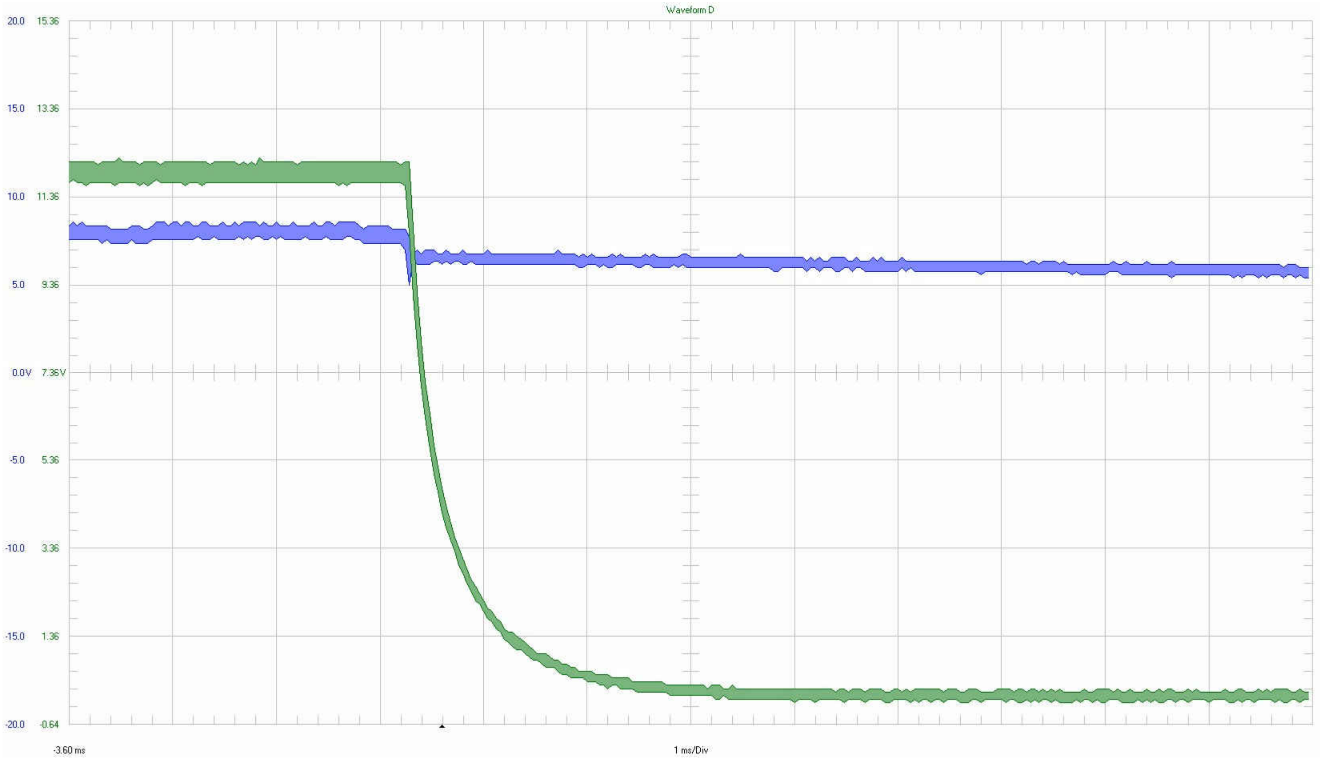


Figure 3-13. Shutdown at 8-V Input Voltage

V_{IN} (blue curve)

- 5 V / div
- 20-MHz bandwidth

V_{OUT}

- 2 V / div
- 20-MHz bandwidth

1 ms / div

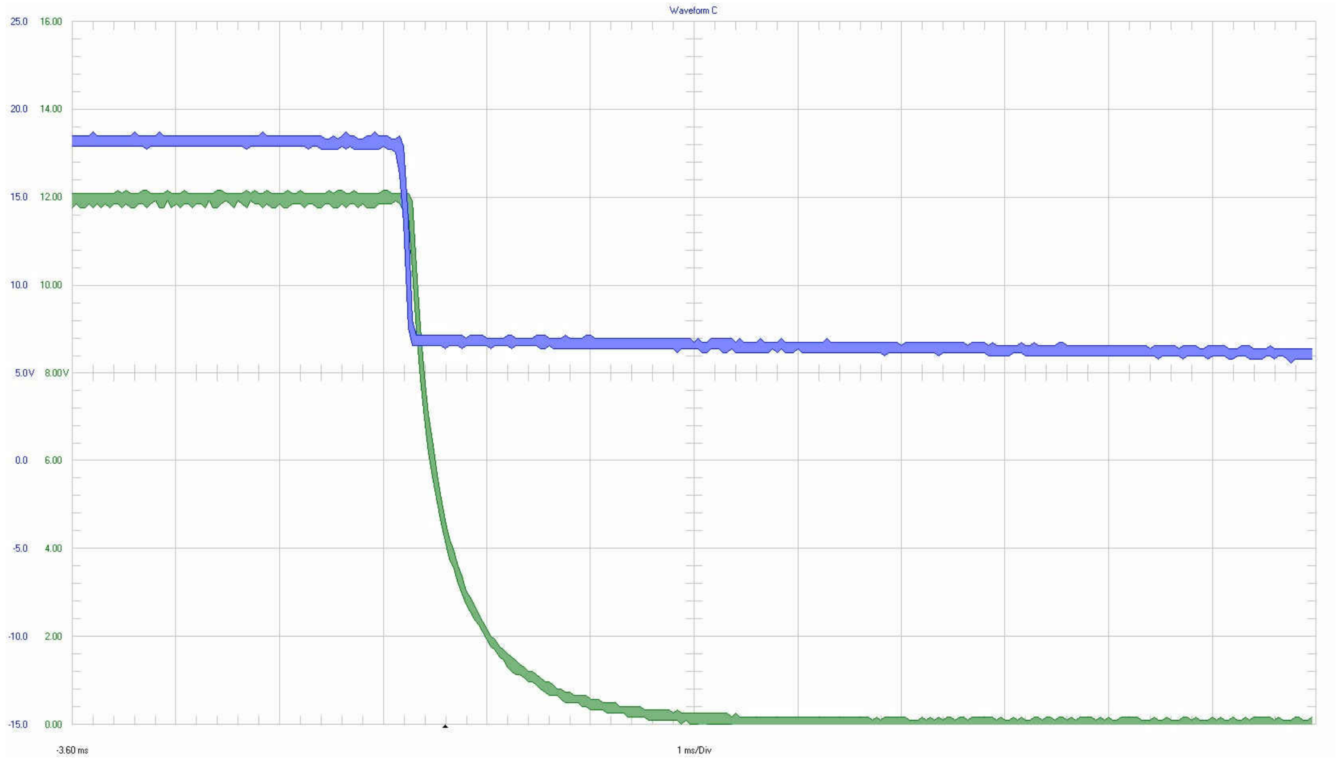


Figure 3-14. Shutdown at 18-V Input Voltage

V_{IN} (blue curve)

- 5 V / div
- 20-MHz bandwidth

V_{OUT}

- 2 V / div
- 20-MHz bandwidth

1 ms / div

3.7 Spread Spectrum Feature

The spread spectrum features are demonstrated in the following figures.

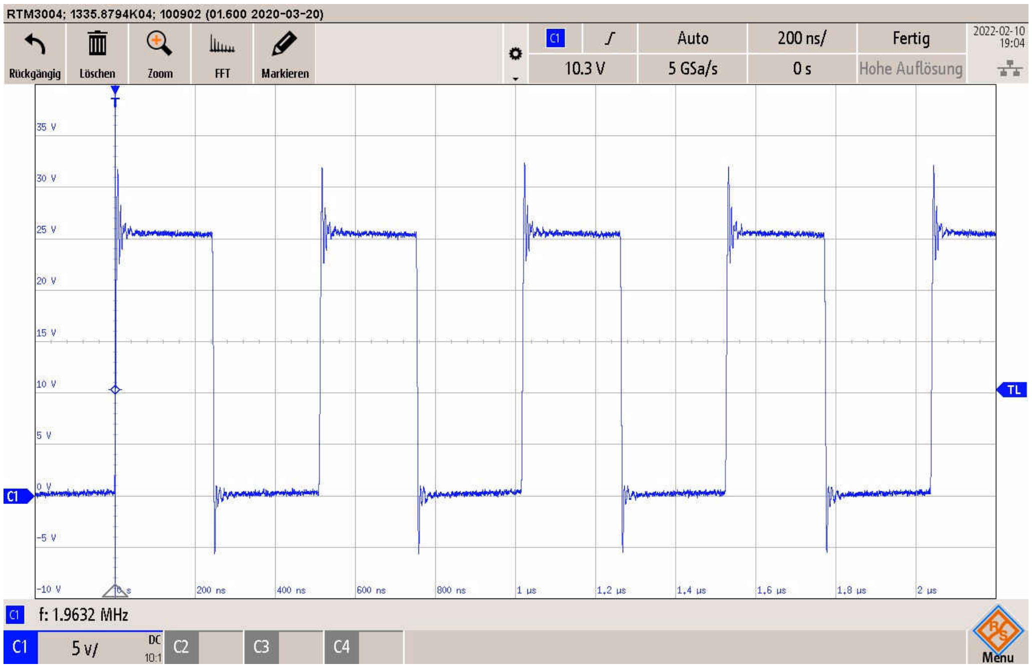


Figure 3-15. Disabled, MODE Tied to AGnd Using a 0-Ω Resistor

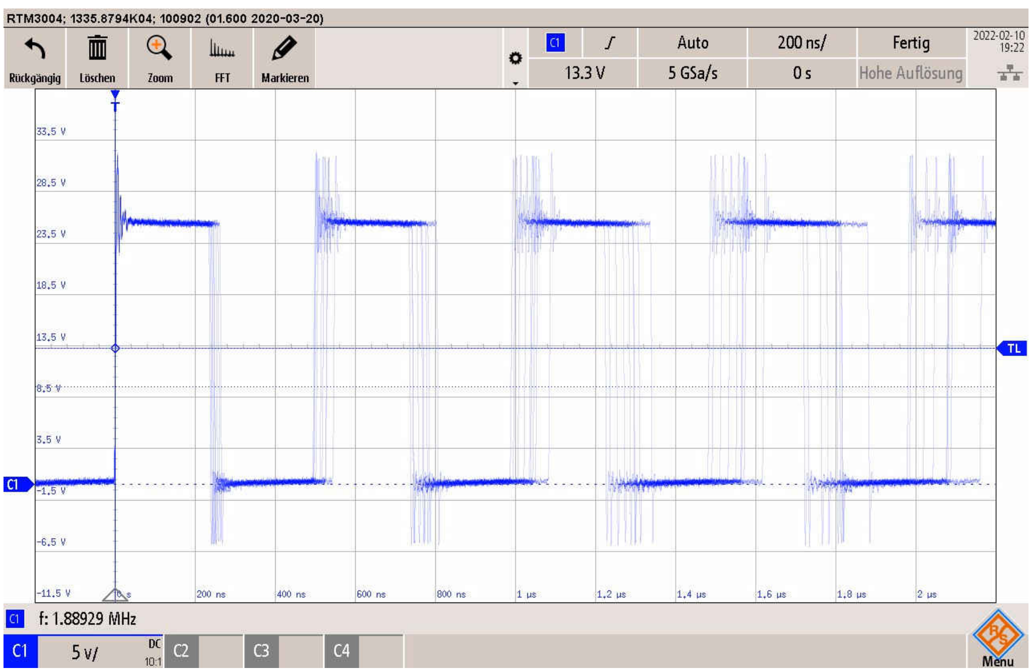


Figure 3-16. Enabled, MODE Across R10 = 37.4-kΩ to AGnd

DRSS, pseudo-dual random spread spectrum: low-frequency triangular switching frequency modulation, and triangular control voltage varies in its modulation frequency itself. In addition this control voltage is superimposed with a random noise, results in best noise reduction at switching frequency and closer harmonics as well as in the high RF range FM band and beyond.