

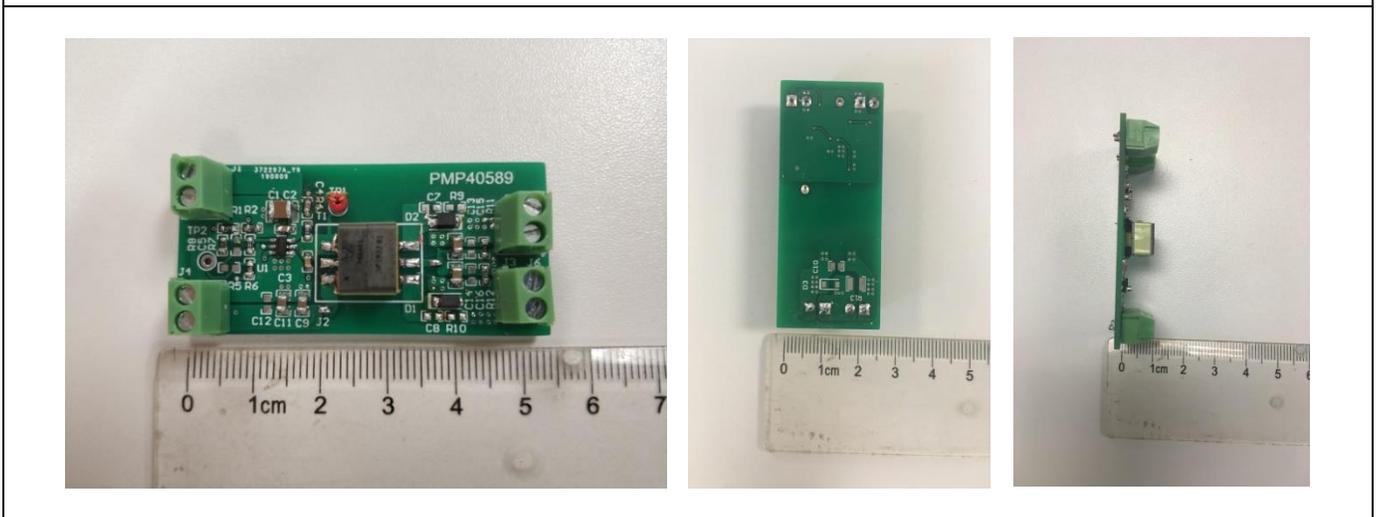
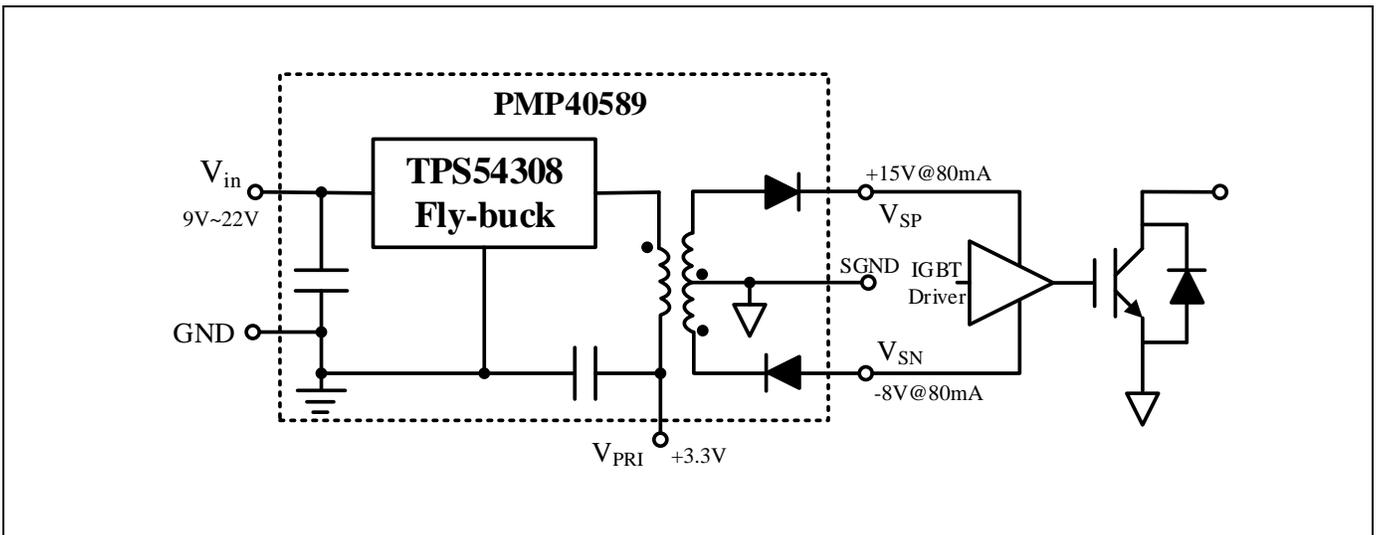
Test Report: PMP40589

2-W Auxiliary Power Supply for a Single IGBT Driver Reference Design



Description

In many applications, simple, low part-count, isolated power supplies working from an input voltage are needed. A popular solution to these requirements is an isolated buck power supply. The Fly-Buck has the advantages of primary side regulation (with no need of opto-coupler feedback) and good cross regulation. This PMP40589 reference design is a dual output isolated Fly-Buck power module for single IGBT driver bias, and uses the TPS54308 synchronous buck converter. It takes 9V-22V input voltage, generates one non-isolated output of +3.3V with 400mA current capability and two isolated outputs of +15V and -8V with 80mA current capability.



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input voltage range (V_{in})	9 – 22 V
Primary output voltage (V_{out1})	3.3 V
Positive isolated output voltage (V_{out2})	15 V
Negative isolated output voltage (V_{out3})	-8 V
Primary load current (I_{out1})	0.4 A
Positive isolated load current (I_{out2})	0.08 A
Negative isolated load current (I_{out3})	0.08 A
Switching frequency (f_{sw})	350 kHz
Total output power	3.16 W

1.2 Required Equipment

- DC source: GWinstek, GPS-3303C
- Electronic load: Chroma, 6314A
- Oscilloscope: Tektronix, DPO 3054
- Frequency Response Analyzer: AP instruments, Model 300 · 30MHz
- Infrared Thermal Camera: Fluke, TiS55
- True-RMS-Multimeter: Fluke, 287C

2 Testing and Results

2.1 Efficiency Graphs

The efficiency was measured at different input voltages under balanced load at Vout1, Vout2 and Vout3. All the outputs load are the same percentage to full load output current respectively.

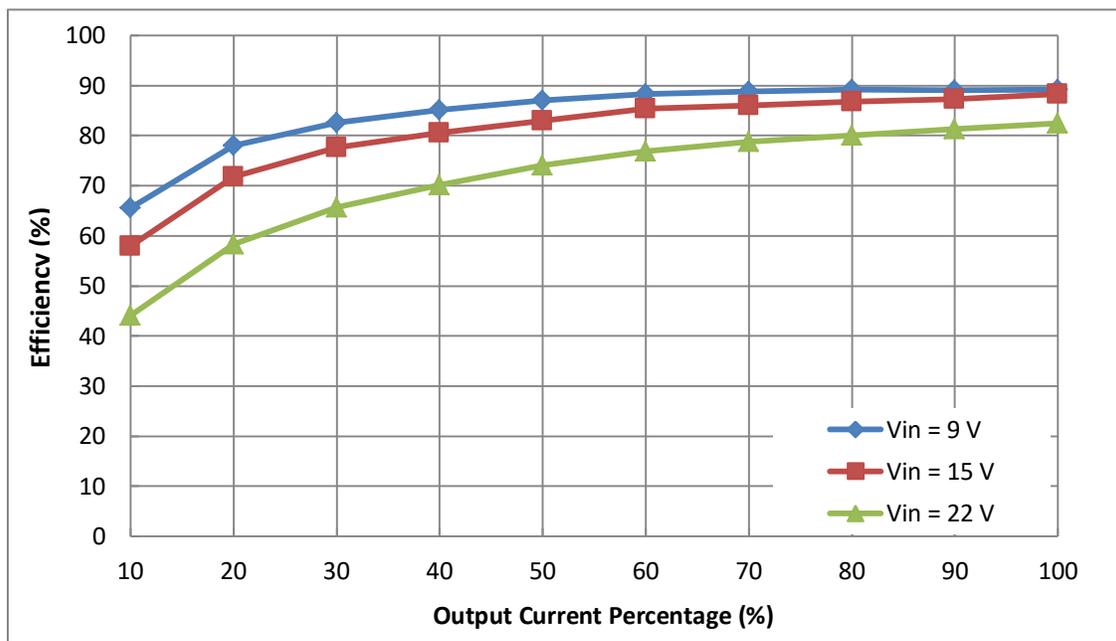


Figure 1. Power efficiency vs balanced load at Vout1, Vout2 and Vout3

The efficiency was measured at different input voltages under balanced load at Vout2 and Vout3 with no load at Vout1. The output loads at Vout2 and Vout3 was increased linearly.

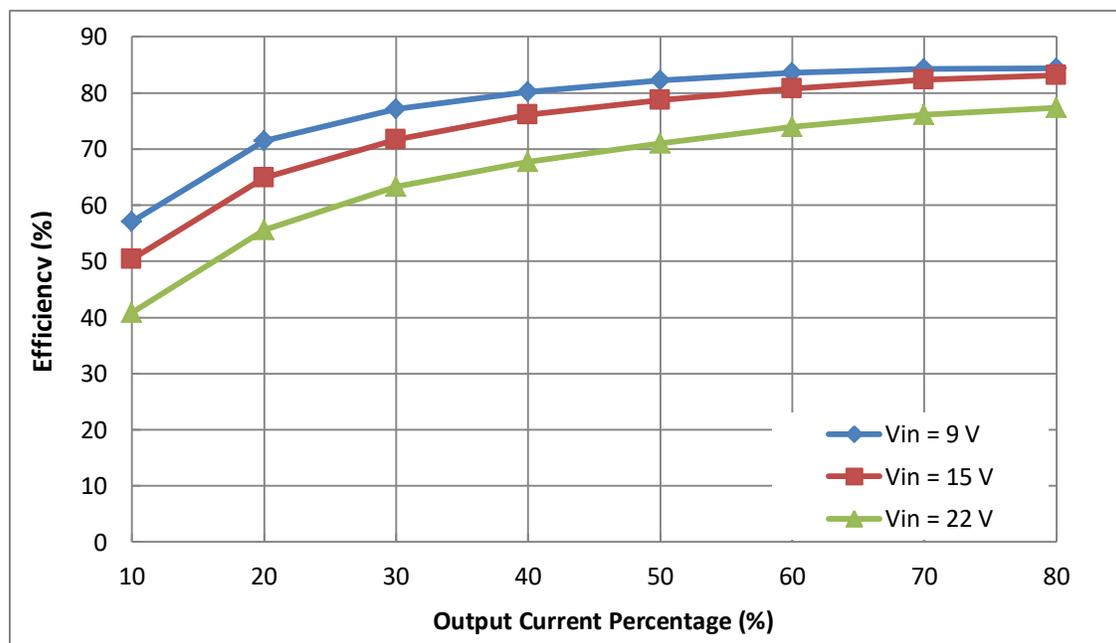


Figure 2. Power efficiency vs balanced load at Vout2 and Vout3 (Iout1 = 0A)

2.2 Cross Regulation

Under balanced load condition, the primary 3.3V and two outputs +15V and -8V were loaded with the same percentage of full load output current respectively. Figure 3 and Figure 4 shows the output regulation under balanced load.

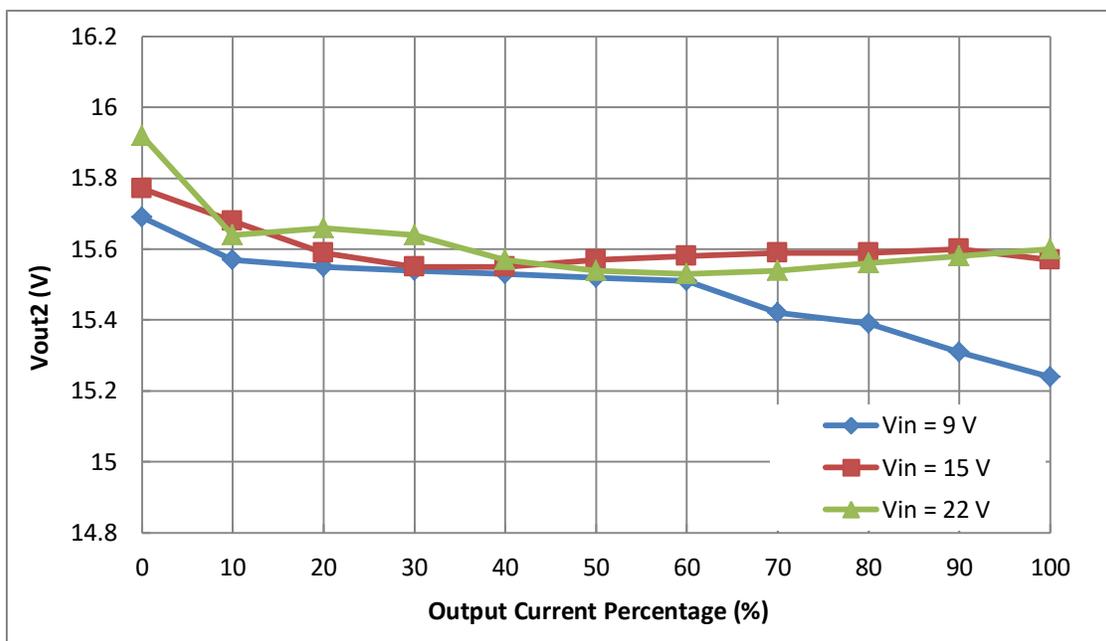


Figure 3. Vout2 vs balanced load on Vout1, Vout2 and Vout3

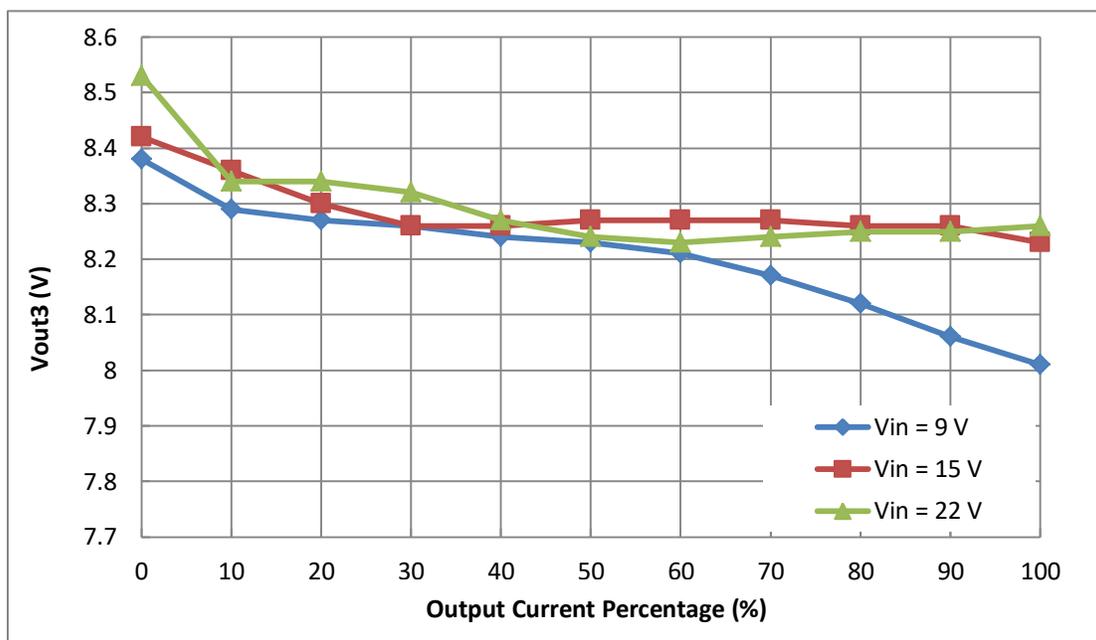


Figure 4. Vout3 vs balanced load on Vout1, Vout2 and Vout3

The unbalanced load condition was tested by varying the load at one isolated output while no load at another isolated output and the primary output. Figure 5 and Figure 6 show the output regulation of +15V and -8V with variation load at Vout2, no load at Vout1 and Vout3. Figure 7 and Figure 8 show the output regulation of +15V and -8V with variation load at Vout3, no load at Vout1 and Vout2.

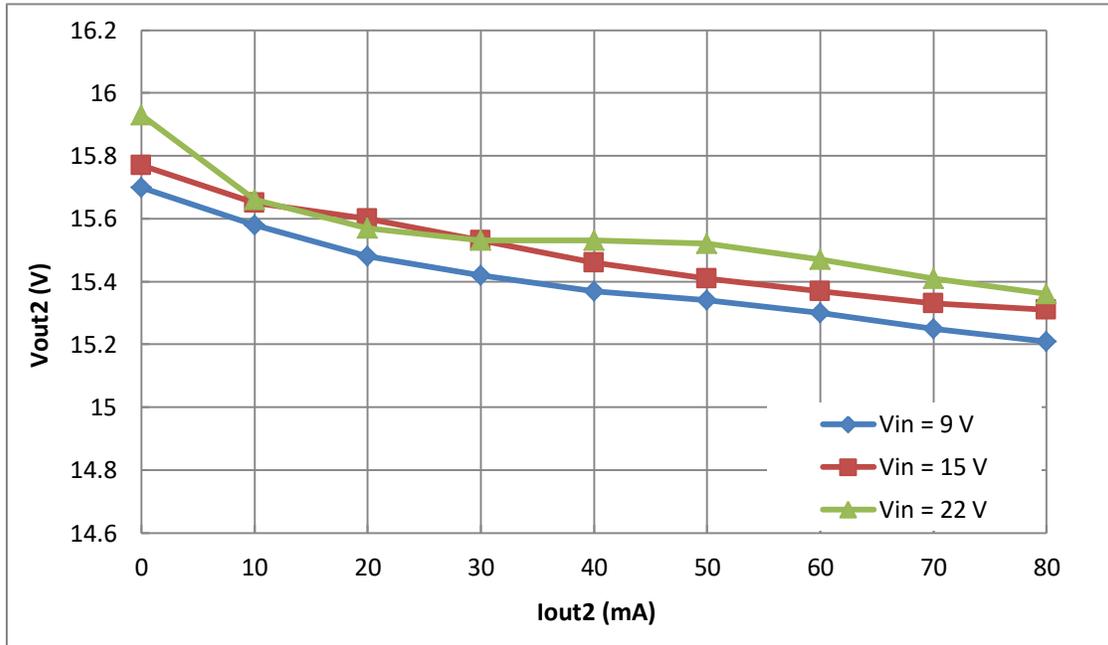


Figure 5. Vout2 vs Iout2 (Iout1 = 0A, Iout3 = 0A)

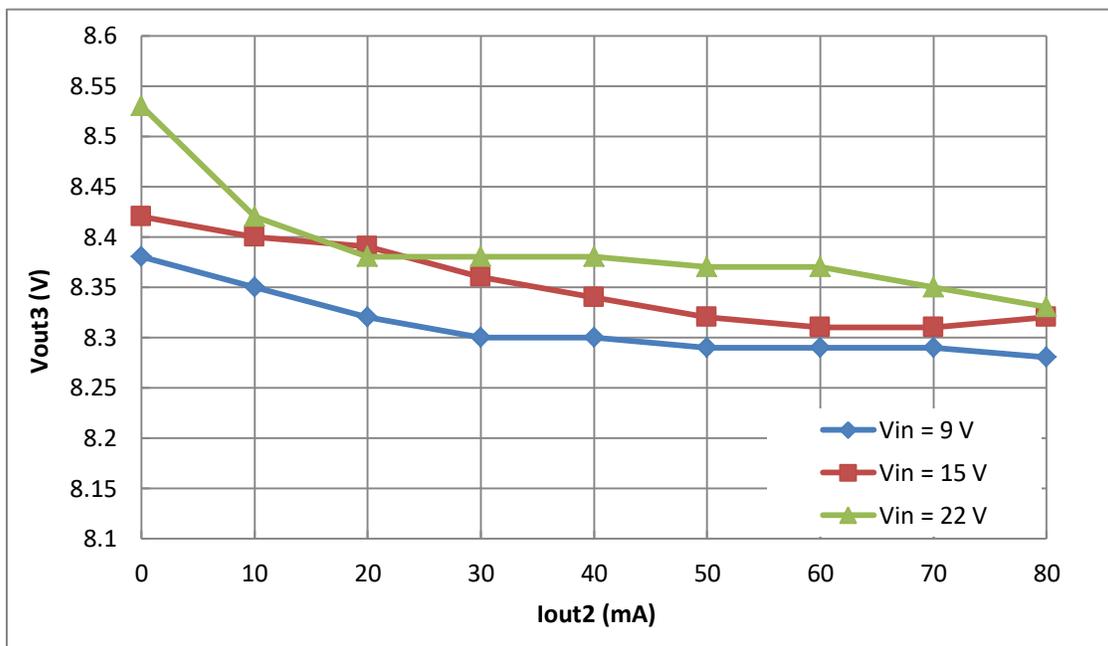


Figure 6. Vout3 vs Iout2 (Iout1 = 0A, Iout3 = 0A)

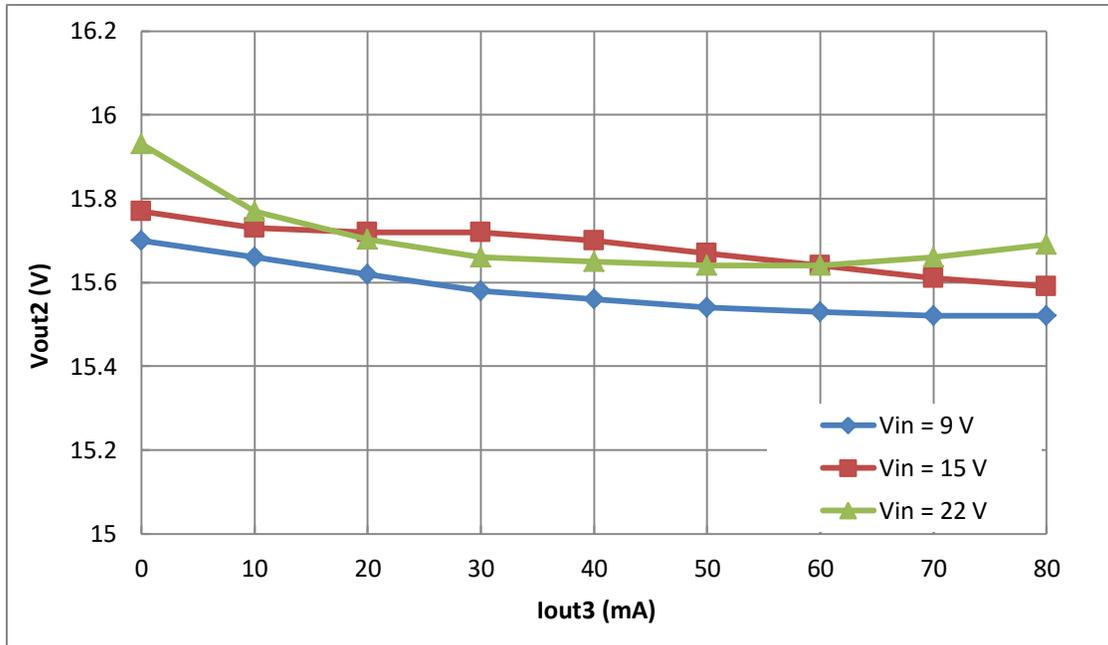


Figure 7. Vout2 vs Iout3 (Iout1 = 0A, Iout2 = 0A)

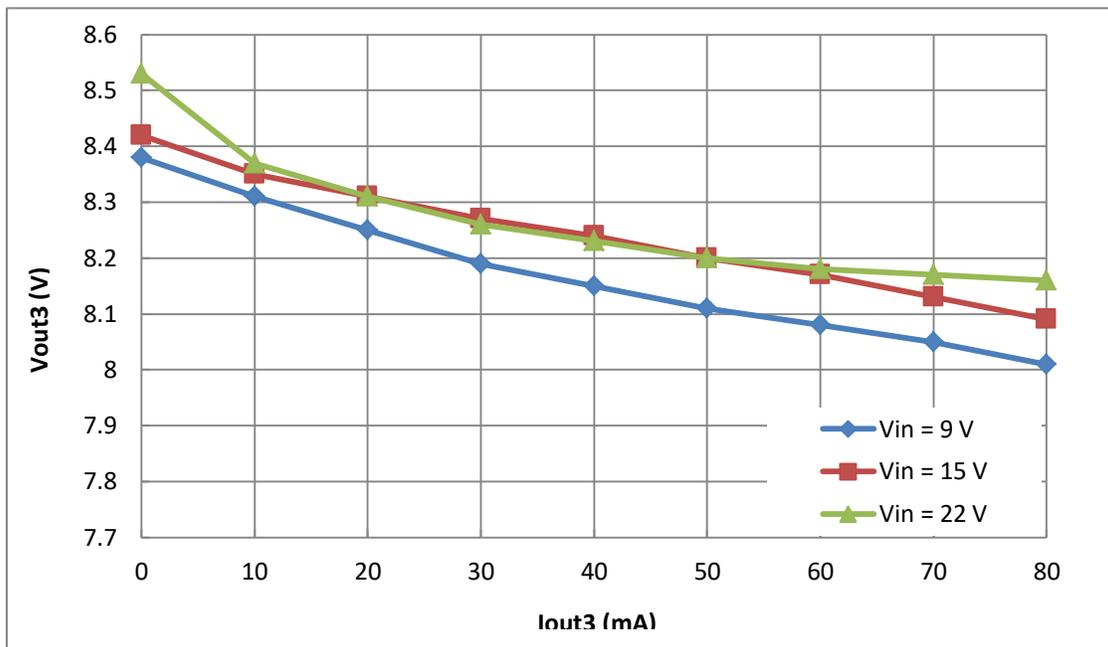
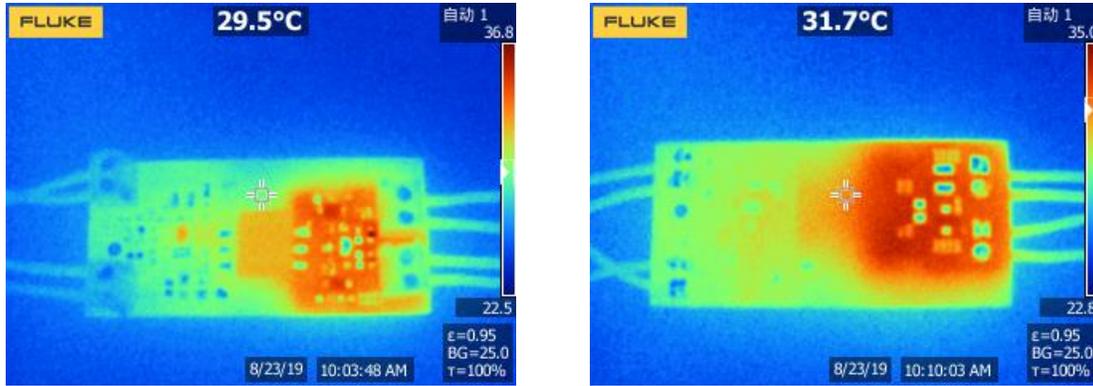


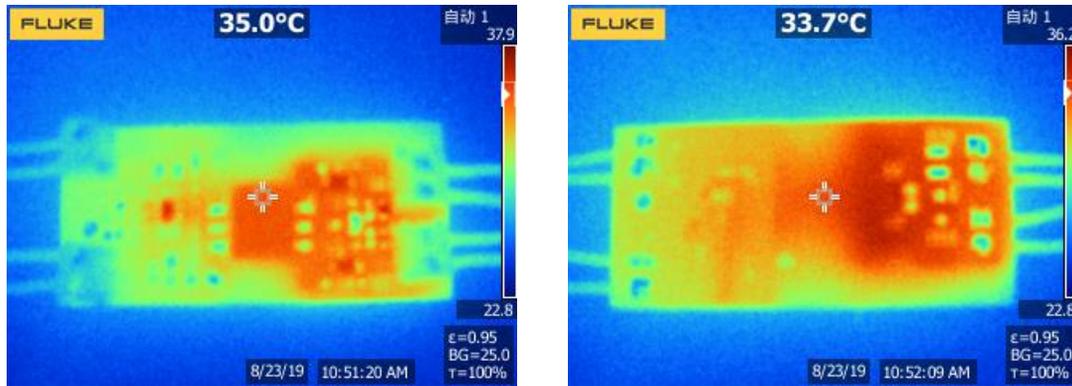
Figure 8. Vout3 vs Iout3 (Iout1 = 0A, Iout2 = 0A)

2.3 Thermal Images

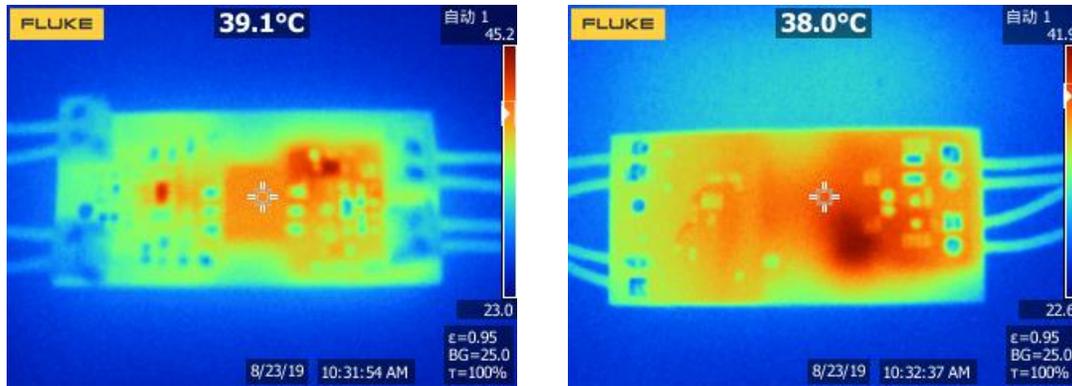
Below thermal images were taken at 23°C room temperature, no air flow. The board was operating at 9V, 15V and 22V input separately, full load on the all outputs.



Top Bottom
 Figure 9. Thermal image with $V_{in} = 9V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$



Top Bottom
 Figure 10. Thermal image with $V_{in} = 15V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$



Top Bottom
 Figure 11. Thermal image with $V_{in} = 22V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

3 Waveforms

3.1 Start-up

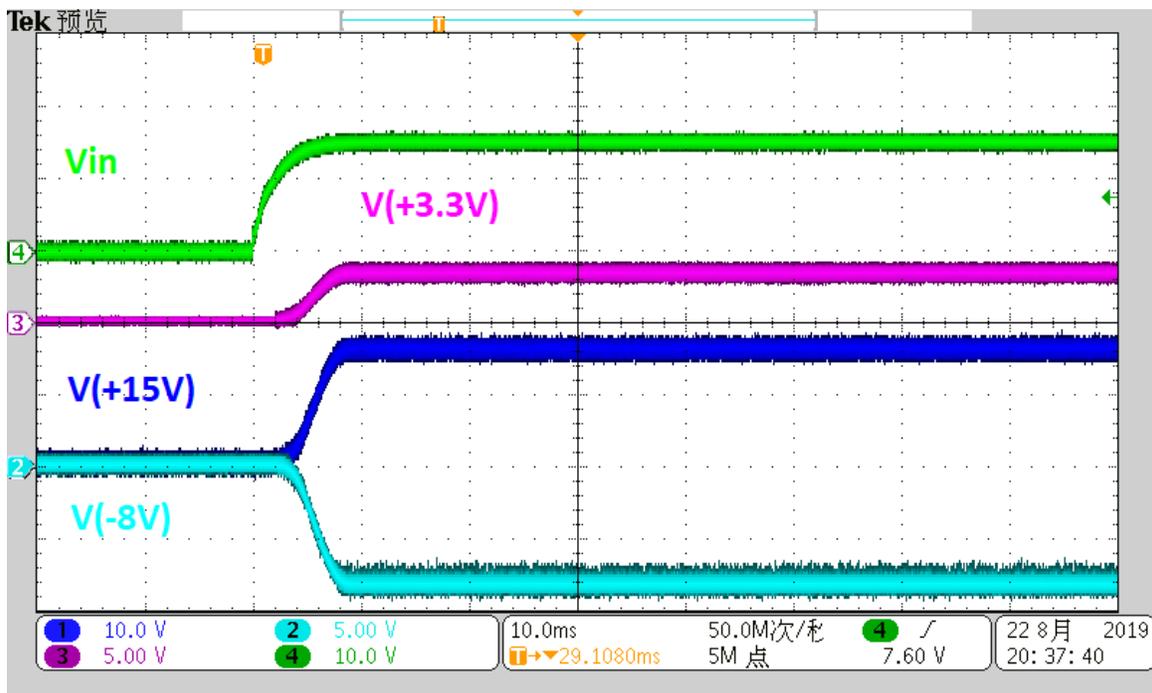


Figure 12. Power up waveform with $V_{in} = 15V$, $I_{out1} = 0A$, $I_{out2} = 0A$, $I_{out3} = 80mA$

3.2 Under voltage Protection

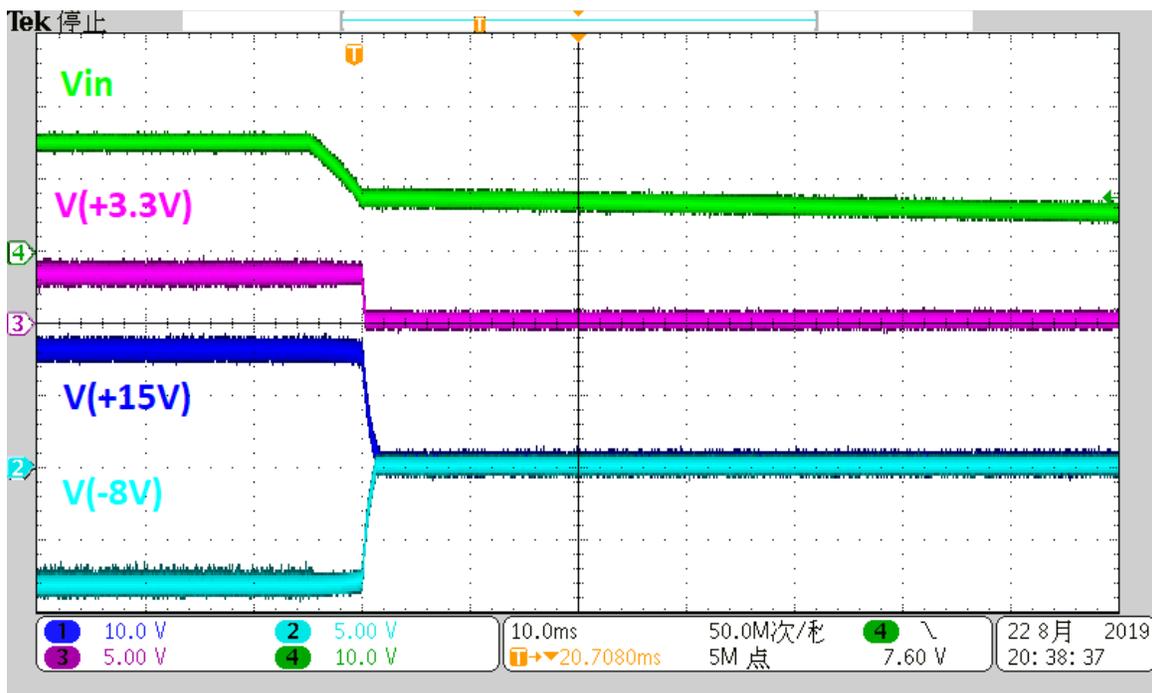


Figure 13. Power off waveform with $V_{in} = 15V$, $I_{out1} = 0A$, $I_{out2} = 0A$, $I_{out3} = 80mA$

3.3 Switching

The primary side switch node voltage was measured with no load and full load condition at 15V input voltage.

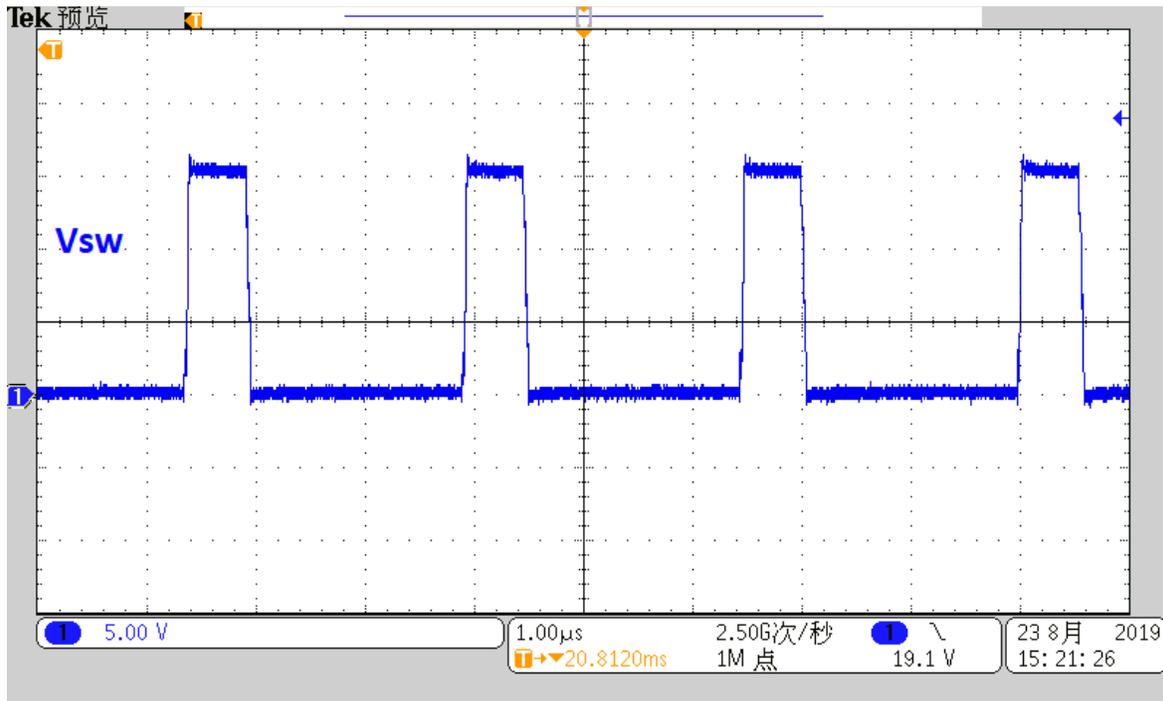


Figure 14. Switch node voltage, $V_{in} = 15V$, $I_{out1} = 0A$, $I_{out2} = 0A$, $I_{out3} = 0A$

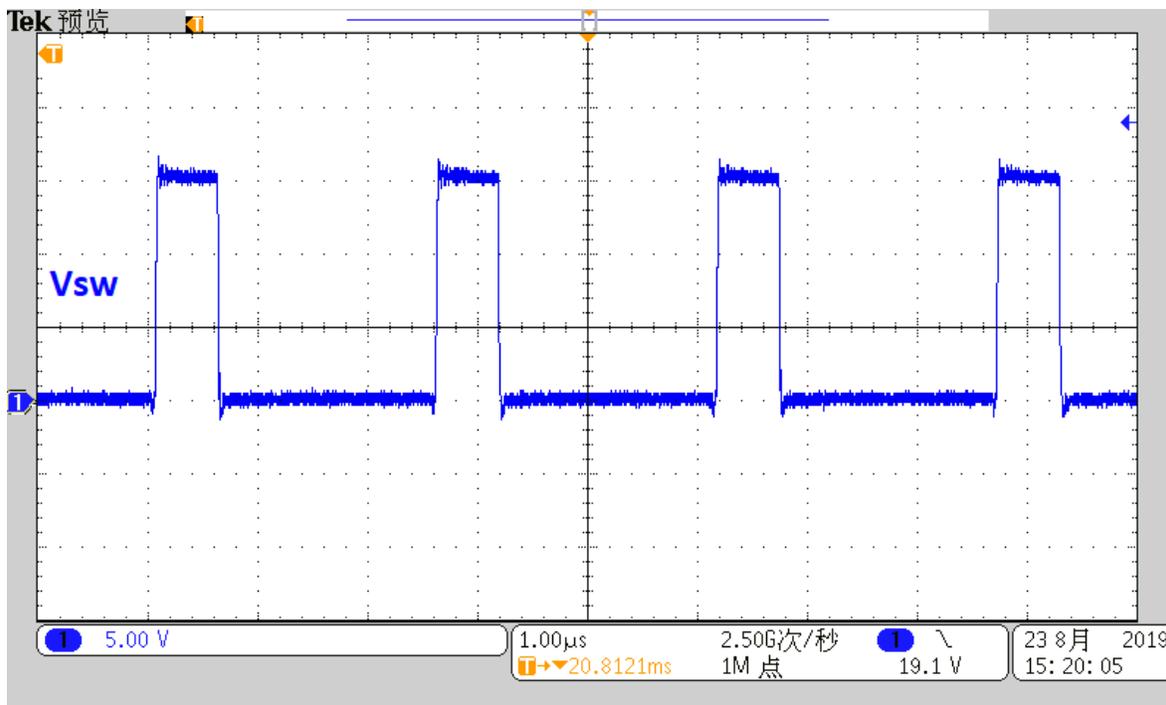


Figure 15. Switch node voltage, $V_{in} = 15V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

3.4 Output Voltage Ripple

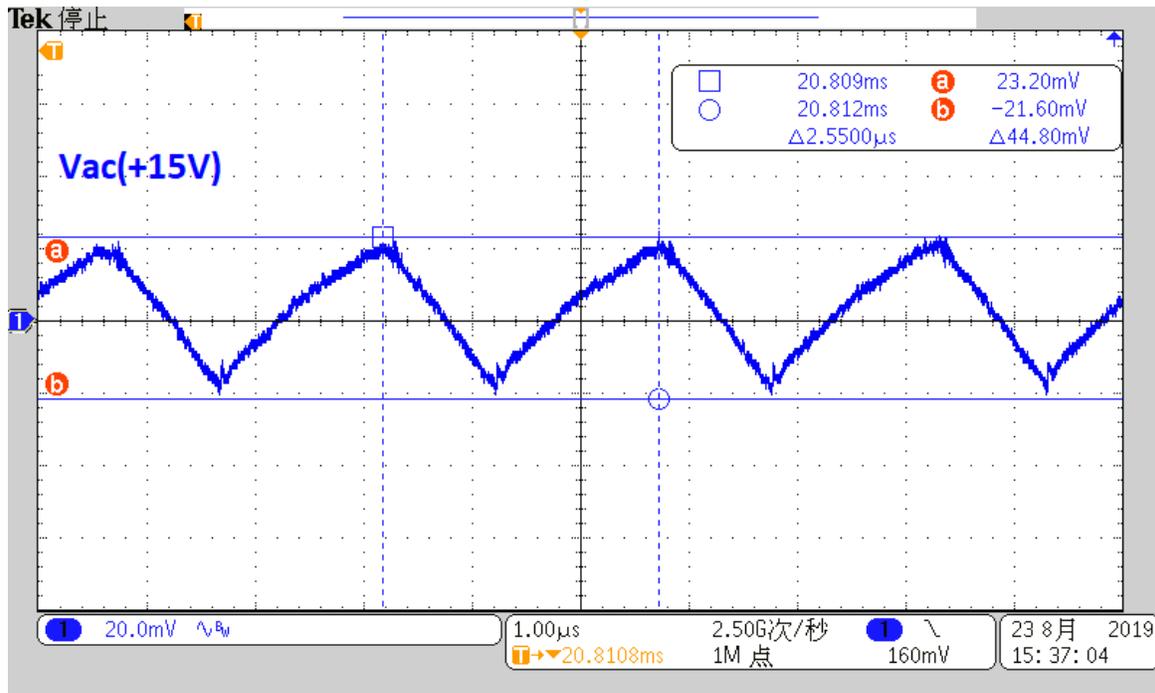


Figure 16. +15V output ripple, $V_{in} = 15V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

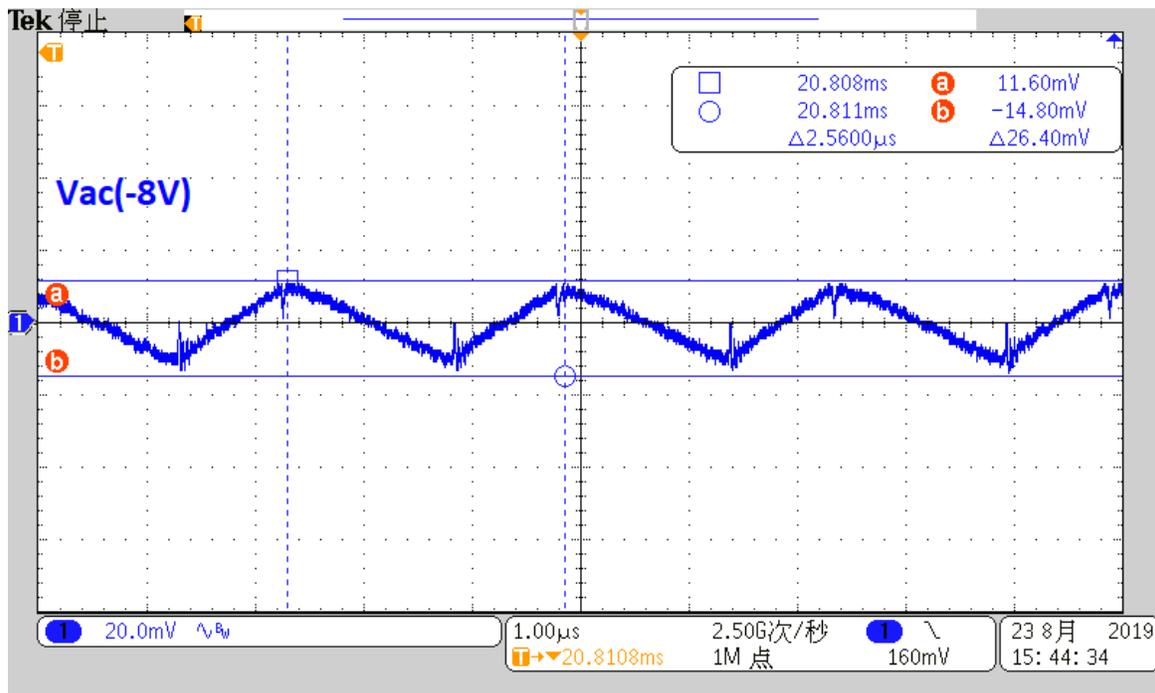


Figure 17. -8V output ripple, $V_{in} = 15V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

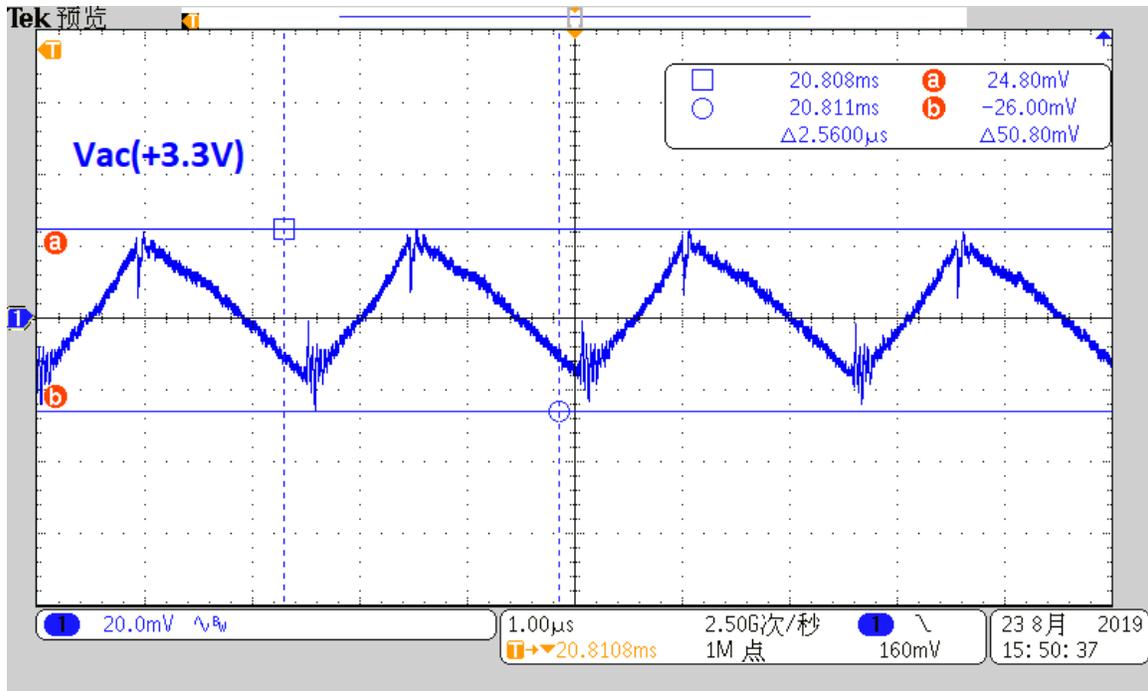


Figure 18. +3.3V output ripple, $V_{in} = 15V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

3.5 Short Circuit Test

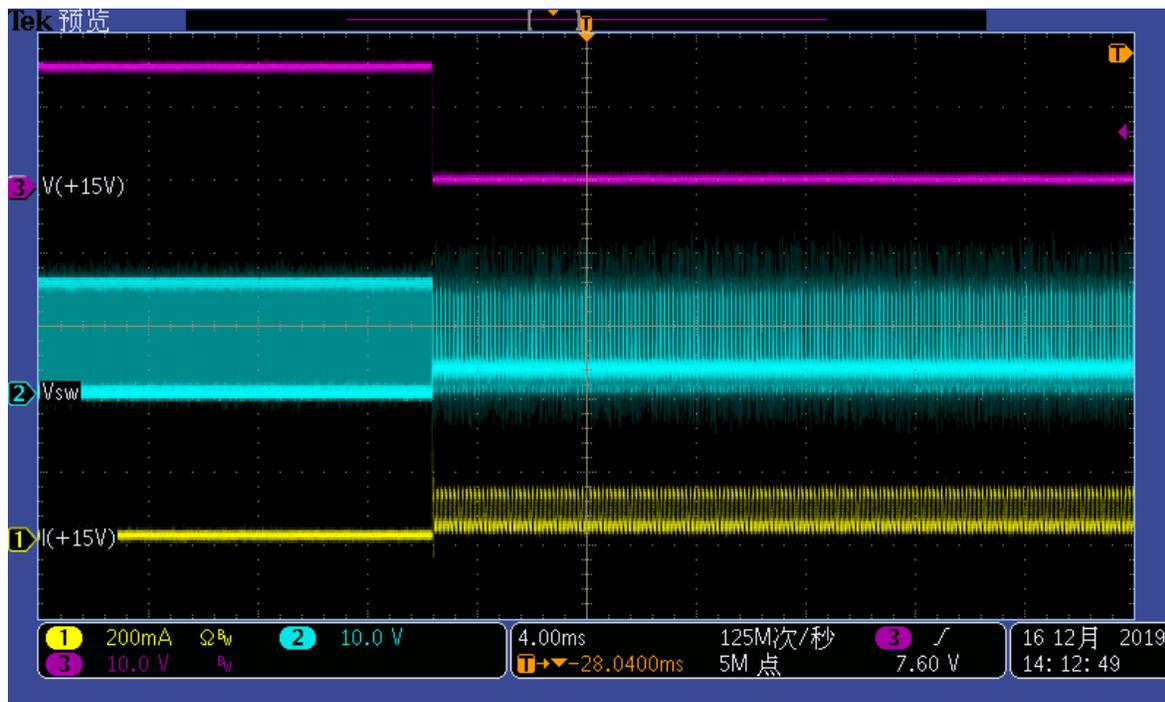


Figure 19. Output short from full load operation to short circuit at 15V input (+15V rail short circuit)

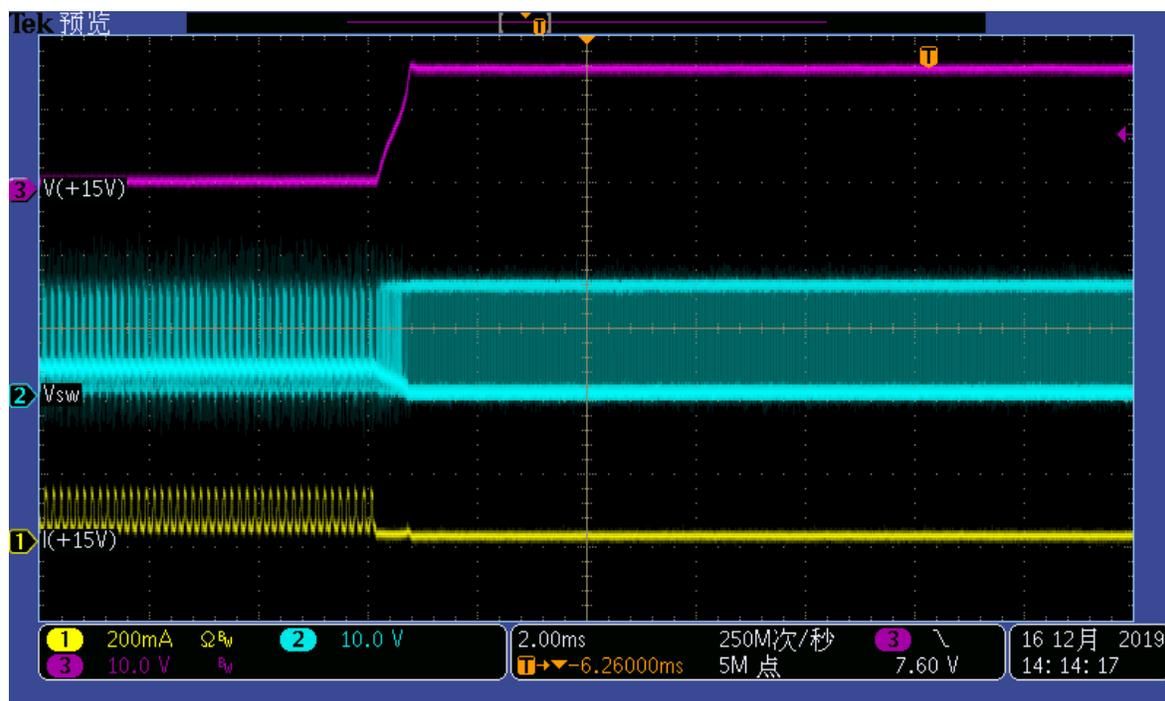


Figure 20. Short circuit removed into full load operation at 15V input (+15V rail short circuit release)

3.6 Load Transients

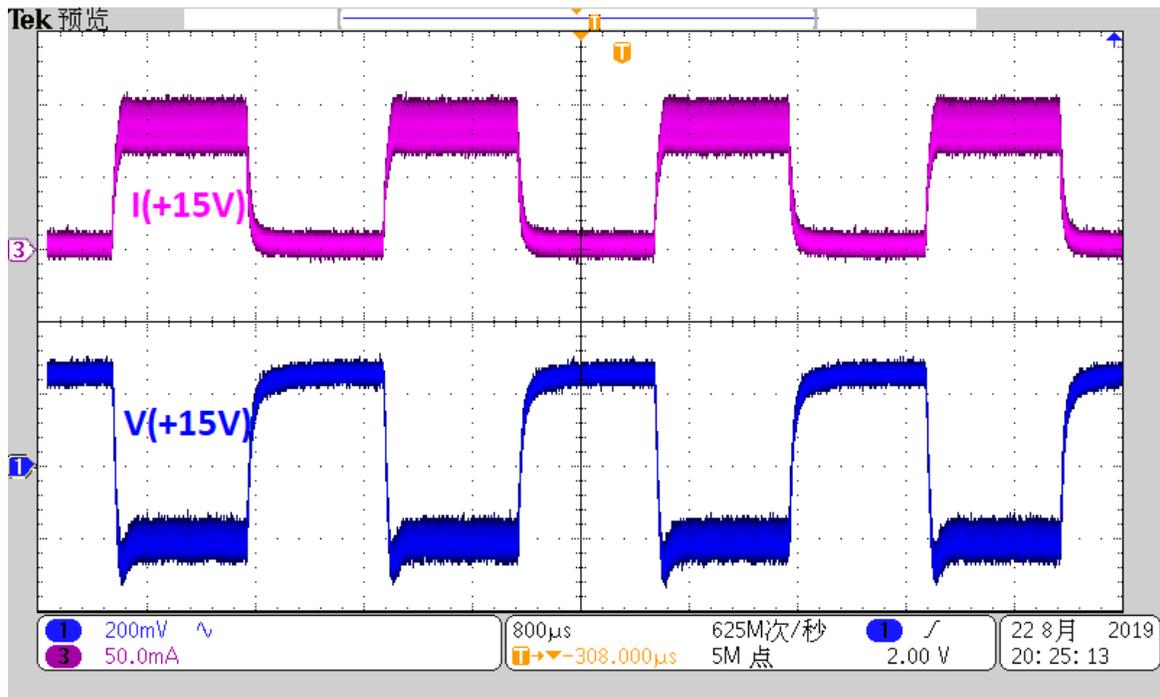


Figure 21. +15V output load transient at 15V input from 0A to 80mA

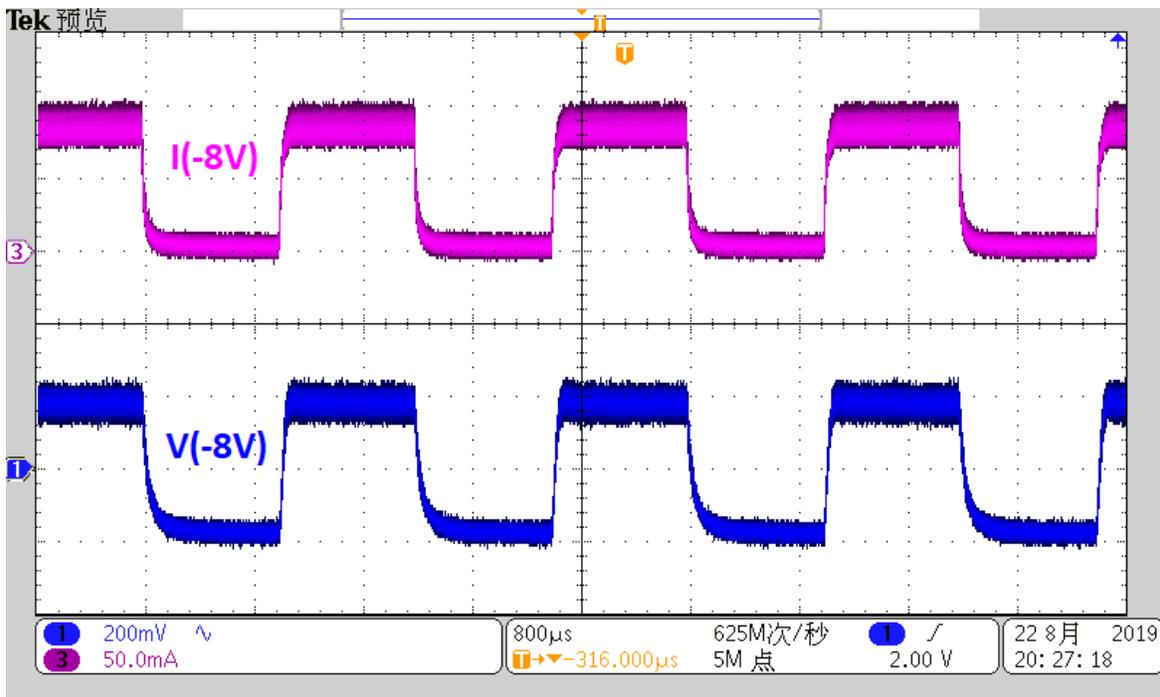


Figure 22. -8V output load transient at 15V input from 0A to 80mA

3.7 Diode Voltage Stress

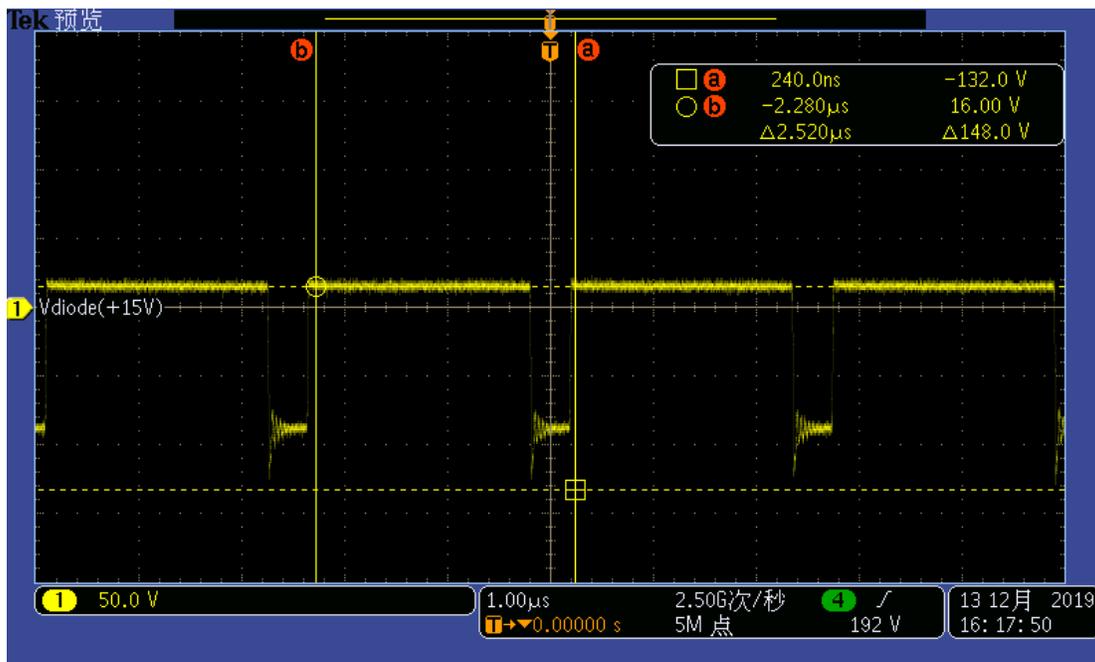


Figure 23. +15V diode voltage stress $V_{in} = 22V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

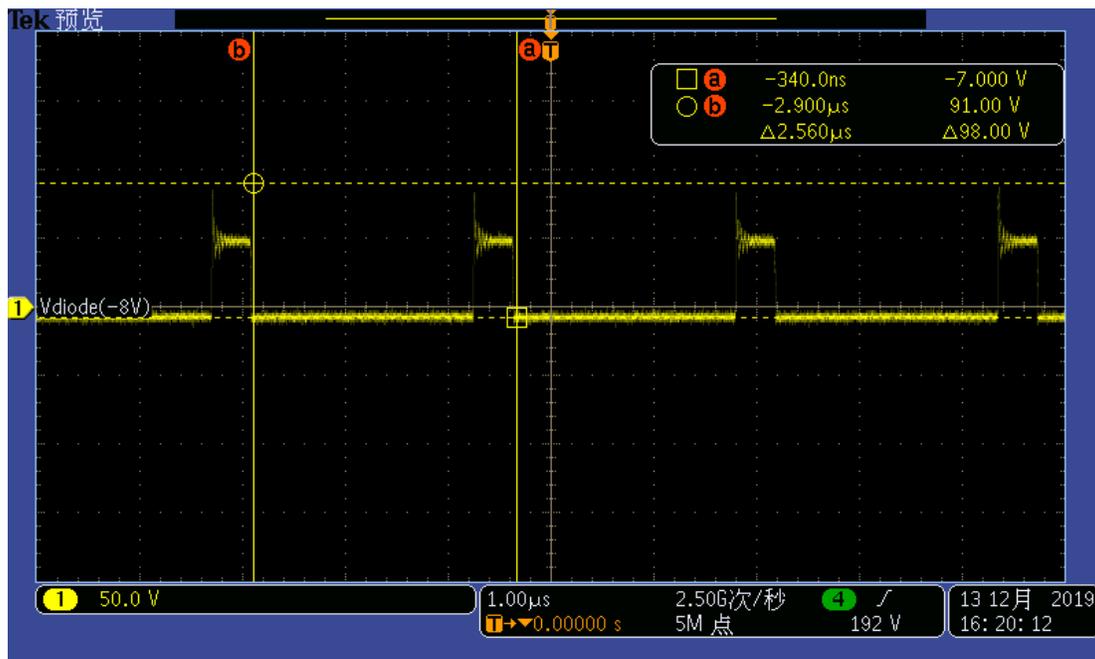


Figure 24. -8V diode voltage stress $V_{in} = 22V$, $I_{out1} = 0.4A$, $I_{out2} = 80mA$, $I_{out3} = 80mA$

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