Test Report: PMP22021

Compact Isolated DC-DC Flyback Reference Design

Description

This reference design uses LM5022 to make an isolated 3.3-V output capable of 1.1-A from a 9-V to 15-V input. All components are placed on one side of the board to reduce assembly complexity and cost. A secondary filter reduces the output ripple to under 30-mV peak-to-peak. The design can achieve 80% efficiency across input conditions.

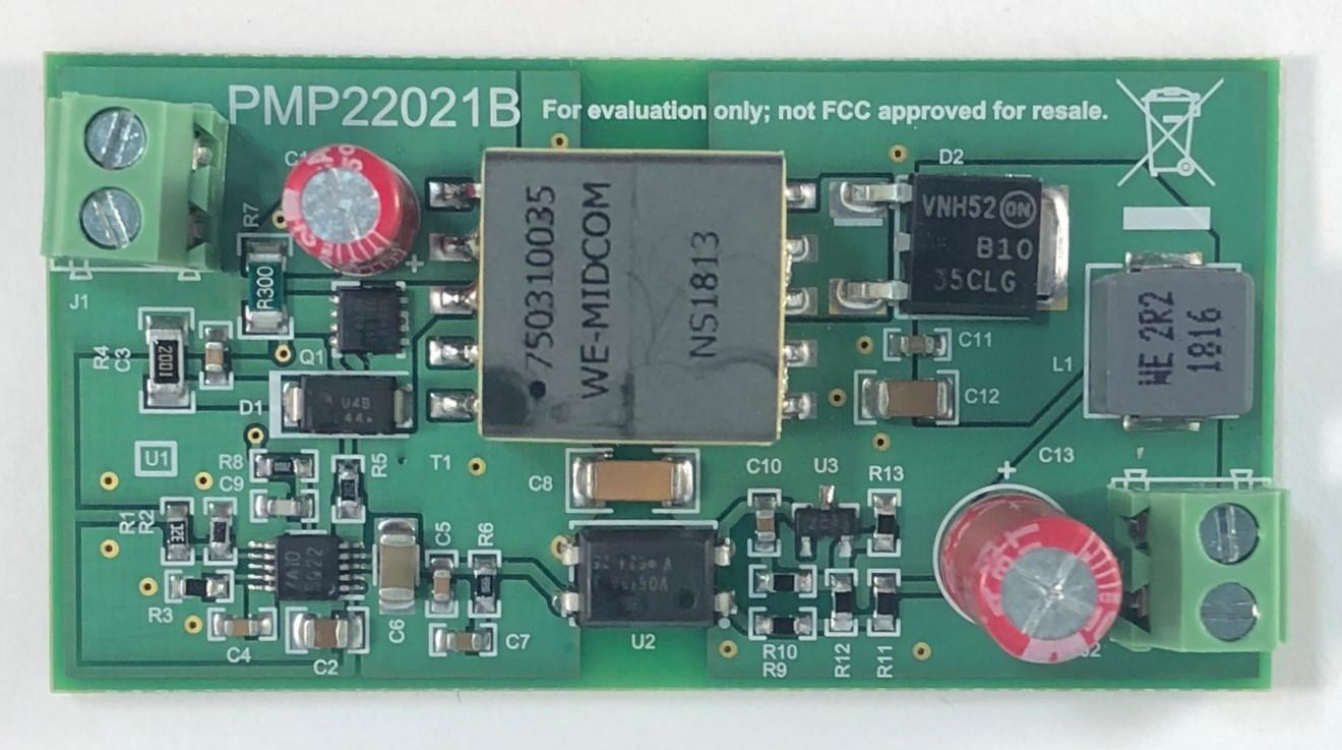

Figure 1. Board Top

1 Test Prerequisites

1.1 Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	9 Vdc – 15 Vdc, 12 Vdc nominal
Output Voltage 1	3.3 V +/- 1%
Output Current 1	1.1 A
Switching Frequency	200 kHz

2 Testing and Results

2.1 Efficiency Graphs

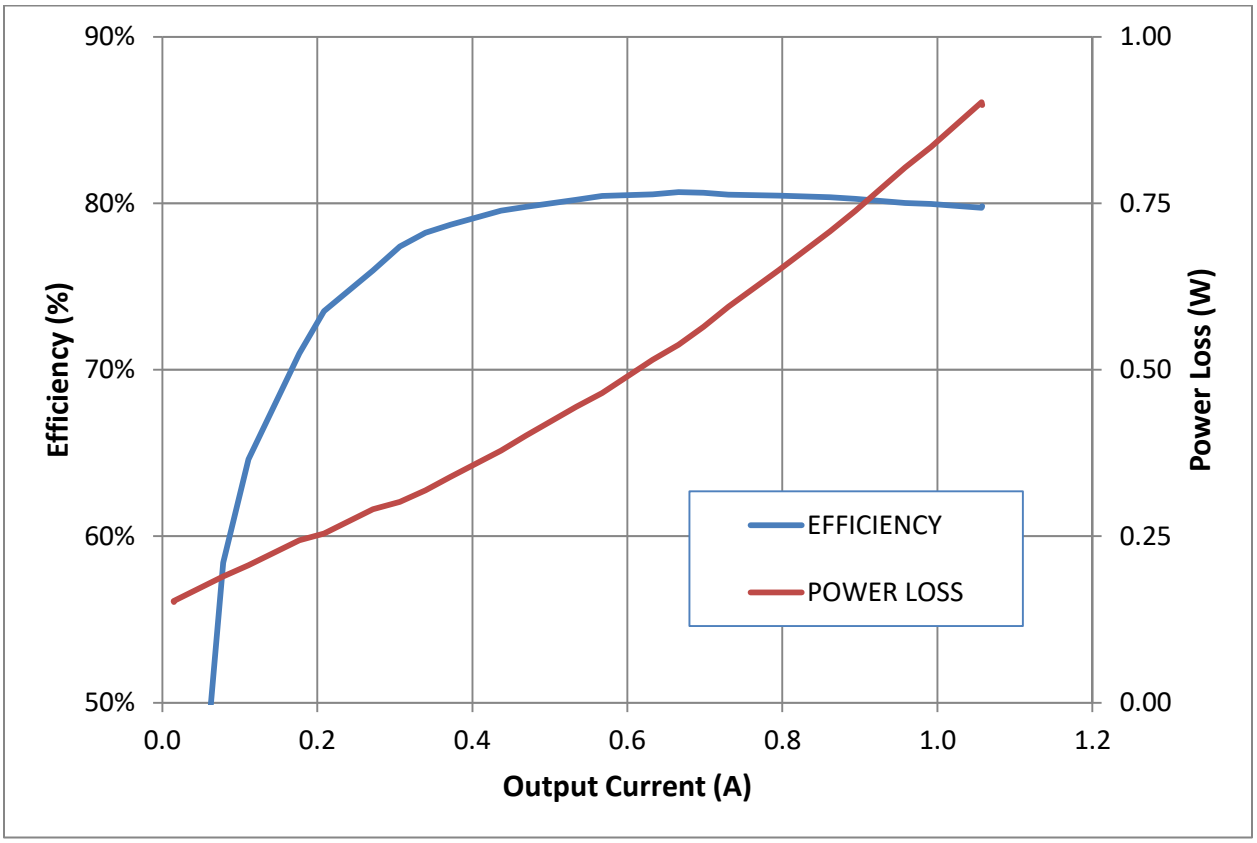

Figure 2. Efficiency with 9 Vdc Input

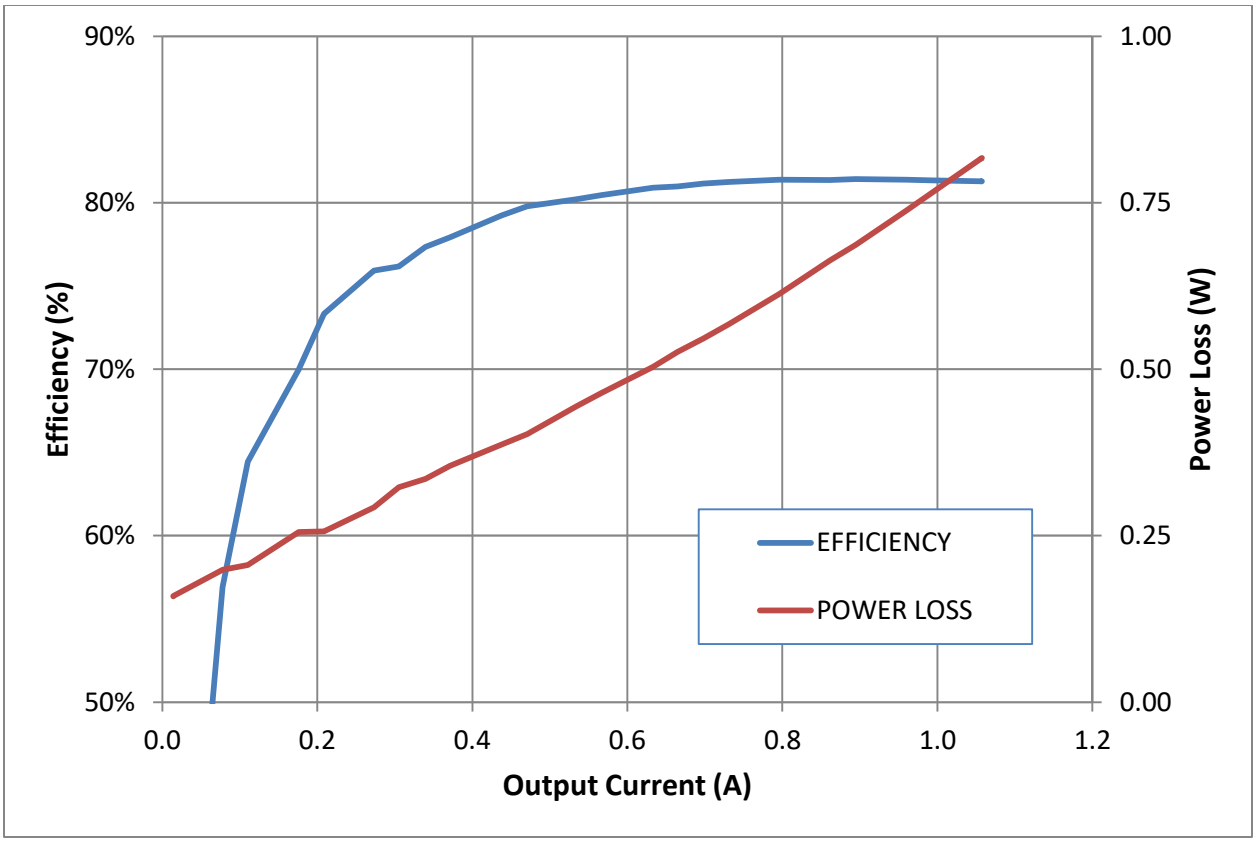

Figure 3. Efficiency with 12 Vdc Input

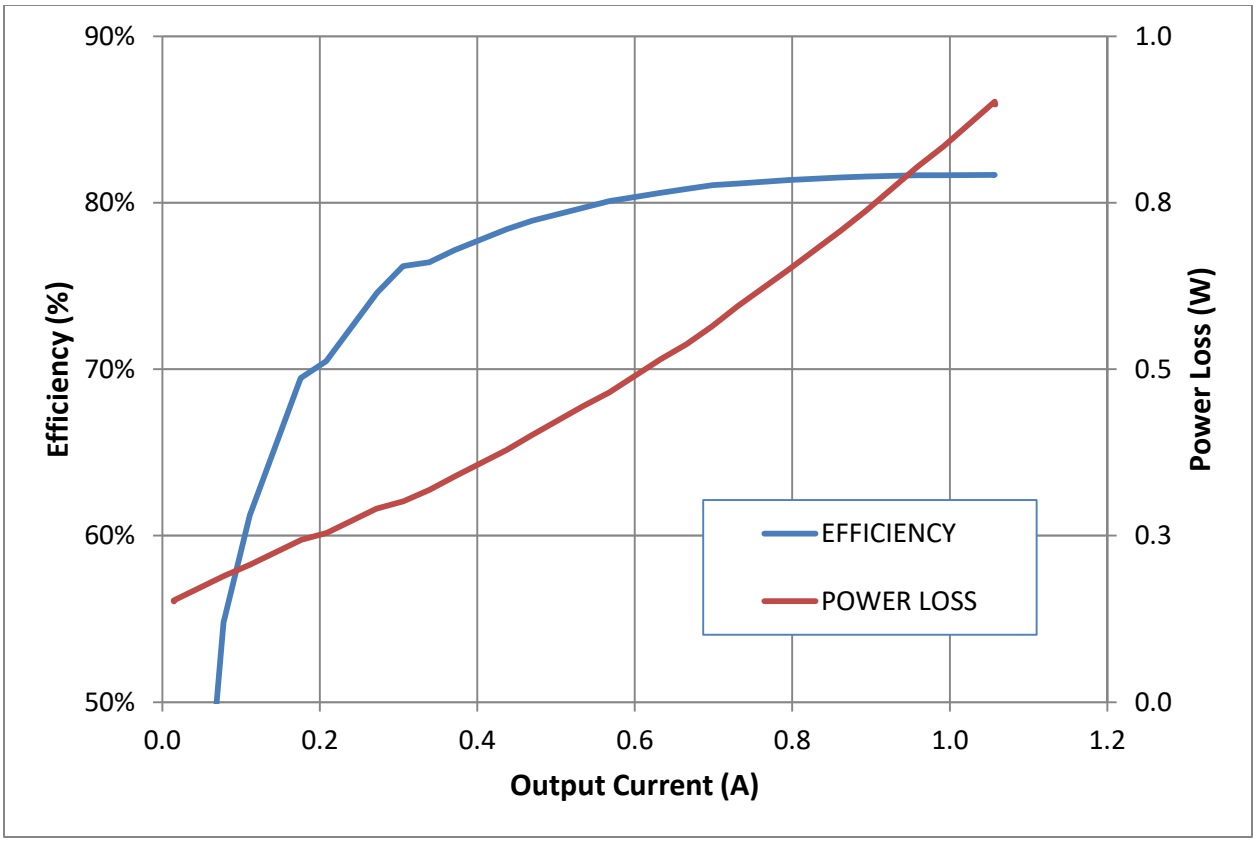

Figure 4. Efficiency with 15 Vdc input

2.2 Efficiency Data

	Input Voltage (V)	Input Current (A)	Input Power (W)	Output Voltage (V)	Output Current (A)	Output Power (W)	Efficiency (%)	Power Loss (W)
9 Vin	8.926	0.023	0.201	3.388	0.015	0.050	24.89	0.151
	8.946	0.135	1.208	3.377	0.272	0.918	75.97	0.290
	8.878	0.253	2.244	3.370	0.534	1.800	80.21	0.444
	8.804	0.378	3.324	3.363	0.795	2.675	80.46	0.649
	8.727	0.510	4.448	3.355	1.058	3.550	79.82	0.898
12 Vin	11.950	0.017	0.207	3.390	0.014	0.048	23.17	0.159
	11.938	0.102	1.215	3.378	0.273	0.922	75.92	0.292
	11.916	0.189	2.246	3.371	0.534	1.802	80.21	0.444
	11.863	0.277	3.291	3.365	0.796	2.678	81.38	0.613
	11.809	0.370	4.367	3.358	1.057	3.550	81.29	0.817
15 Vin	14.969	0.016	0.236	3.391	0.014	0.048	20.47	0.188
	14.725	0.084	1.236	3.379	0.273	0.922	74.59	0.314
	14.938	0.151	2.260	3.372	0.534	1.801	79.70	0.459
	14.897	0.221	3.292	3.366	0.796	2.678	81.37	0.613
	14.855	0.293	4.347	3.360	1.057	3.550	81.66	0.797

Figure 5. Efficiency data from light load, one quarter load, half load, third quarter load, and full load

2.3 Thermal Images

Thermal images were taken after 10 minutes of running with the output at 1.1 A with a 12 Vdc input and no airflow.

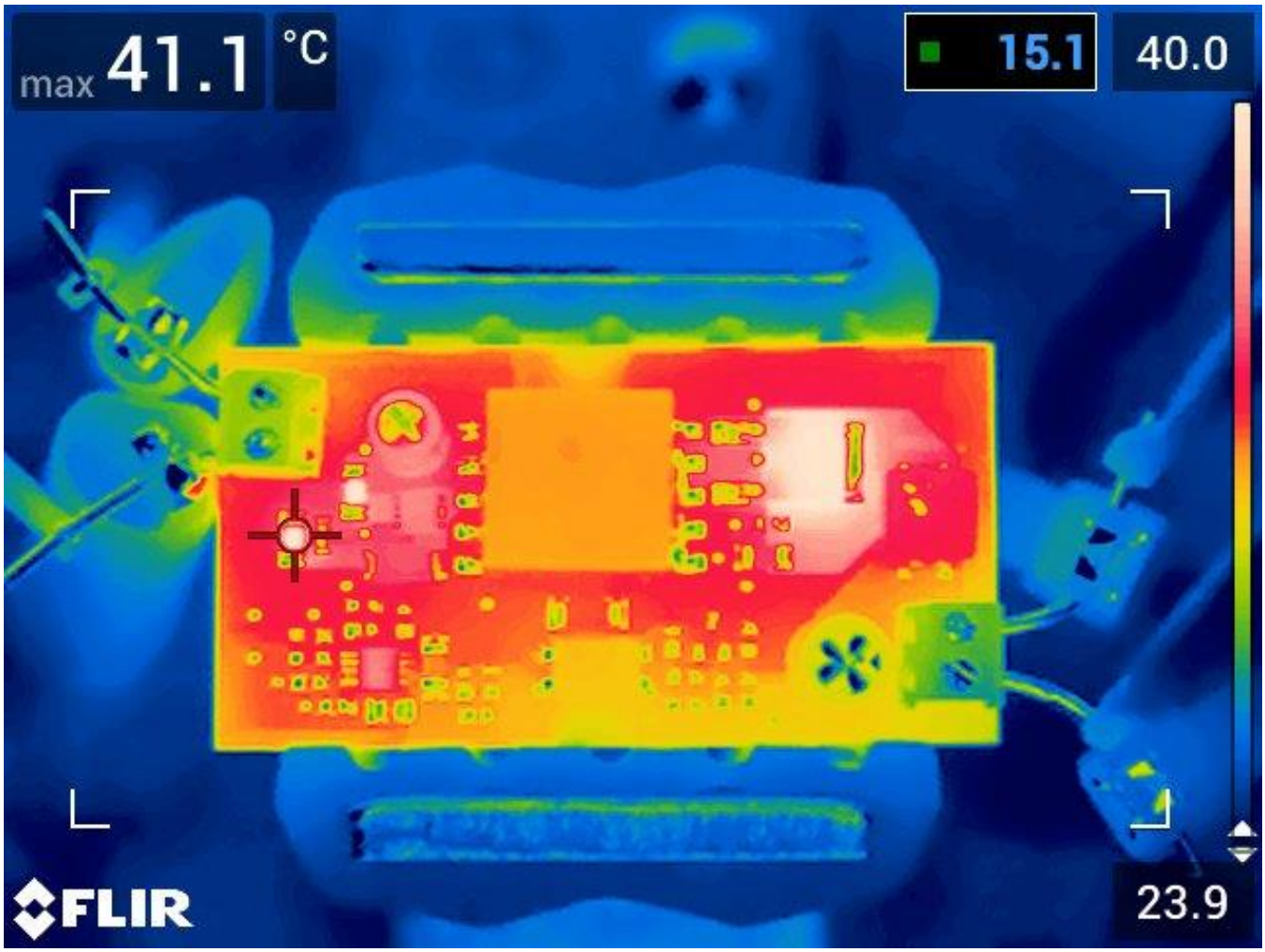

Figure 6. Board Top

3 Waveforms

3.1 Switching

The switch node was measured with the main 15 V output at full load.

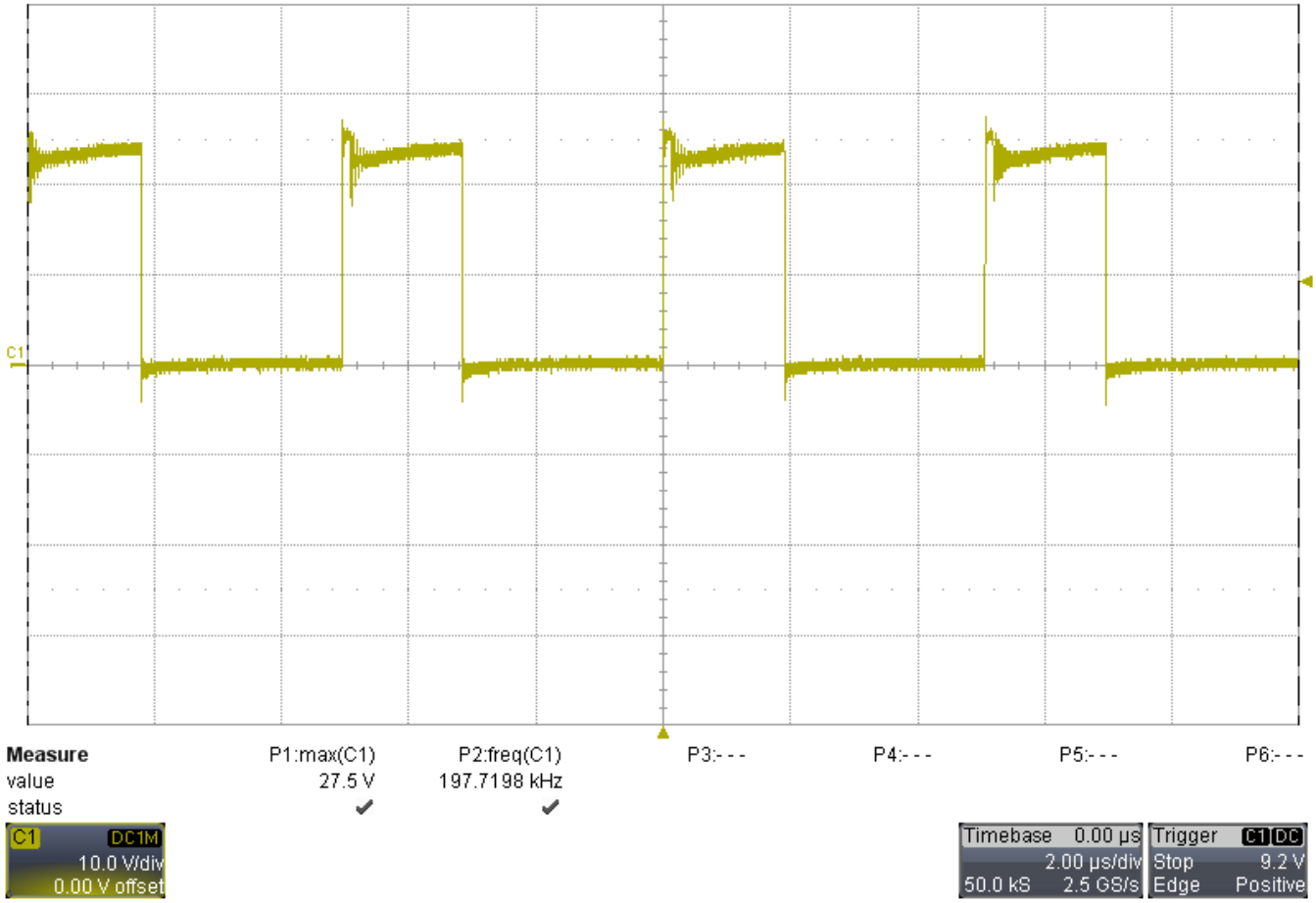

Figure 7. Primary Switching Node with 9 Vdc input

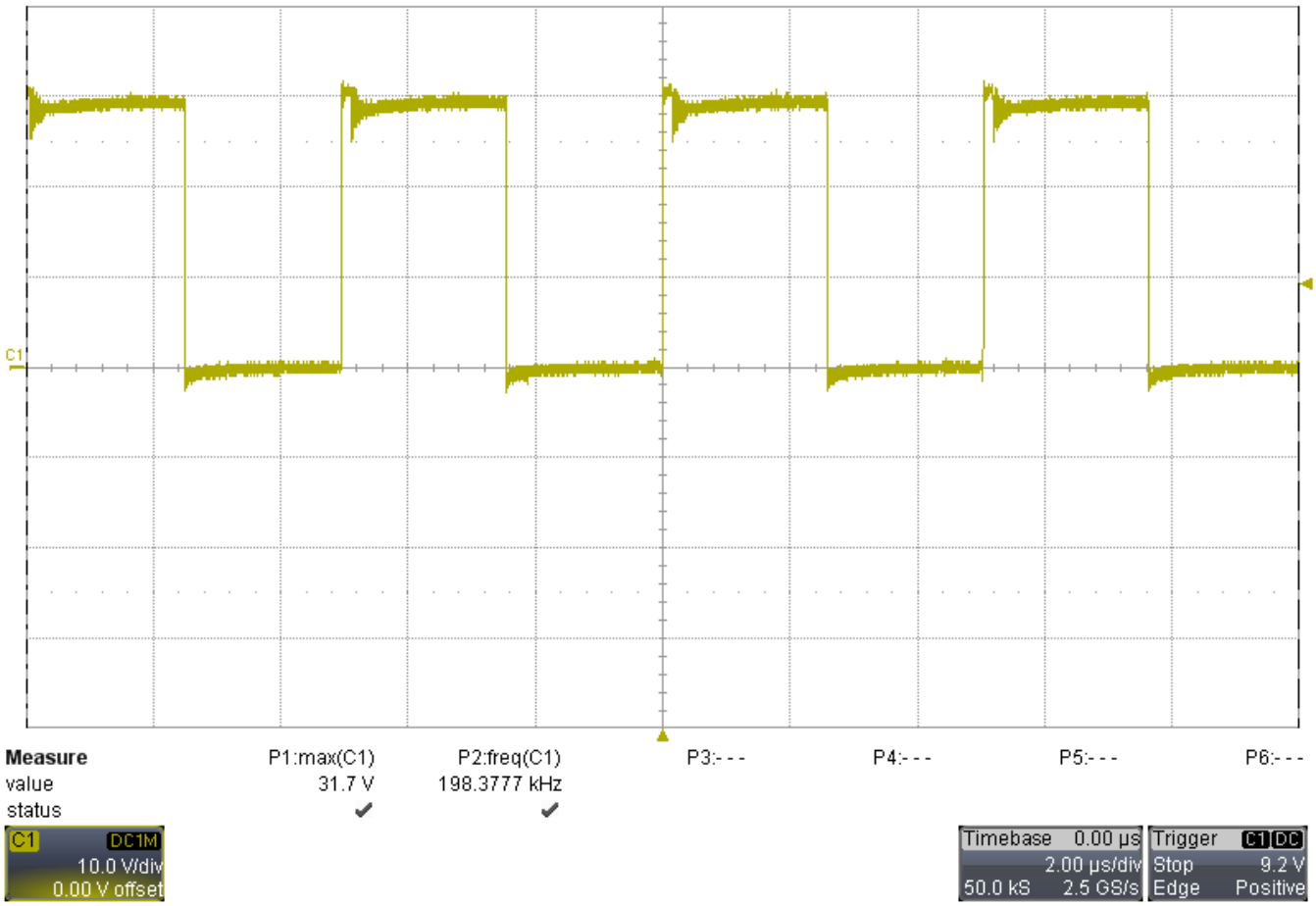

Figure 8. Primary Switching Node with 15 Vdc input

3.2 Output Voltage Ripple

Measurements were taken using the tip and barrel method across the output cap with the output at full load and a 12 Vdc input.

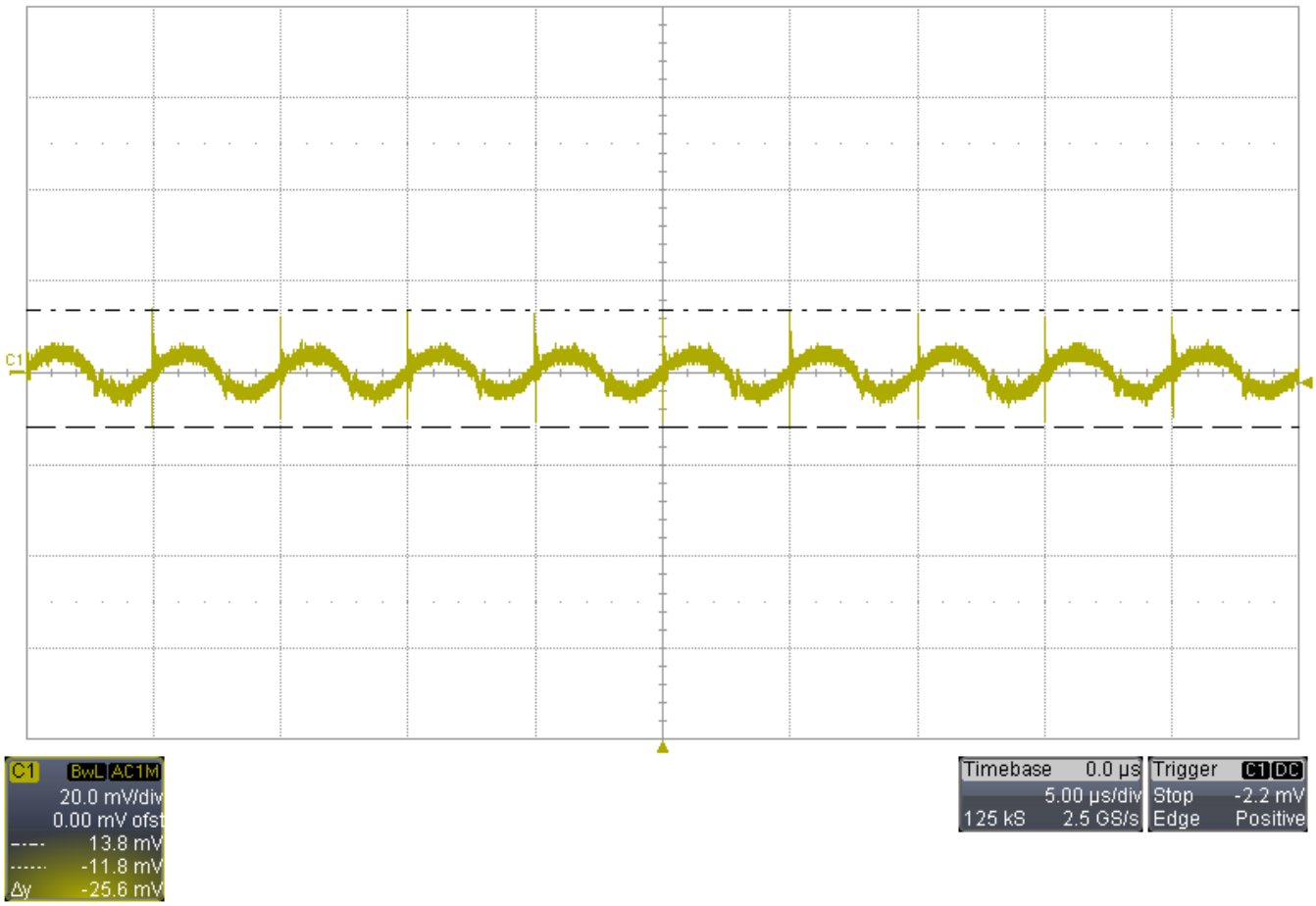

Figure 9.

3.3 Load Transients

For this measurement the output was stepped between 0.1 and 1 A with a 12 Vdc input

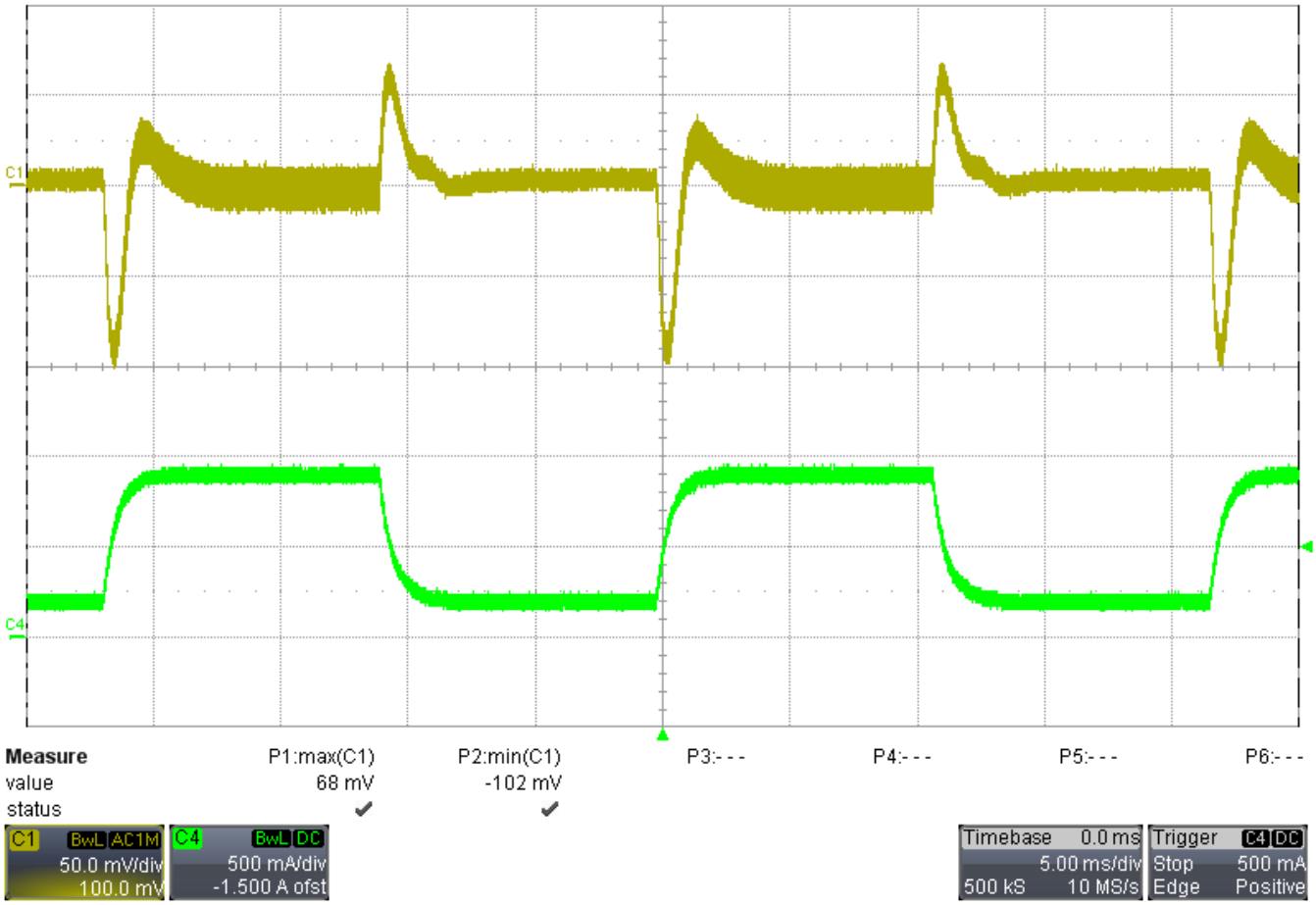

Figure 10.

3.4 Control Loop/Stability

For this measurement the 3.3 V output was loaded to 1.1 A. Measurements are shown for 9 V, 12 V, and 15 V input cases. The table below shows the bandwidth and phase margin measurements for the different input voltages.

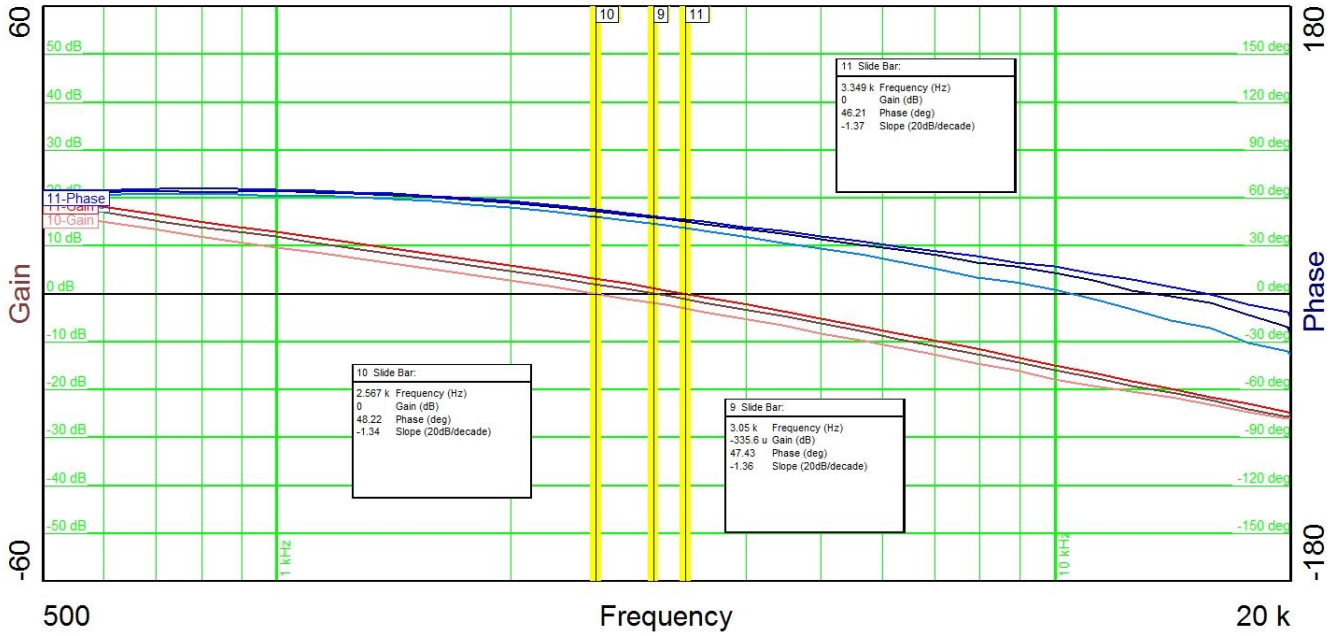

Figure 11.

Input Voltage (V)	Bandwidth (kHz)	Phase Margin (degrees)
9	2.567	48.22
12	3.050	47.43
15	3.349	46.21

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