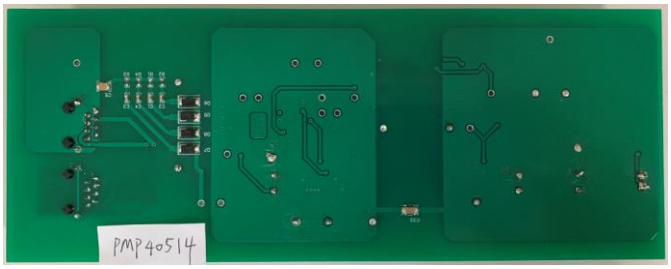
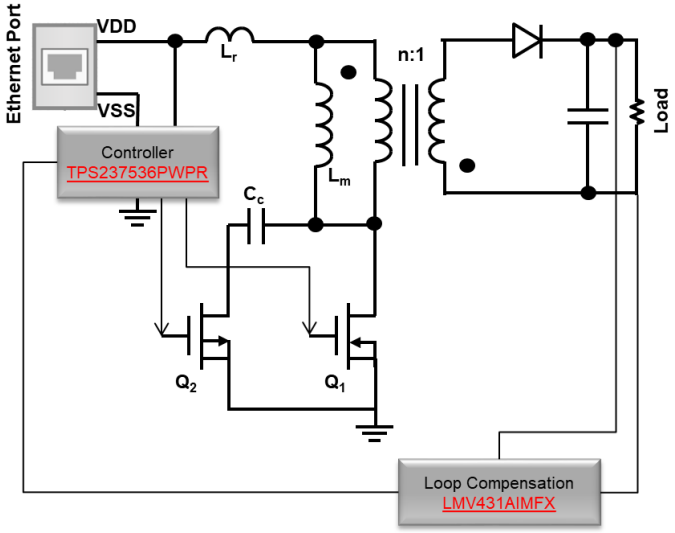
Test Report: PMP40514

Class 3 isolated high-efficiency active clamp flyback converter for PoE power reference design

Description

This design is developed for evaluating 13-W isolated active clamp flyback PD converter system using the IEEE 802.3at PoE interface and DC/DC controller TPS23756. The converter is capable of supporting the 13-W maximum IEEE 802.3at power requirements. It presents good efficiency, load regulation and related electrical performance.





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	36V - 57V, 48V normally
V_{OUT}	12V
I_{OUT}	1Amax
Switching Frequency	150kHz constant

*1.2 Required Equipment**

- Multi-meter(voltage): Agilent 34410A
- Multi-meter(current): Agilent 34410A
- DC Source: Chroma 62006P-100-25
- E-Load: Chroma 6314A
- Thermal Imager: FLIR i50
- Frequency Response Analyzer: AP Instruments FRA3001889

*1.3 Considerations**

The switching frequency is approximately 150 kHz constant. All measurements were done using the DC source to simulate PoE PSE.

2 Testing and Results

2.1 Efficiency Graphs

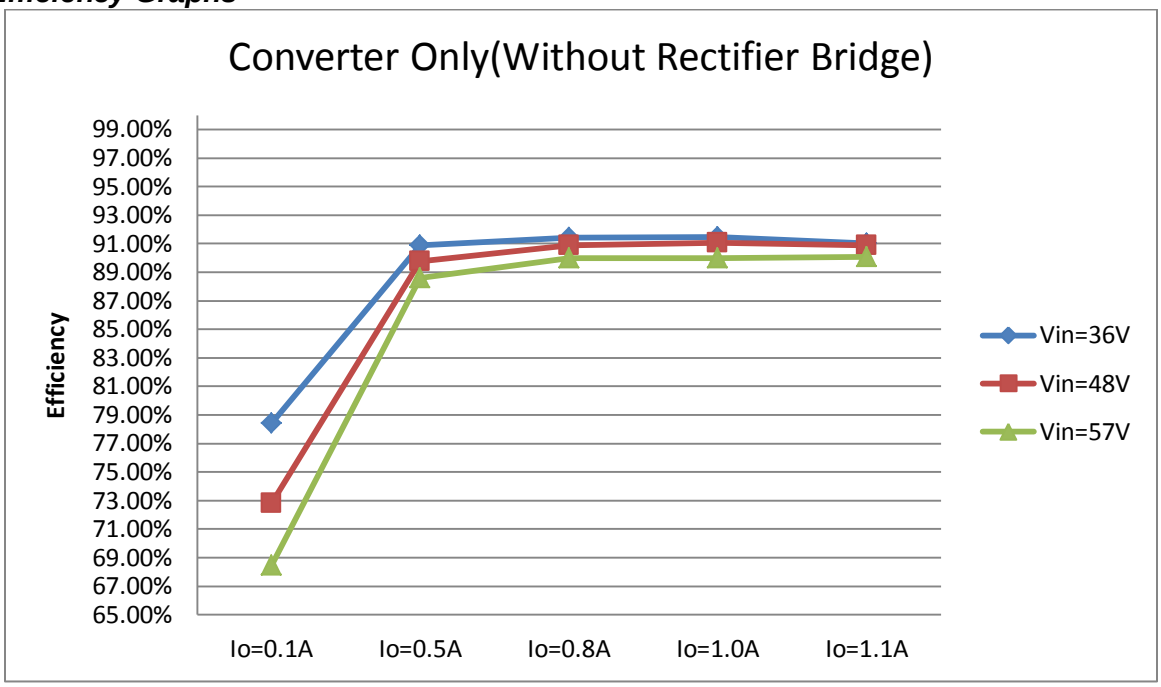


Figure1. Efficiency Graph (Converter Only)

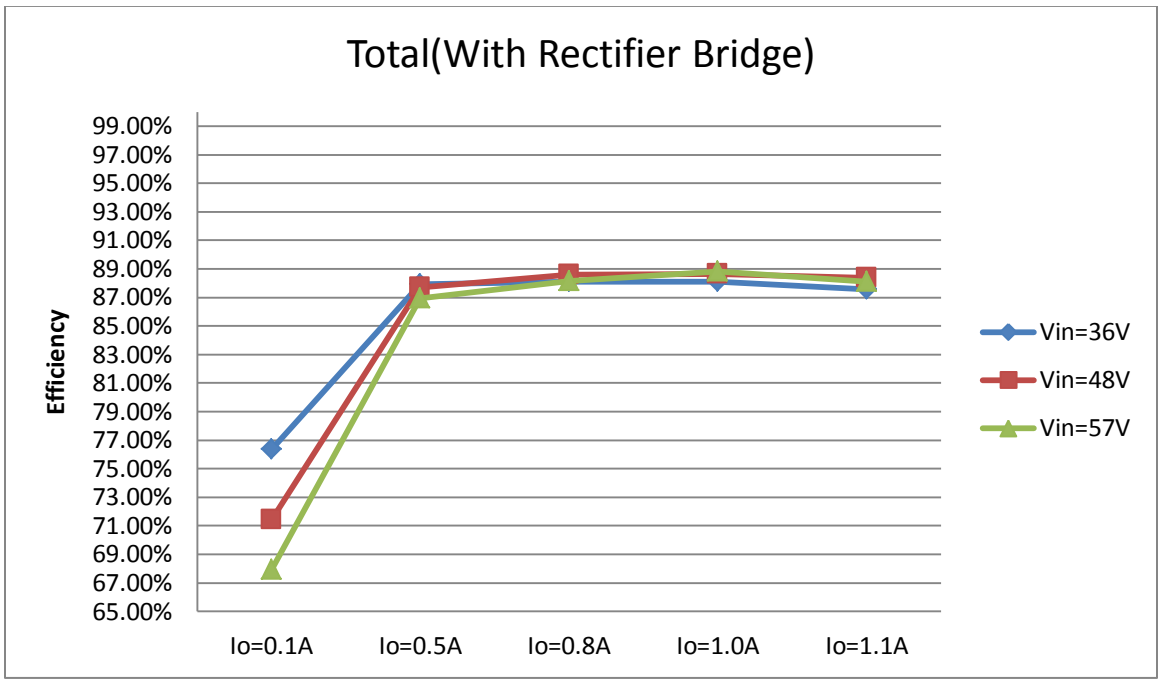


Figure2. Efficiency Graph (Total)

2.2 Efficiency Data*

Table 2. $36V_{IN}$ Efficiency Data

V_{IN_BD}(V)	V_{IN_CONV}(V)	I_{IN}(mA)	V_{OUT}(V)	I_O(mA)	P_{IN_BD}(W)	P_{IN_CONV}(W)	P_{OUT}(W)	Eff_{TOTAL}	Eff_{CONV}
36.28	35.47	8.3	12.036	0	0.301	0.294	0	0	0
36.26	35.44	11.6	12.044	10	0.419	0.410	0.120	28.73%	29.40%
36.18	35.24	43.6	12.045	100	1.577	1.536	1.205	76.36%	78.40%
36.18	35.00	189.5	12.056	500	6.856	6.632	6.028	87.92%	90.89%
36.12	34.82	302.9	12.052	800	10.941	10.547	9.642	88.13%	91.42%
36.07	34.74	381.0	12.106	1000	13.743	13.236	12.106	88.10%	91.46%
36.03	34.66	420.5	12.060	1100	15.151	14.575	13.266	87.56%	91.02%

Table 3. $48V_{IN}$ Efficiency Data

V_{IN_BD}(V)	V_{IN_CONV}(V)	I_{IN}(mA)	V_{OUT}(V)	I_O(mA)	P_{IN_BD}(W)	P_{IN_CONV}(W)	P_{OUT}(W)	Eff_{TOTAL}	Eff_{CONV}
48.38	47.57	8.5	12.027	0	0.413	0.406	0	0	0
48.37	47.55	11.0	12.040	10	0.532	0.523	0.120	22.63%	23.02%
48.31	47.39	34.9	12.042	100	1.686	1.654	1.204	71.42%	72.81%
48.32	47.20	142.5	12.075	500	6.886	6.726	6.038	87.68%	89.76%
48.26	47.04	226.0	12.079	800	10.907	10.631	9.663	88.60%	90.90%
48.23	46.94	282.8	12.091	1000	13.639	13.275	12.091	88.65%	91.08%
48.21	46.90	310.6	12.033	1100	14.974	14.567	13.236	88.40%	90.86%

Table 4. $57V_{IN}$ Efficiency Data

V_{IN_BD}(V)	V_{IN_CONV}(V)	I_{IN}(mA)	V_{OUT}(V)	I_O(mA)	P_{IN_BD}(W)	P_{IN_CONV}(W)	P_{OUT}(W)	Eff_{TOTAL}	Eff_{CONV}
57.45	56.64	8.7	12.020	0	0.501	0.494	0	0	0
57.45	56.63	10.8	12.038	10	0.620	0.612	0.12038	19.40%	19.68%
57.39	56.94	30.9	12.041	100	1.773	1.759	1.2041	67.90%	68.44%
57.40	56.32	120.7	12.046	500	6.928	6.798	6.023	86.93%	88.60%
57.36	56.17	190.8	12.056	800	10.944	10.717	9.6448	88.13%	89.99%
57.08	56.33	238.5	12.089	1000	13.613	13.435	12.089	88.80%	89.98%
57.31	56.04	261.9	12.020	1100	15.009	14.677	13.222	88.09%	90.09%

2.3 Thermal Images

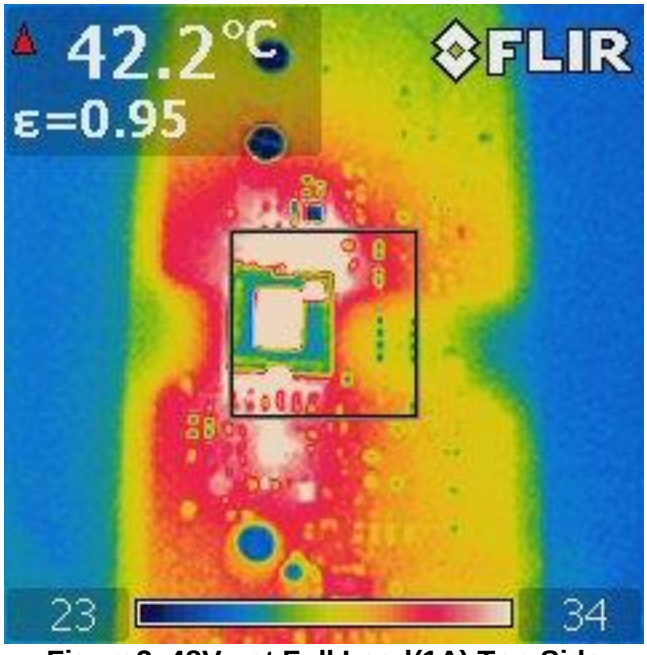


Figure2. $48V_{IN}$ at Full Load(1A) Top Side

3 Waveforms

*3.1 Switching**

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

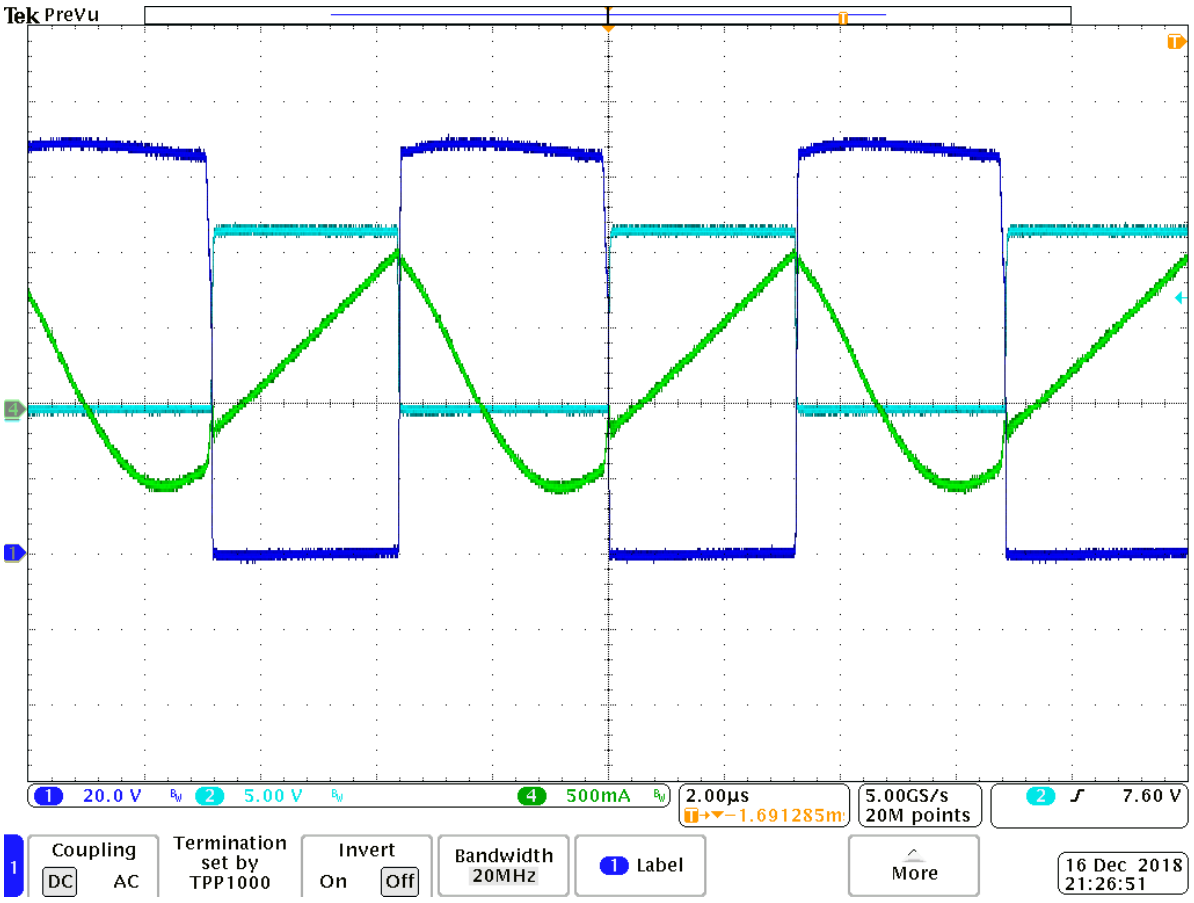


Figure3. Main Waveforms at 57V_{IN} and Full Load(1A)

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

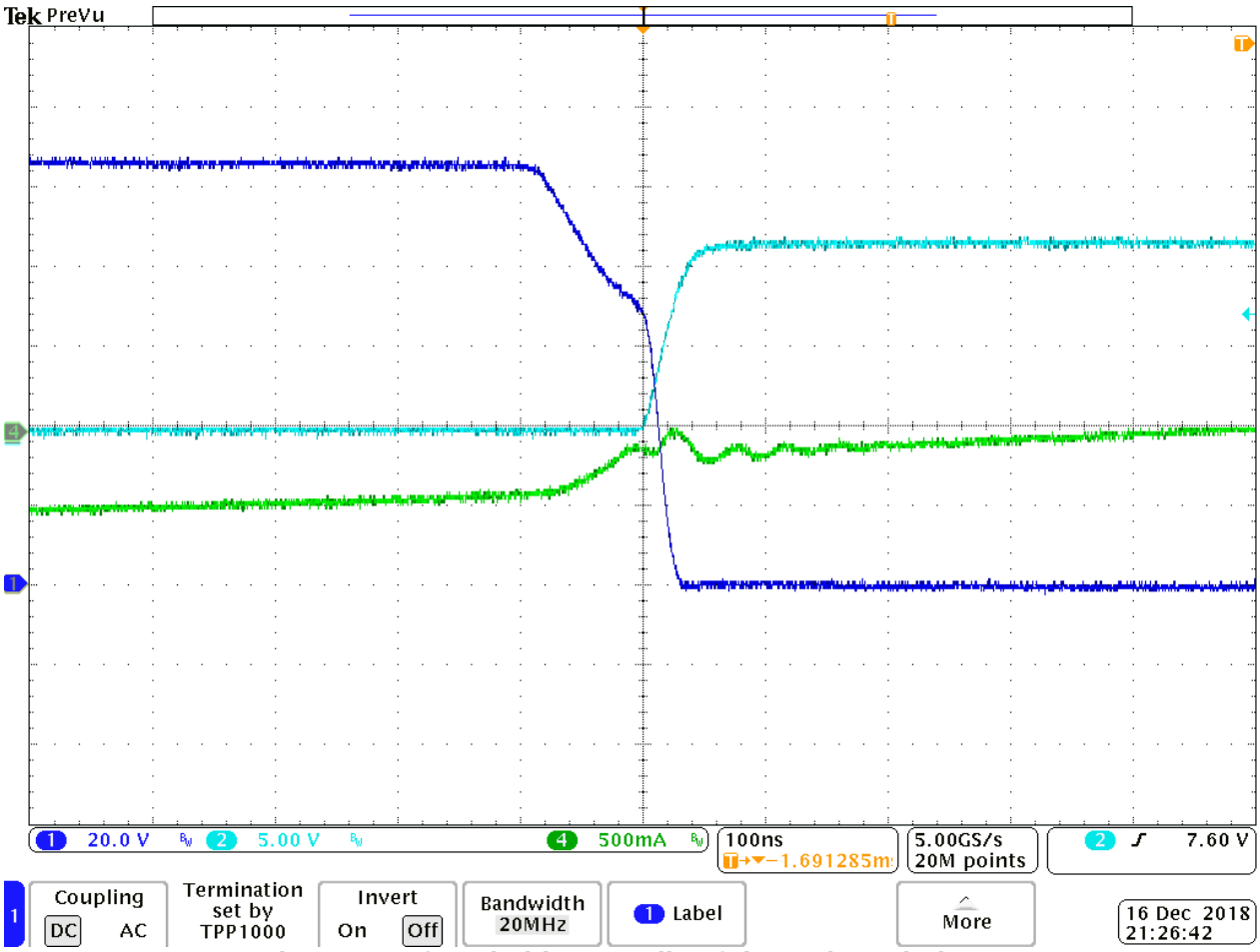


Figure4. Soft Switching Details of the Main Switch Q1 at 57V_{IN} and Full Load(1A)

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

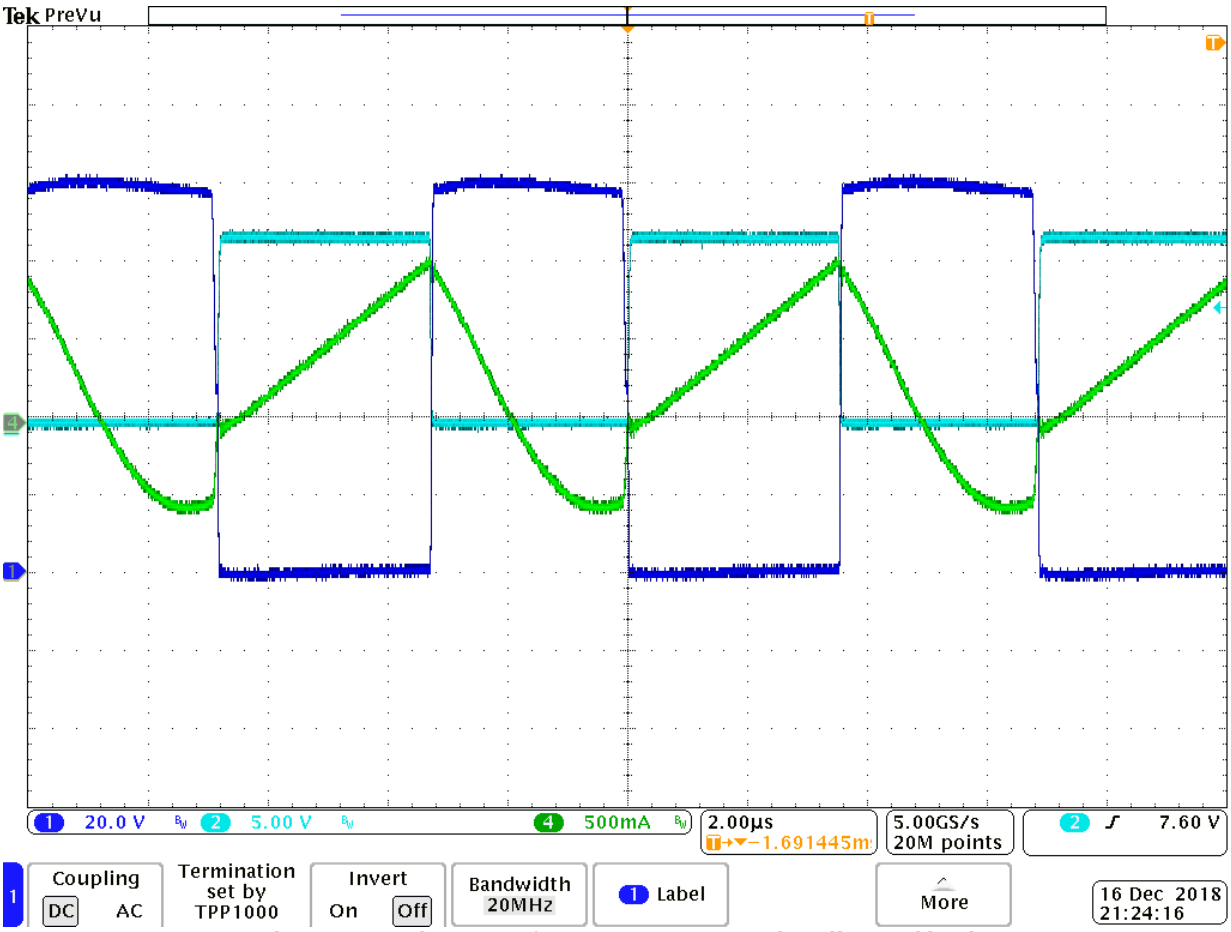


Figure5. Main Waveforms at 48V_{IN} and Full Load(1A)

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

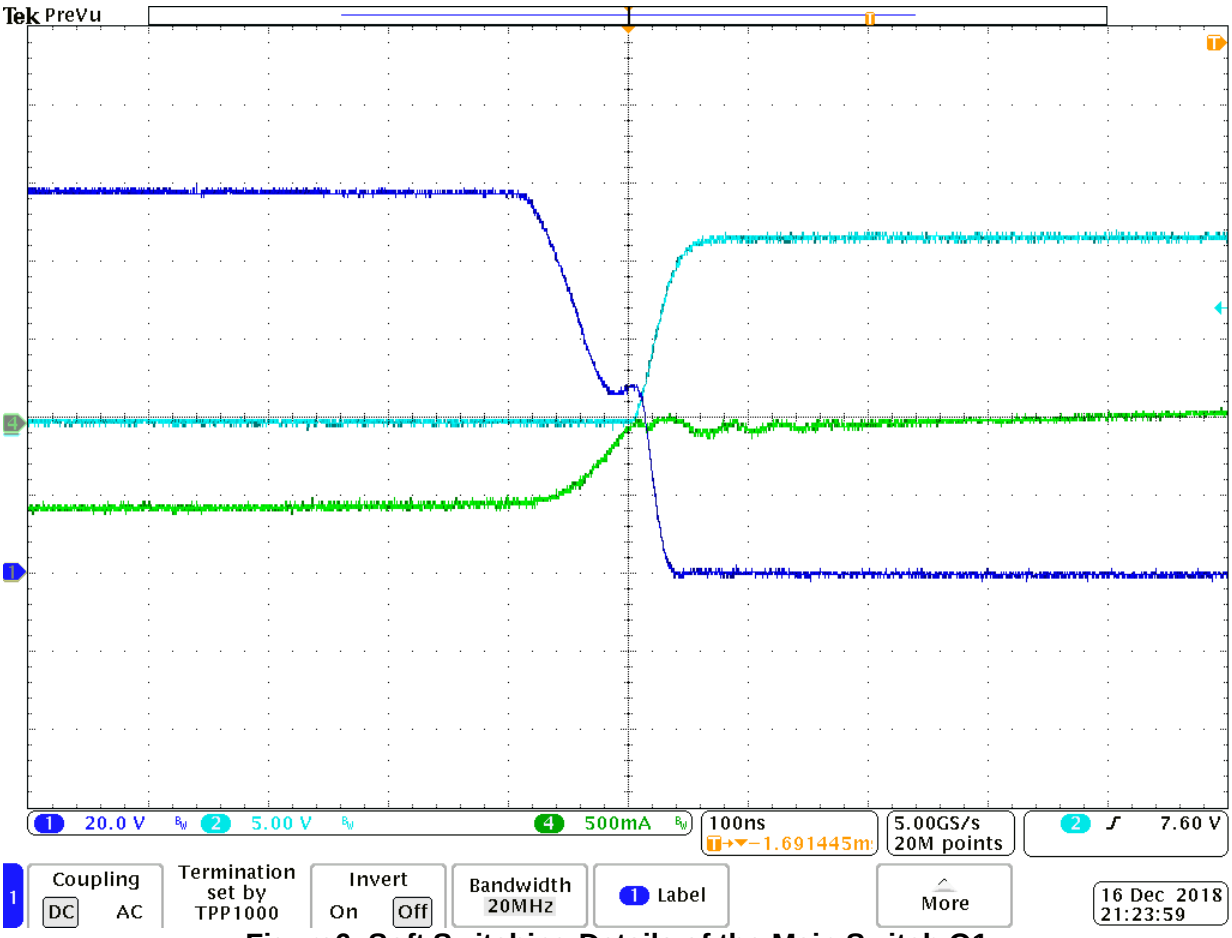


Figure6. Soft Switching Details of the Main Switch Q1 at 48V_{IN} and Full Load(1A)

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

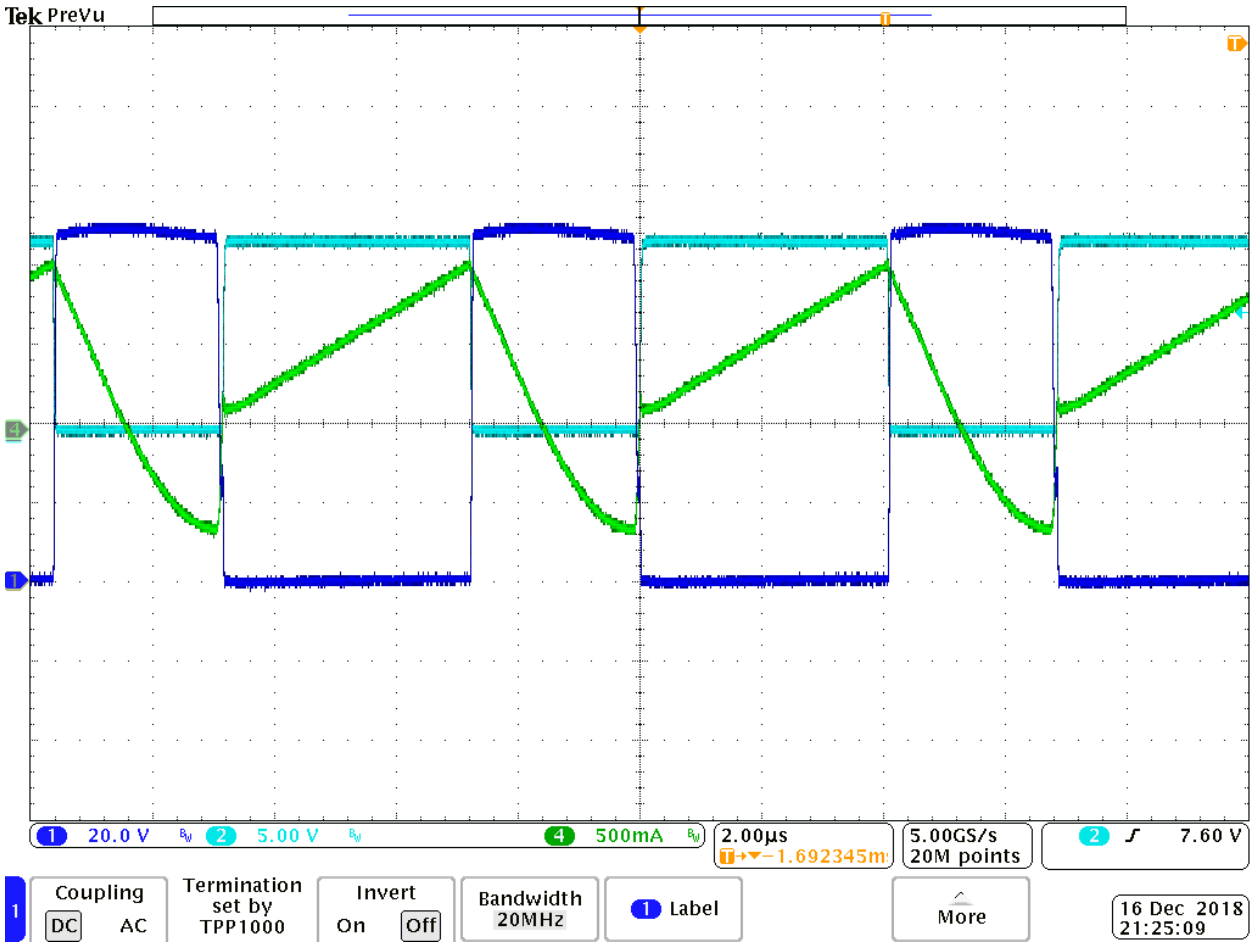


Figure7. Main Waveforms at 36V_{IN} and Full Load(1A)

Ch1: gate signal V_{gs} of the main switch Q1
Ch2: drain-source V_{ds} of the main switch Q1
Ch4: the resonant current I_{Lr} at the primary side

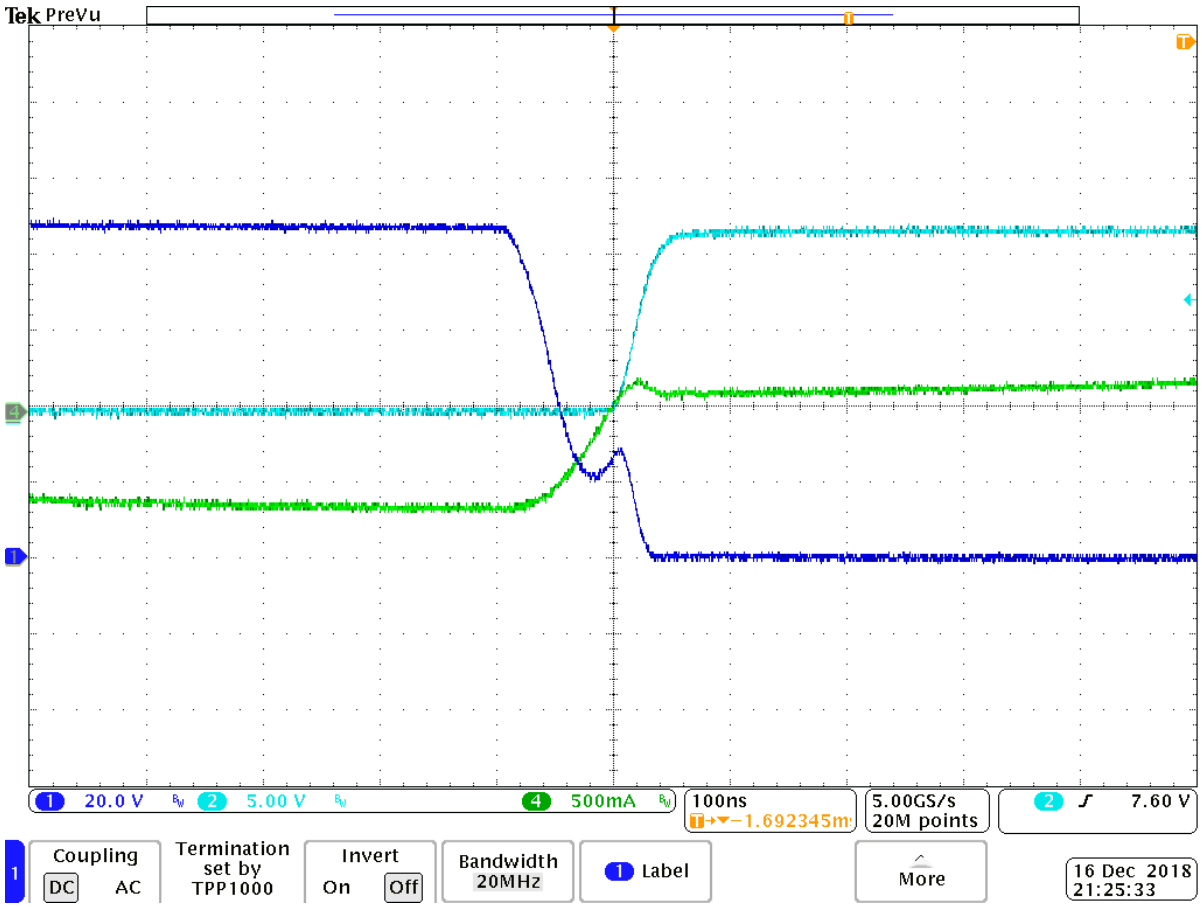


Figure8. Soft Switching Details of the Main Switch Q1 at 36V_{IN} and Full Load(1A)

Ch1-Ch2: the primary side voltage V_P of the transformer
Ch4: the resonant current I_{Lr} at the primary side

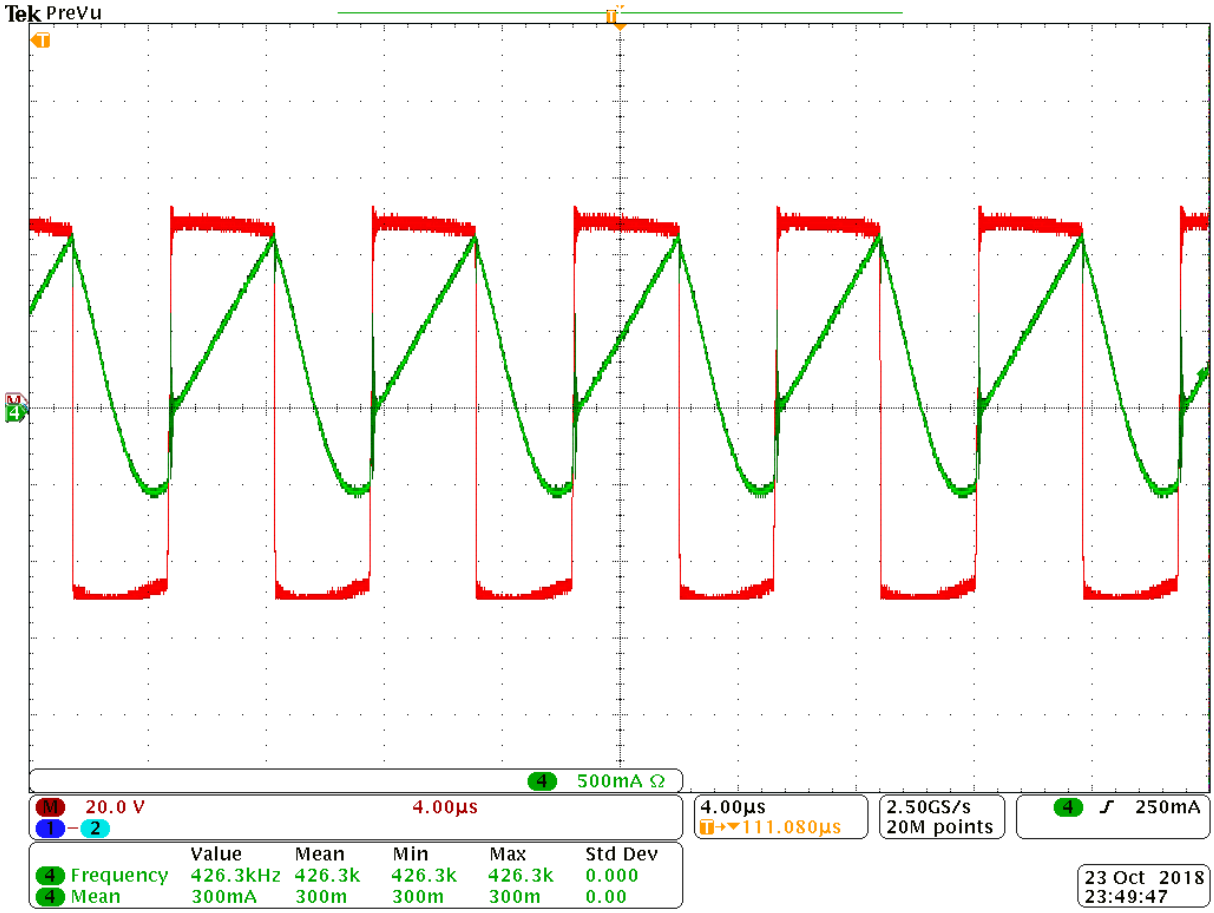


Figure5. Transformer Primary Side Waveforms at 48V_{IN} and Full Load(1A)

Ch1: the secondary side voltage V_S of the transformer
Ch4: the resonant current I_{Lr-S} at the secondary side

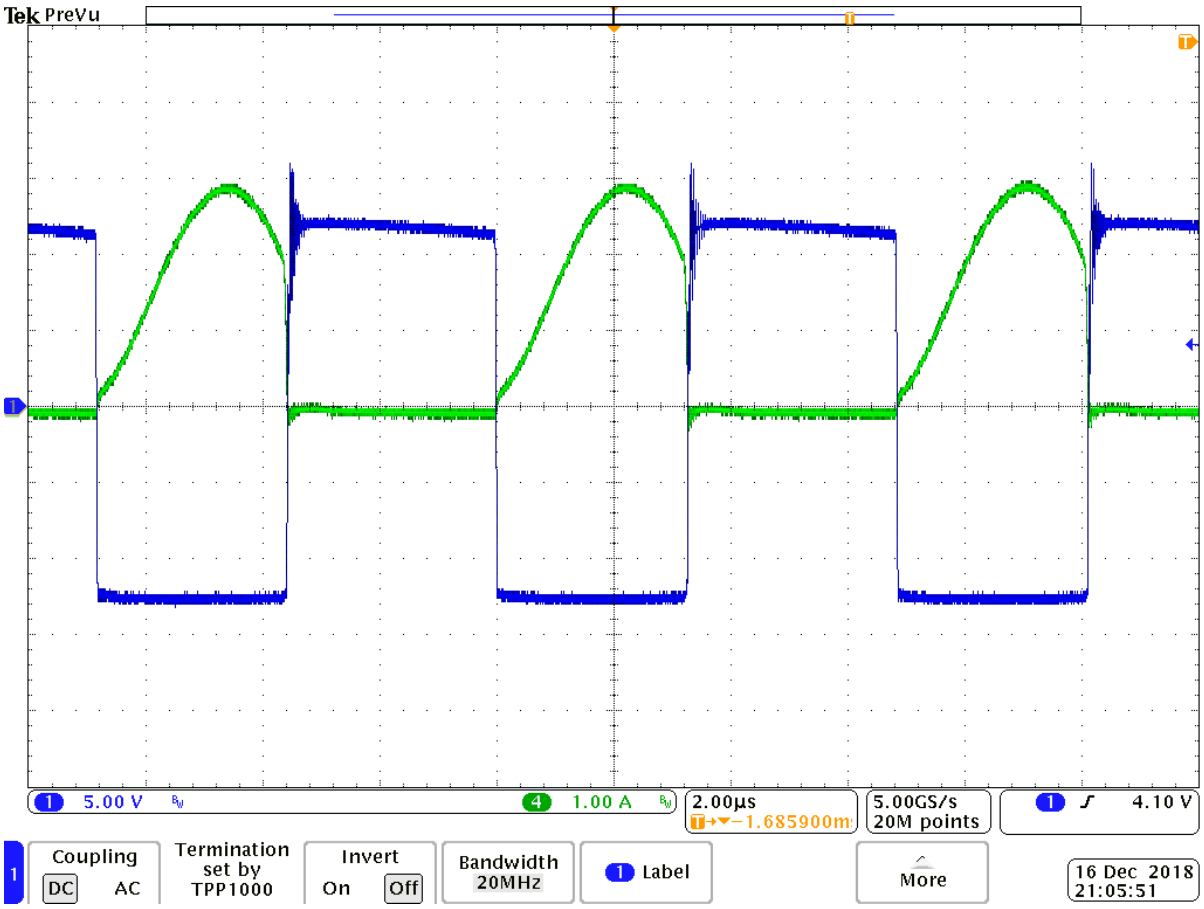


Figure6. Transformer Secondary Side Waveforms at 48V_{IN} and Full Load(1A)

3.2 Input Voltage Ripple*

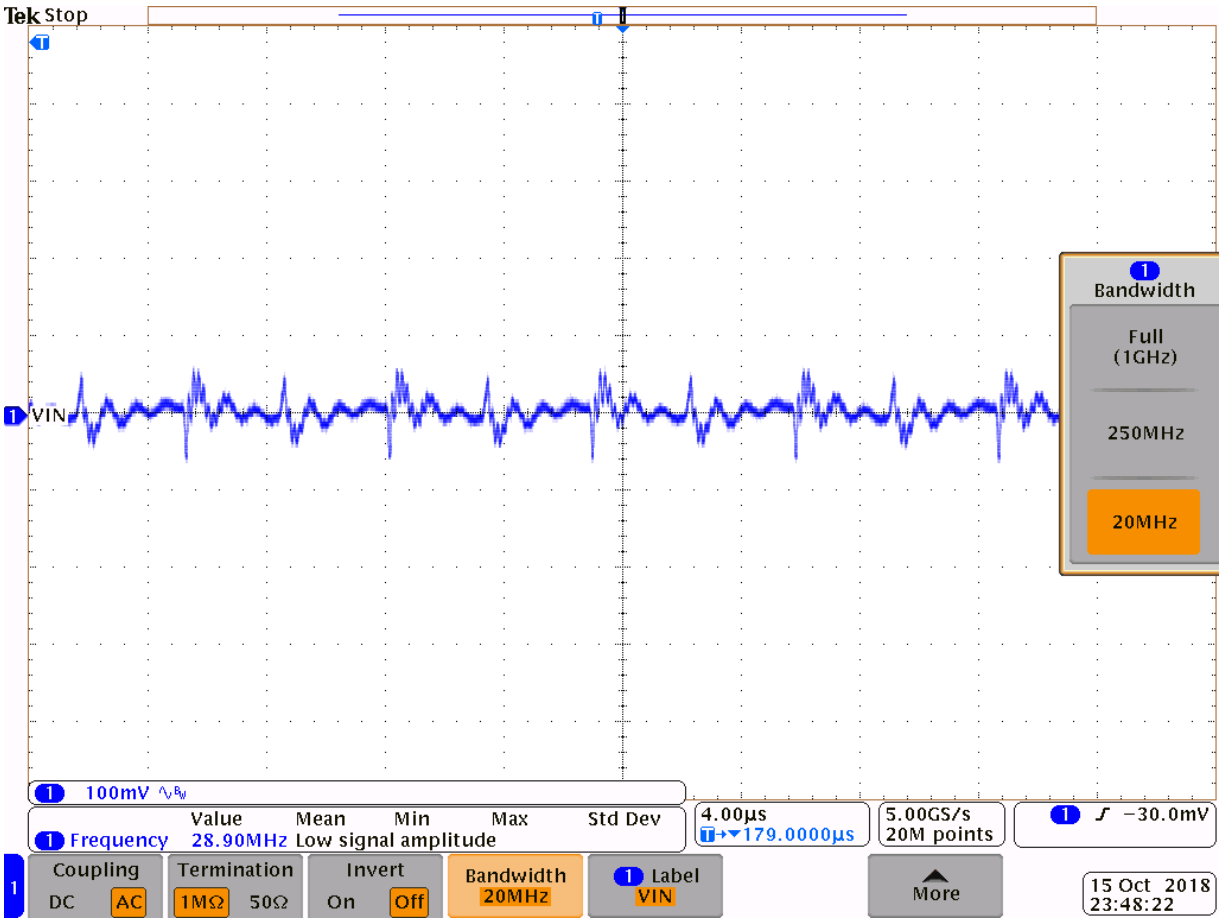


Figure7. Input Voltage AC Waveforms at 48V_{IN} and Full Load(1A)

3.3 Output Voltage Ripple*

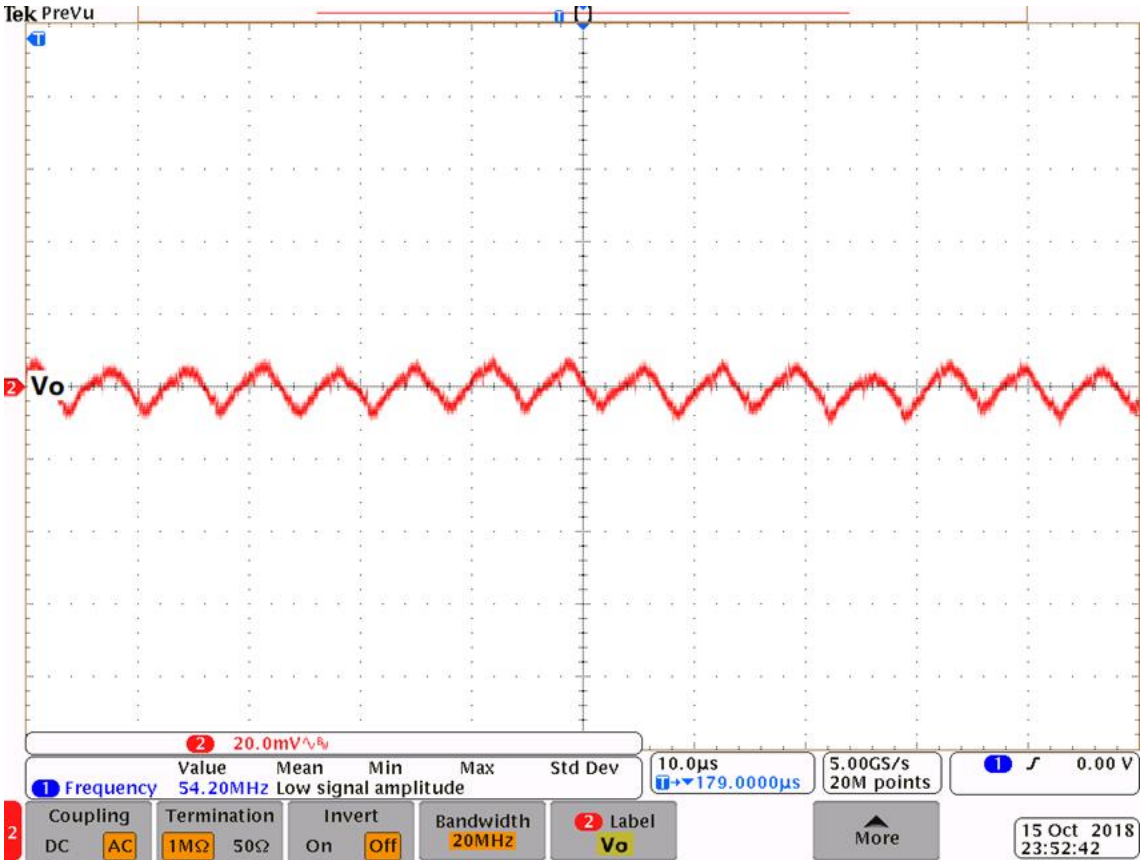


Figure8. Output Voltage AC Waveforms at 48V_{IN} and Full Load(1A)

3.4 Load Transients*

Ch1: the output AC voltage
Ch4: the output current from 0A to 1A(0.25A/us)

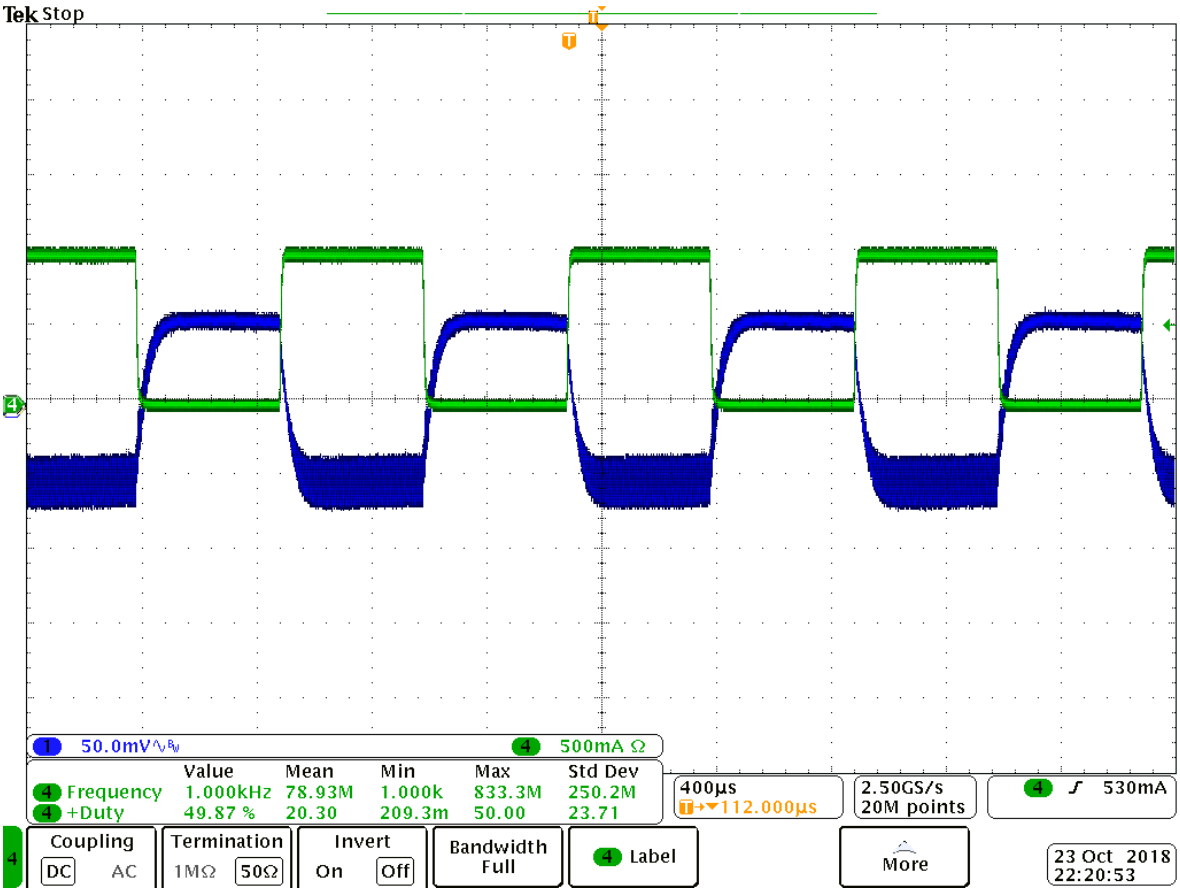


Figure9. Output Voltage AC Waveforms and Output Current Waveforms at 48V_{IN} and Full Load(1A)

3.5 Start-up*

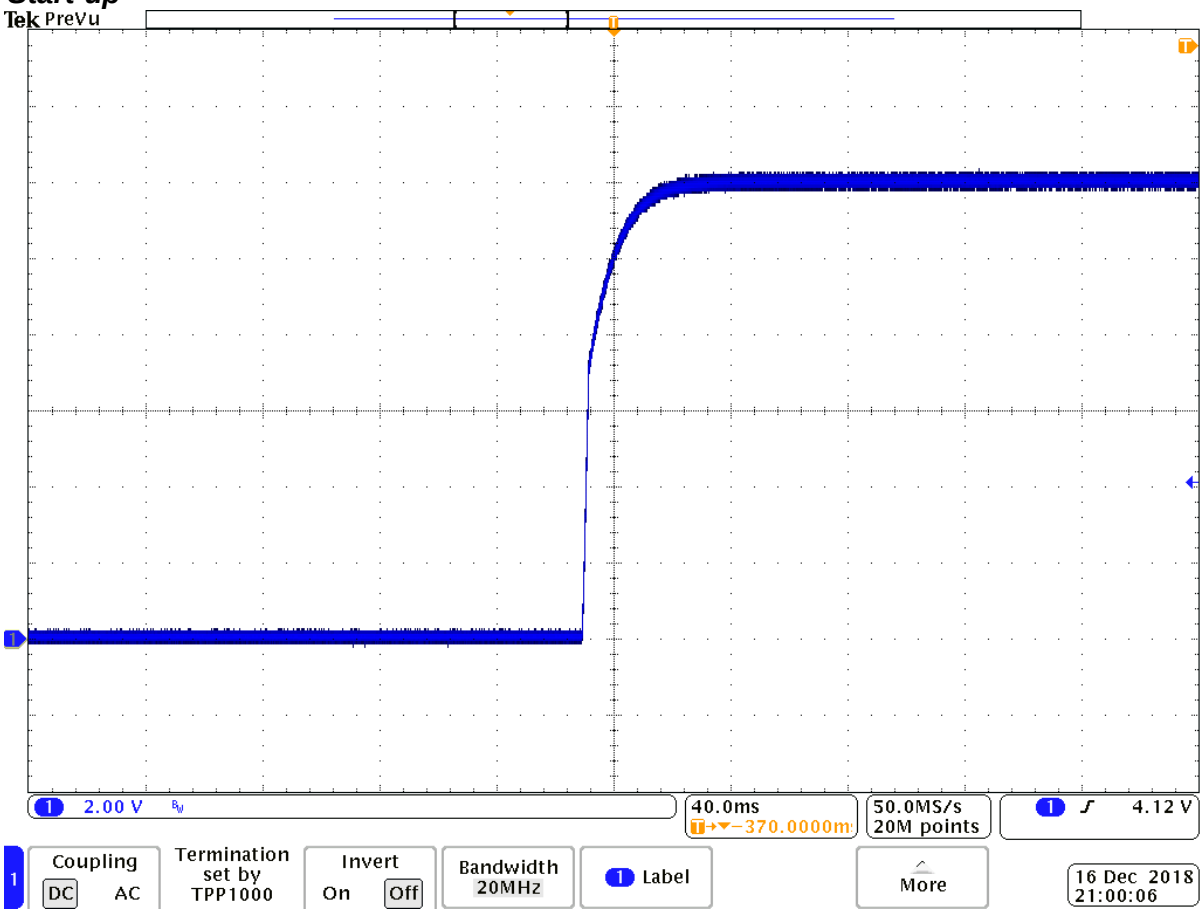


Figure10. Output Voltage Start-up Waveform at 48V_{IN} and Full Load(1A)

3.6 Control Loop Gain and Stability*

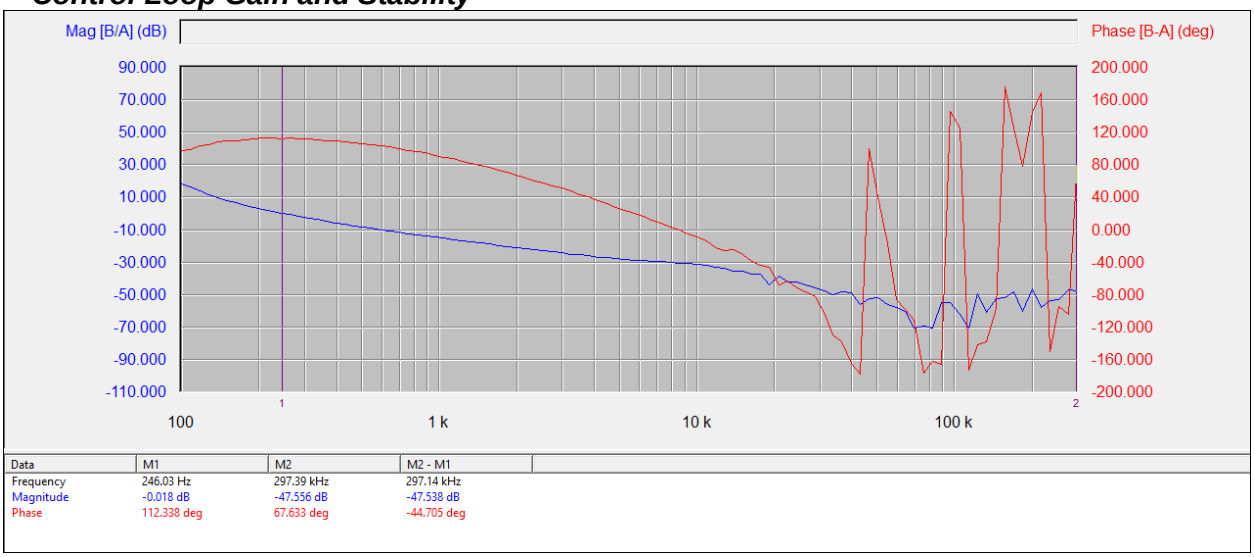


Figure11. Bode Plot at 48V_{IN} and No Load

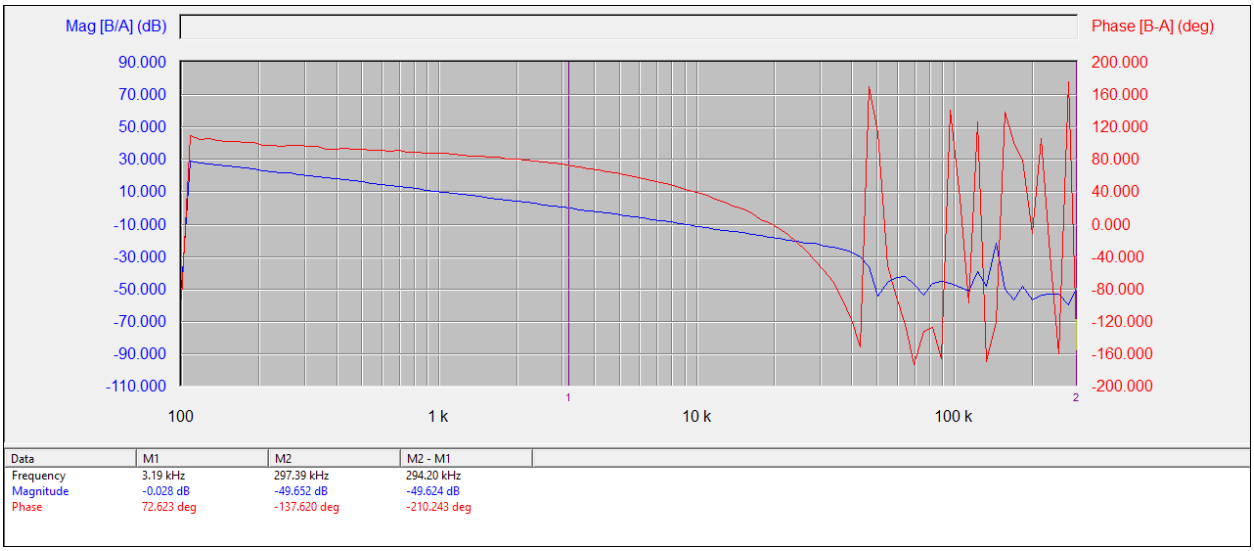


Figure12. Bode Plot at $48V_{IN}$ and Half Load(0.5A)

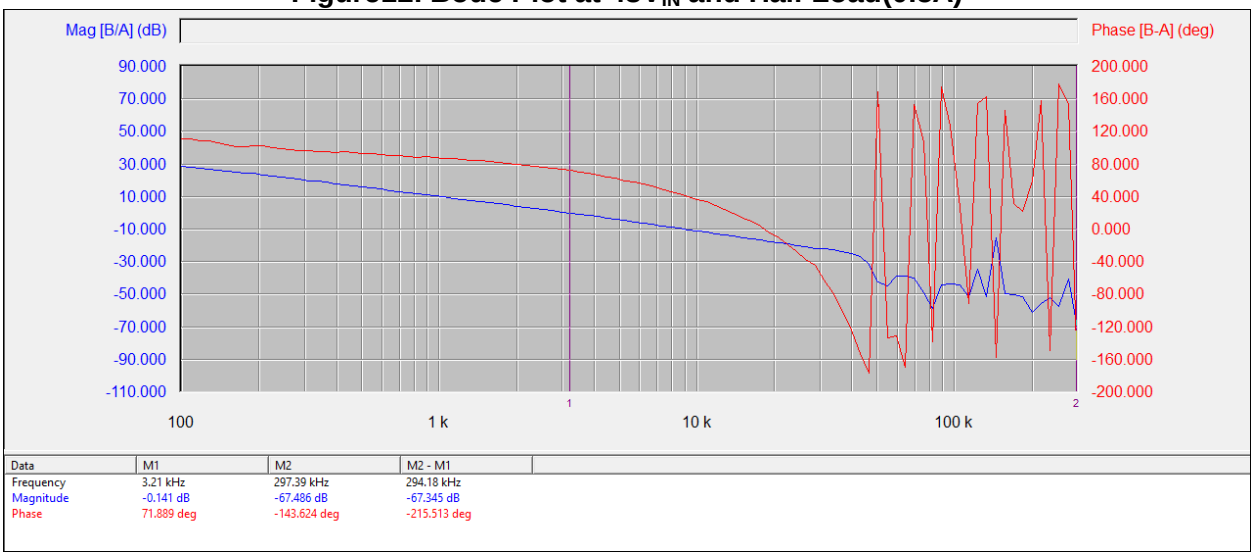


Figure13. Bode Plot at $48V_{IN}$ and Full Load(1A)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265