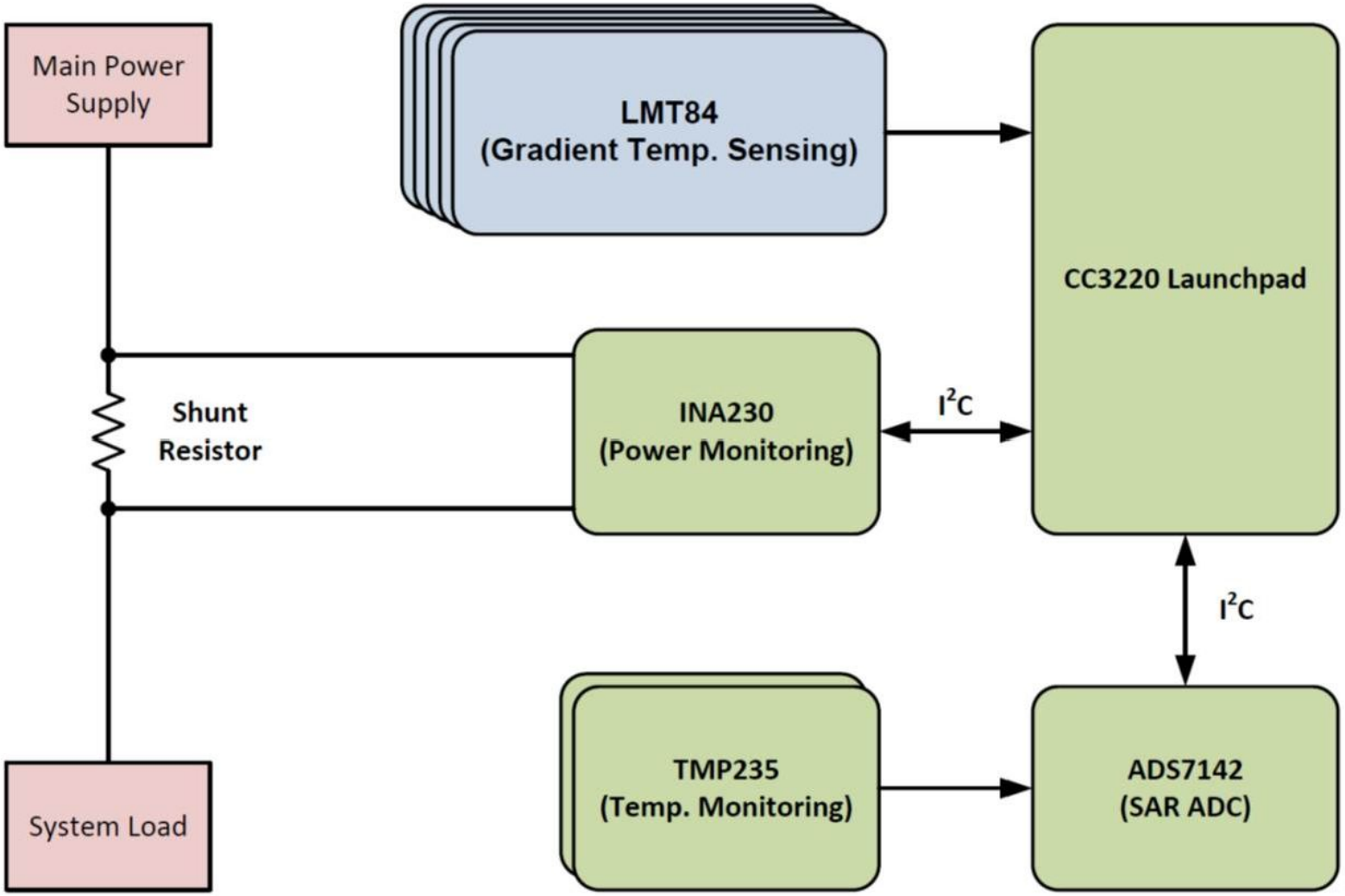
Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



Orderable: N/A	Designed for: Public Release	Mod. Date: 11/16/2017
TID #: TIDA-01596	Project Title: Smart Thermostat Temperature Compensation	
Number: TIDA-01596 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 4
Drawn By:	File: CoverSheet.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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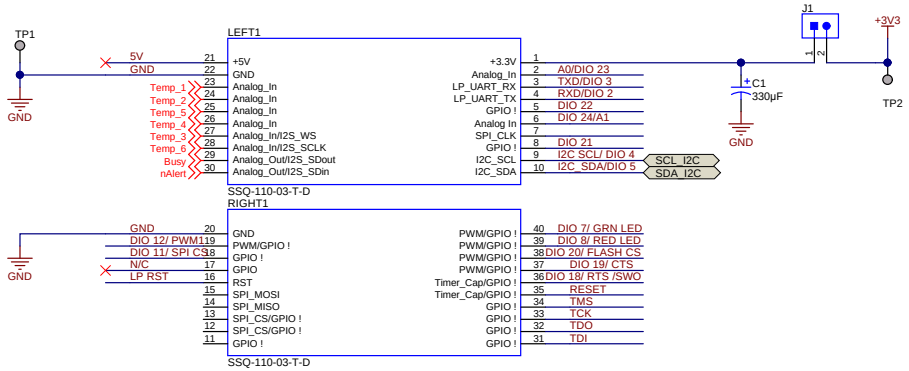

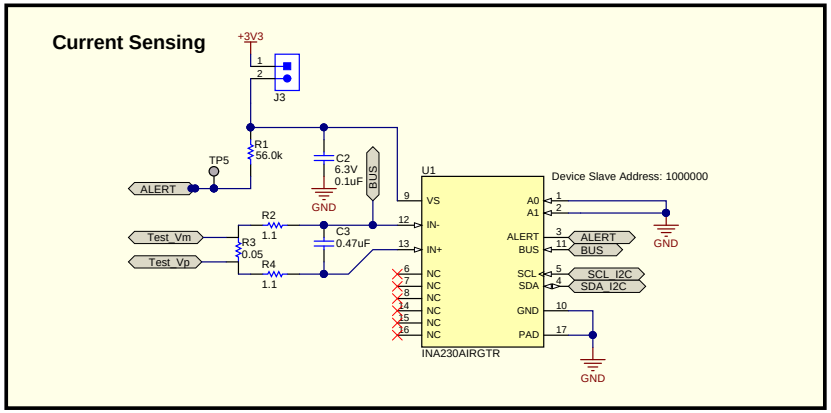

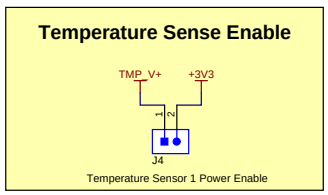

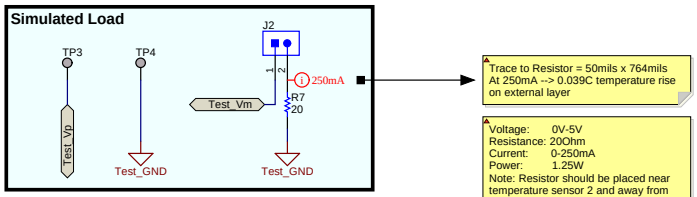

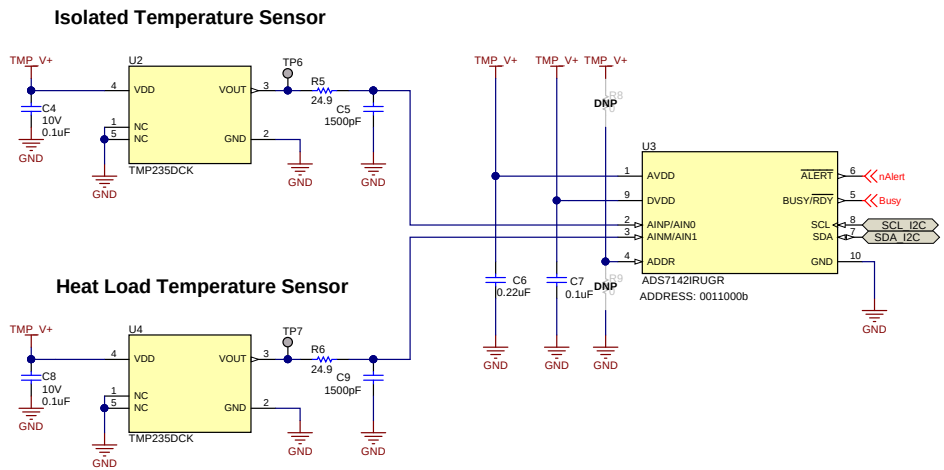

Orderable: N/A	Designed for: Public Release	Mod. Date: 1/31/2018
TID #: TIDA-01596	Project Title: Smart Thermostat Temperature Compensation	
Number: TIDA-01596 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 4
Drawn By:	File: Main Board.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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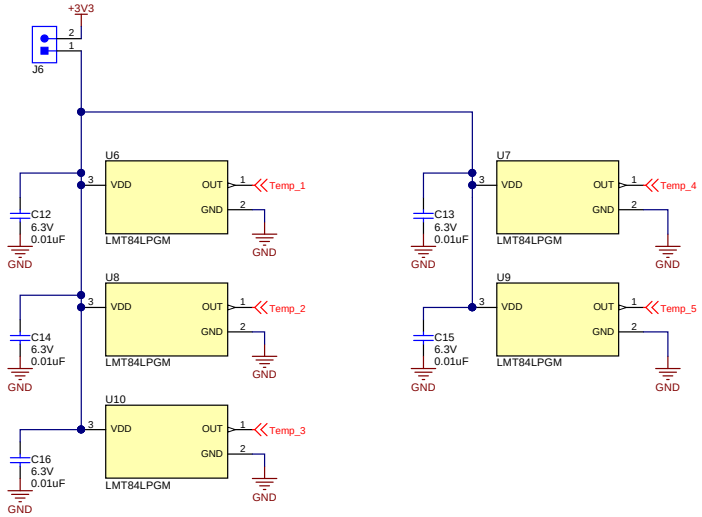

Orderable: N/A	Designed for: Public Release	Mod. Date: 11/16/2017
TID #: TIDA-01596	Project Title: Smart Thermostat Temperature Compensation	
Number: TIDA-01596 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 4
Drawn By:	File: Gradient Board Temp Sensors.SchDoc	Size: B
Engineer: Brian Dempsey	Contact: http://www.ti.com/support	

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H1 1
NY PMS 440 0025 PH

H2 1
NY PMS 440 0025 PH

H3 1
NY PMS 440 0025 PH

H4 1
NY PMS 440 0025 PH

H5
1902C

H6
1902C

H7
1902C

H8
1902C

SH-J1 SH-J2 SH-J3 SH-J4

DNP FID1

DNP FID2

DNP FID3

PCB Number: TIDA-01596
PCB Rev: E1

PCB LOGO

PCB LOGO

Variant/Label Table	
Variant	Label Text
001	TIDA-01596

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ3
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ4
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

Orderable: N/A		Designed for: Public Release	Mod. Date: 11/16/2017
TID #: TIDA-01596		Project Title: Smart Thermostat Temperature Compensation	
Number: TIDA-01596	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: 001	Sheet: 4 of 4
Drawn By:		File: EVM_Hardware.SchDoc	Size: B
Engineer: Brian Dempsey		Contact: http://www.ti.com/support	

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 2	FR-4 High TG	5.00mil	4.2	
5	Signal Layer	Copper	1.42mil		
6	Dielectric1	FR-4 High TG	9.00mil	4.2	
7	Main Power	Copper	1.42mil		
8	Dielectric 3	FR-4 High TG	5.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 31 MIL (0.8mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
[ ] MATTE [X] SEMI-GLOSS

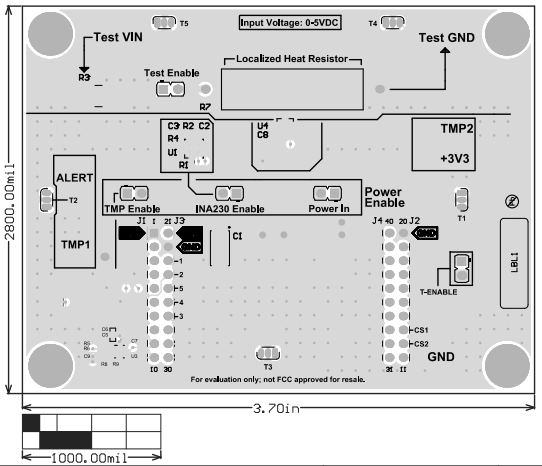
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [X] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [ ] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[ ] XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
[ ] LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



SH-J3

SH-J1 SH-J2 SH-J4

TEXAS INSTRUMENTS

PROJECT TITLE: Smart Thermostat Temperature Compensation

DESIGNED FOR: Public Release

FILE NAME: PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01596	REV: E1	SVN REV: Not In VersionControl
	TID #: TIDA-01596		
PLOT NAME = Multilayer Composite Print	GENERATED : 2/1/2018 7:24:45 AM	TEXAS INSTRUMENTS	

ENGINEER:	LAYOUT BY:
Brian Dempsey	Brian Dempsey
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472

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