Connectors

P8 Header

J1

	1	2	
MMC1_DAT6	3	4	MMC1_DAT7
MMC1_DAT2	5	6	MMC1_DAT3
TIMER4	7	8	TIMER7
TIMER5	9	10	TIMER6
GPIO1_13	11	12	GPIO1_12
EHRPWM2B	13	14	GPIO0_26
GPIO1_15	15	16	GPIO1_14
GPIO0_27	17	18	GPIO2_1
EHRPWM2A	19	20	MMC1_CMD
MMC1_CLK	21	22	MMC1_DAT5
MMC1_DAT4	23	24	MMC1_DAT1
MMC1_DAT0	25	26	GPIO1_29
LCD_VSYNC	27	28	LCD_PCLK
LCD_HSYNC	29	30	LCD_DE
LCD_DATA14	31	32	LCD_DATA15
LCD_DATA13	33	34	LCD_DATA11
LCD_DATA12	35	36	LCD_DATA10
LCD_DATA8	37	38	LCD_DATA9
LCD_DATA6	39	40	LCD_DATA7
LCD_DATA4	41	42	LCD_DATA5
LCD_DATA2	43	44	LCD_DATA3
LCD_DATA0	45	46	LCD_DATA1

SSHQ-123-D-08-F-LF

DGND DGND

EXPANSION HEADER

Outputs available from P8 header pins:

P8-11 PTO
P8-12 PTO
P8-15 PRU0_in
P8-16 PRU0_in

P8-7 Timer - DigO ser cape subaddress
P8-8 Timer - DigO - TIDA-00320
P8-9 Timer - DigO - TIDA-00320
P8-10 Timer - DigO - TIDA-00320
P8-13 EHRPWM2B DigO
P8-14 DigO - TIDA-00320

P8-17 DigO - TIDA-00320
P8-18 DigI - TIDA-00320
P8-19 EHRPWM2A
P8-26 DigI - TIDA-00320

Cape adressing:

Data transfer is done via SPI0. D0 is used as a signal from BBB to MSP430 and LED (MOSI). D1 is used as a signal from MSP and LED to BBB (MISO). P9-11 and P9-13 are the cape address lines. If they match the I2C address setting from switch S1 then the SPI access goes to this cape. P8-7 is a sub address which determines the onboard resource to access. If it is low then the SPI access goes to the output drivers, if high then to the 16 LEDs.

P9-23 is the interrupt (IRQ) line. An IRQ pulls it low via open drain from U26. The host (BBB) needs to poll all capes which have interrupt capability configured to identify the issuer of the IRQ.

P9 Header

J2

DGND	1	2	DGND
VDD_3V3B	3	4	VDD_3V3B
VDD_5V	5	6	VDD_5V
SYS_5V	7	8	SYS_5V
PWR_BUT	9	10	SYS_RESETn
UART4_RXD	11	12	GPIO1_28
UART4_TXD	13	14	EHRPWM1A
GPIO1_16	15	16	EHRPWM1B
SPI0_CS	17	18	SPI0_D1
I2C2_SCL	19	20	I2C2_SDA
SPI0_D0	21	22	SPI0_SCLK
GPIO1_17	23	24	UART1_TXD
GPIO3_21	25	26	UART1_RXD
GPIO3_19	27	28	SPI1_CS0
SPI1_D0	29	30	SPI1_D1
SPI1_SCLK	31	32	VDD_ADC
AIN4	33	34	GNDA_ADC
AIN6	35	36	AIN5
AIN2	37	38	AIN3
AIN0	39	40	AIN1
CLKOUT2	41	42	GPIO0_7
	43	44	
	45	46	

MISO MOSI

SSHQ-123-D-08-F-LF

DGND DGND

EXPANSION HEADER

Outputs available from P9 header pins:

P9-11 ser cape A0
P9-12 DigO - TIDA-00320
P9-13 ser cape A1
P9-14 PWM option
P9-15 DigO - TIDA-00320
P9-16 PWM option
P9-17 I2C1 SCL
P9-18 I2C1 SDA

P9-21 DigO - TIDA-00320
P9-22 DigO - TIDA-00320
P9-23 DigO - TIDA-00320
P9-24 UART1 TXD

P9-26 UART1 RXD
P9-27 PTO

VDD_3V3B
C2 0.1µF
DGND

Check level during boot
SPI0_CS

VDD_3V3B
C1 0.1µF
DGND

VDD_3V3B
U1A SN74LVC2G86DCTR
UART4_RXD
ser A0
DGND VDD_3V3B

U1B SN74LVC2G86DCTR
UART4_TXD
ser A1
DGND

VDD_3V3B
U2 SN74LVC1G332DCKR
DGND

MMC1_DAT5 R16 Close to P8
10.0

TP2

VDD_3V3B
U3
SN74LVC1G19DCKR
DGND

TP3

/CS1

GPIO1_17 R1 0 /XSDRDY
GPIO1_16 R2 0 XRST_n
SPI0_D0 R3 Close to P9 10.0 MOSI
SPI0_SCLK R5 Close to P9 10.0 SCLK
R6 Close to U3 10.0 /CS0
R7 Close to Iso 10.0 MISO

VDD_3V3B
R4 453
D1 Green
DGND

VDD_3V3B
U8 SN74LVC1G125DCKR
SPI0_D1
DGND

VDD_3V3B
C3 0.1µF
DGND

VDD_3V3B
C6 0.1µF
DGND

VDD_3V3B
C4 0.1µF
DGND

R8 5.62k
32KByte needed
U6
S1
219-4LPST
R9 5.62k
R10 5.62k
R11 5.62k
R12 5.62k
R13 5.62k
R18 10.0
I2C2_SCL
I2C2_SDA
SYS_5V
CAT24C256WI-G
DGND

C7 0.1µF
DGND

VDD_3V3B
TP4
LED_SOUT
U7 SN74LVC1G125DCKR
DGND

Alternatively R17 or U4 + R14 + C1

VDD_3V3B
C5 0.1µF
DGND

VDD_3V3B
R17 0
U4
SN74LVC1G58DCKR
/CS1
R14 5.62k
C8 100pF
DGND

U5
SPI0_SCLK
SPI0_D0
LED_SOUT
TP1
R15 21.0k
TLC5928DBQ
VDD_3V3B
DGND

D2 Orange
D3 Orange
D4 Orange
D5 Orange
D6 Orange
D7 Orange
D8 Orange
D9 Orange
D10 Red
D11 Red
D12 Red
D13 Red
D14 Red
D15 Red
D16 Red
D17 Red

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TID #: TIDA-01552	Project Title: 1A 8-Channel High Side Driver for PLC	
Number: TIDA-01552 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 2 of 7
Drawn By:	File: TIDA-01552_pg-1_BB_Connector.SchDoc	Size: B
Engineer: Ingolf Frank	Contact: http://www.ti.com/support	

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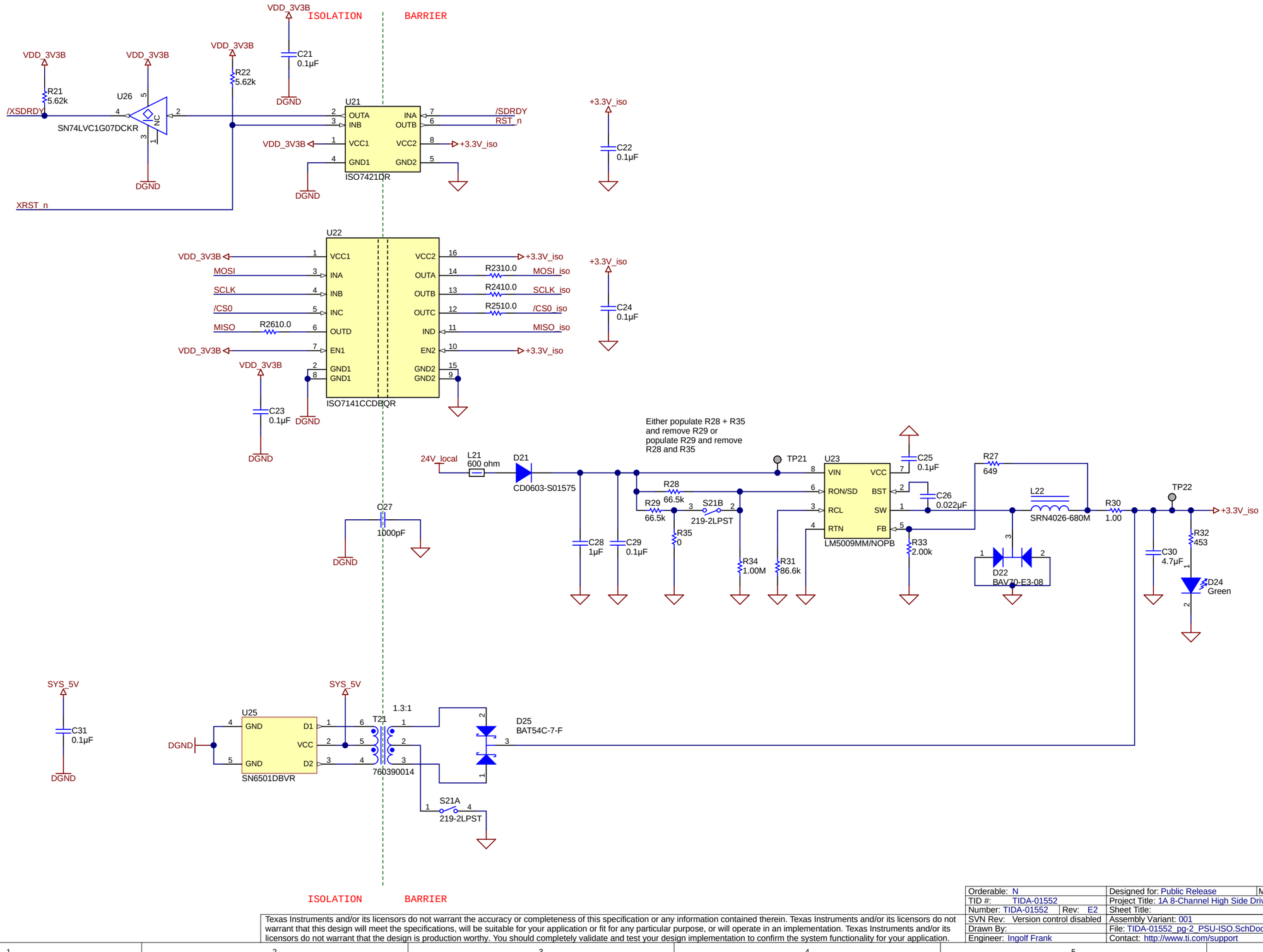
PSU isolation



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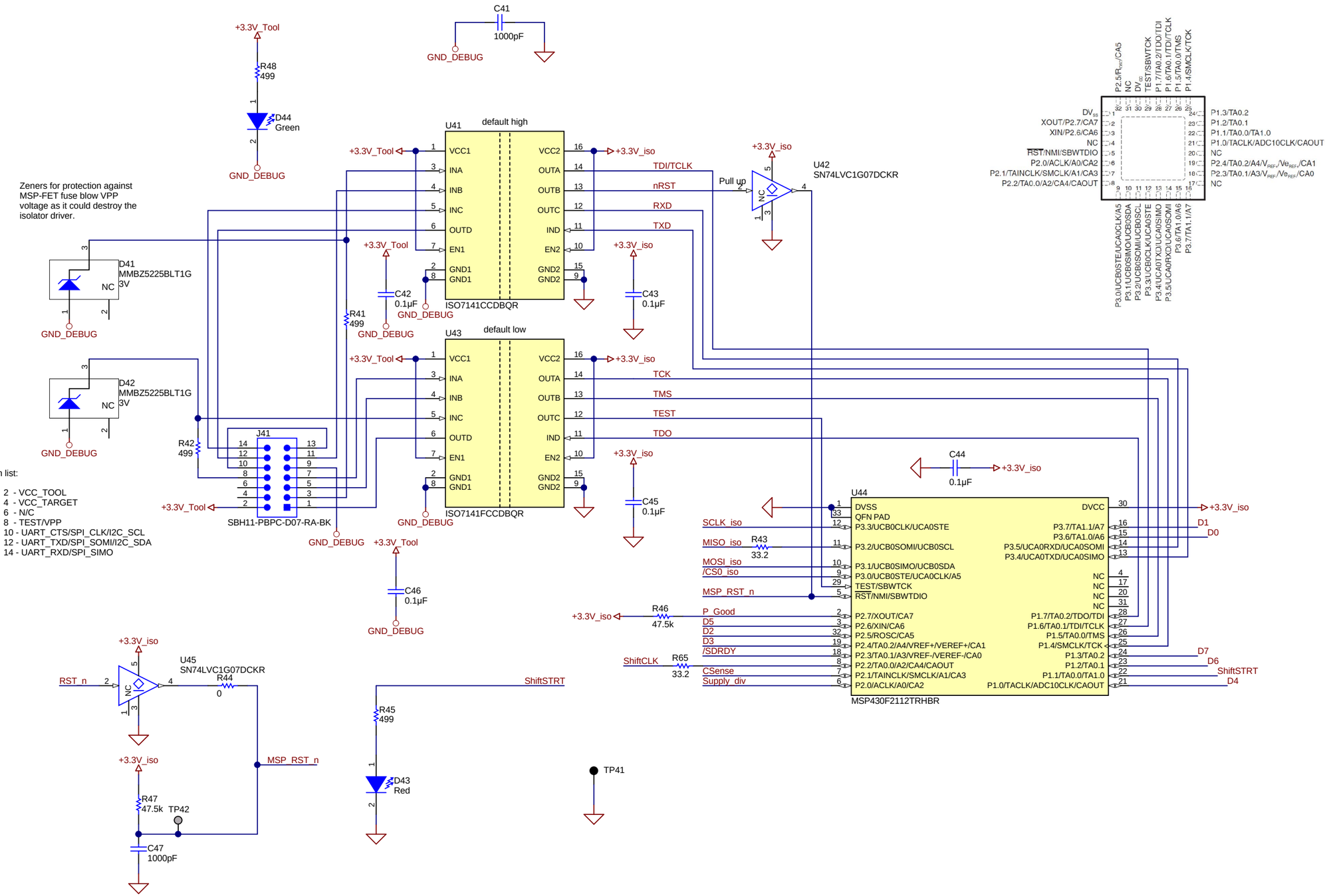
TID #: TIDA-01552	Project Title: 1A 8-Channel High Side Driver for PLC	
Number: TIDA-01552 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 7
Drawn By:	File: TIDA-01552_pg-2_PSU-ISO.SchDoc	Size: B
Engineer: Ingolf Frank	Contact: http://www.ti.com/support	

SerDes and debug



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Number: TIDA-01552 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 4 of 7
Drawn By:	File: TIDA-01552_pg-3_MCU.SchDoc	Size: B
Engineer: Ingolf Frank	Contact: http://www.ti.com/support	

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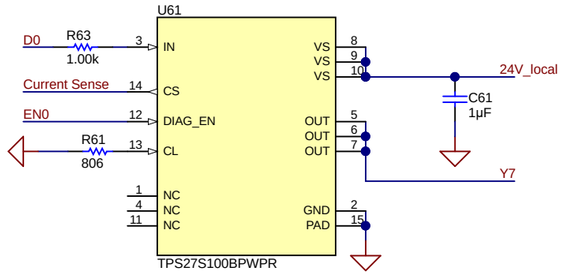
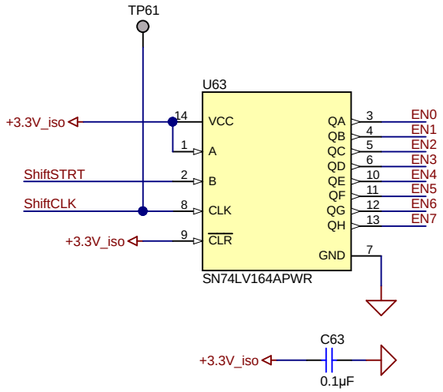
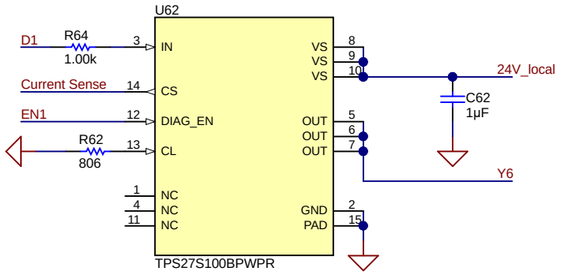
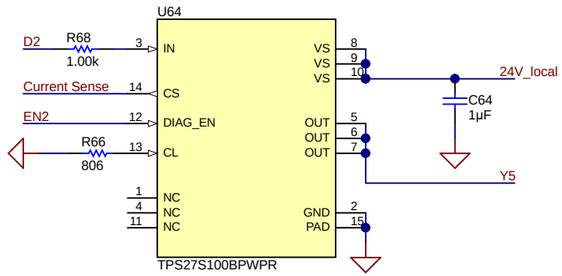
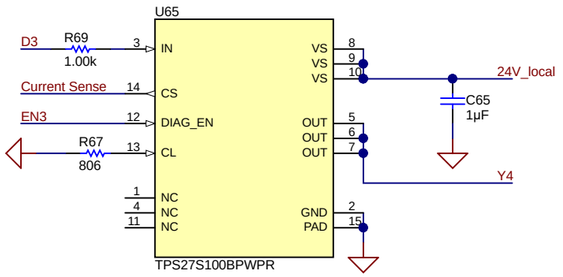
Power stages



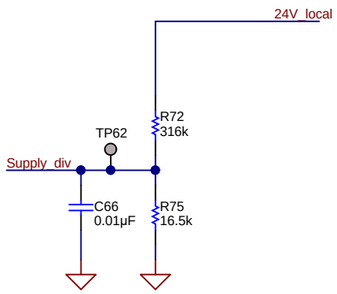


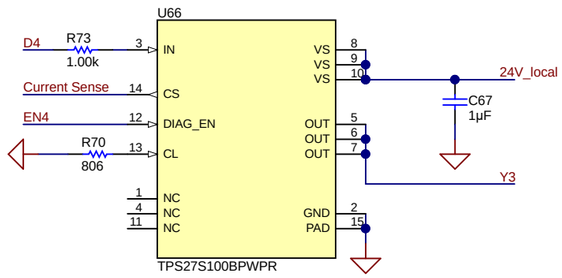


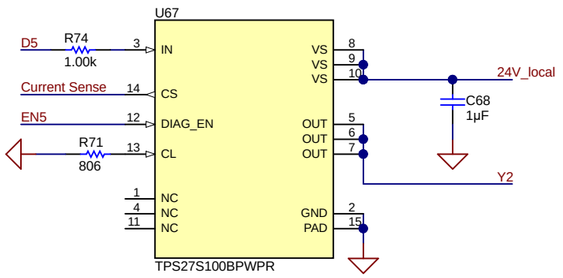




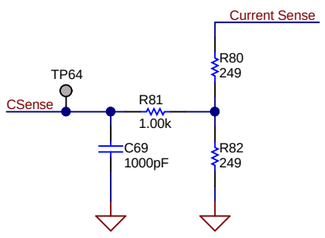
Filter frequency 1 kHz (-3dB), Ratio 20:1

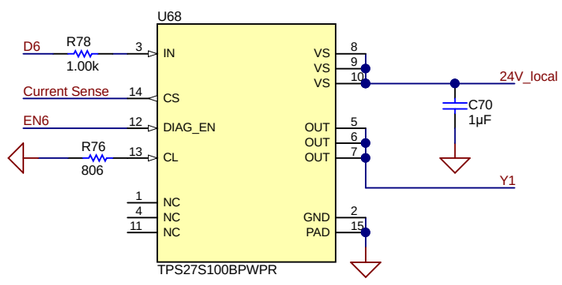


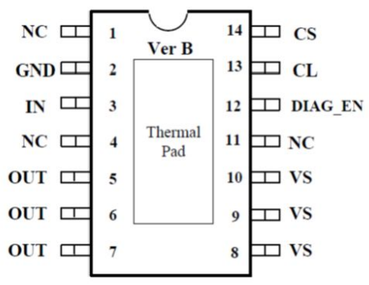


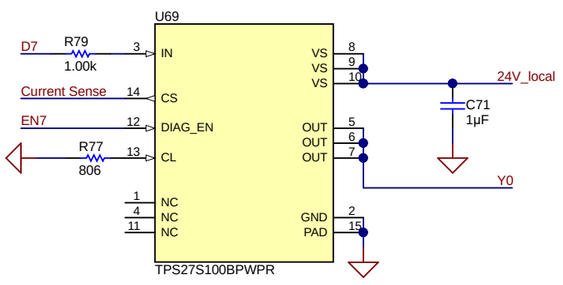


Filter frequency 100 kHz (-3dB), Ratio 2:1









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TID #: TIDA-01552	Project Title: 1A 8-Channel High Side Driver for PLC	
Number: TIDA-01552 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 5 of 7
Drawn By:	File: TIDA-01552_pg-4_Driver.SchDoc	Size: B
Engineer: Ingolf Frank	Contact: http://www.ti.com/support	

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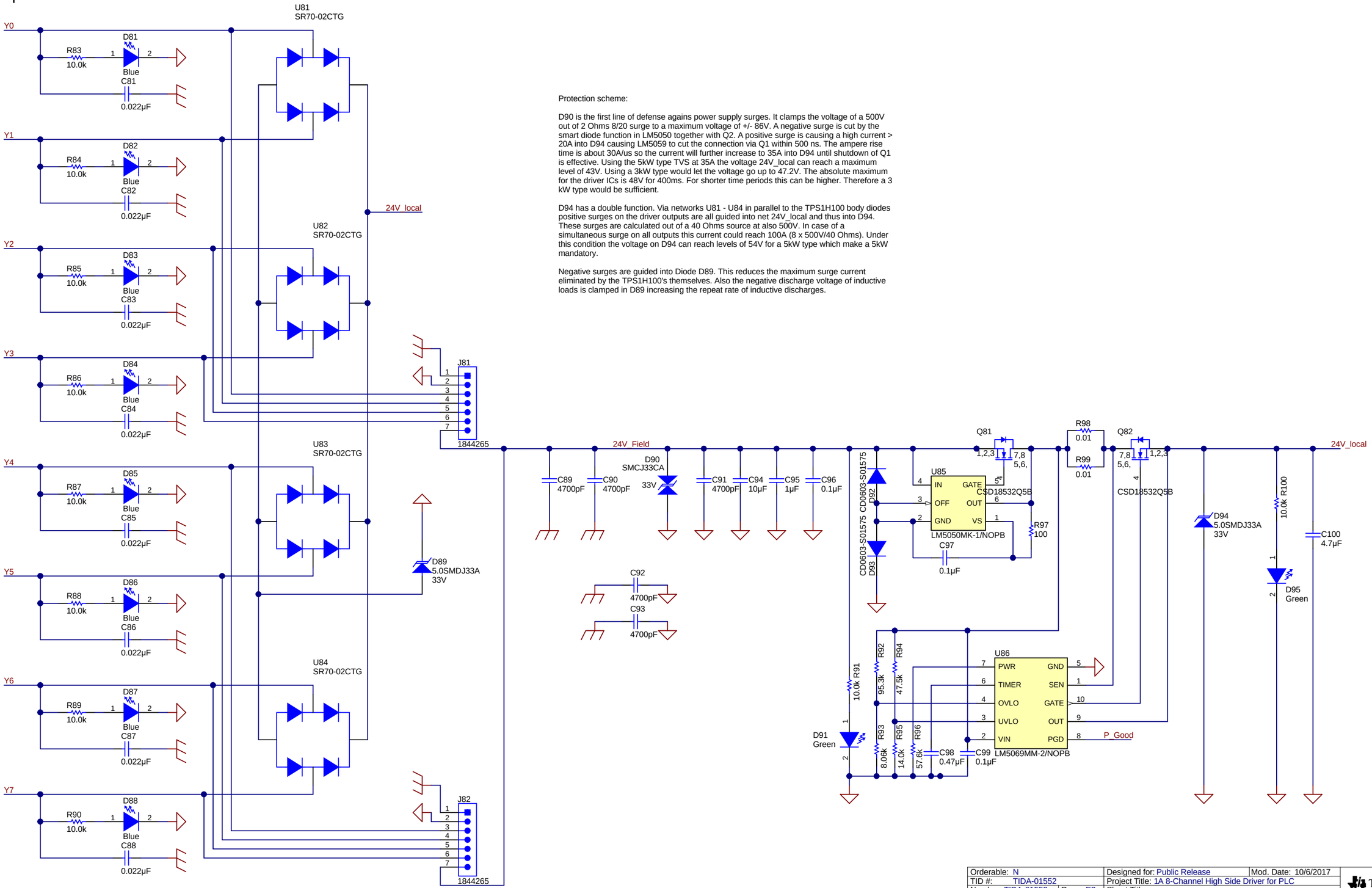
Output connectors



Protection scheme:

D90 is the first line of defense agains power supply surges. It clamps the voltage of a 500V out of 2 Ohms 8/20 surge to a maximum voltage of +/- 86V. A negative surge is cut by the smart diode function in LM5050 together with Q2. A positive surge is causing a high current > 20A into D94 causing LM5059 to cut the connection via Q1 within 500 ns. The ampere rise time is about 30A/us so the current will further increase to 35A into D94 until shutdown of Q1 is effective. Using the 5kW type TVS at 35A the voltage 24V_local can reach a maximum level of 43V. Using a 3kW type would let the voltage go up to 47.2V. The absolute maximum for the driver ICs is 48V for 400ms. For shorter time periods this can be higher. Therefore a 3 kW type would be sufficient.

D94 has a double function. Via networks U81 - U84 in parallel to the TPS1H100 body diodes positive surges on the driver outputs are all guided into net 24V_local and thus into D94. These surges are calculated out of a 40 Ohms source at also 500V. In case of a simultaneous surge on all outputs this current could reach 100A (8 x 500V/40 Ohms). Under this condition the voltage on D94 can reach levels of 54V for a 5kW type which make a 5kW mandatory.

Negative surges are guided into Diode D89. This reduces the maximum surge current eliminated by the TPS1H100's themselves. Also the negative discharge voltage of inductive loads is clamped in D89 increasing the repeat rate of inductive discharges.

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SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 6 of 7
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Engineer: Ingolf Frank	Contact: http://www.ti.com/support	

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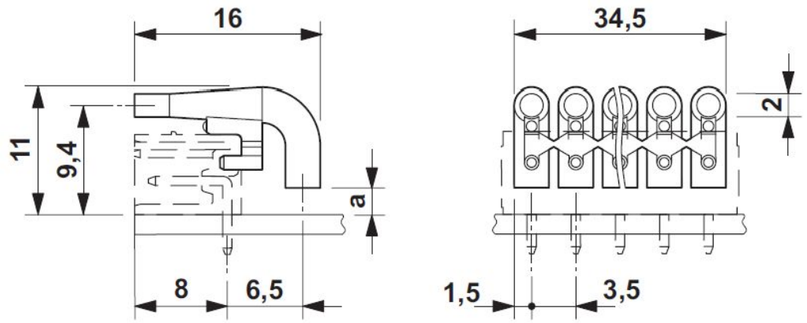
MH1 MH2 MH3 MH4 MH5 MH6

FID1 FID2 FID3 FID4 FID5

H1
MECH
1841161

H2
MECH
1841161

Dimensional drawing



PCB
LOGO
Pb-Free Symbol

LBL1
PCB Label
Size: 0.65" x 0.20 "

Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ3
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

ZZ4
Assembly Note
This Assembly Note will show in the PcbDoc and associated outputs

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Number: TIDA-01552 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 7 of 7
Drawn By:	File: TIDA-01552_TID_Hardware.SchDoc	Size: B
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