COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY

REVISIONS

| REV | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| A | ECO 2149913: Initial Release | 4/13/2015 | DH |
| B | ECO 2150627 | 5/15/2015 | DH |
| C | ECO 2150877 | 6/25/2015 | DH |
| D | ECO 2153403 | 9/15/2015 | DH |

## NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P1P1V" represents connection to the +1.1V FPGA power plane
2. The netname "P1P1V_FIL" represents connection to the +1.1V filtered FPGA power plane
3. The netname "P1P1V_M" represents connection to the +1.1V Master ASIC power plane
4. The netname "P1P1V_S" represents connection to the +1.1V Slave ASIC power plane
5. The netname "P1P15V" represents connection to the +1.15V FPGA power plane
6. The netname "P1P15V" represents connection to the +1.15V filtered FPGA power plane
7. The netname "P1P5V" represents connection to the +1.5V FPGA power plane
8. The netname "P1P5V_FIL" represents connection to the +1.5V filtered FPGA power plane
9. The netname "P1P8V_M" represents connection to the +1.8V Master ASIC power plane
10. The netname "P1P8V_S" represents connection to the +1.8V Slave ASIC power plane
11. The netname "A1P8V_M" represents connection to the +1.8V Master ASIC power plane for the PLLs
12. The netname "A1P8V_S" represents connection to the +1.8V Slave ASIC power plane for the PLLs
13. The netname "P2P5V" represents connection to the +2.5V FPGA power plane
14. The netname "P2P5V_FIL" represents connection to the +2.5V filtered FPGA power plane
15. The netname "P2P5V_M" represents connection to the +2.5V Master ASIC power plane
16. The netname "P2P5V_S" represents connection to the +2.5V Slave ASIC power plane
17. The netname "P3P3V" represents connection to the +3.3V FPGA power plane
18. The netname "P3P3V_M" represents connection to the +3.3V Master ASIC power plane
19. The netname "P3P3V_S" represents connection to the +3.3V Slave ASIC power plane
20. The netname "P5V_M" represents connection to the +5V Master ASIC power plane
21. The netname "P5V_S" represents connection to the +5V Slave ASIC power plane
22. The netname "P12V" represents the connection to the +12.0V power plane.
23. The netname "GND" represents connection to the ground plane
24. A "Z" suffix on a signal name indicates an active low signal
25. All components with designators "U*", "Q*", "D*" are electrostactic discharge sensitive.
26. All components with designators above 500 are mounted on the bottom side of the board.
27. All resistor values are in ohms.

## INDEX



| | | | |
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| | | DWN Ben Uhing | DATE 9/30/2016 |
| | | ENGR Scott Vestal | 4/9/2015 |
| | | APVD | |
| | | MFG | |
| | | QA | |
| NEXT ASSY | USED ON | | |
| APPLICATION | | SW Cadence 16.6 | |

**TEXAS INSTRUMENTS**



TITLE: TIDA-01347 P66 4KUHD Formatter Board

A3 | DRAWING NO 2514423 | REV E

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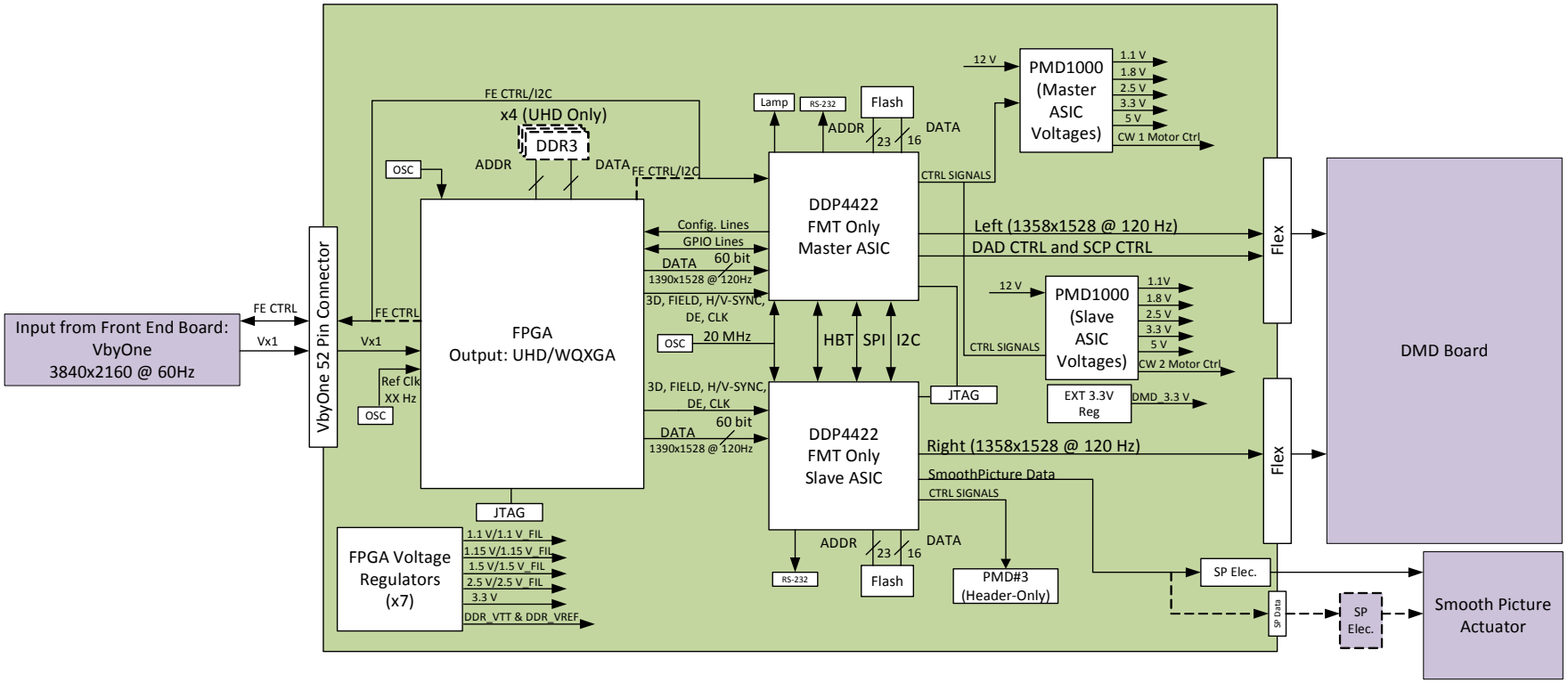
# Block Diagram



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| TEXAS INSTRUMENTS | DWN Amy White | DATE 4/13/2015 | A3 | DRAWING NO 2514423 REV D |
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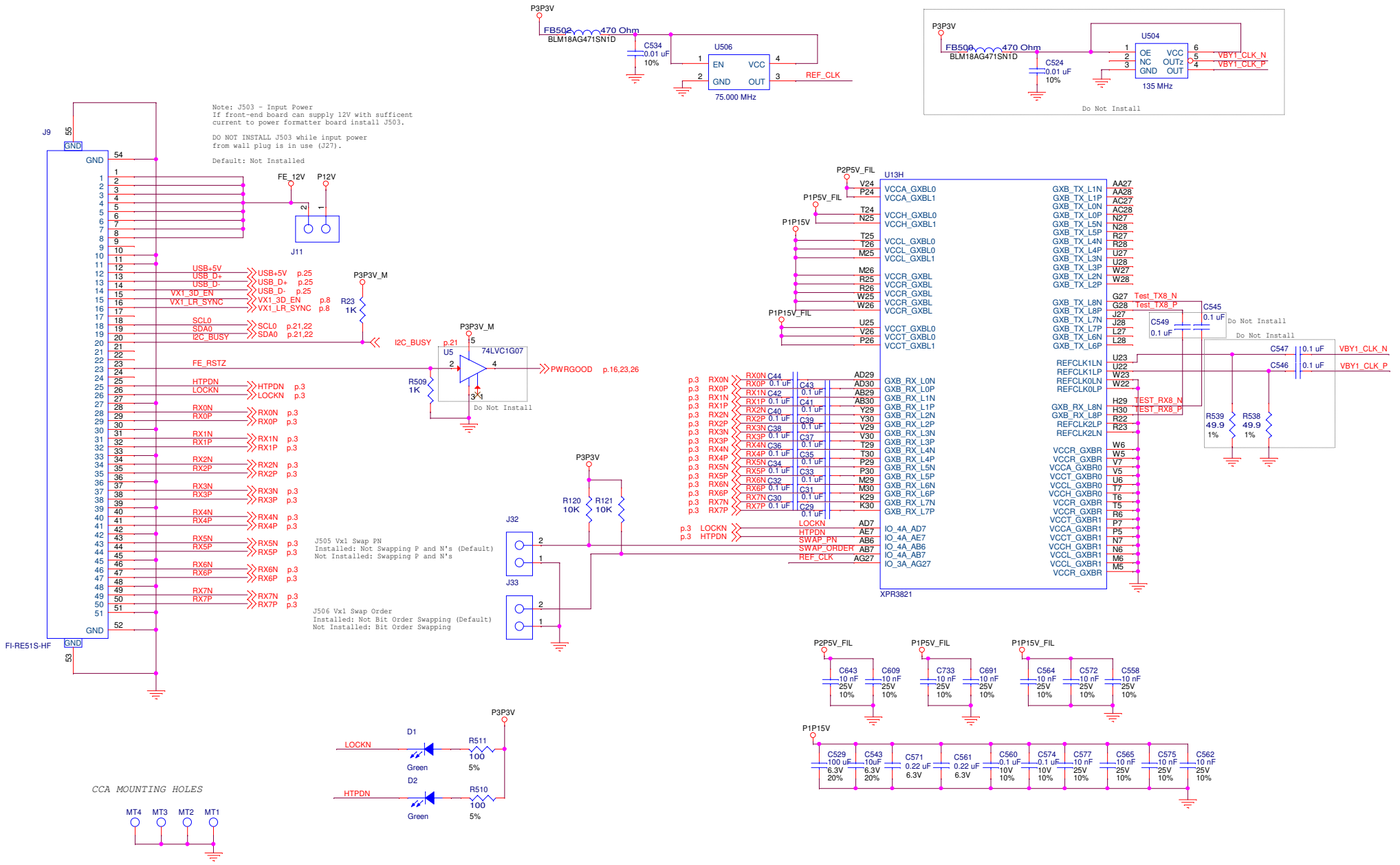




FPGA - Front-End I/F

| | | | | | |
|---|---|---|---|---|---|
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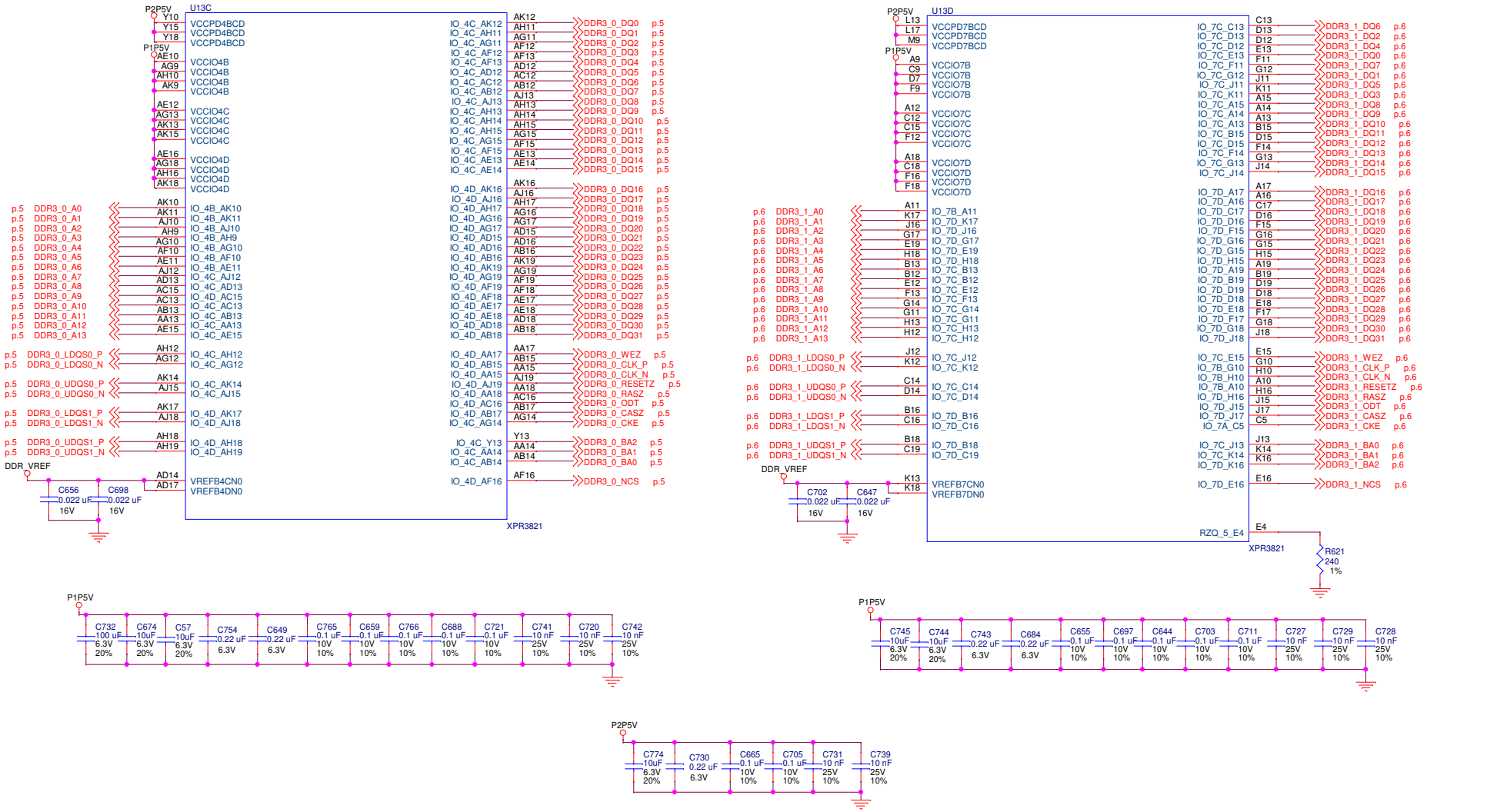


FPGA - DDR3 Interface



| | | | | | |
|---|---|---|---|---|---|
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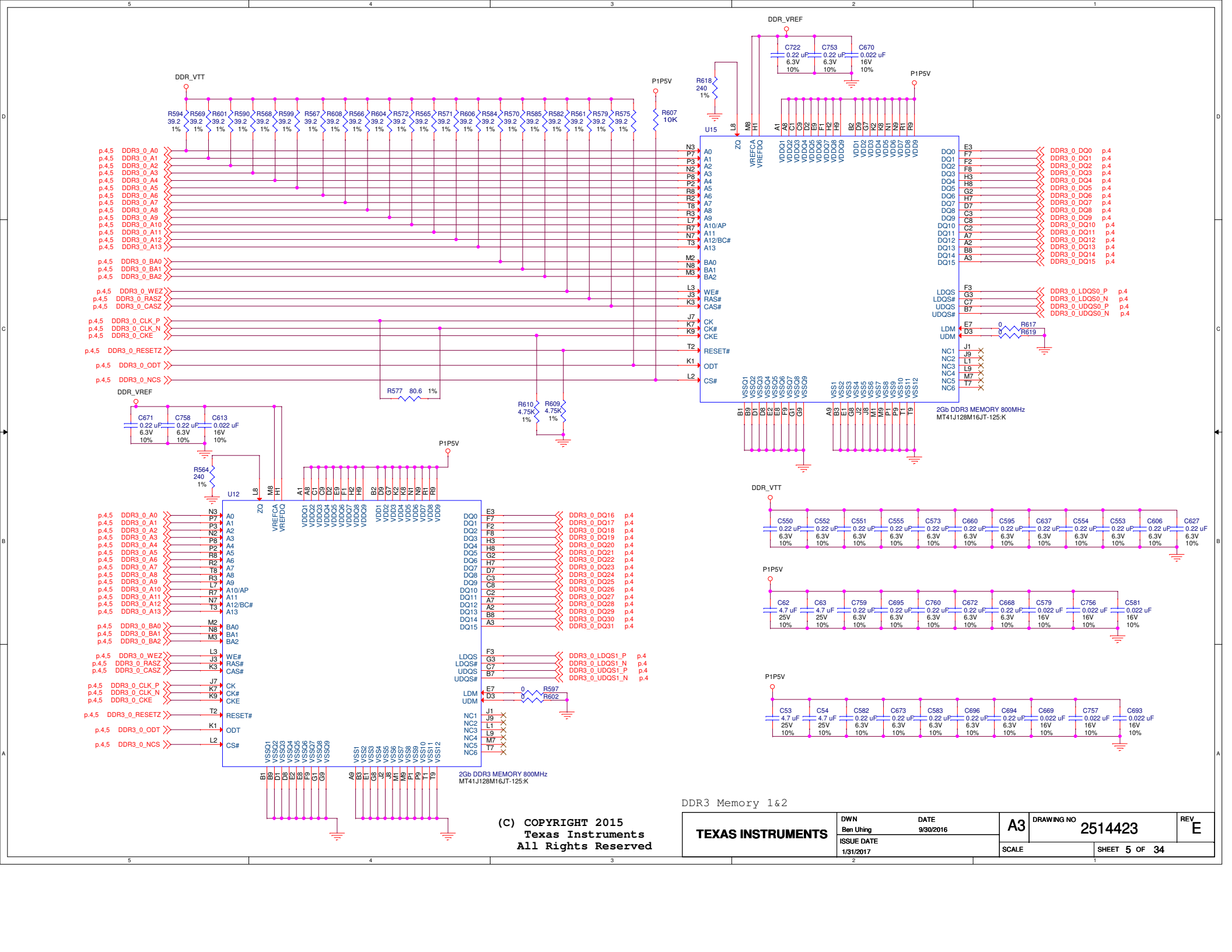




DDR3 Memory 1&2

| | | | | |
|---|---|---|---|---|
| TEXAS INSTRUMENTS | DWN Ben Uhing | DATE 9/30/2016 | A3 | DRAWING NO 2514423 REV E |
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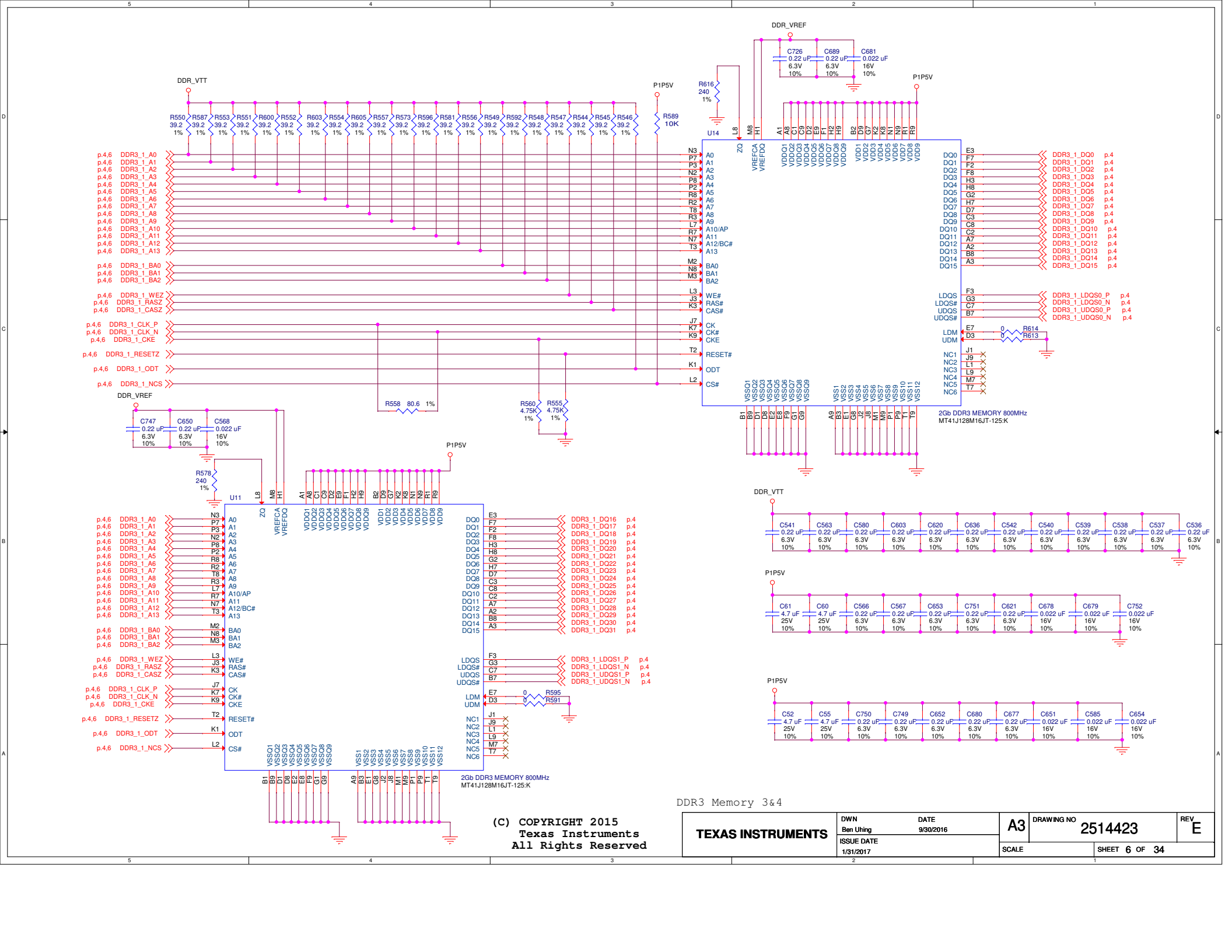




| | | | |
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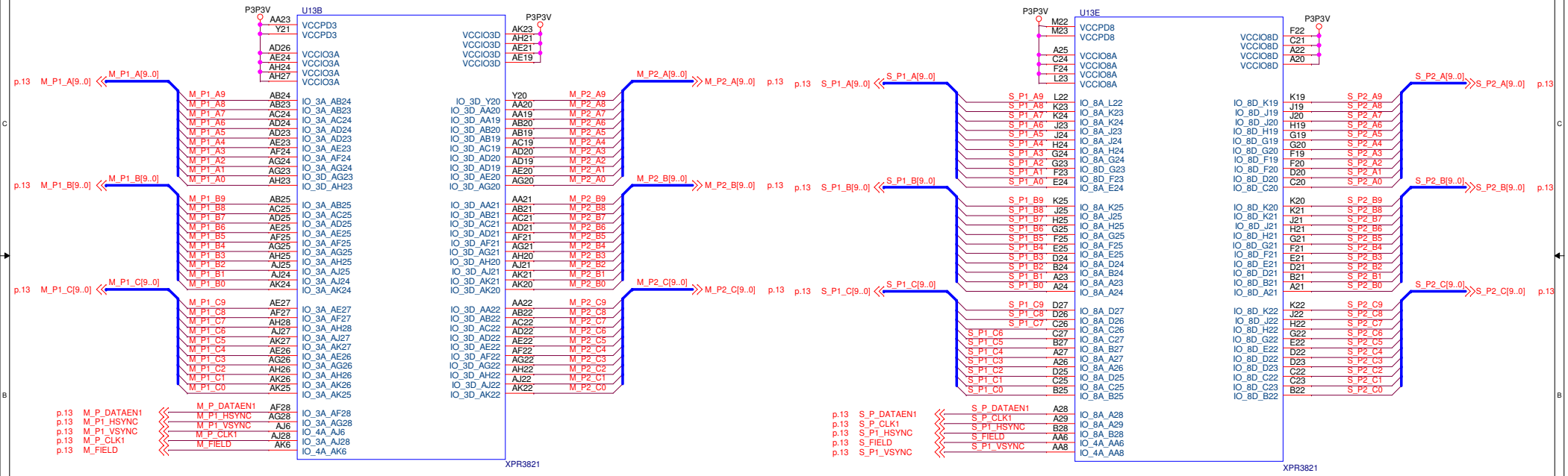




FPGA - Video I/F

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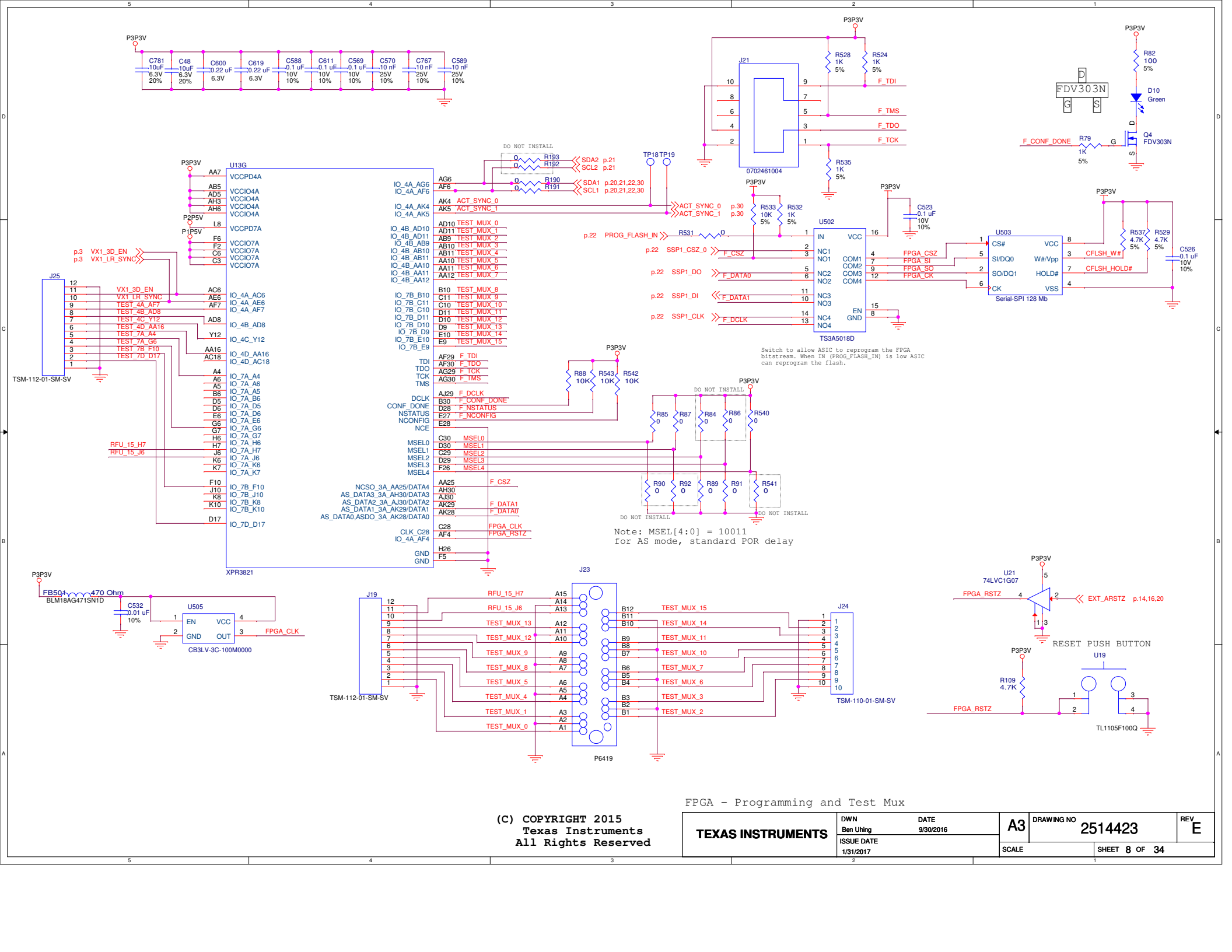


FPGA – Programming and Test Mux



| | | | | | |
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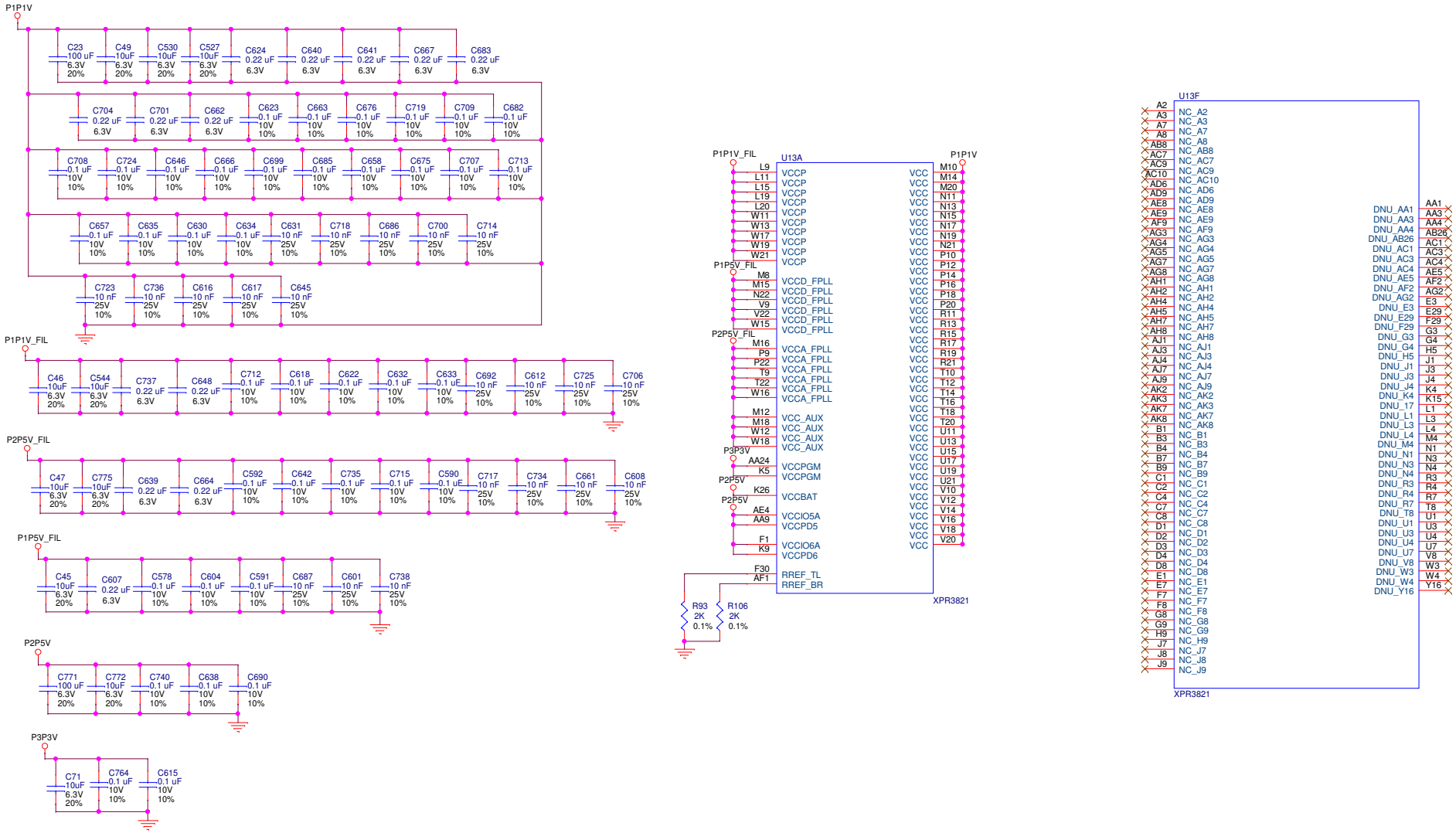


FPGA - Power



TEXAS INSTRUMENTS

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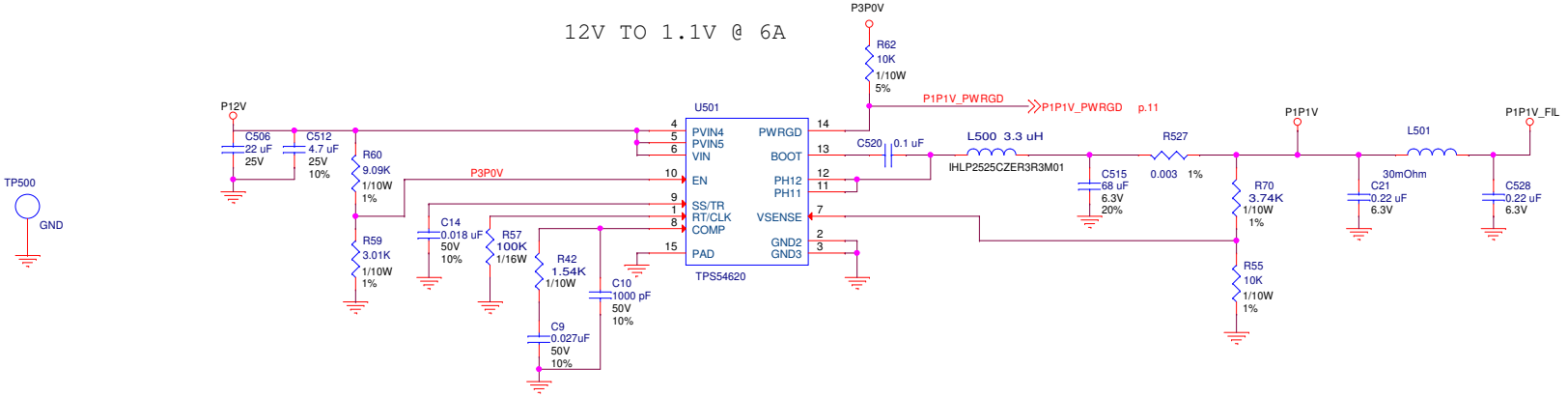
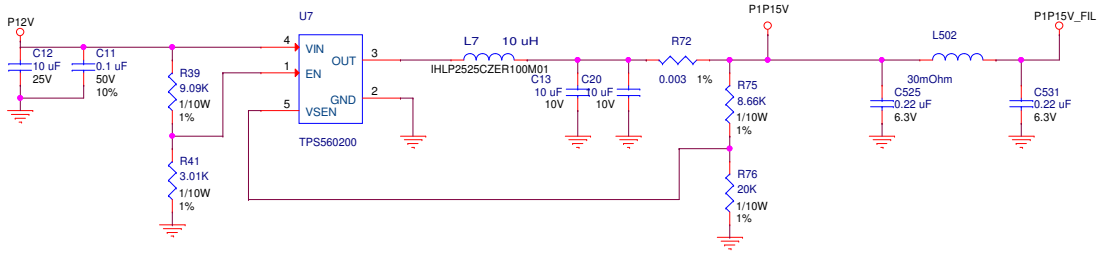
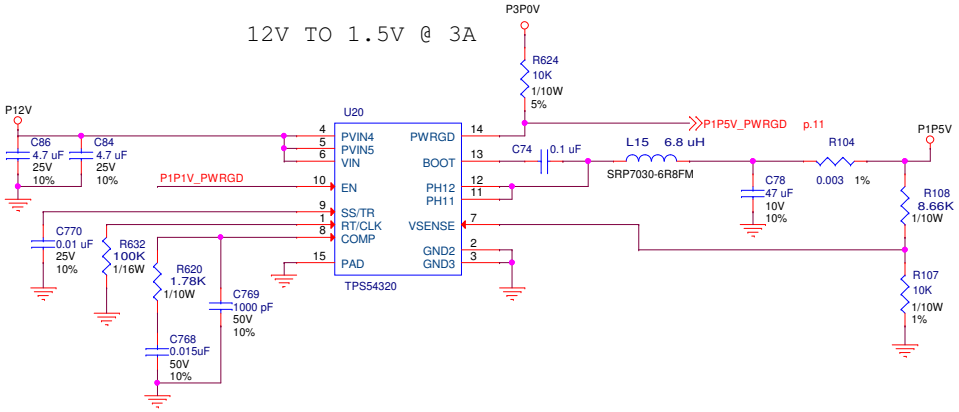
## 12V TO 1.1V @ 6A




## 12V TO 1.15V @ 500mA




## 12V TO 1.5V @ 3A






| | | | | | |
|---|---|---|---|---|---|
| TEXAS INSTRUMENTS | DWN Ben Uhing | DATE 9/30/2016 | A3 | DRAWING NO 2514423 | REV E |
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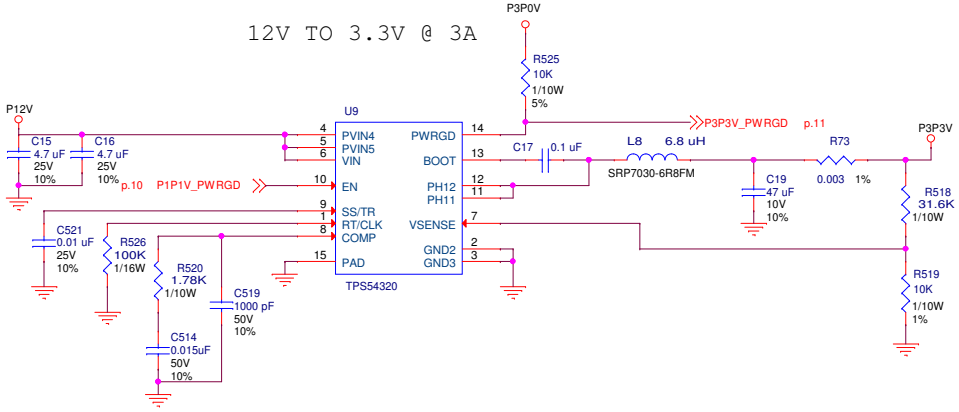
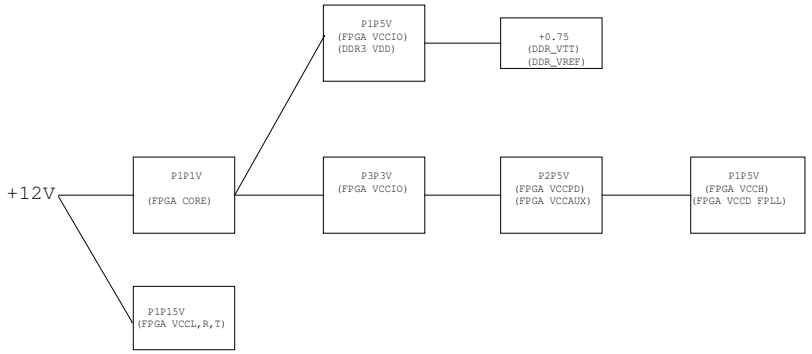
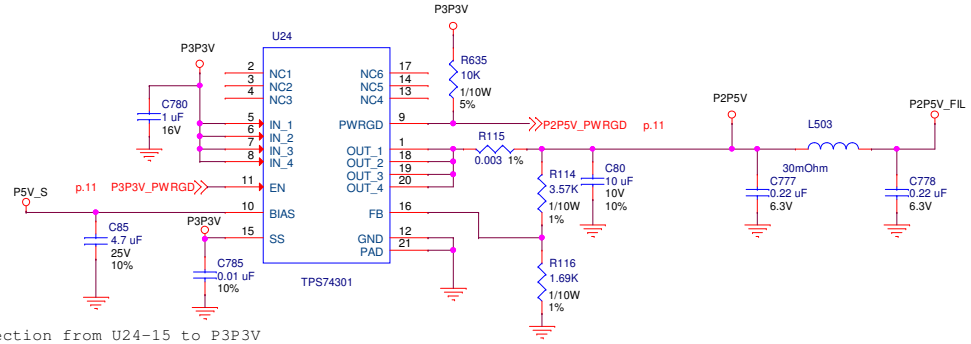
## 12V TO 3.3V @ 3A




## Power Sequence

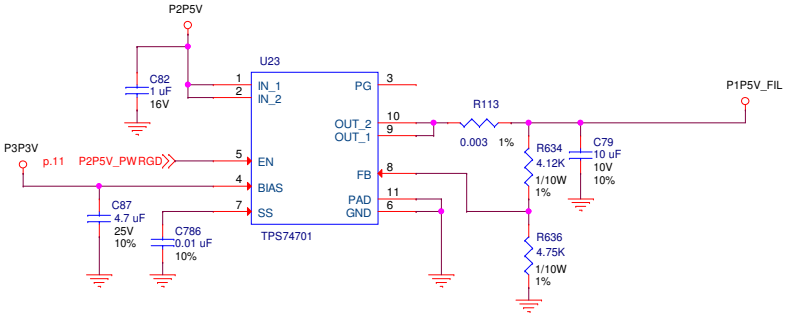



## 3.3V TO 2.5V @ 1.5A

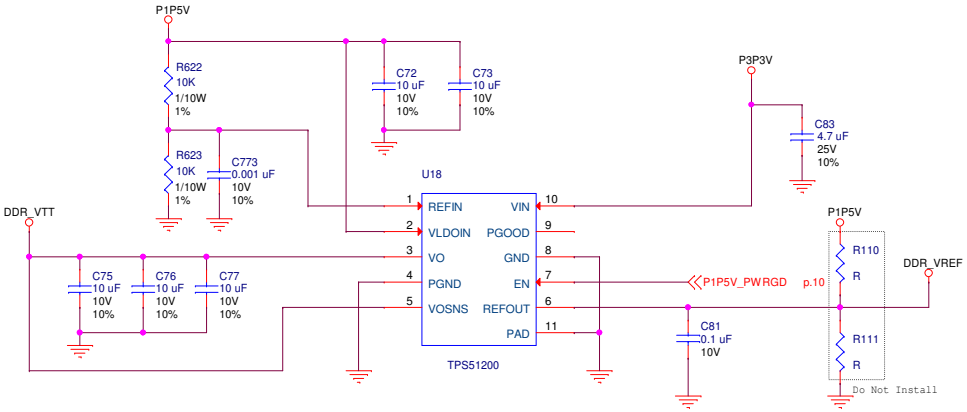



The connection from U24-15 to P3P3V
is a blue wire on existing Rev A pwb's.

## 2.5V TO 1.5V @ 500mA




## 1.5V TO 0.75V DDR_VTT & DDR_VREF




DDR TERMINATION VOLTAGE



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FPGA – GND



| | | | | | |
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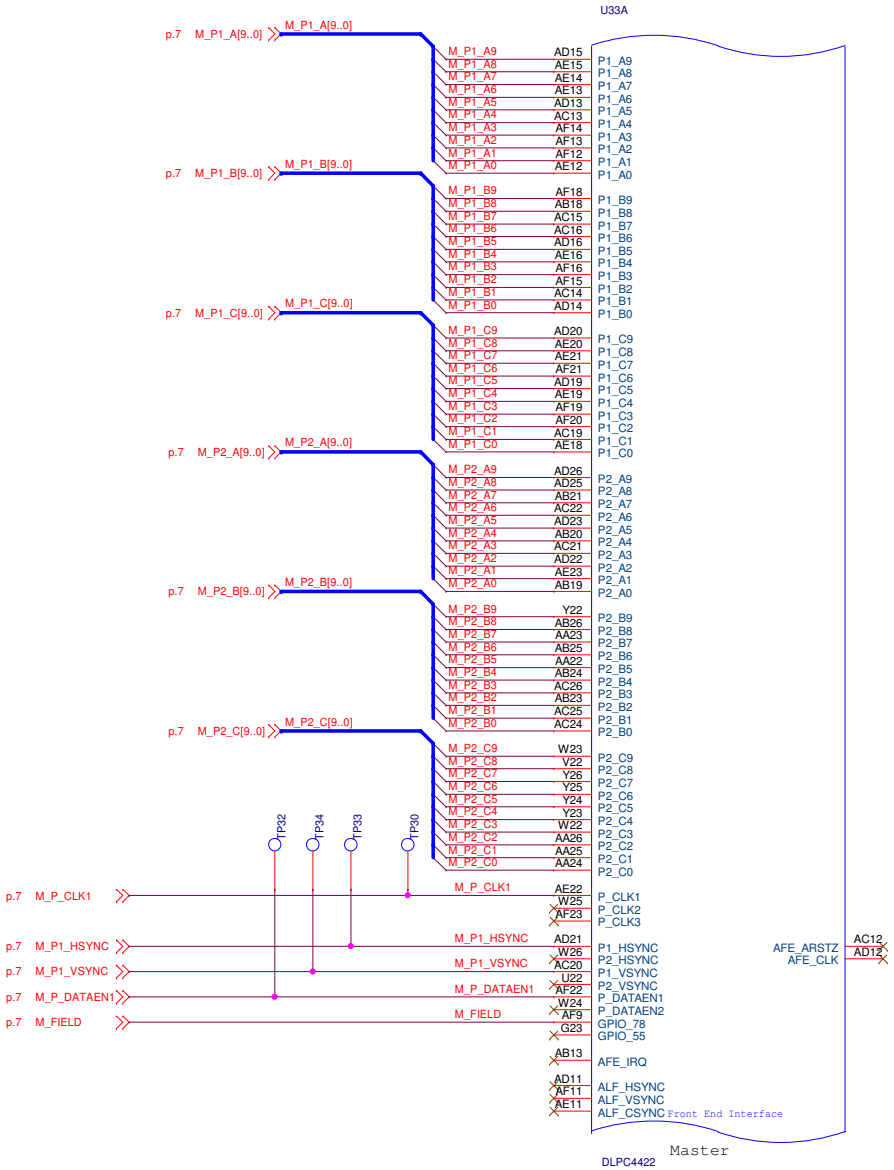


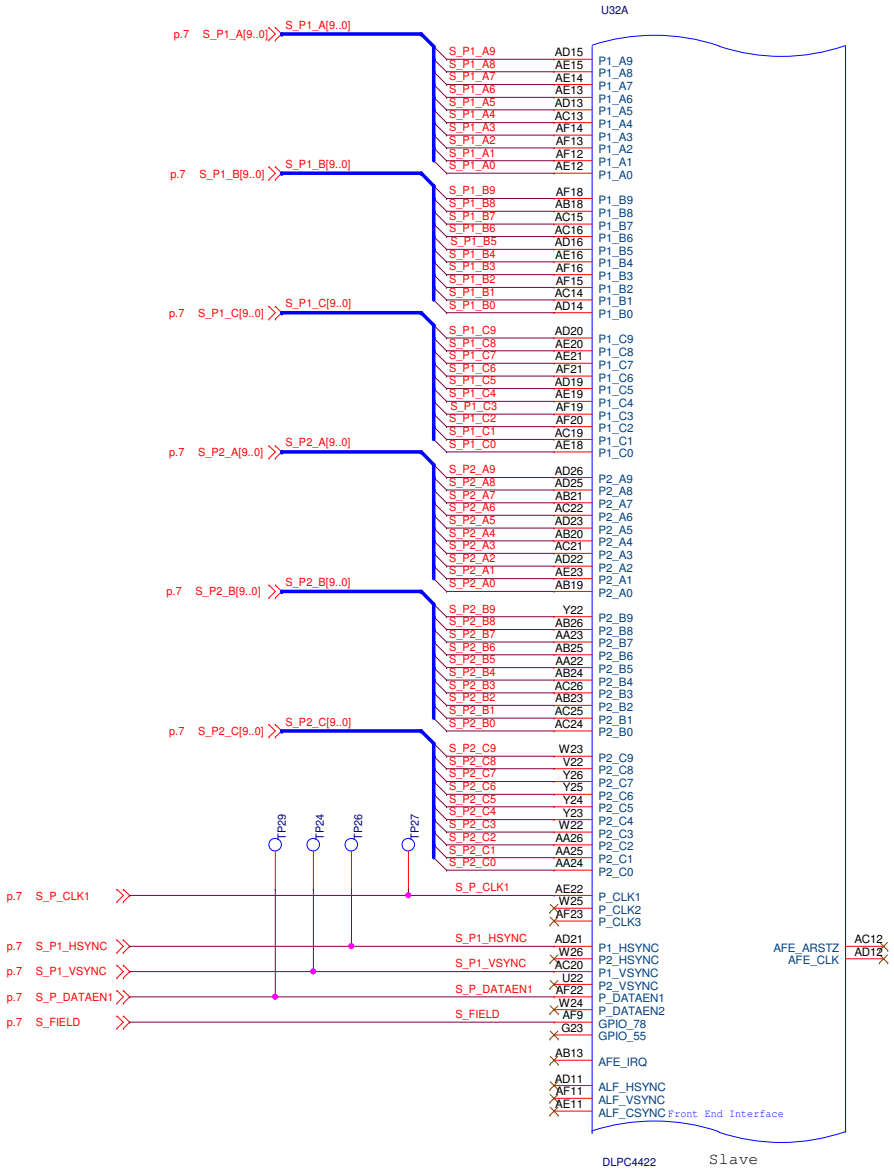




Master and Slave Front End Interface

| | | | | | |
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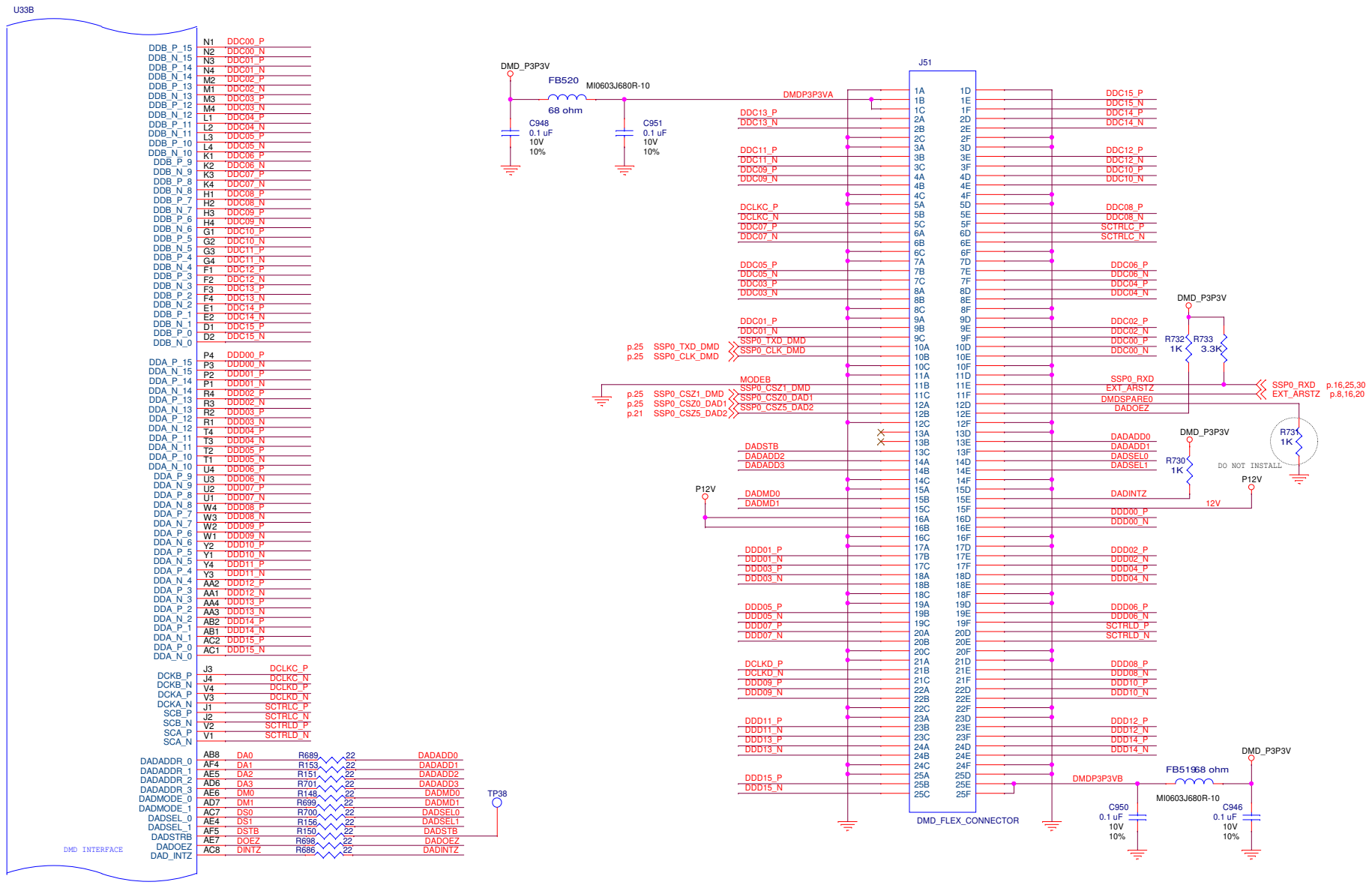




Master DLPC4422 DMD Flex Interface

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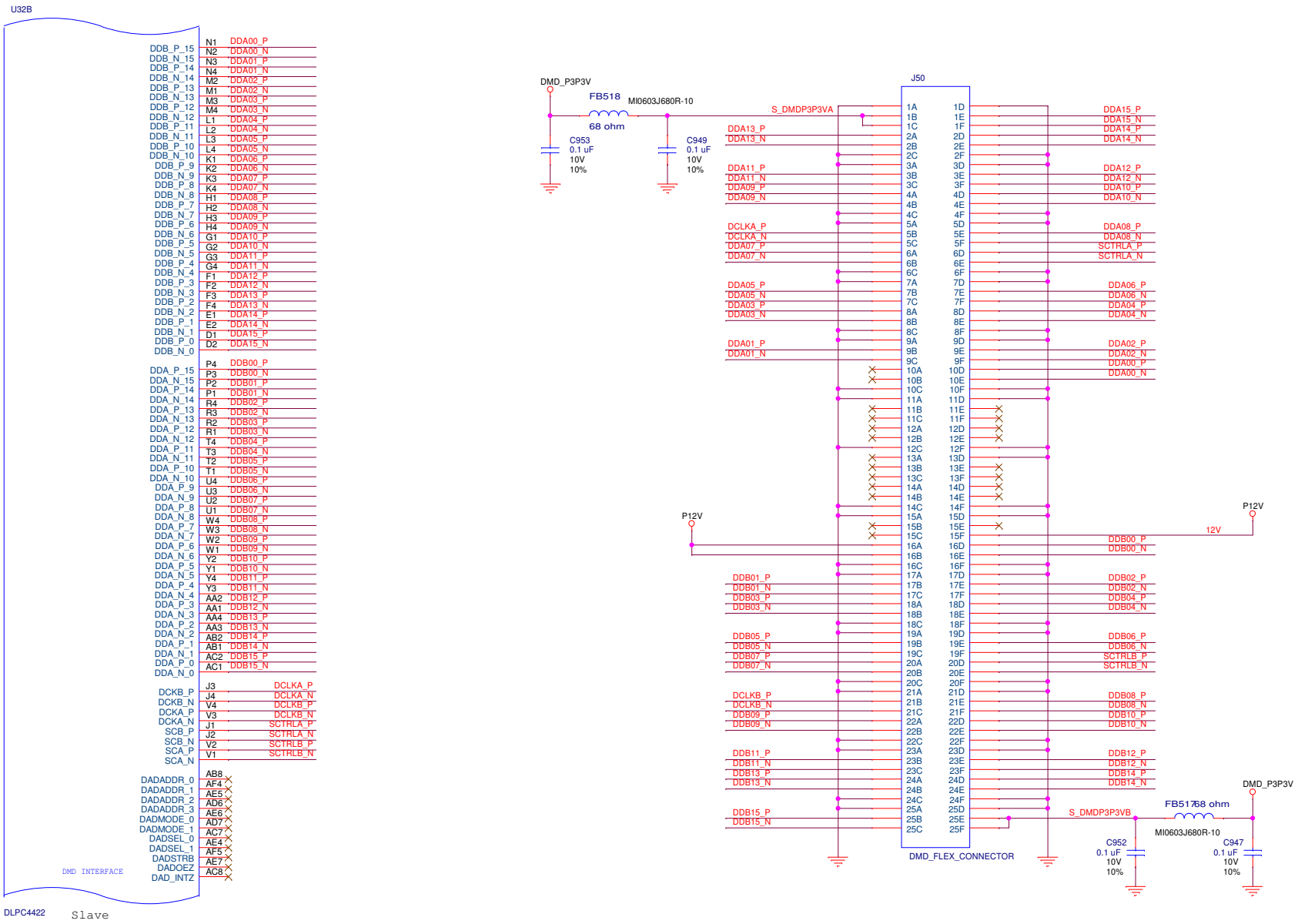


Slave DLPC4422 DMD Flex Interface



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|---|---|---|---|---|---|
| TEXAS INSTRUMENTS | DWN Ben Uhing | DATE 9/30/2016 | A3 | DRAWING NO 2514423 | REV E |
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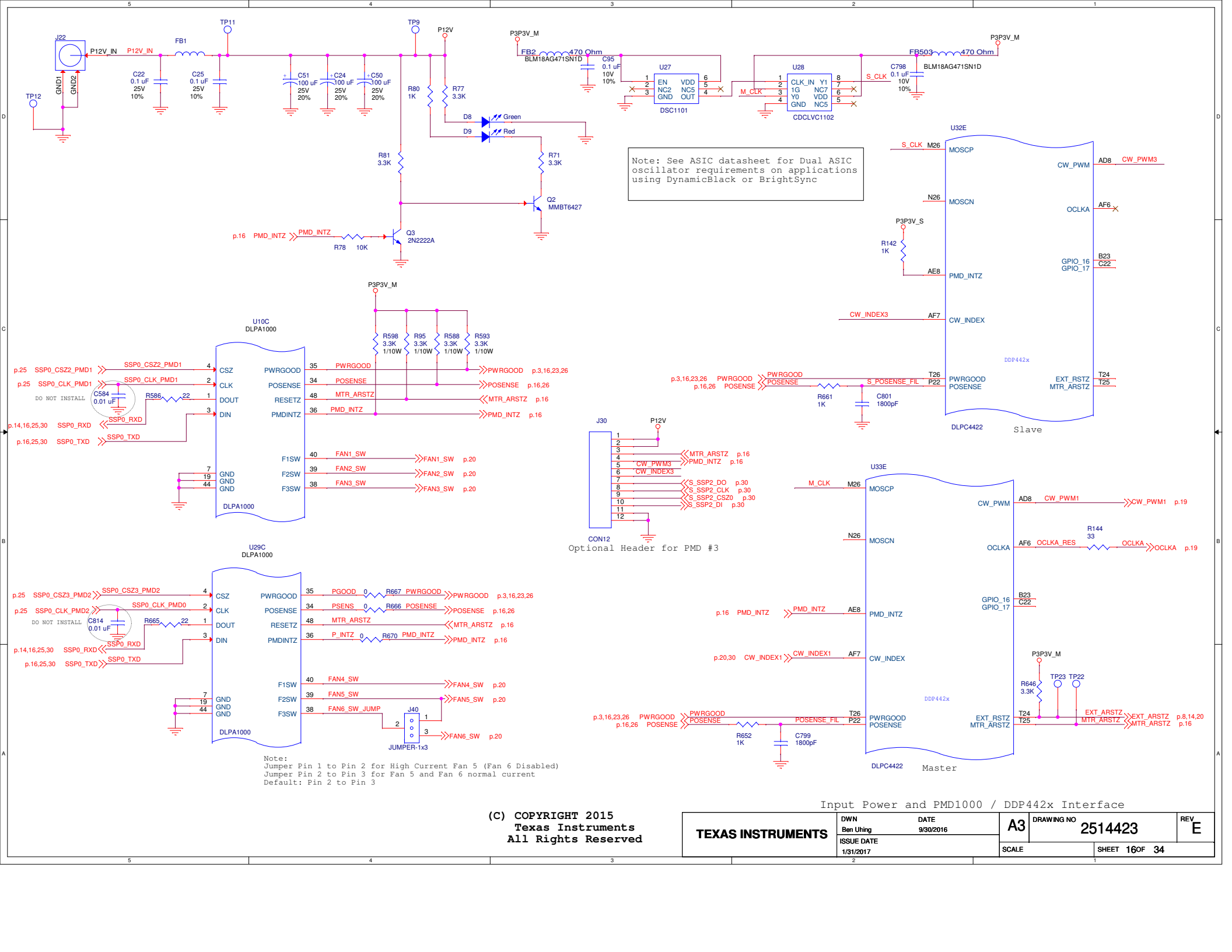




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|---|---|---|---|---|---|
| TEXAS INSTRUMENTS | DWN Ben Uhing | DATE 9/30/2016 | A3 | DRAWING NO 2514423 | REV E |
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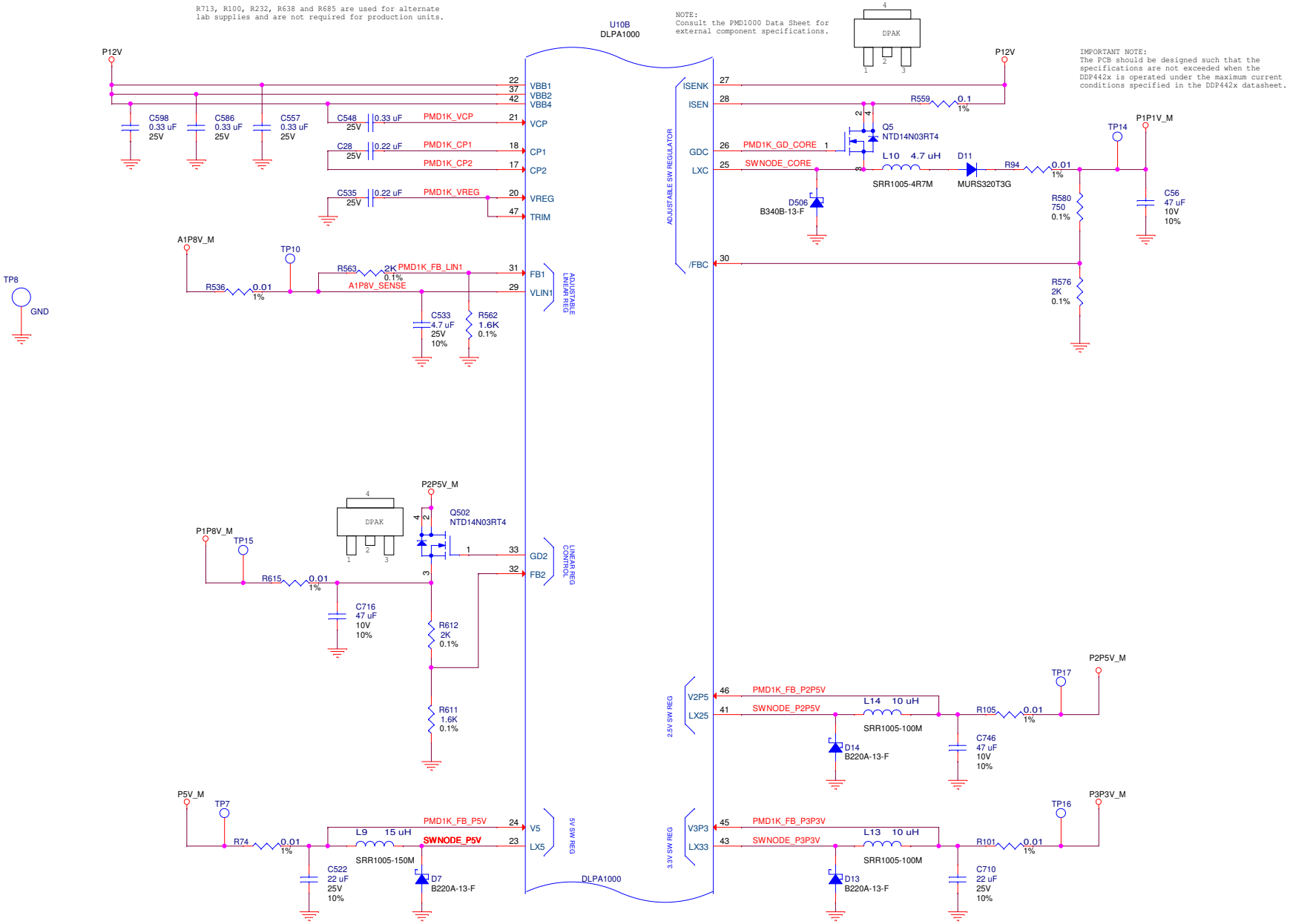


Primary DLPA1000 Power Supplies



| | | | | | |
|---|---|---|---|---|---|
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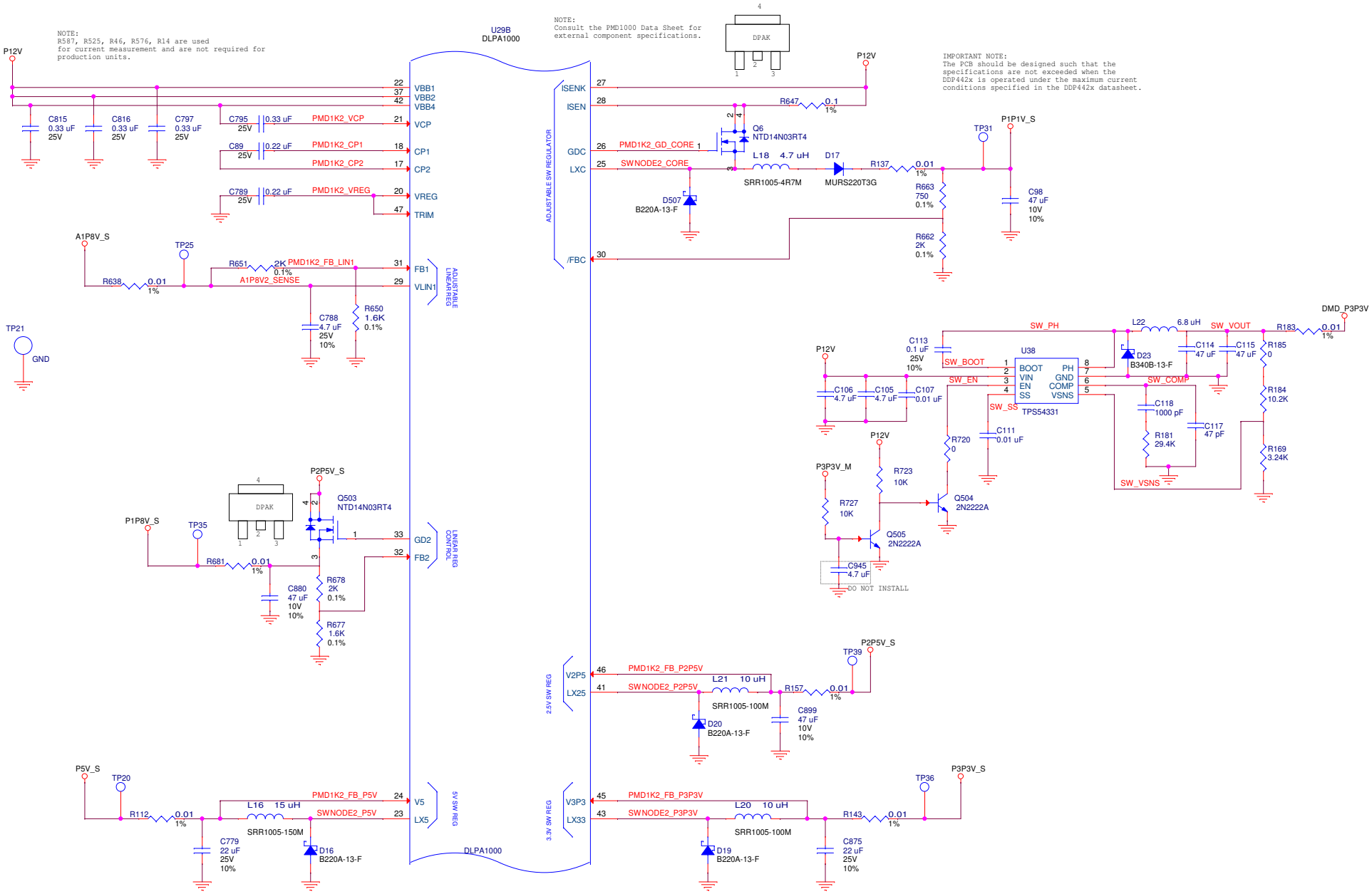




Secondary DLPA1000 Supplies

| | | | | | |
|---|---|---|---|---|---|
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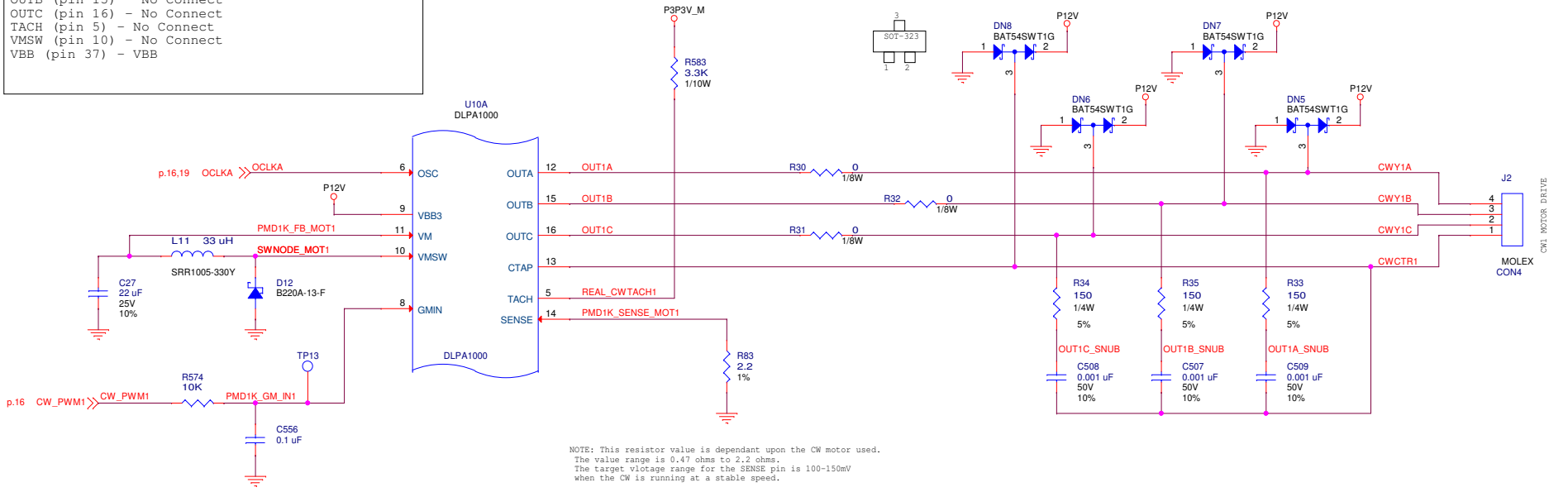
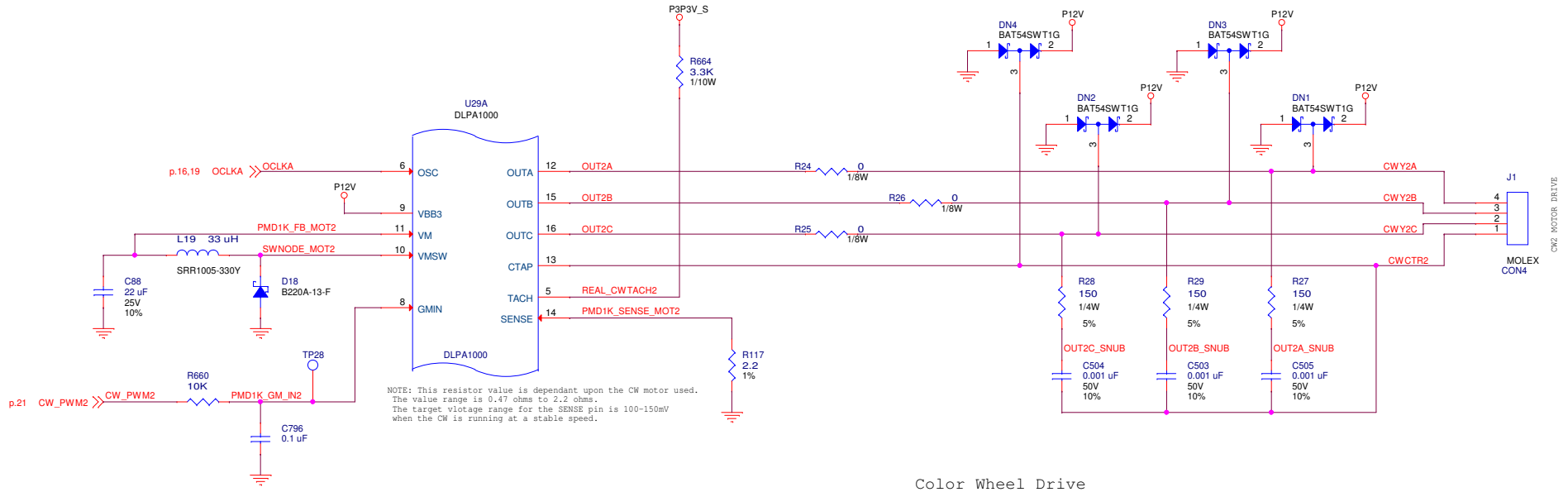
Note: If not using the motor driver on the
DLPA1000 follow these guidelines for unused pins:
GMIN (pin 8) - Ground
OSC (pin 6) - Ground
SENSE (pin 14) - Ground
CTAP (pin 13) - VBB
VM (pin 11) - VBB
OUTA (pin 12) - No Connect
OUTB (pin 15) - No Connect
OUTC (pin 16) - No Connect
TACH (pin 5) - No Connect
VMSW (pin 10) - No Connect
VBB (pin 37) - VBB




NOTE: This resistor value is dependant upon the CW motor used.
The value range is 0.47 ohms to 2.2 ohms.
The target vlotage range for the SENSE pin is 100-150mV
when the CW is running at a stable speed.




NOTE: This resistor value is dependant upon the CW motor used.
The value range is 0.47 ohms to 2.2 ohms.
The target vlotage range for the SENSE pin is 100-150mV
when the CW is running at a stable speed.



Color Wheel Drive

| | | | | | |
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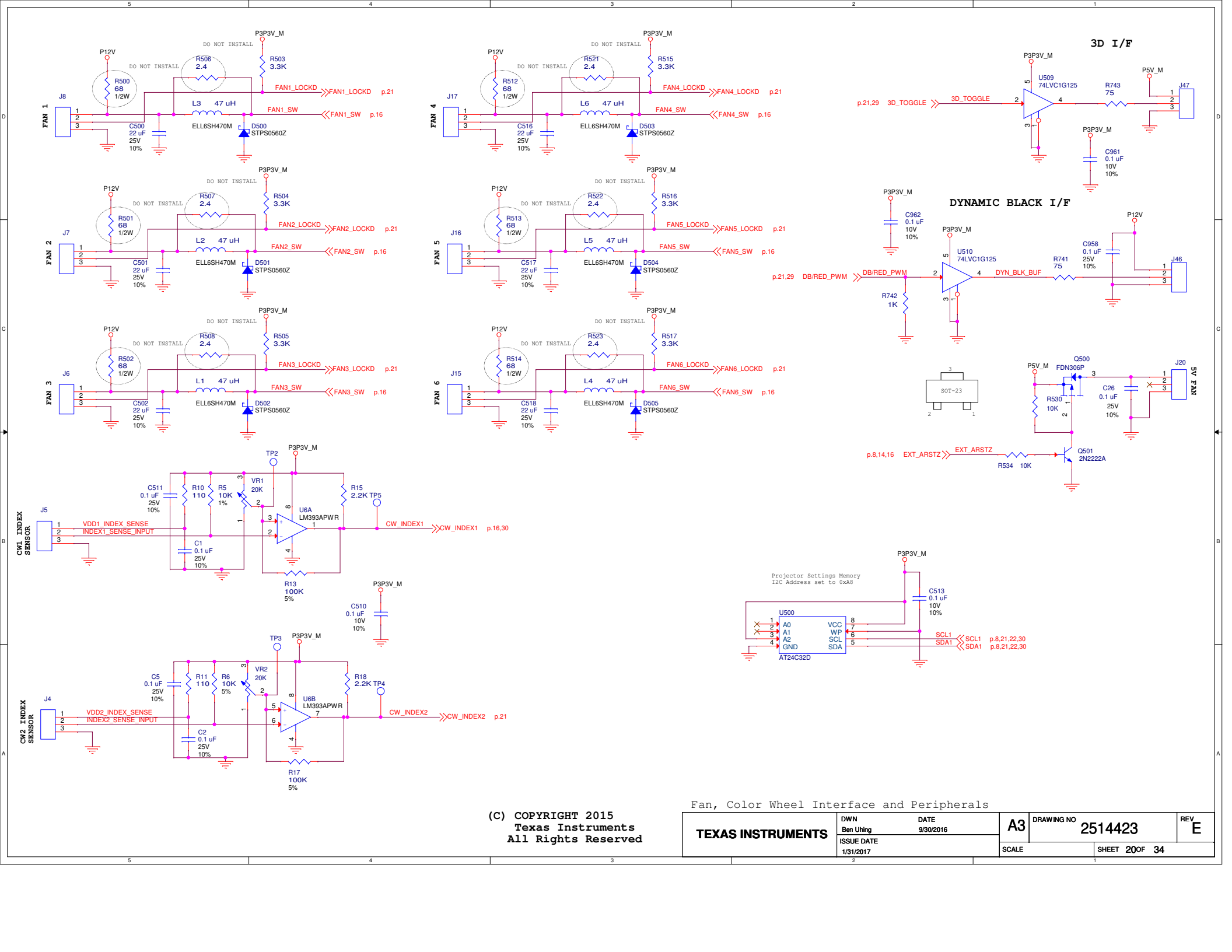




Fan, Color Wheel Interface and Peripherals

| | | | | |
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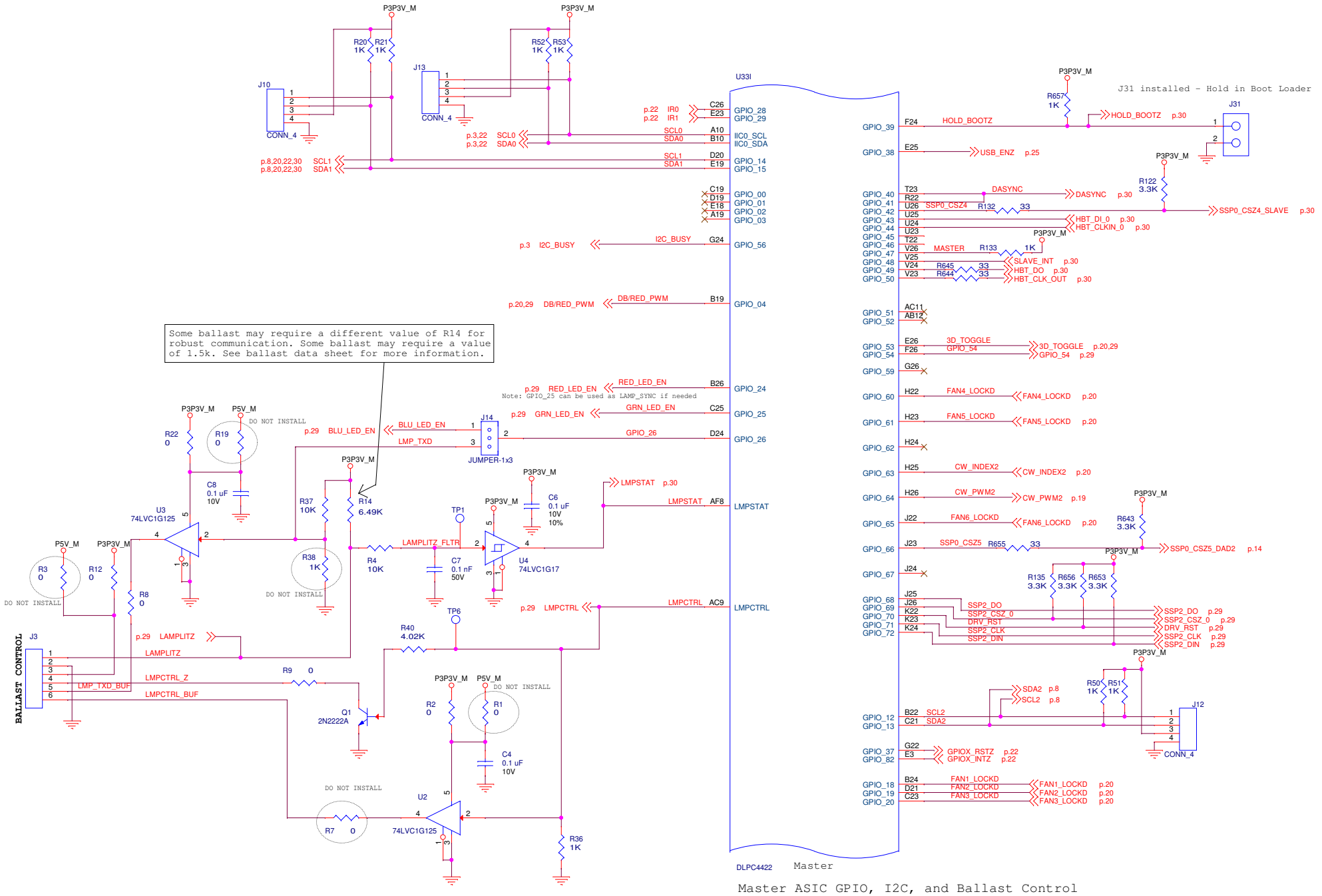
Some ballast may require a different value of R14 for robust communication. Some ballast may require a value of 1.5k. See ballast data sheet for more information.
J31 installed - Hold in Boot Loader
BALLAST CONTROL
U33I
DLPC4422
Master
(C) COPYRIGHT 2015
Texas Instruments
All Rights Reserved
Master ASIC GPIO, I2C, and Ballast Control
TEXAS INSTRUMENTS
DWN Ben Uhing
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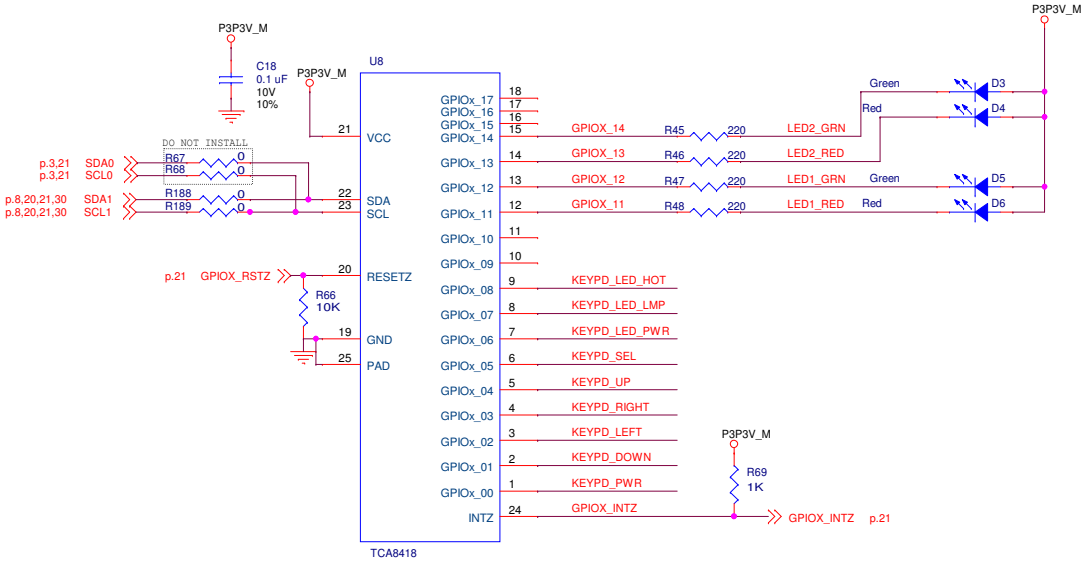
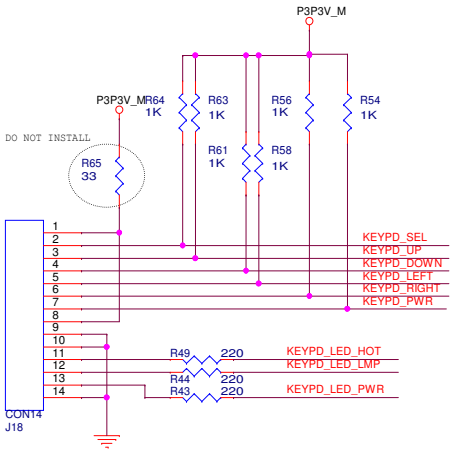
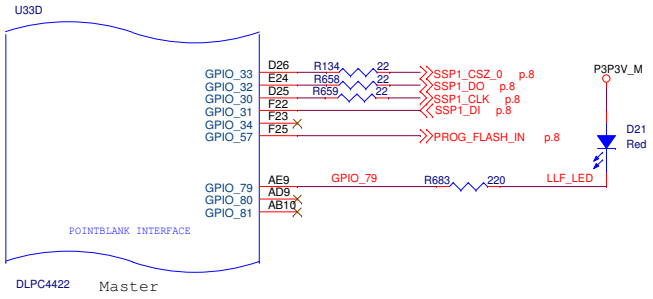
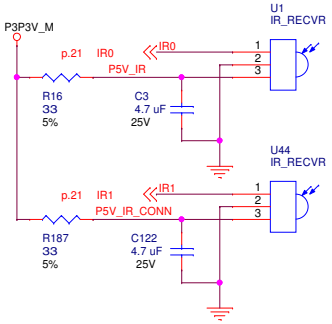



## KEYBOARD INTERFACE




GPIO Expander, Keypad Interface and IR Interface



| | | | | | |
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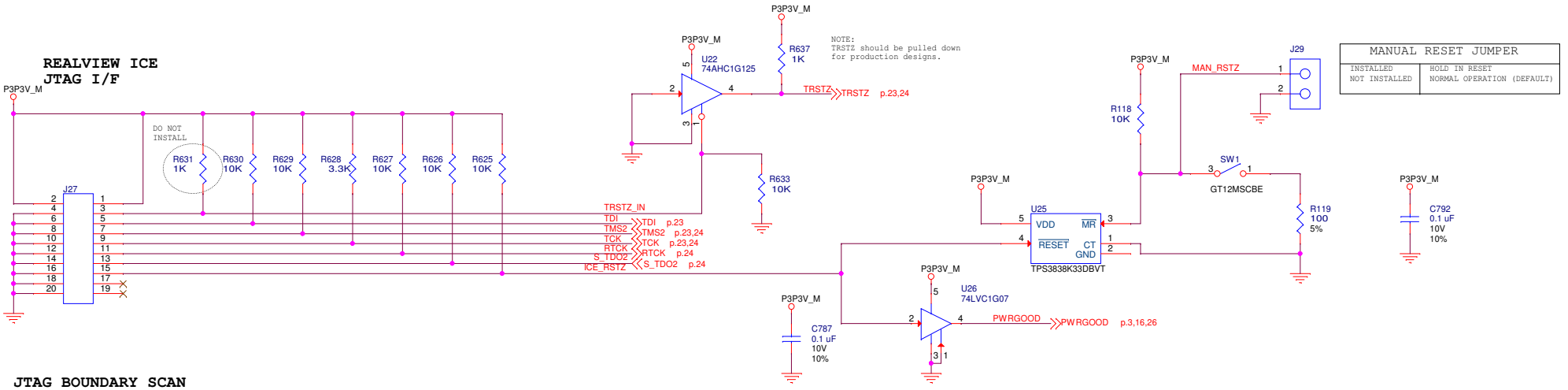
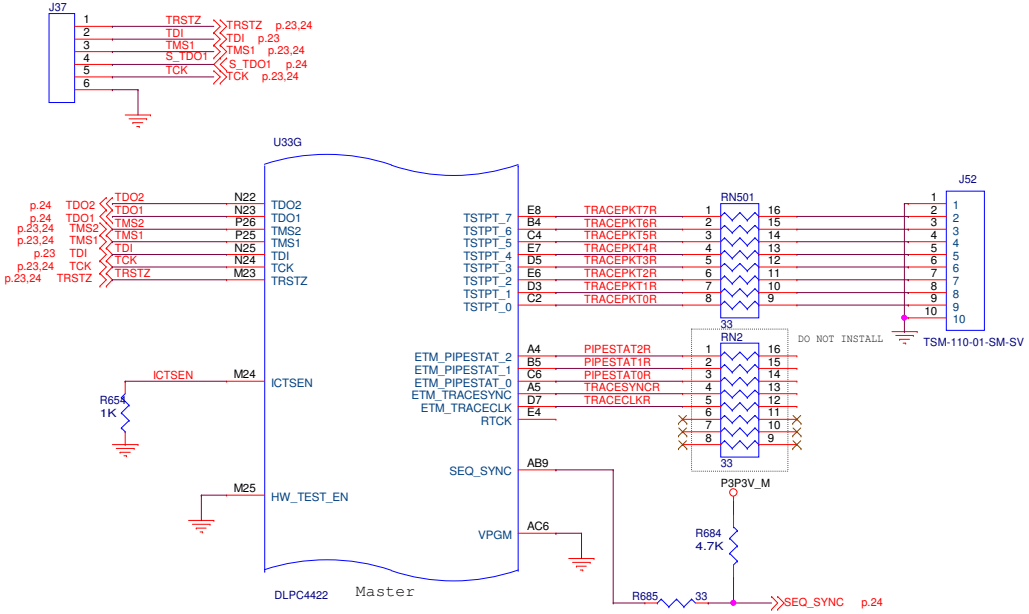
## REALVIEW ICE JTAG I/F




| MANUAL RESET JUMPER | |
|---|---|
| INSTALLED | HOLD IN RESET |
| NOT INSTALLED | NORMAL OPERATION (DEFAULT) |

## JTAG BOUNDARY SCAN






Master ASIC Test Points, ARM Trace, JTAG, and Reset

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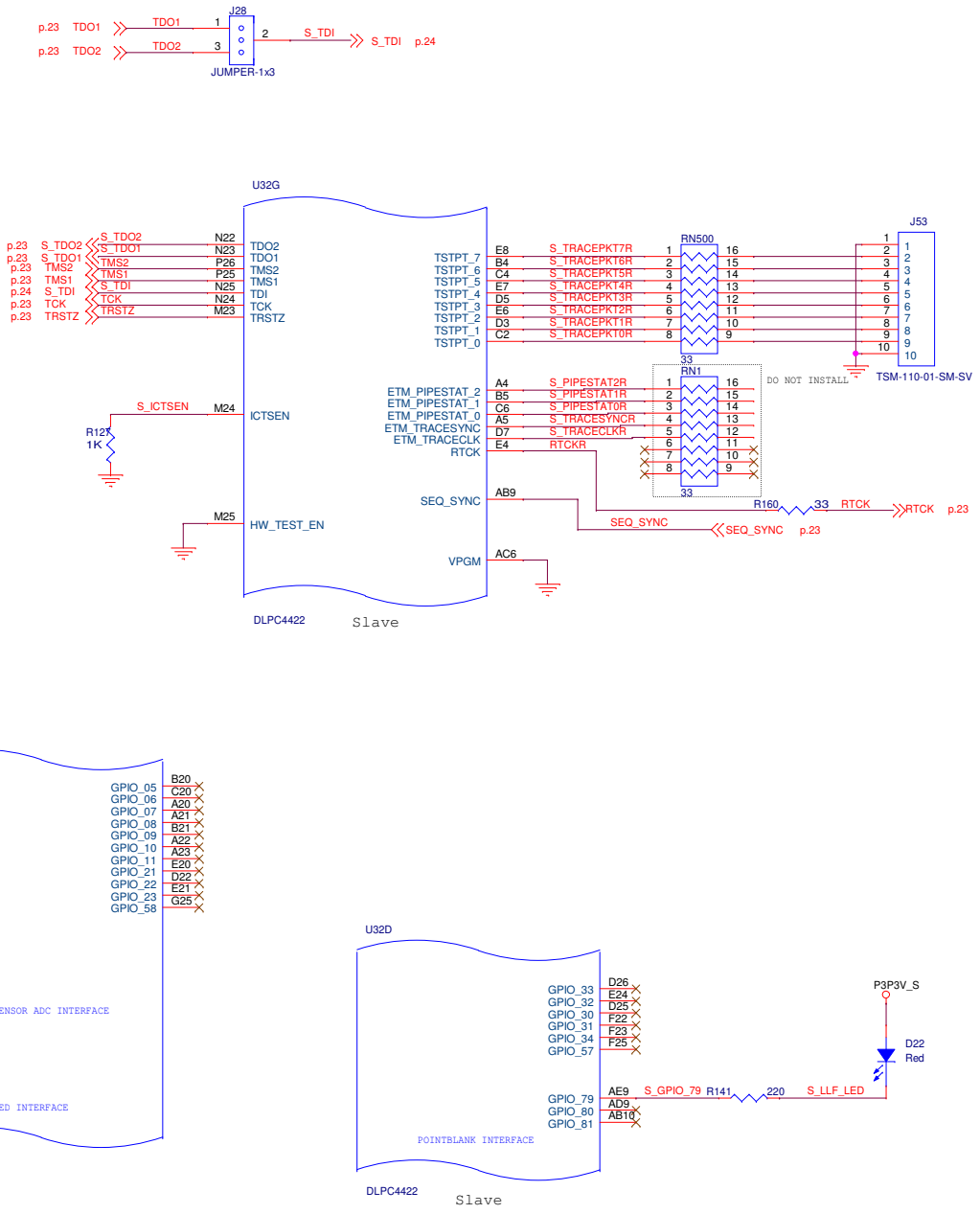


Slave ASIC Test Points, ARM Trace, and JTAG



| | | | | | |
|---|---|---|---|---|---|
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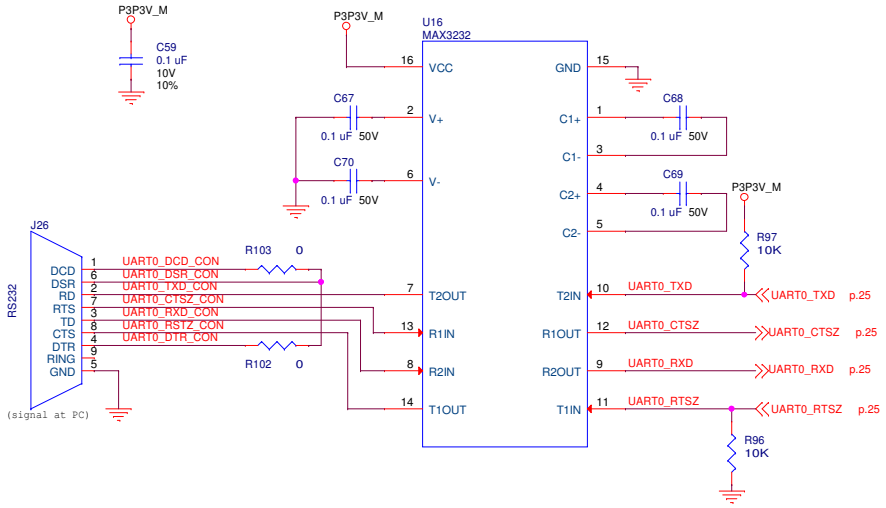
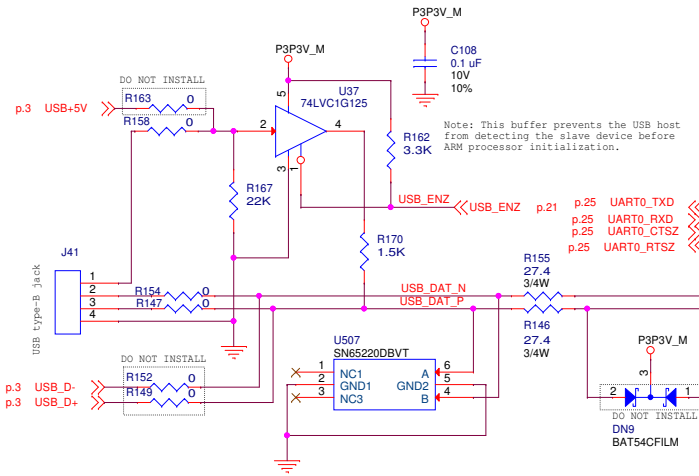
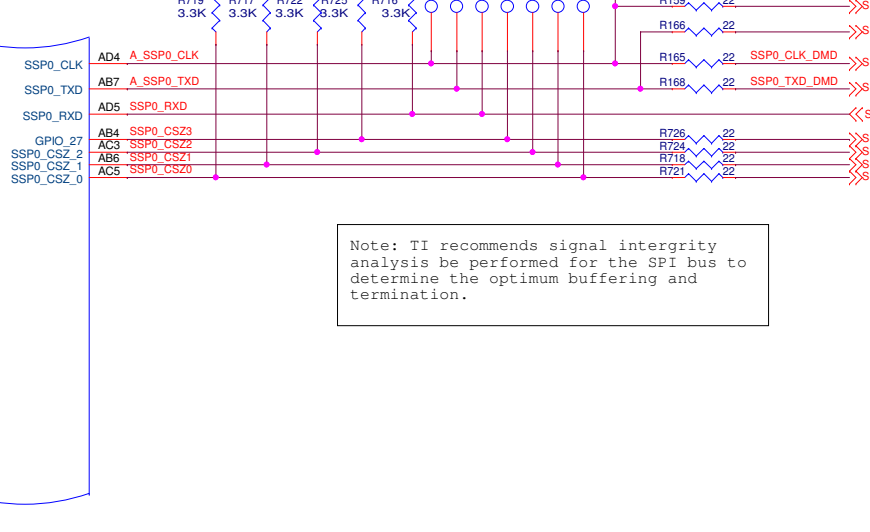
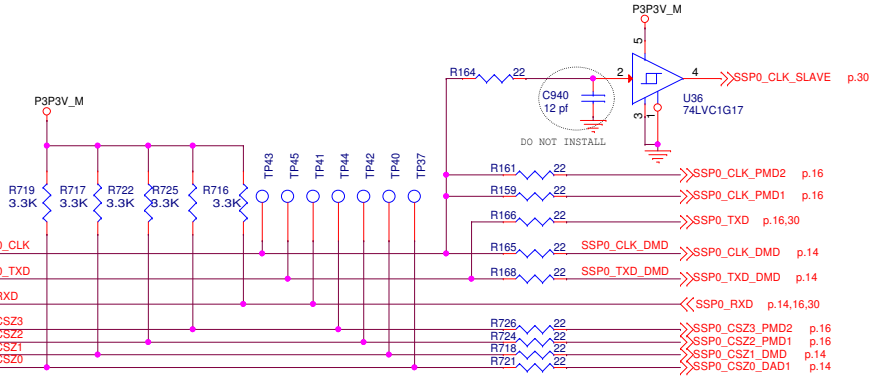
RS - 232 PORT 0




Note: TI recommends signal intergrity analysis be performed for the SPI bus to determine the optimum buffering and termination.



Master ASIC RS-232, Synchronous Serial Port, and USB

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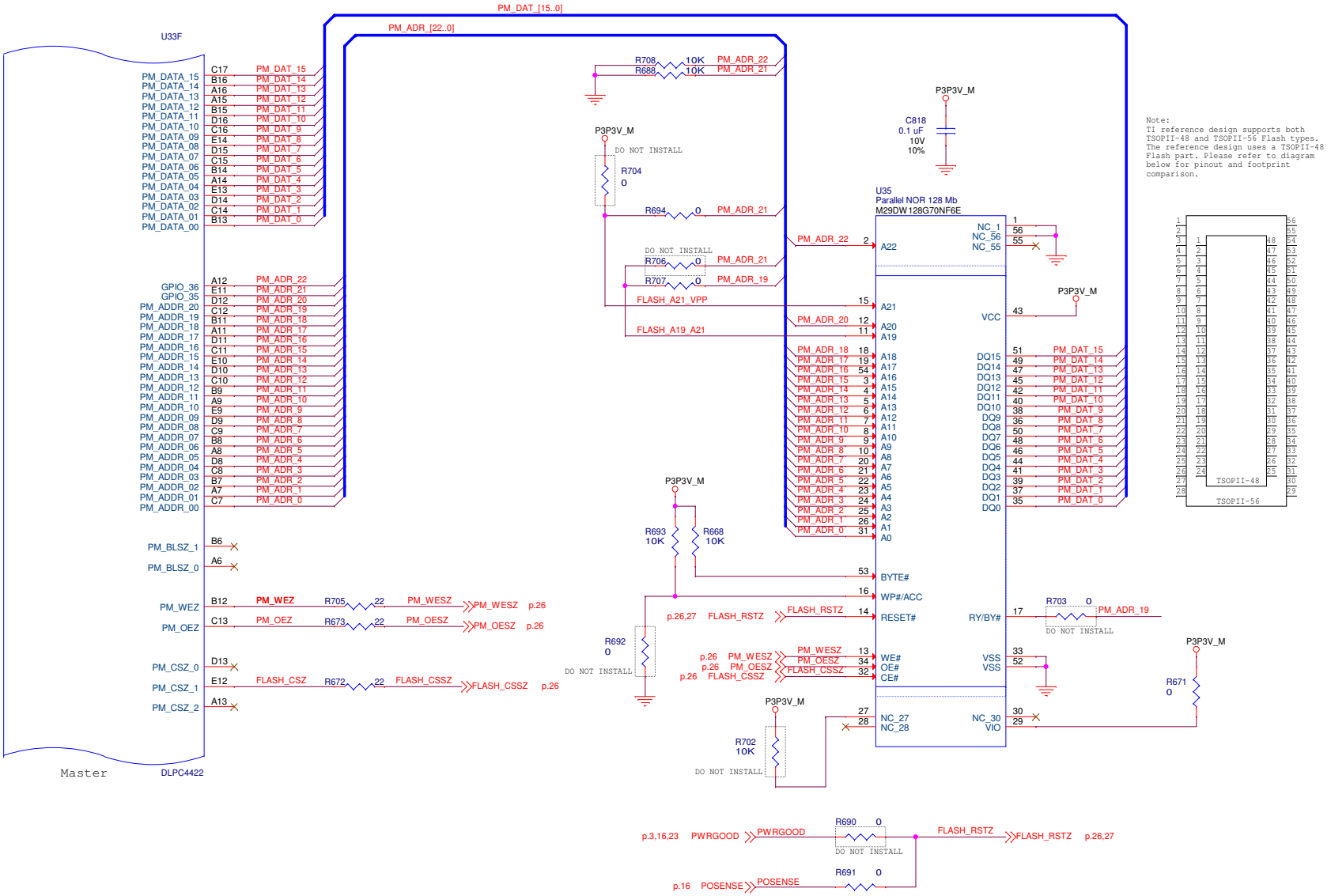
PM_DAT_[15..0]
PM_ADR_[22..0]
U33F
Master
DLPC4422
U35
Parallel NOR 128 Mb
M29DW128G70NF6E
P3P3V_M
DO NOT INSTALL
R704
R694
R706
R707
R708
R688
C818
0.1 uF
10V
10%
FLASH_A21_VPP
FLASH_A19_A21
R693
R668
R692
R702
R703
R671
R690
R691
R705
R673
R672
PM_WESZ
PM_OESZ
FLASH_CSSZ
FLASH_RSTZ
PWRGOOD
POSENSE
Note:
TI reference design supports both TSOPII-48 and TSOPII-56 Flash types. The reference design uses a TSOPII-48 Flash part. Please refer to diagram below for pinout and footprint comparison.
TSOPII-48
TSOPII-56
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Master ASIC Flash Memory Interface
TEXAS INSTRUMENTS
DWN Ben Uhing
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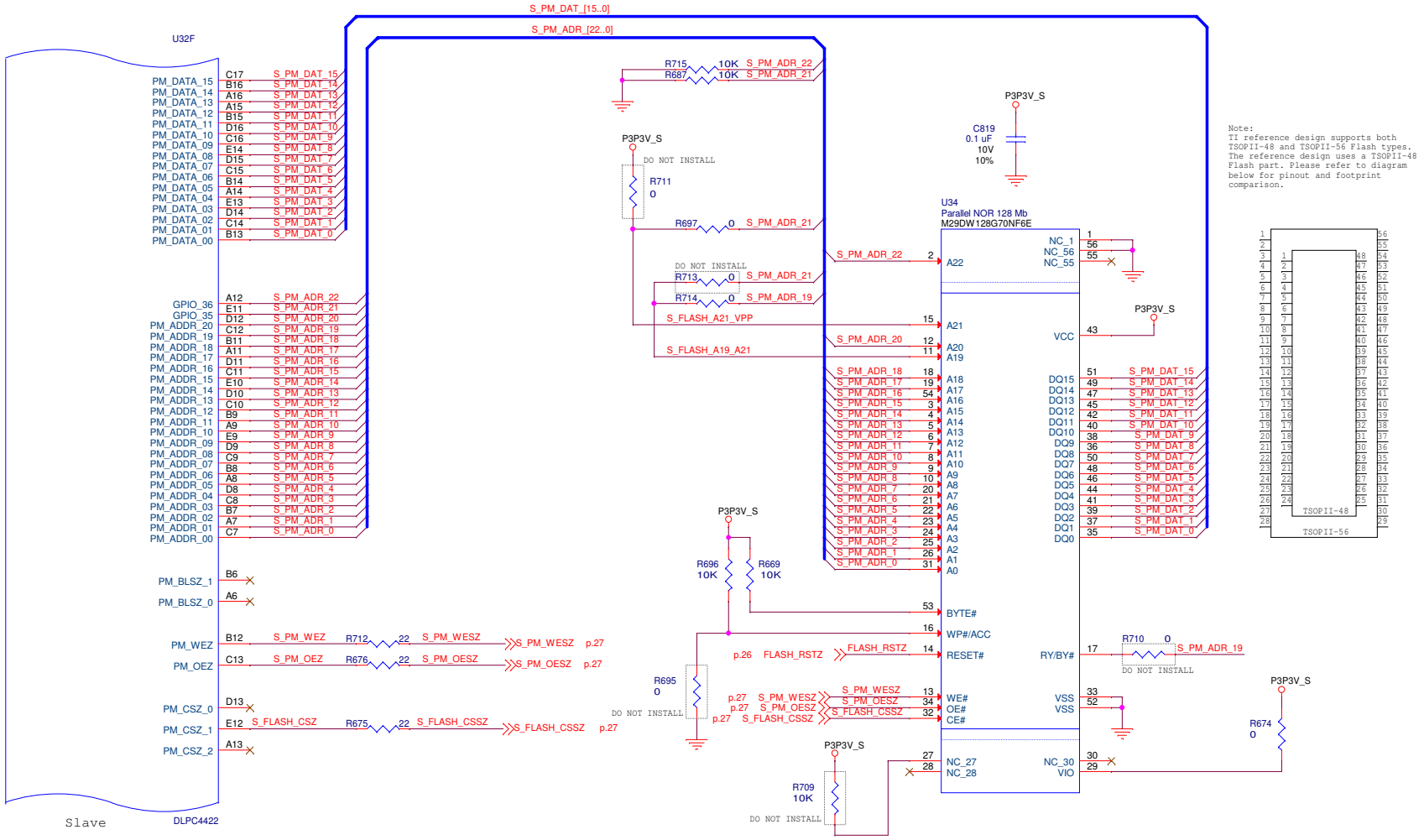




Slave ASIC Flash Memory Interface

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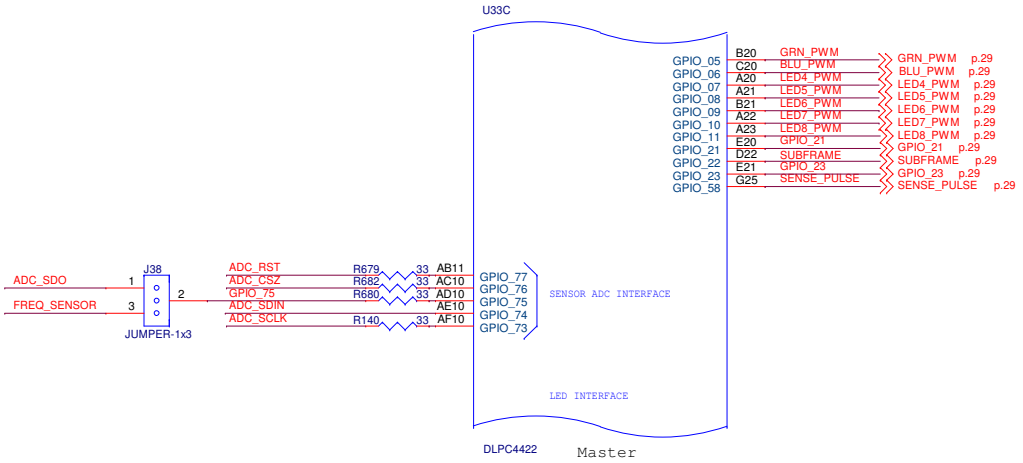
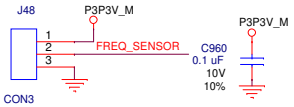
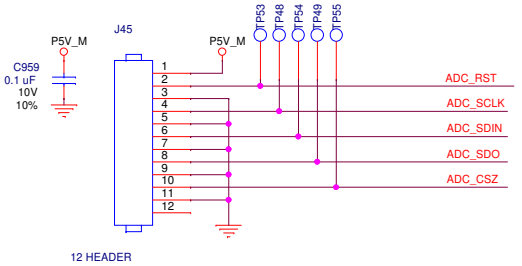



## LIGHT TO FREQUENCY SENSOR I/F




## ADC INTEGRATING SENSOR BOARD I/F






Master ASIC SSI Sensor Interface

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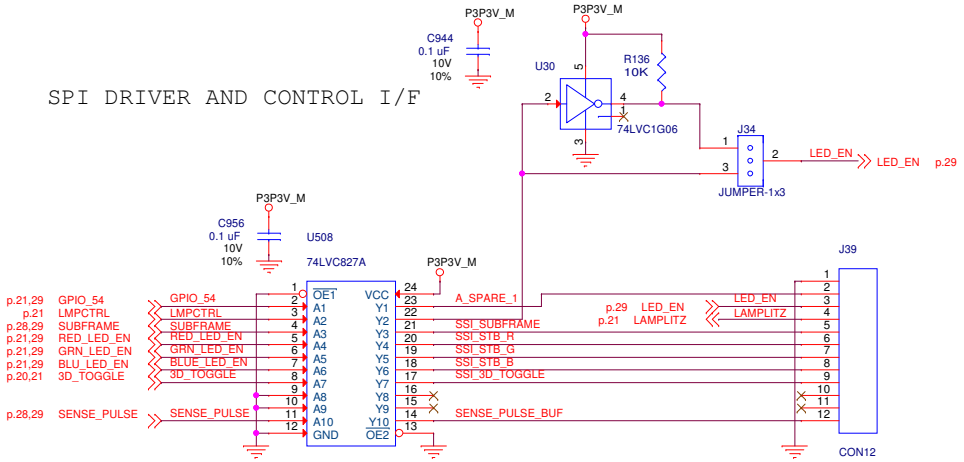
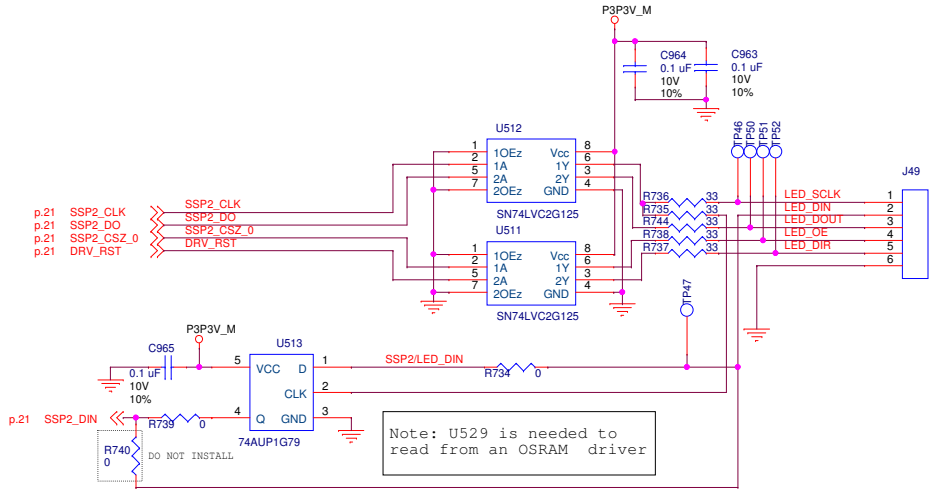
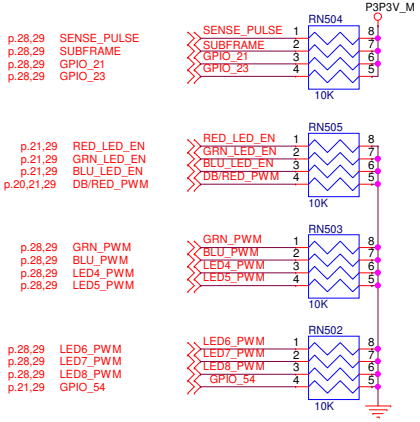
## SPI DRIVER AND CONTROL I/F

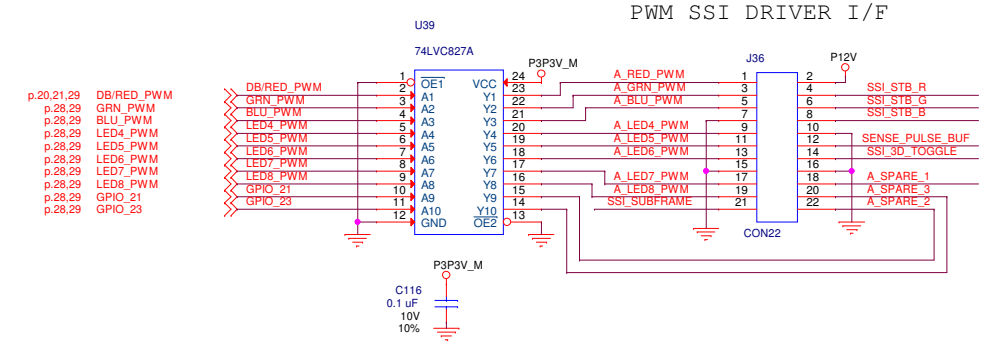


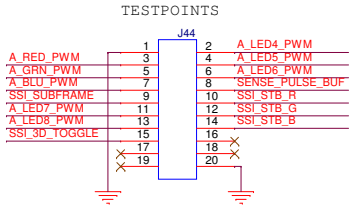

## PULL-UP/PULL-DOWN RESISTORS




## PWM SSI DRIVER I/F




## TESTPOINTS






SSI Driver Interfaces

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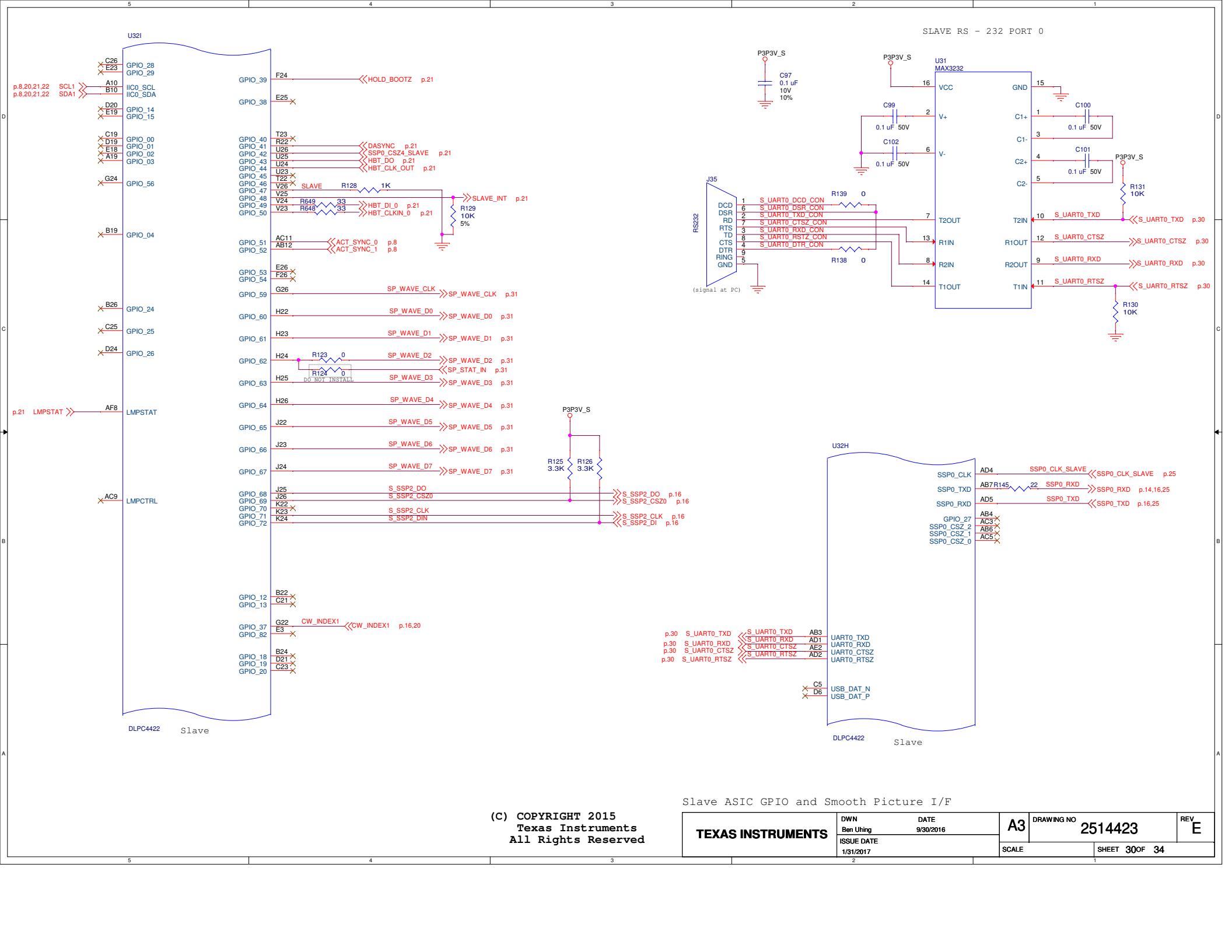




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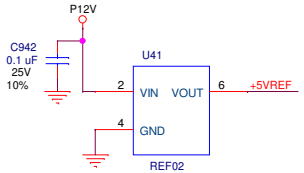
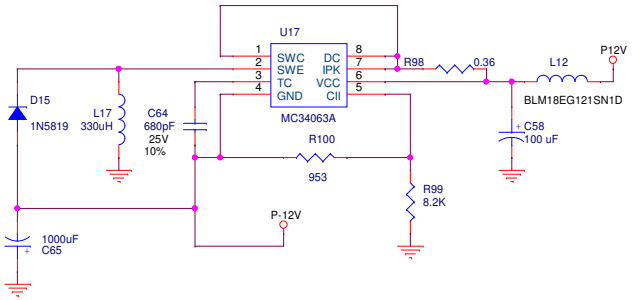
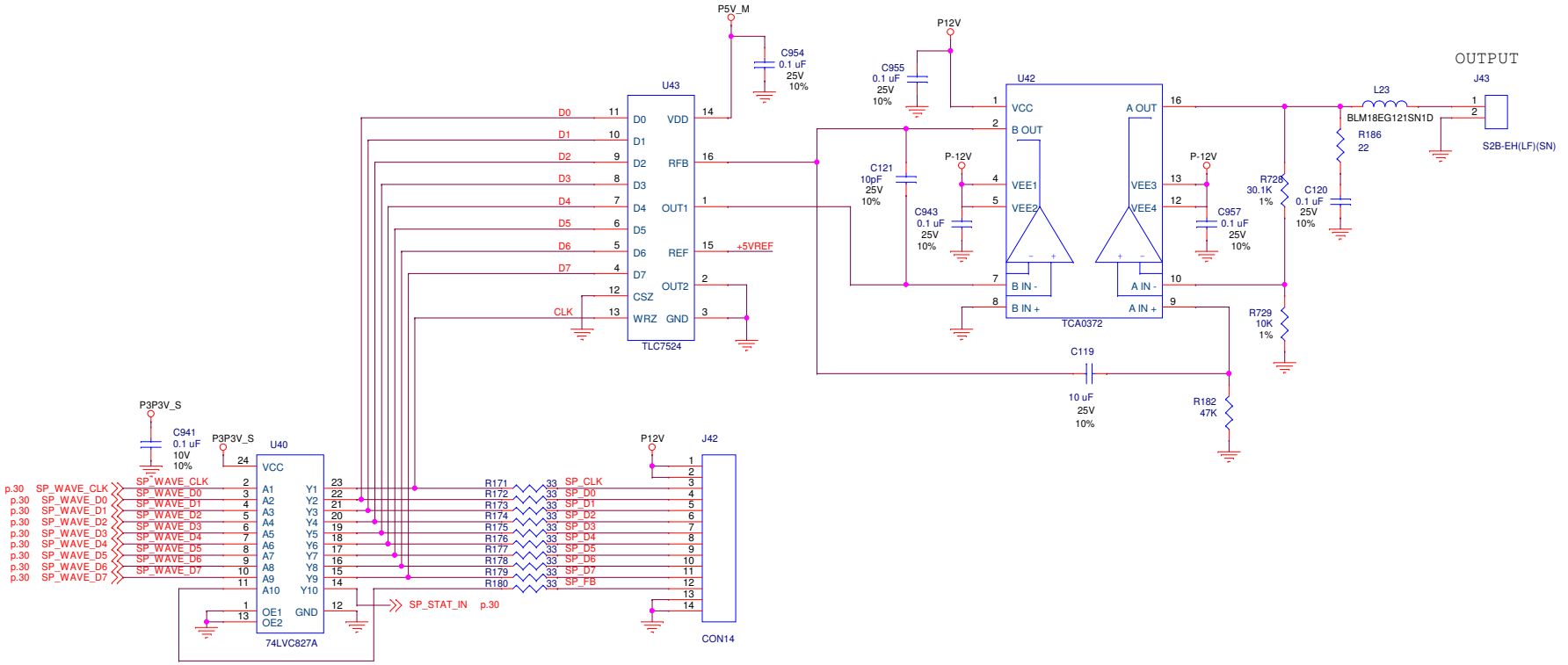
+5V REF




-12V Reg




Actuator I/F



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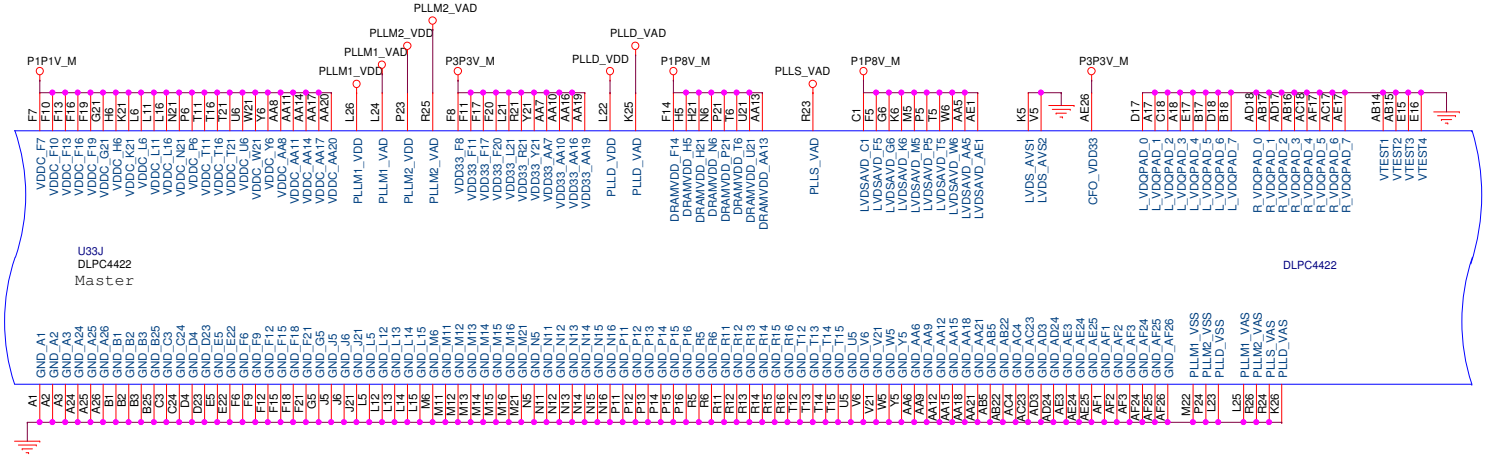


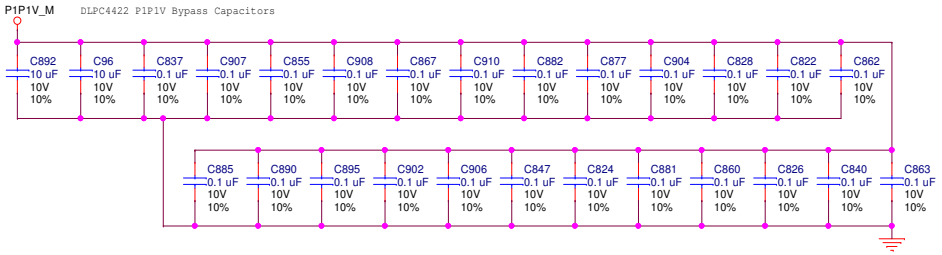


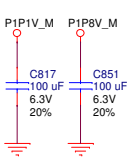


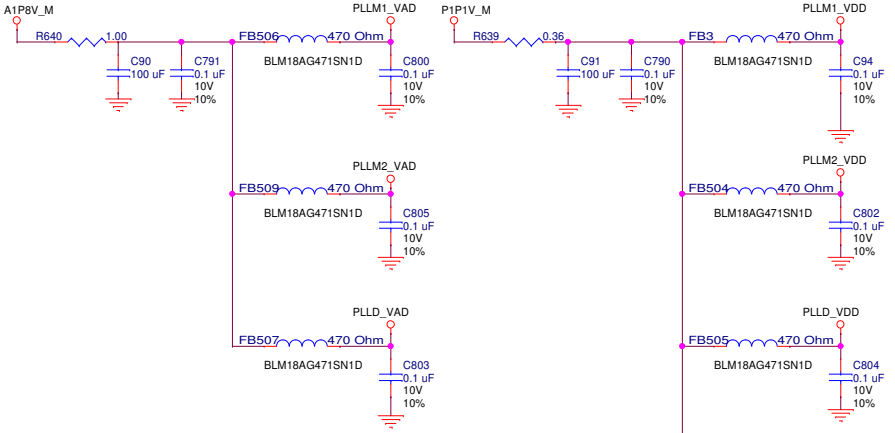


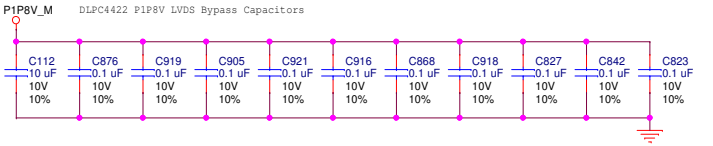


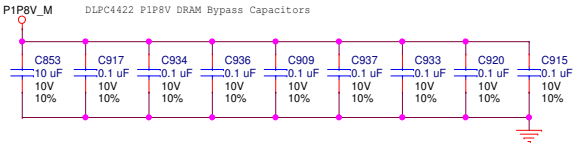


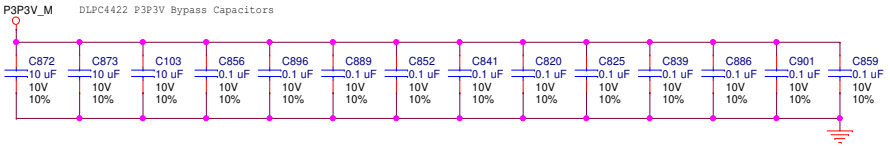




Master DLPC4422 Power and Bypass Capacitors

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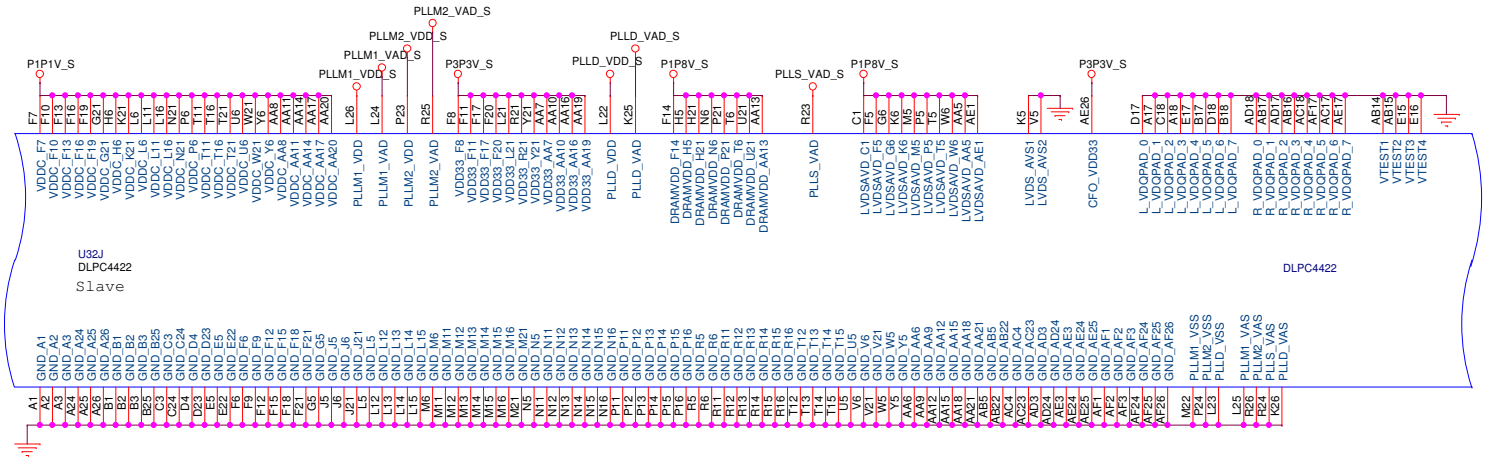


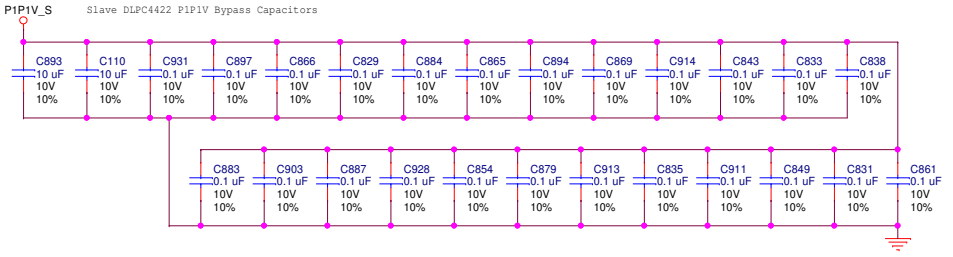


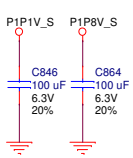


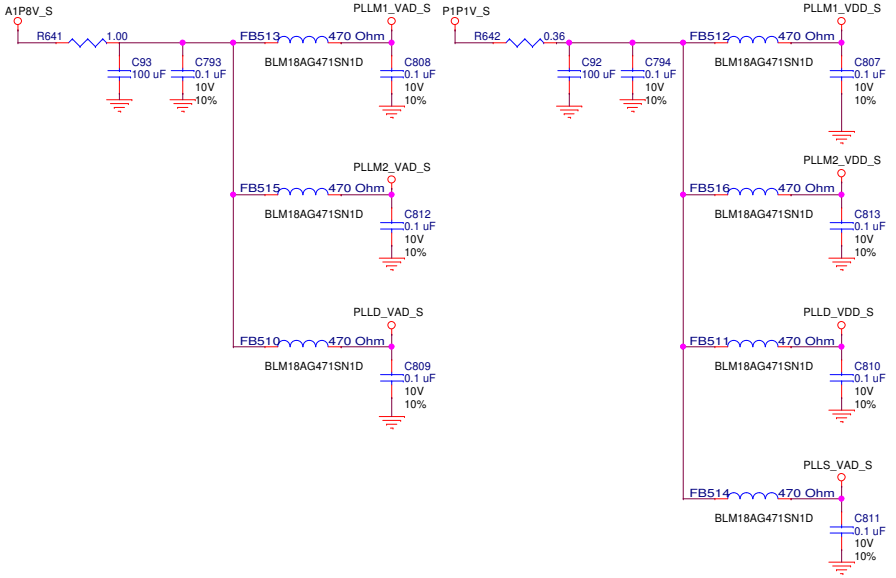


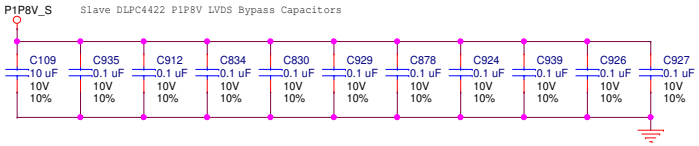


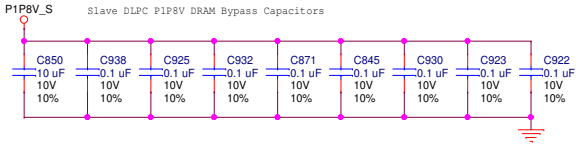


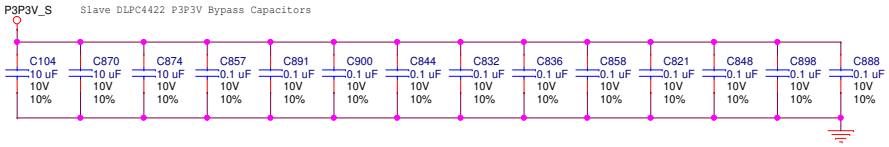


Slave DLPC4422 Power and Bypass Capacitors



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Revision B:
All Pages: Resequenced reference designators to align with layout
Page 1: Updated notes with correct voltage names
        Updated index
Page 4: Rearranged DDR3_1_DQ[15:0] for routability

Revision C:
Page 3: Change U5 to Do Not Install
        Updated C545 and C549 as Do Not Install
        Changed U506 to 75 Mhz
Page 11: Added Note Connecting pin 15 of U24 to P3P3V
Page 8:  Changed R89, R90, R91, R92, and R541 to 0 ohms.

Revision D:
Page  3:  Changed net name TEST_4A_AC6 to VX1_3D_EN.
          Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page  8:  Added R190, R191, R192, and R193.
          Changed net name TEST_4A_AC6 to VX1_3D_EN.
          Changed net name TEST_4A_AE6 to VX1_LR_SYNC.
Page 11:  Connected pin 15 of U24 to P3P3V.
Page 16:  Changed C799 and C801 to 1800pF.
Page 21:  Added note to ballast circuit.
Page 22:  Added R188 and R189.
Page 23:  Changed RN501 to Install, added J52 header.
Page 24:  Changed RN500 to Install, added J53 header.

Revision E:
Page 11:  Changed U24-10, C85 connection from P3P3V to P5V_S.

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