CC1150 Silicon Errata

Table 1. Advisory List

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PLL Lock Detector Output   *PLL lock detector output is not 100% reliable*

Revision(s) Affected   This errata note applies to all batches and revisions of the chip.

Details   The PLL lock detector output is not 100% reliable and might toggle even if the PLL is in lock. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. The PLL is not in lock if the lock detector output is constantly logic low. It is not recommended to check for PLL lock by reading PKTSTATUS[0] with GDO0_CFG=0.

Workaround(s)   PLL lock can be checked reliably as follows:

1. Program register *IOCFG0.GDO0_CFG=0x0A* and use the lock detector output available on the GDO0 pin as an interrupt for the MCU. A positive transition on the GDO0 pin means that the PLL is in lock.

2. Read register . The PLL is in lock if the register content is different from 0x3F.

   With both of the above workarounds, the CC1500 PLL calibration should be carried out without the automatic selection of high/low frequency settings for the VCO, (the selection should be done manually). The manual selection is done by writing a zero to TEST0 [1] to disable the automatic selection, and writing a zero or one to FSCAL2 [5] for selecting low or high VCO setting, respectively. The FSCAL2 [5] setting to use is depending on the operating frequency, and is calculated automatically by SmartRF™ Studio.

   It must be noted that the TEST0 register content is not retained in POWER DOWN state, and thus it is necessary to write to this register as described above when returning from the POWER DOWN state.

SPI Read Synchronization Issue   *SPI read synchronization results in incorrect read values for register fields that are continuously updated*

Revision(s) Affected   This errata note applies to all batches and revisions of the chip.

Details   A bug affecting the synchronization mechanism between the SPI clock domain (using a user supplied SCLK) and the internal 26 MHz clock domain (XCLK in this document) will sometimes result in incorrect read values for register fields that are continuously updated. The frequency with which this occurs is very low and guidelines for application design to avoid this issue are provided in this section. The issue does not affect writes to registers or the TX FIFO at any time..

Symptoms

When reading multi-bit register fields that are updated by the radio hardware such as the MARCSTATE or TXBYTES registers over the SPI interface, occasionally nonsensical or erroneous values will be read.

For example, in an application that sends packets longer than the 64-byte TX FIFO, the TX FIFO must be topped up with additional data during packet transmission. Assuming this is done by initially transferring 64 bytes to the TX FIFO, starting transmission, and then continuously polling TXBYTES to see when space for additional bytes is available, and then transferring the required number of bytes until the end of the packet. In this case the expected sequence of values read from TXBYTES would be:

64, 64, …, 63, (write byte), 64, 64, …, 63, (write byte), 64, ...

Due to the SPI synchronization issue the following might (infrequently) be seen instead:

64, 64, …, 63, (write byte), 64, 64, …, 64, 89, 63, …

The erroneous value read is highlighted in red. The register read is changing from the value 64 (01000000b) to the value 63 (00111111b) on the XCLK clock at the same time that its value is latched into the SPI output shift register on the SCLK clock. If the two clock edges occur sufficiently close in time, the improper synchronization mechanism will latch some bit values from the previous register value and some bits from the next register value, resulting in the erroneous value 89 (01011001b).

Description

During an SPI read transaction, the SPI output register latches the read value on the last falling edge of SCLK during an SPI address byte. For a burst read operation, subsequent register values are latched on the falling edge of SCLK in the last bit of each previous data byte.

Due to this synchronization issue, if the register being read changes value (synchronously with XCLK) during a certain period of time after this falling edge of SCLK then some of the bits in the read value will come from the previous value and some from the next value. This so-called window of uncertainty is about 1.3 ns for typical conditions and increases to about 2.0 ns for worst-case conditions (1.8 V VDD, 85 °C).
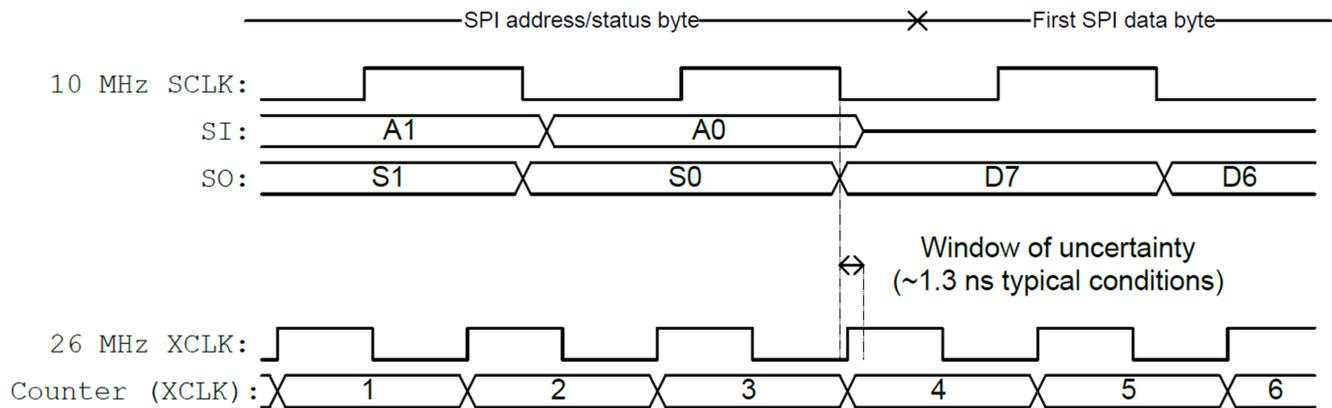
Figure 1. Window of Uncertainty (drawing not to scale)

Figure 1 shows a timing diagram of an SPI read that fails when reading a fictitious counter being updated internally each XCLK. Since the counter update from value 3 (011b) to 4 (100b) within the window of uncertainty, the read value could be any one of 0-7 (000b, 001b, 010b, 011b, 100b, 101b, 110b, 111b) depending on exactly when the positive edge of XCLK falls within the window of uncertainty.

What Kinds of Register Fields Are Affected?

This issue does not affect:

- Reading of the static configuration registers (registers 0x00-0x2F)
- Reading static status registers (PARTNUM, VERSION) or FS calibration (VCO_VC_DAC)
- Single-bit fields (all fields in PKTSTATUS, TXBYTES.TXFIFO_UNDERFLOW)

This issue does affect:

- The SPI status byte (shifted out while the host MCU supplies the address byte) fields STATE and FIFO_BYTES_AVAILABLE.
- Reading MARCSTATE at any other time than when the device is inactive (IDLE).
- Reading TXBYTES while transmitting a packet.

How Often Does the Issue Corrupt Read Values?

The probability of reading a corrupt value is given by the frequency with which the read value changes, f_c, and the length of window of uncertainty, T_{WU} (typically 1.3 ns). The probability that the two events overlap, and thus that the read value is potentially corrupted, is given by:

$$P_{corrupt} = \frac{T_{WU}}{T_c} = T_{WU} f_c$$

(1)

In the example given in the symptoms above, the probability of any single read from TXBYTES being corrupt, assuming the maximum data rate is used, is approximately $P_{corrupt} = T_{WU} f_c = 1.3 \text{ ns} \cdot 500 \text{ kbps} / 8b \approx 80 \text{ ppm}$ or less than once every 10000 reads.

In many situations the underlying received packet failure rate in the communication system is so much higher that any packet transmission/reception failure attributable to the issue described here will be negligible.

Workaround(s)   In a typical radio system a packet error rate of at least 1% should be tolerated in order to ensure robustness. In light of this, the negligible contribution to the number of packets lost due to, for example, occasionally reading incorrect FIFO byte count values or the wrong radio state from MARCSTATE, can probably be ignored in most applications. However, care should be taken to ensure that reading an incorrect value does not jeopardize an application. Examples of commonsense things to do include:

- For packets longer than the TX FIFO, configure the device to signal on a GDO pin when there is enough room to fill up with a new block of data (using the TX_THR threshold). If polling TXBYTES is necessary due to pin constraints, read TXBYTES repeatedly until the same value is returned twice in succession – such a value can always be trusted.

- Do not rely on the internal radio state machine through transient states (that is, CALIBRATE – SETTLING – TX – IDLE). It is, however, perfectly safe to poll for the end of transmission by waiting for MARCSTATE = IDLE.

- Always average RSSI and LQI values over several packets before using them in decision algorithms (that is, for FH channel selection).

- Avoid using the SPI status byte STATE and FIFO_BYTES_AVAILABLE fields during packet transmission.

If it is important to ensure that read values are not corrupted, reading of one of the affected registers should be done repeatedly until the same value is read twice in succession. If the rate at which the register is read is specified to be at least twice as fast as the expected register update rate, then an upper bound on the number of required reads is four and the average number of reads slightly more than two.

The same method can be used to ensure that the SPI status byte fields that provide simplified radio FSM state and saturated FIFO byte count are correct. This only makes sense when polling the status byte with SNOP as the address.

Compliance With Regulatory Limits *Reduced output power might be required at certain frequencies to ensure compliance with regulatory limits*

Revision(s) Affected   This errata note applies to all batches and revisions of the chip.

Details   The level of phase noise and close-in spurious emission, when using CC1150 in TX mode, is dependent on the operating frequency. Therefore reduced output power might be required at certain frequencies to ensure compliance with regulatory limits.

Workaround(s)   The level of close-in spurs is affected by crystal frequency, output power and the frequency being used. Thus changing crystal frequency or operating frequency might allow higher output power to be used. Since antenna performance affects output power, applications using a low gain antenna might not be affected by this issue.

Extra Byte Transmitted in TX   *Repetition of the first byte of the next transmission*

Revision(s) Affected   This errata note applies to all batches and revisions of the chip.

Details   If a transmission is aborted (TX mode exit) during the transmission of the first half of any byte, there will be a repetition of the first byte of the next transmission. This issues is caused by a state machine controlling an internal signal within the modulator. This signal asserts at the start of transmission of each full byte, then deasserts after half the byte has been transmitted. If transmission is aborted after a byte has started but before half the byte is transmitted this signal remains asserted and the first byte in the next transmission will be repeated.

Workaround(s)   As long as the packet handling features of the CC1150 are used, this will not be a problem since the chip will always exit TX mode after the transmission of the last bit in the last byte of the packet. If, however, one disables the packet handling features (MDMCFG2.SYNC_MODE=0) and wants to exit TX mode manually by strobing IDLE, one should make sure that the IDLE strobe is being issued after clocking out 12 dummy bits (8 dummy bits are necessary due to the TX latency, but since this would mean that transmission is aborted within the first half of a byte, 4 extra bits are added).

Revision History

Changes from C Revision (January 2007) to D Revision **Page**

- Removed ETSI and FCC sections. 2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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