

# CC2510Fx, CC2511Fx

## Silicon Errata



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## **CC2510Fx, CC2511Fx Silicon Errata**

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### **1 Known Design Exceptions to Functional Specifications**

**Table 1. Advisory List**

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**Issue 1** *Part May Hang in Power Mode*


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**Revision(s) Affected** All revisions affected

**Details** The following applies only to power mode 2 and power mode 3.

When waking up from power mode 2 and power mode 3, there is a small chance that the SLEEP.MODE bits are faulty set to a value other than zero before the PCON.IDLE bit is cleared by the CPU. This causes the chip to re-enter power mode immediately. Because an enabled interrupt is pending at this point, the chip will wake up and re-enter power mode continuously and appear to hang.

When the device hangs, only a system reset will get the chip back to normal operation.

**Workaround(s)** By ensuring that the SLEEP.MODE bits are written to zero at the instant the chip wakes from power mode, the chip will never re-enter power mode unintentionally.

If the following conditions are met, this can be done by setting up a DMA transfer to the SLEEP register that is triggered right before writing the PCON.IDLE bit.

- The chip is running at the HS RC oscillator at the highest possible clock speed setting
- The high-speed crystal oscillator is powered down
- Flash Cache is disabled

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**NOTE:** The requirements stated in the following chapters of the data sheet, *Low-Power SoC (System-on-Chip) with MCU, Memory, 2.4 GHz RF Transceiver, and USB Controller (SWRS055)* still apply:

- *Power Management Control*
  - *Sleep Timer and Power Modes*
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**NOTE:** The code in [Figure 1](#) assumes the chip is already running at the HS RC oscillator with the highest clock speed setting possible and this must be handled by the application. The code marked blue below is timing critical and must be done in the order as shown here with no intervening code.

---

```

// Initialization of source buffers and DMA descriptor for the DMA transfer
unsigned char __xdata PM2_BUF[7] = {0x06,0x06,0x06,0x06,0x06,0x06,0x04};
unsigned char __xdata PM3_BUF[7] = {0x07,0x07,0x07,0x07,0x07,0x07,0x04};
unsigned char __xdata dmaDesc[8] = {0x00,0x00,0xDF,0xBE,0x00,0x07,0x20,0x42};

// Store current DMA channel 0 descriptor and abort any ongoing transfers if //
the channel is in use
unsigned char storedDescHigh = DMA0CFGH;
unsigned char storedDescLow = DMA0CFGL;
DMAARM |= 0x81;

// Update descriptor with correct source
// NB! Replace &PM2_BUF with &PM3_BUF if powermode 3 is chosen instead
dmaDesc[0] = (unsigned int)& PM2_BUF >> 8;
dmaDesc[1] = (unsigned int)& PM2_BUF;

// Associate the descriptor with DMA channel 0 and arm the DMA channel
DMA0CFGH = (unsigned int)&dmaDesc >> 8;
DMA0CFGL = (unsigned int)&dmaDesc;
DMAARM = 0x01;

// NOTE! At this point, make sure all interrupts that will not be used to
// wake from PM are disabled as described in chapter 13.1.3 of the datasheet.

// Align with positive 32 kHz clock edge as described in chapter 13.8.2
// of the datasheet.
char temp = WORTIME0;
while( temp == WORTIME0);

// Make sure XOSC is powered down when entering PM2/3 and that the flash
// cache is disabled
// NB! Replace 0x06 with 0x07 if power mode 3 is chosen instead
MEMCTR |= 0x02;
SLEEP = 0x06;

// Enter power mode as described in chapter 13.1.3 in the datasheet.
// Make sure DMA channel 0 is triggered just before setting PCON.IDLE
asm("NOP");
asm("NOP");
asm("NOP");
if( SLEEP & 0x03 ) {
    asm("MOV 0xD7,#0x01");    // DMAREQ = 0x01;
    asm("NOP");              // Needed to perfectly align the DMA transfer
    asm("ORL 0x87,#0x01");    // PCON |= 0x01;
    asm("NOP");
}

// Enable Flash Cache
MEMCTR &= ~0x02;

// Update DMA channel 0 with original descriptor and arm channel if it was in //
use before PM was entered
DMA0CFGH = storedDescHigh;
DMA0CFGL = storedDescLow;
DMAARM = 0x01;

```

**Figure 1. Example Code**

## Issue 2 *RX\_OVERFLOW Issue*

**Revision(s) Affected** All revisions affected

**Details**

In addition to the RFD register, the CC251xFx devices have several internal buffers for status registers, CRC bytes, and buffers used when FEC is enabled. If there is a byte in the RFD register and more bytes are written to this register by the radio, the radio will enter RX\_OVERFLOW state. However, there are some cases where the radio will be stuck in RX state instead of entering RX\_OVERFLOW state, as it should. [Table 2](#) lists the register settings that will cause this problem. APPEND\_STATUS is found in the PKTCTRL1 register, CRC\_EN is found in the PKTCTRL0 register, and FEC\_EN is in the MDMCFG1 register. In [Table 2](#), x is the number of bytes that will be written to the RFD register by the radio (including the status bytes if APPEND\_STATUS = 1). Assume that the radio is configured to enter IDLE state after a packet has been received.

When the radio is stuck in RX state like this, it will draw current as in RX state, but it will not be able to receive any more data. Neither RFIF.IRQ\_DONE nor RFIF.IRQ\_RX\_OVF will be asserted. The only way to proceed is by issuing an SIDLE strobe command (RFST = 0x04).

**Table 2. Register Settings That May Lead to RX\_OVERFLOW Issue**

Register Settings	# of Bytes Read from the RFD Register	MARSTATE	Comment
APPEND_STATUS = 1 CRC_EN = 0 FEC_EN = 0	x - 1	RX_OVERFLOW	Ok
	x	IDLE	Ok
APPEND_STATUS = 1 CRC_EN = 0 FEC_EN = 1	x - 6	RX_OVERFLOW	Ok
	x - 5	RX	Not ok. Stuck in RX
	x - 4	RX	Not ok. Stuck in RX
	x - 3	RX	Not ok. Stuck in RX
	x - 2	RX	Not ok. Stuck in RX
	x - 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok
APPEND_STATUS = 1 CRC_EN = 1 FEC_EN = 0	x - 3	RX_OVERFLOW	Ok
	x - 2	RX	Not ok. Stuck in RX
	x - 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok
APPEND_STATUS = 1 CRC_EN = 1 FEC_EN = 1	x - 5	RX_OVERFLOW	Ok
	x - 4	RX	Not ok. Stuck in RX
	x - 3	RX	Not ok. Stuck in RX
	x - 2	RX	Not ok. Stuck in RX
	x - 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

**Table 2. Register Settings That May Lead to RX\_OVERFLOW Issue (continued)**

Register Settings	# of Bytes Read from the RFD Register	MARCSTATE	Comment
APPEND_STATUS = 0 CRC_EN = 0 FEC_EN = 0	x - 1	RX_OVERFLOW	Ok
	x	IDLE	Ok
APPEND_STATUS = 0 CRC_EN = 0 FEC_EN = 1	x - 4	RX_OVERFLOW	Ok
	x - 3	RX	Not ok. Stuck in RX
	x - 2	RX	Not ok. Stuck in RX
	x - 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok
APPEND_STATUS = 0 CRC_EN = 1 FEC_EN = 0	x - 1	RX_OVERFLOW	Ok
	x	IDLE	Ok
APPEND_STATUS = 0 CRC_EN = 1 FEC_EN = 1	x - 3	RX_OVERFLOW	Ok
	x - 2	RX	Not ok. Stuck in RX
	x - 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

**Workaround(s)**

In applications where the DMA is used to read the RFD register, it is important to configure the DMA in accordance with the chosen radio configuration (see [SWRA164](#), *Design Note DN107 DMA and Radio Configuration*, for more details). If the RFD register is read manually, it is important that the register is read when the RFTXRIF flag in the TCON register has been asserted. If the RFTXR interrupt is used, it is important that this interrupt has a high priority. If a polling scheme is used, ensure that enabled interrupts will not prevent the RFD register to be read before a new byte is received.

**Issue 3** *Premature XOSC\_STB Assertion*

**Revision(s) Affected** All revisions affected

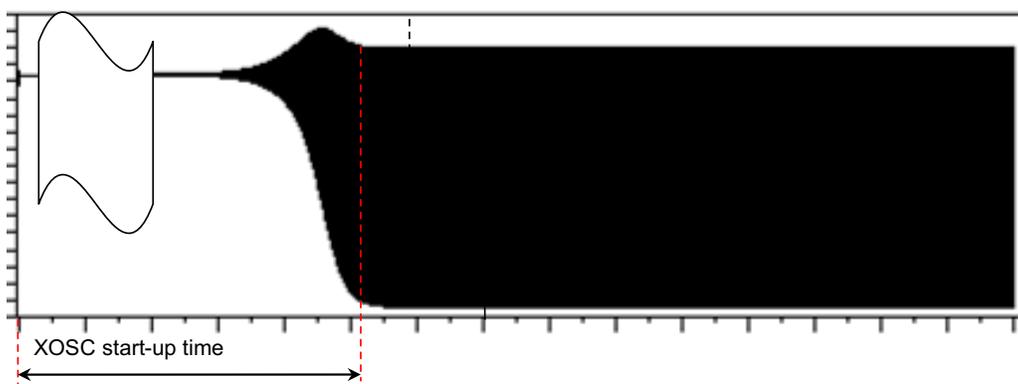
**Details** The XOSC\_STB signal (crystal oscillator stable signal) is derived from an internal ripple counter that counts clock pulses during oscillator start-up. Due to the very small oscillation amplitude during the initial crystal start-up, the ripple counter can, in some cases, trigger on power noise instead of the actual crystal swing, and there is a finite possibility that the ripple counter used to set XOSC\_STB can assert XOSC\_STB prematurely.

If the HS XOSC is turned on by selecting it as source for the system clock (CLKCON.OSC = 0), CLKCON.OSC will remain 1 (and keep the HS RCOSC as source) until the SLEEP.XOSC\_STB bit is asserted. In the cases where XOSC\_STB is asserted prematurely, the system clock will change clock source prematurely and end up running on an unstable clock, which causes unpredictable behavior.

**Workaround(s)** The HS XOSC must be turned on by setting SLEEP.OSC\_PD = 0. A SW delay should then be implemented to make sure the crystal is stable before selecting the HS XOSC as system clock (CLKCON.OSC = 0). The SW delay must be greater than the maximum start-up time of the crystal.

```
SLEEP &= ~0x04; // Power up both oscillators (HS XOSC and HS RCOSC)
delay(); // Delay longer than max crystal start-up time
CLKCON &= ~0x40; // Set high speed crystal oscillator as system clock
```

Figure 2 shows the XOSC\_Q1 pin as the crystal is turned on. When measuring on XOSC\_Q1, use a high-impedance probe to avoid loading the crystal.



**Figure 2. XOSC Start-Up Time**

When finding the max start-up time, measure on several crystals over temperature. A 100% margin should be added to the measured start-up time to account for process variations.

## 2 Revision History

Revision	Date	Description
SWRZ014D	8/14/2015	Updated with issue related to the XOSC_STB signal.
SWRZ014C	12/21/2007	Updated with issue related to RX_OVERFLOW state. Removed <i>Batches Affected</i> because there is only one revision available for this product.
SWRZ014B	9/18/2007	Updated with clarified conditions to fix and update the code to remove instability.
SWRZ014A	9/6/2007	Released for RTM.
1.2	6/6/2006	Removed <i>Switching Between Power Modes</i> issue due to a floating signal causing the problem under testing.
1.1	6/1/2006	Added general information. Minor text changes.
1	5/30/2006	First edition.

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