Technical Article

High-frequency resonant converter design considerations, Part 1

Sheng-Yang Yu

High-frequency resonant converter design considerations include component selections, design with parasitic parameters, synchronous rectifier design, and voltage gain design. This power tip focuses on key parameters that affect switching component selection, as well as the effect of transformer intrawinding capacitance in a high-frequency resonant converter.

The commercialization of wide bandgap (WBG) devices over the past decade has enabled the operation of power converters at much higher frequencies for higher power density. High-performance power supplies are just starting to include WBG devices – especially silicon carbide and gallium nitride field-effect transistors (FETs) – because of their output capacitance (C_{oss}), gate charge (Q_g), on-resistance ($R_{DS(on)}$), and reverse-recovery charges (Q_{rr}), all lower (or nonexistent) than silicon or silicon super-junction FETs at the same breakdown voltage level. A lower Q_g reduces the driving power needed – $P_{drive} = V_{drive}\ Q_g\ F_{sw}$ – and a lower $R_{DS(on)}$ reduces the conduction loss, where V_{drive} is the driving voltage and F_{sw} is the FET switching frequency. Other than Q_g and $R_{DS(on)}$, it's also important to consider C_{oss} and Q_{rr} when selecting components in high-frequency converters.

In a resonant converter like the inductor-inductor-capacitor-series resonant converter (LLC-SRC) shown in Figure 1 , the current in the resonant tank charges/discharges the C_{oss} of the FETs (state 1 in Figure 2) in order to achieve zero voltage switching (ZVS). ZVS means that the FET drain-to-source voltage (V_{DS}) reaches zero before its gate voltage goes high. Therefore, a lower C_{oss} enables a shorter dead time under the same resonant tank current level to achieve ZVS. A shorter dead time means a larger duty cycle and a lower root-mean-square (RMS) current on the primary-side resonant tank and FETs, which means higher efficiency and the ability to operate the converter at a higher switching frequency.

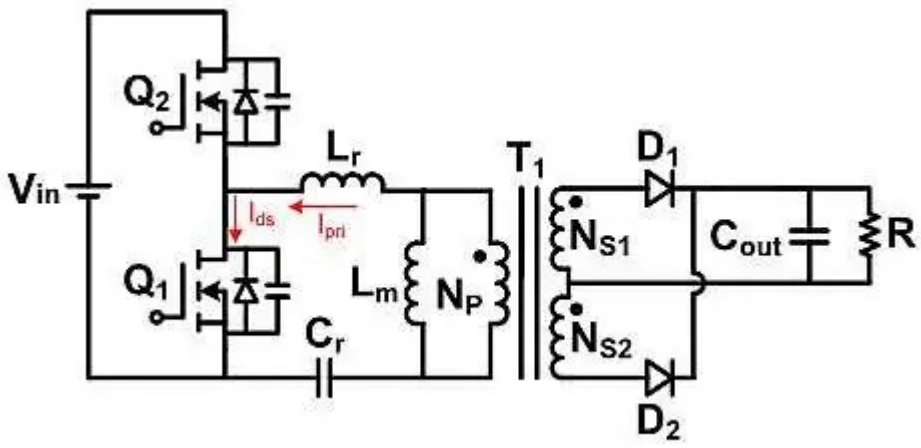

Figure 1. LLC-SRC

To achieve ZVS, there is always a period during which the body diode of the FET conducts current – state 2 in Figure 2 . If the FET has Q_{rr} and is turned on again when the body diode still conducts current, the FET itself will create a reverse current to discharge Q_{rr} and cause hard switching and high voltage stress – potentially damaging the FET.

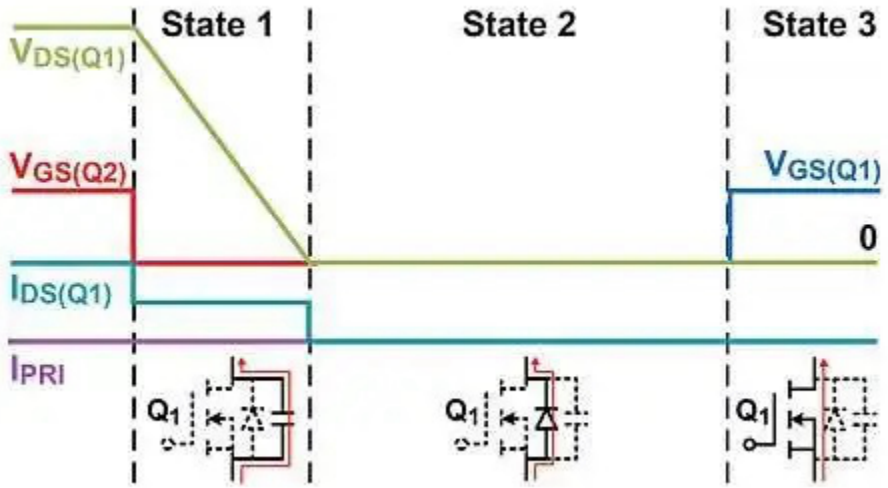

Figure 2. Switching transitions of an LLC-SRC

Figure 3 illustrates this hard switching phenomenon during the startup process of an LLC-SRC as illustrated in Figure 1. When FET Q_2 first conducts current, inductor current I_{PRI} is built up. The current I_{PRI} then conducts through FET Q_1 channel and body diode. Without allowing the current to go in the reverse direction, FET Q_2 turns on again. Because of the Q_{rr} , FET Q_1 self-generates a reverse current to discharge Q_{rr} , which results in high voltage stress.

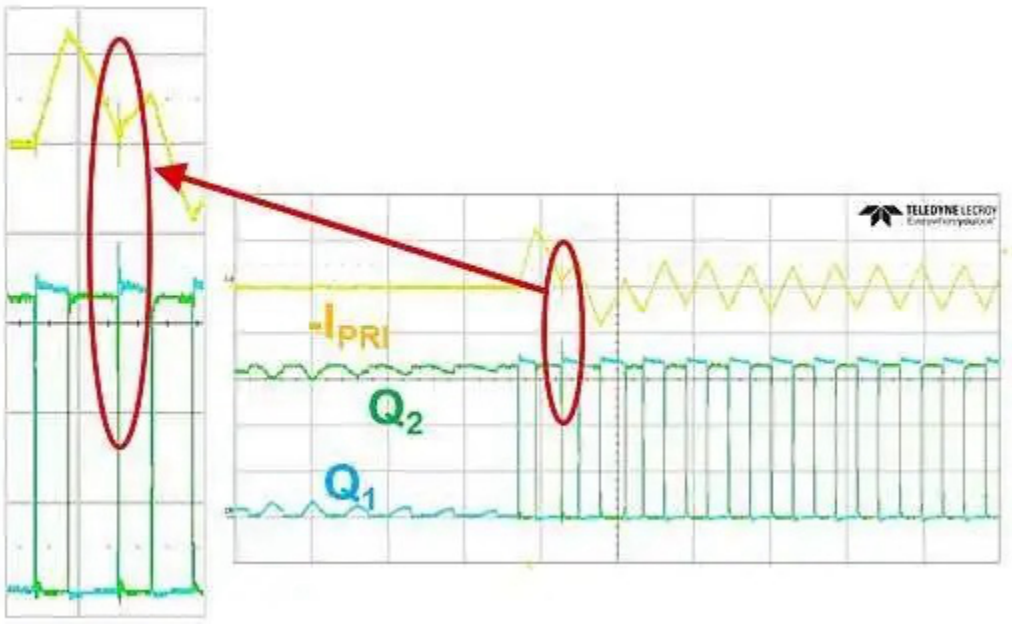

Figure 3. Hard switching due to Q_{rr}

In a high-frequency resonant converter, the resonant tank impedance is generally much lower than that in a low-frequency resonant converter. Therefore, the startup inrush current in a high-frequency resonant converter is expected to be higher. Using the LLC-SRC in Figure 1 as an example, when the output voltage is zero (the initial condition at startup), the only impedance limiting the startup current when Q_2 first conducts is L_r – the series resonant inductor in the LLC-SRC. High-efficiency and high-frequency resonant converter designs, especially bus converters, generally minimize L_r in order to improve efficiency. A smaller L_r value makes the startup current higher under the same startup frequency and thus more vulnerable to Q_{rr} -related hard switching. Therefore, it is essential to use low Q_{rr} FETs in high-frequency resonant converters.

Harnessing the aforementioned benefits of WBG devices, it is possible to operate isolated resonant converters in the megahertz range, which is 5 to 10 times faster than traditional isolated power supplies. In this “higher frequency” domain, many parameters once considered “negligible” during the converter design process are no longer negligible, such as the transformer intrawinding capacitor.

In the traditional resonant converter design process, the designer must ensure that the energy stored in the resonant tank is higher than the energy stored in the FET C_{oss} so that C_{oss} depletes the energy stored in the resonant tank to achieve ZVS. Taking the LLC-SRC shown in Figure 1 as an example, Equation 1 ensures the validity of this inequality:

$$L_m I_{L_m}^2 \geq 2 C_{oss} V_{in}^2 \tag{1}$$

where I_{Lm} is the peak current of the magnetizing inductor L_m and V_{in} is the input voltage of the LLC-SRC. Equation 1 can be rewritten as Equation 2 by applying Ohm’s law for the inductor to L_m :

$$L_m \leq \frac{n^2 V_{out}^2}{32 C_{oss} V_{in}^2 F_{sw}^2} \tag{2}$$

where n = N_p :N_{s1} (assuming N_{s1} = N_{s2}) is the transformer turns ratio and V_{out} is the output voltage.

When resonant converter designs need to cover a wide operation range and holdup time, L_m is generally much smaller than the value on the right side of Equation 2 in order to keep L_n = L_m /L_r low (applying L_n values from 4 to 10 in a closed-loop LLC-SRC design). When resonant converter designs such as bus converters require high converter efficiency, maximizing L_m lowers the primary RMS current for a lower conduction loss. In this case, the L_m value will be closed to the value on the right side of Equation 2. Equation 2 only represents the ideal condition with an ideal transformer, however. In a real transformer, many parameters could affect the C_{oss} charge and discharge capability. The most critical parameter is the intrawinding capacitance.

Figure 4 shows a simplified circuit model during a switching transient in an LLC-SRC, where current on L_m (I_{Lm}) discharges C_{eq} (the C_{oss} of two FETs in series with resonant capacitor C_r), assuming C_r as a voltage source. Without the transformer intrawinding capacitance (C_{TX}), all of I_{Lm} goes to C_{eq} and Equation 2 is valid. But with the presence of C_{TX} , some of I_{Lm} has to go to C_{TX} to change the transformer winding polarity, which reduces the C_{oss} discharge capability and creates the possibility of losing ZVS. Therefore, it is essential to keep C_{TX} lower by keeping layers of primary winding apart from each layer with distance as well as layers distance of secondary windings.

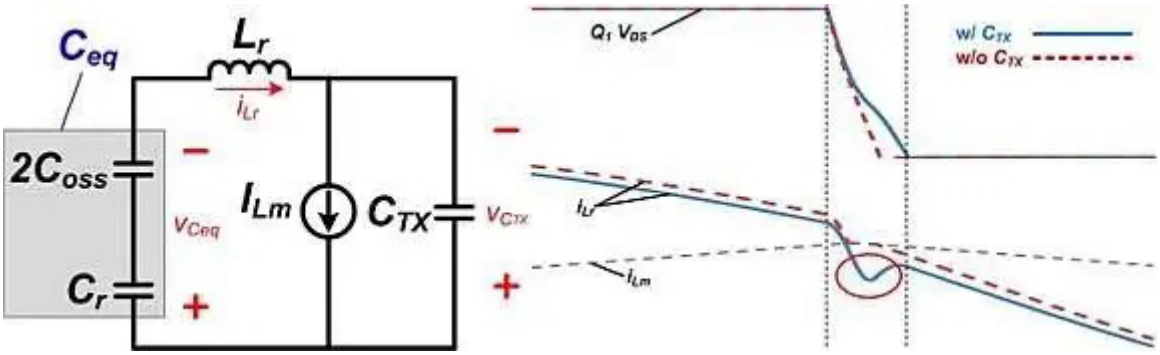

Figure 4. The effect of a transformer intrawinding capacitor

A rule of thumb in determining the L_m value is to use just half of the maximum L_m value calculated using Equation 2, as it is generally difficult to predict the C_{TX} value before actually building a transformer. C_{TX} generally falls inside the range of 22 pF to 100 pF in a converter with a 400-V input. It is also very useful to model C_{TX} in a circuit simulation once the transformer structure is fixed, in order to ensure a low-enough L_m with margin.

In the next installment of this series, I will focus on synchronous rectifier design challenges in high-frequency resonant converter designs.

Related articles:

- Power Tips #84: Think outside the LLC series resonant converter box
- MOSFET Qrr: Ignore at your peril in the pursuit of power efficiency
- Design considerations when selecting half bridge resonant LLC converters and primary side MOSFETs
- Using quasi-resonant and resonant converters

Previously published on EDN.com.

Trademarks

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265