Technical Article

Complete Clock-tree Solutions That Make a Hardware Designer's Life Easier

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Are you solving your system clocking needs using discrete crystals and clock oscillators? It does seem like an obvious approach for most hardware designers, who do not have the time to scour the internet for optimized clock-tree solutions including clock generator ICs and buffer/distribution devices. Although less time consuming, the approach of using discrete crystals and oscillators can often lead to an increase in bill-of-materials (BOM) cost and lower performance of the overall system. WEBENCH® Clock Architect is the industry's first clock and timing tool that recommends a system clock-tree solution covering devices from TI's extensive clocking portfolio. The patented, multiple-part recommendation algorithm – the backbone of the tool – provides quick solutions and a hassle-free experience for designers searching for high-performance, flexible clocking solutions.

Aside from recommending optimized clock-tree solutions, the tool features advanced phased-locked loop (PLL) filter-design capability and phase-noise simulation, enabling you to simulate and optimize clock-tree designs to meet your system needs. Let's take a look at some of the more recent feature upgrades.

You can now enter custom phase-noise profiles for external references such as crystal oscillators (XOs), voltage-controlled crystal oscillators (VCXOs) and voltage-controlled oscillators (VCOs). Accurate modeling of external reference sources helps greatly improve the accuracy of the device output clock-phase noise/jitter-simulation results. See Figure 1.

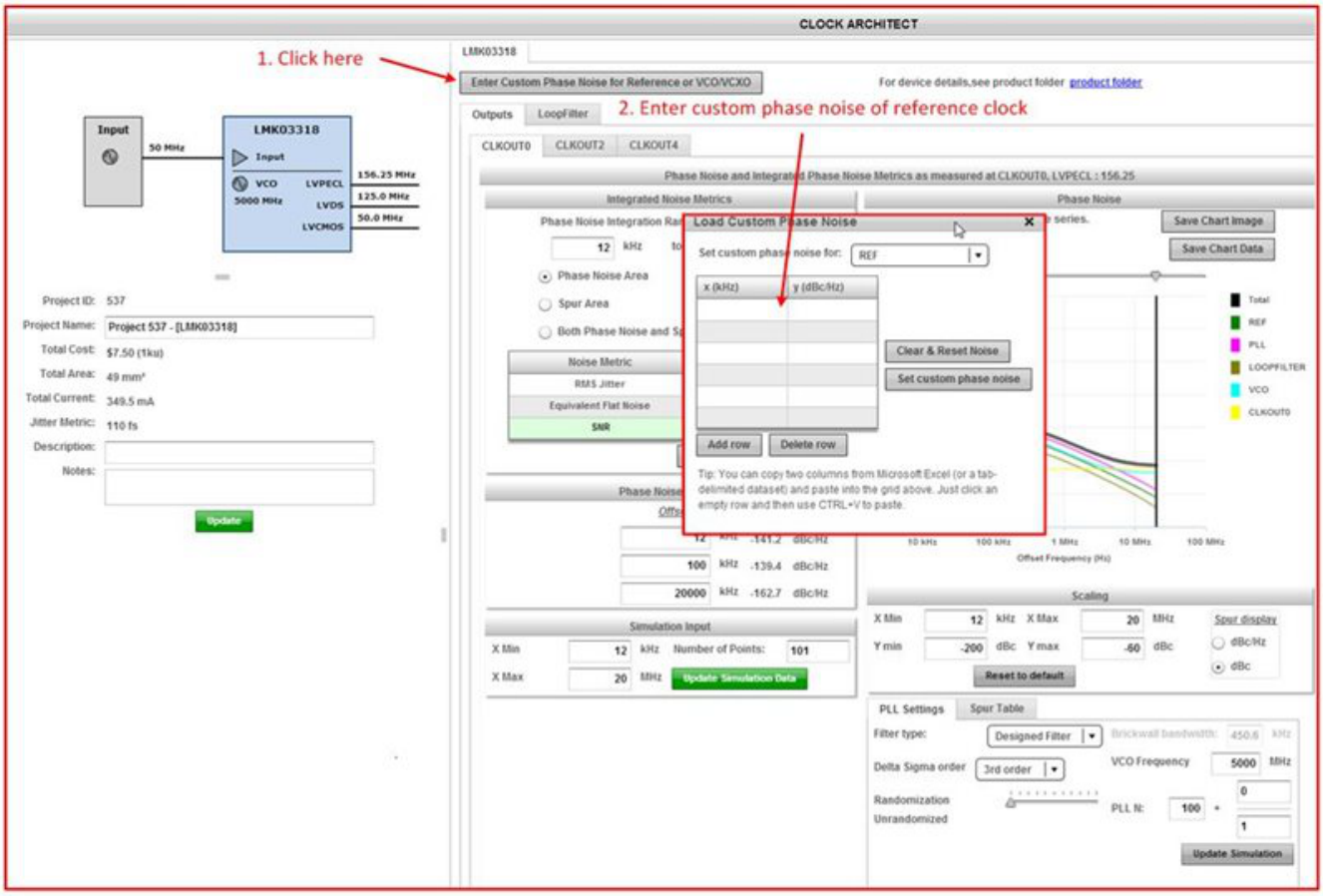

Figure 1. Enter Custom Phase-noise for Reference Clocks

WEBENCH Clock Architect lets you select a specific TI clocking device (or multiple devices using regular expressions) from a drop-down list. Figure 2 is a screenshot of the step during which you select the device of your choice, enter the input and output frequencies, and design a loop filter or simulate phase noise.

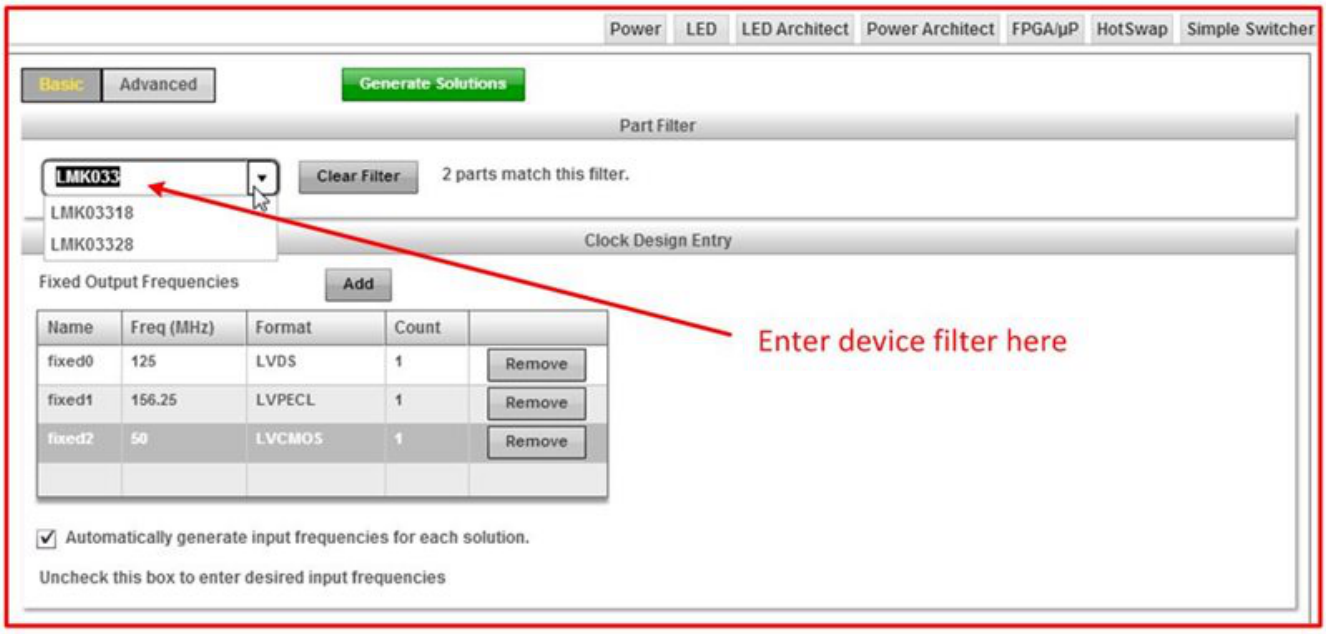

Figure 2. Device Filter

The phase-noise simulation results from the tool match actual silicon performance closely. However, until recently, the phase-noise simulation of fractional-N PLLs did not include spurs. The latest upgrade to WEBENCH Clock Architect includes modeling of the PLL phase detector and fractional, subfractional and other part-specific spurs for a majority of devices. We constantly strive to improve spur modeling in the tool and continue to add part-specific upgrades. Figure 3 shows an example of a fractional-N PLL generated output clock phase-noise plot with spurs.

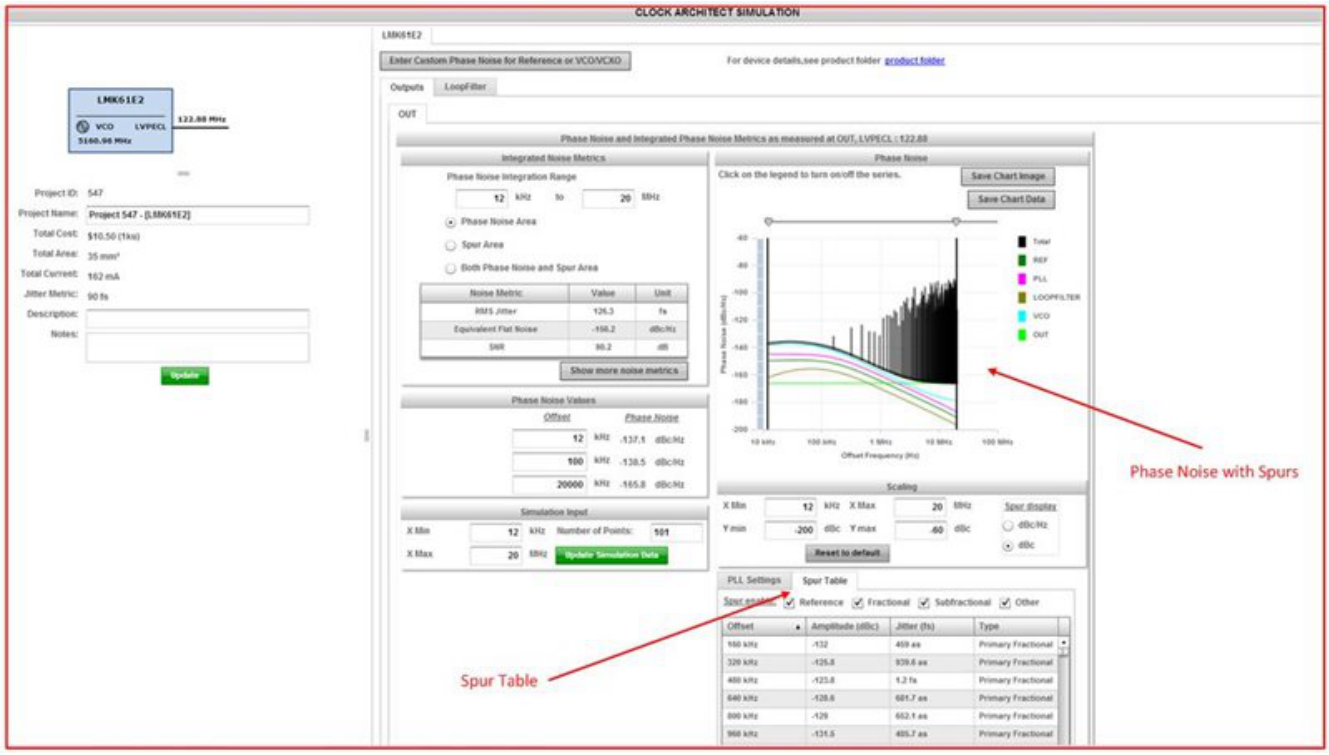

Figure 3. Output Clock Phase-noise Plot with Spurs

We have also made some upgrades to the PLL filter-design capabilities. With the latest release, advanced users can customize loop-filter parameters such as PLL bandwidth, phase margin and gamma, shown in the screenshot of Figure 4. You can enter custom loop-filter component values or select from a list of integrated values (when available for the device), and then check loop stability by monitoring the Bode plot (See Figure 5). With the inclusion of PLL lock-time modeling capability, you can verify the impact of your loop-filter design strategies to the PLL lock time (and phase noise) and consider necessary trade-offs (Figure 6).

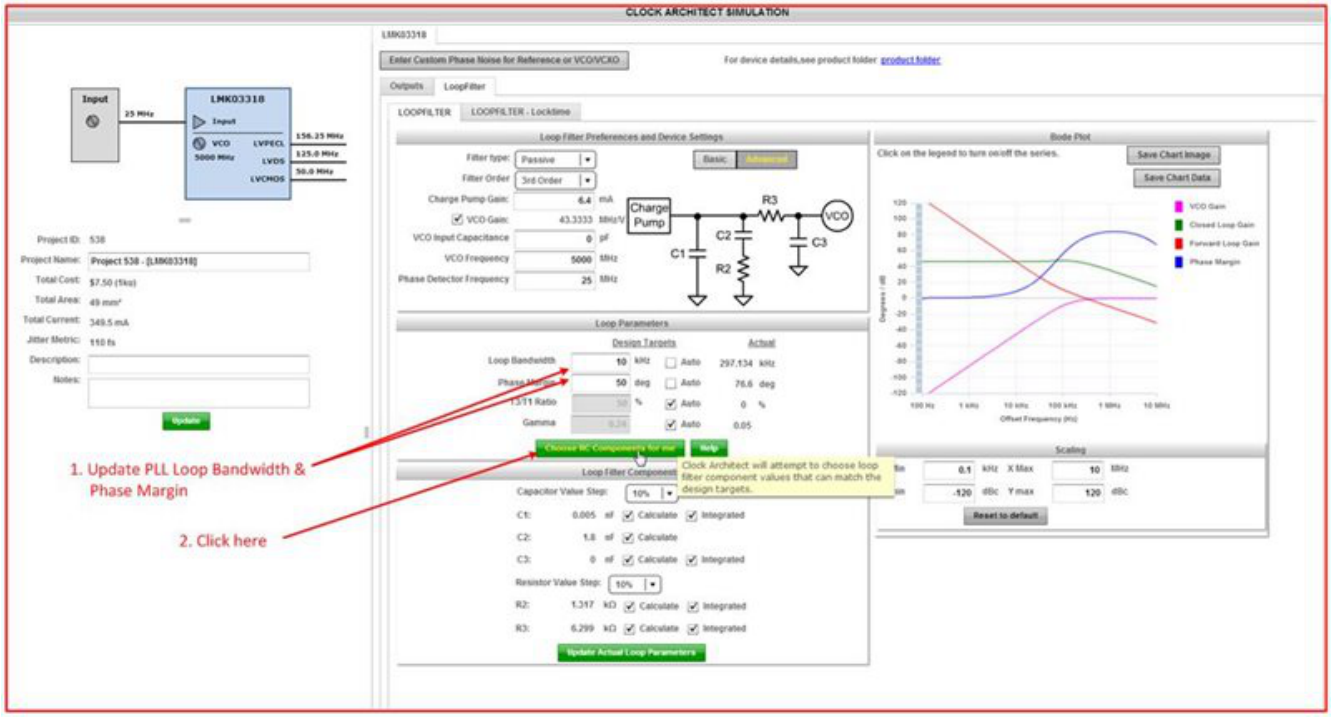

Figure 4. Custom Loop Parameter Selection

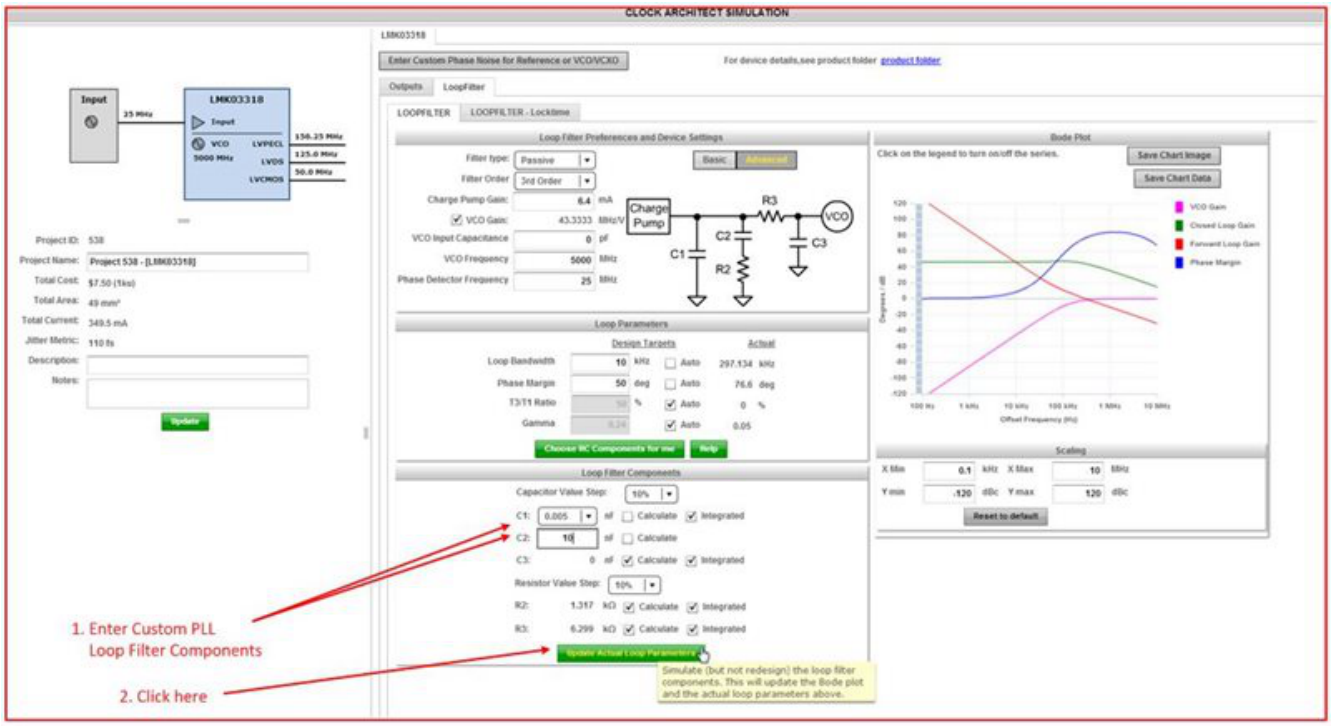

Figure 5. Custom Loop Filter Component Selection and Simulation

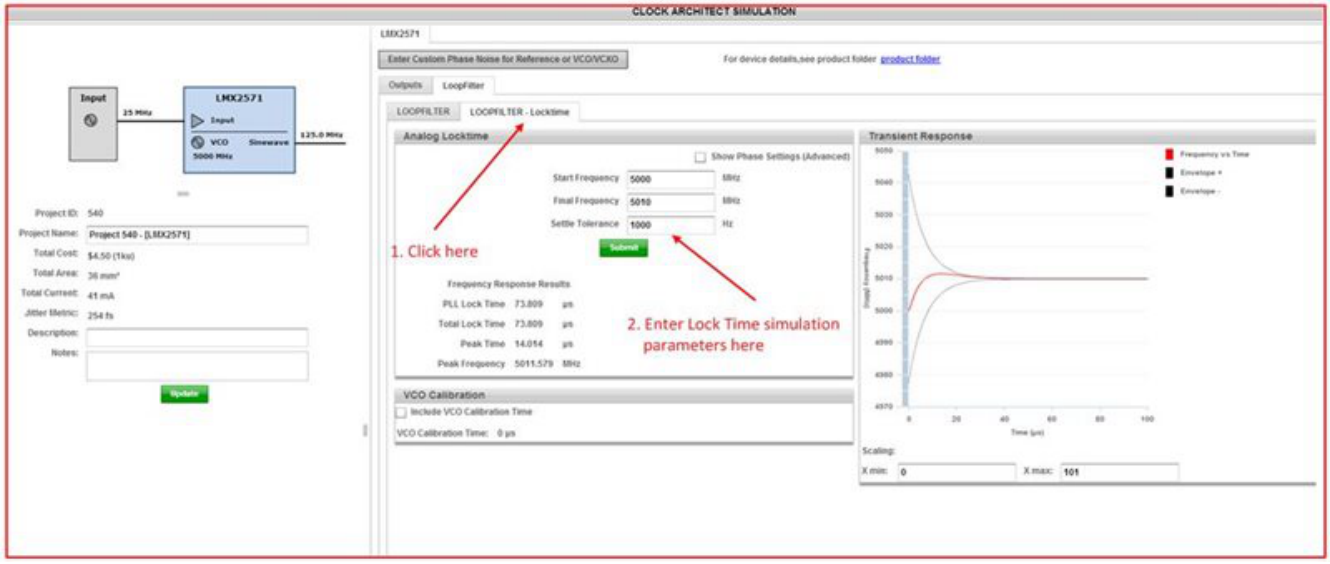

Figure 6. Lock Time Simulation and Estimation

Until recently, WEBENCH Clock Architect supported passive loop-filter design only. Now, with the latest upgrades, the tool supports active loop-filter designs (under Advanced settings). Passive-loop filters are typically preferable to active-loop filters given their low cost, simplicity and in-band phase noise. But in certain cases – where the VCO requires a higher tuning voltage than the PLL charge pump can provide, or when the input impedance of the VCXO is inadequate – active filters are necessary. See the drop-down menu in Figure 7.

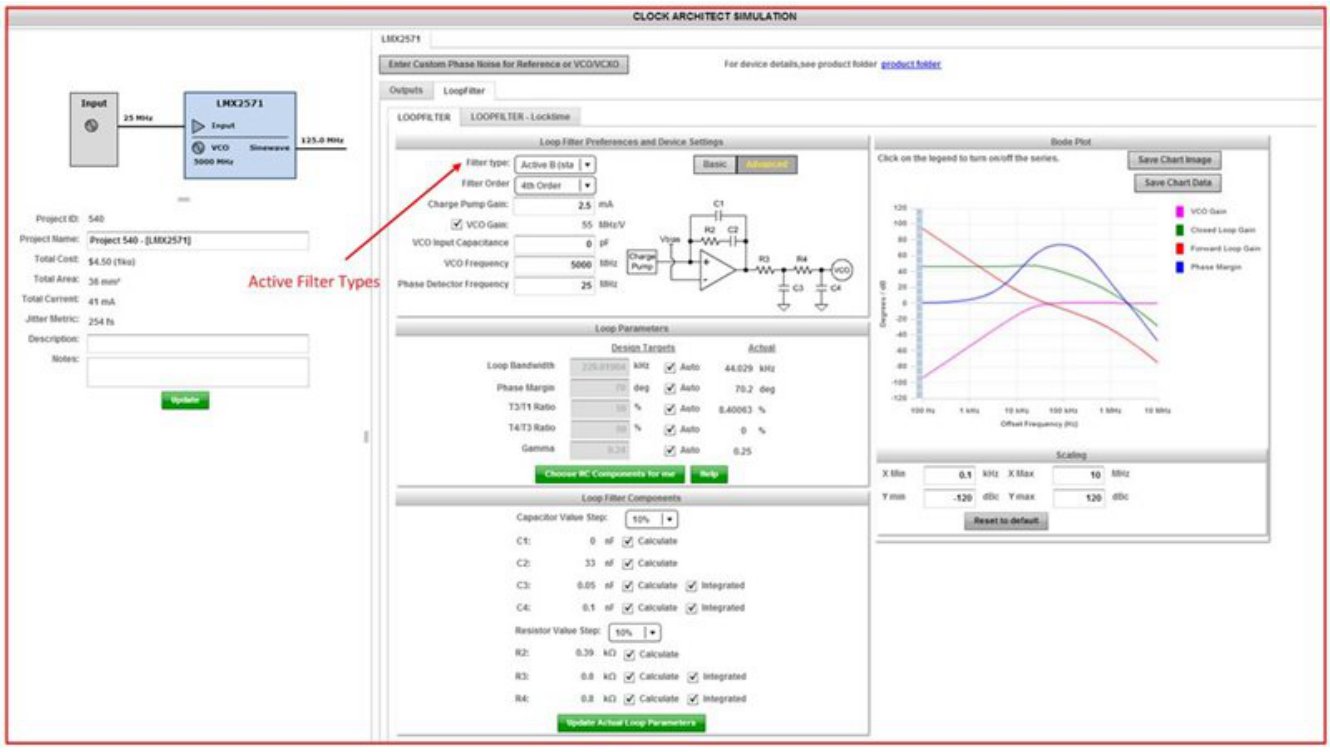

Figure 7. Active Loop Filter Selection and Simulation

The last major upgrade to WEBENCH Clock Architect is the ability to share designs with other users. You can generate a PDF report containing all of your design details with a single click of the Share Project button shown in Figure 8.

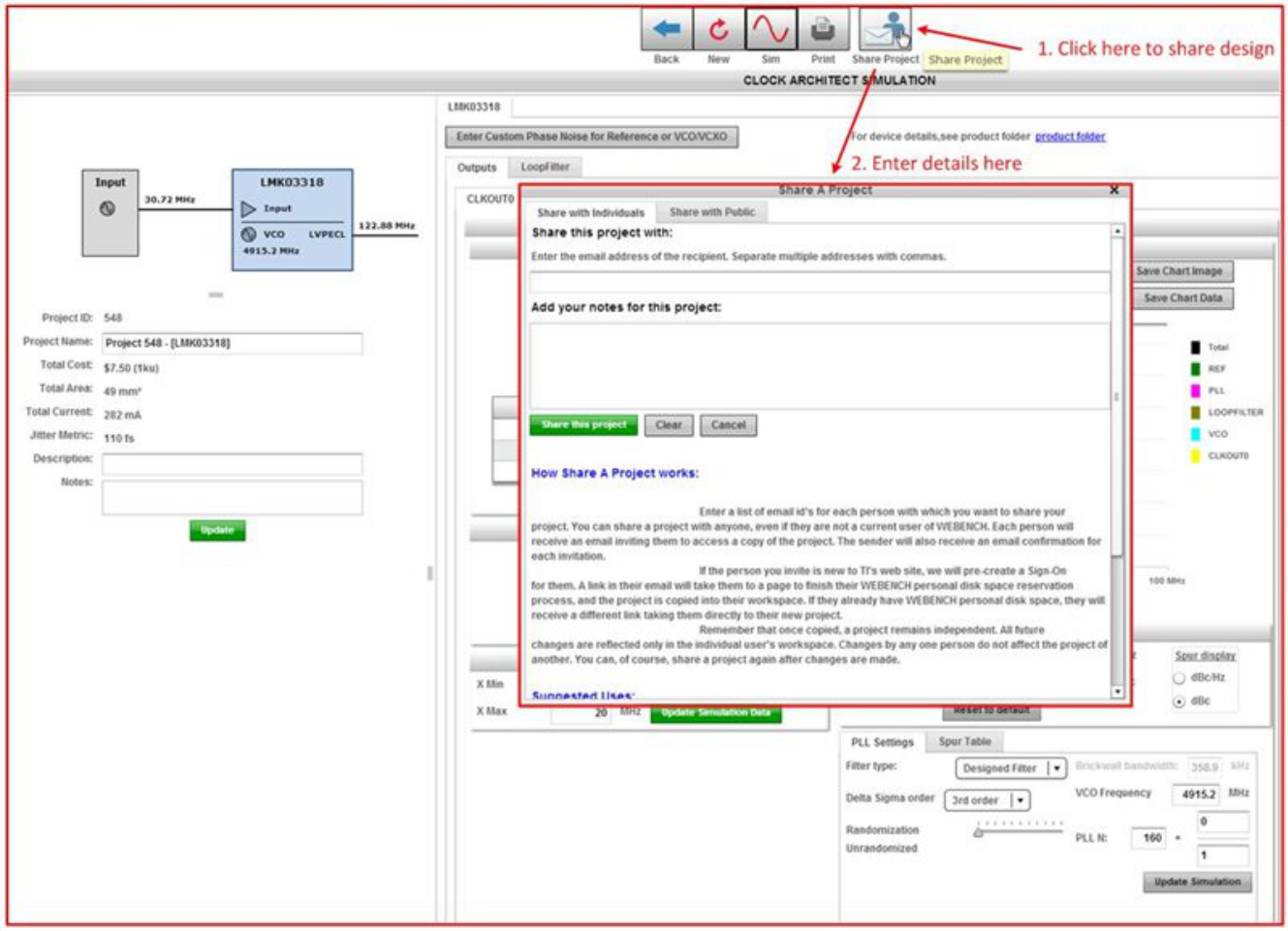

Figure 8. Share Designs

TI has a healthy portfolio of flexible and high-performance clock generators, clock jitter cleaners, radio frequency (RF) PLLs/synthesizers, clock buffers and oscillators to meet the stringent needs of your applications.

My favorite clock generator and programmable oscillator are the LMK03328 and LMK61E2, respectively. These devices have ultra-low RMS jitter performance (100fs typical), flexibility (integrated EEPROM and ROM) and are feature-rich (support frequency-margining). You can use WEBENCH Clock Architect to simulate the phase noise for your next design using these devices and many more at TI.com.

Additional Resources

- View WEBENCH Clock Architect training videos:
- WEBENCH Clock Architect Updates
- WEBENCH Clock Architect Introduction
- WEBENCH Clock Architect Simulation & Optimization
- Find out more about TI's clock and timing portfolio.
- Read other blog posts about clocks and timing.
- Additional PLL simulator software http://www.ti.com/tool/pllatnumsim-sw

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