Technical Article

Optimizing Layout for Synchronous Buck Converters

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Buck DC/DC converters (see Figure 1) are a very popular switching DC/DC regulator topology in many electrical and electronic applications, from cloud infrastructure to personal electronics to factory and building automation. They represent >75% of all nonisolated switching regulator topologies today.

The layout of a buck converter is just as important as the simulation and design, but the lack of good layout practices can hamper development time or cause operational and reliability issues down the line.

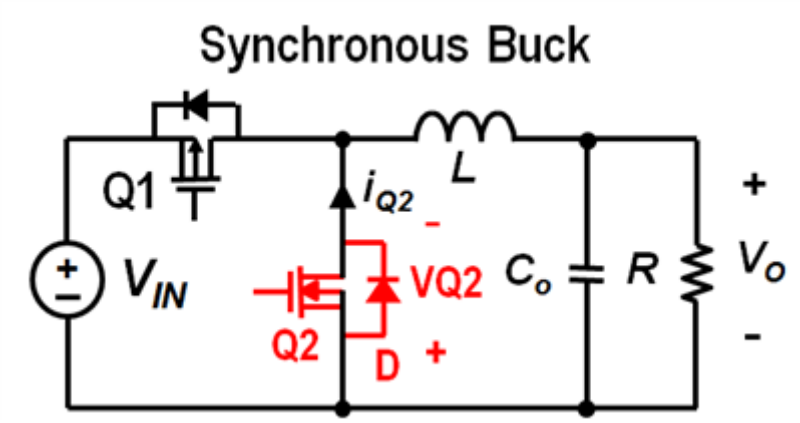

Figure 1. Synchronous Buck DC/DC Converter

Layout considerations include the placement of bypass capacitors, feedback compensation network components, power components, parasitic components, and ground loops and connections.

Bypass Capacitors

When it comes to bypass capacitors, it's important to minimize the lead inductance by minimizing the bypass loop area, shortening lenghts on high di/dt (current slew rate) paths, using ground planes where possible, bringing current paths across capacitor terminals and avoiding multiple layouts. Also, paralleling different capacitor types for reduced impedance across a capacitor band is important, as it can reduce impedance in the 2MHz-to-20MHz frequency range (with typical capacitor values of 0.1µF to 0.01µF). Drawing the capacitors closer to the integrated circuit (IC) pin also shows layout designers the critical nodes and areas, as illustrated in Figure 2.

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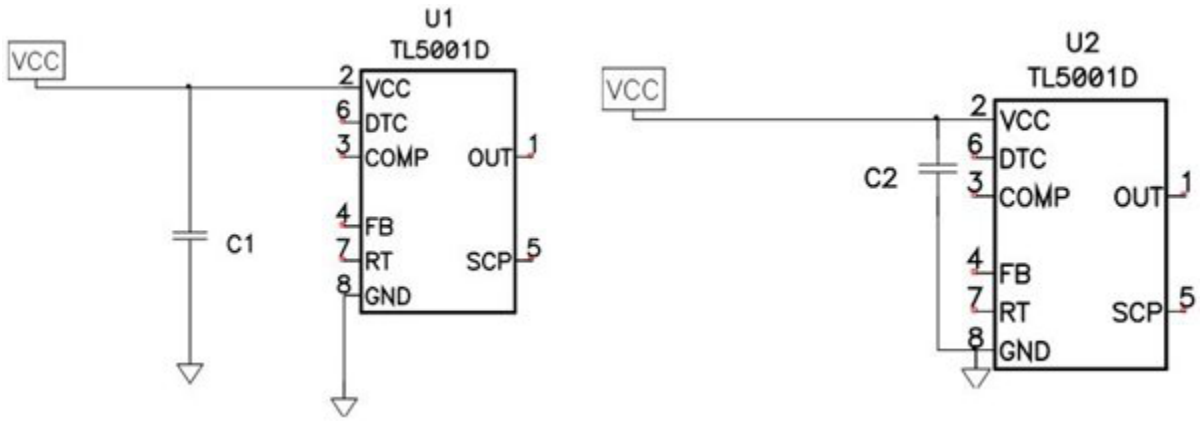

Figure 2. Bypass Capacitor Circuit Connections Indicating Critical Loop Areas

Feedback Compensation Network

Place the compensation network close to the IC error amplifier. Place resistors so that they're directly connected to the inverting input of the error amplifier (FB pin), as shown in Figure 3.

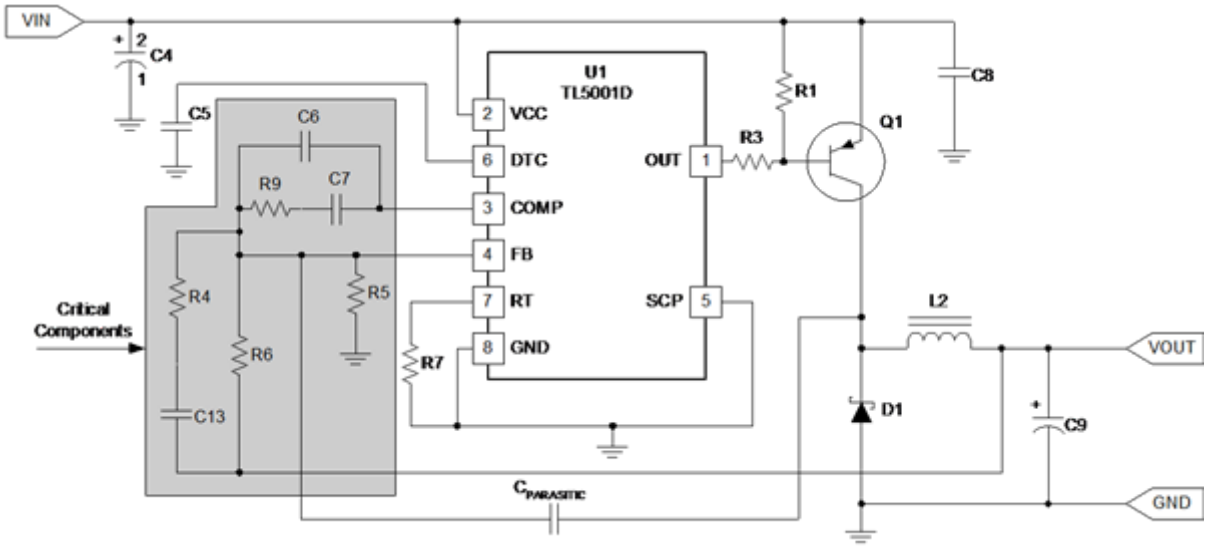

Figure 3. Feedback compensation network placement

Power Components

Make sure that you connect power components properly, as there is high di/dt (current slew rate) in current paths, as shown in Figure 4. Any inductance in the path will result in switch-node ringing, which can exceed the power FET's absolute maximum rating and also cause harmonics and unwanted noise in the system. The goal is to minimize the loop area by perhaps using two-sided printed circuit board (PCB) mounting, with MOSFETs on one side of the PCB and capacitors on the other. Make sure to place and route components accordingly. A proper design will not require a snubber circuit to reduce the switch-node ringing.

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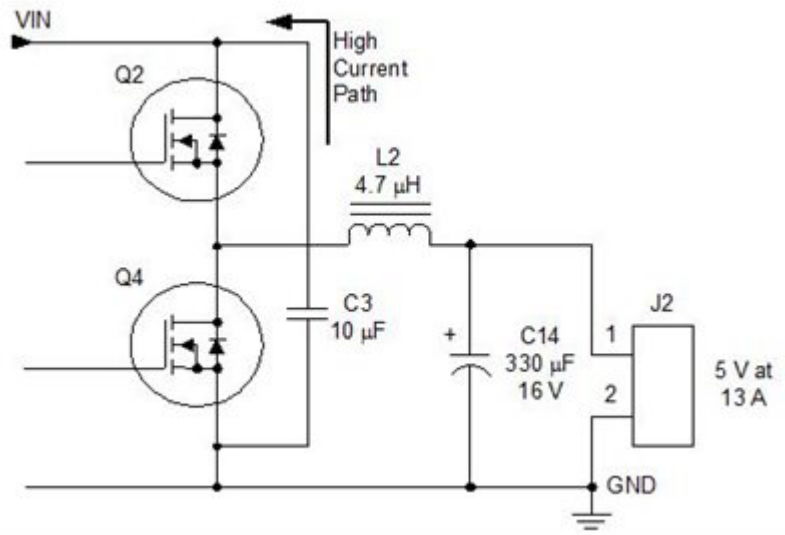

Figure 4. Power Component Connections Indicating a High-current Path

Parasitic Components

Watch out for parasitic components, as they can introduce and increase impedance in the power supply, which can then cause stability and operational issues. Look out for wiring inductance, especially low-impedance circuits and filters, power switching and timing circuits. Use ground planes and wide traces to minimize inductance.
In terms of board capacitance, pay attention to high impedance or noise-sensitive circuits, and watch out for coupling between board planes/layers and to component pads. Magnetic coupling can also occur, for example, from inductor to inductor, especially toroid inductors; in this case, consider alternate mounting directions. Magnetic coupling could also occur between loops, so minimize loop areas and use ground planes.

Ground Loops and Connections

Single-point grounds present a problem whether in series or in parallel, as shown in Figure 5.

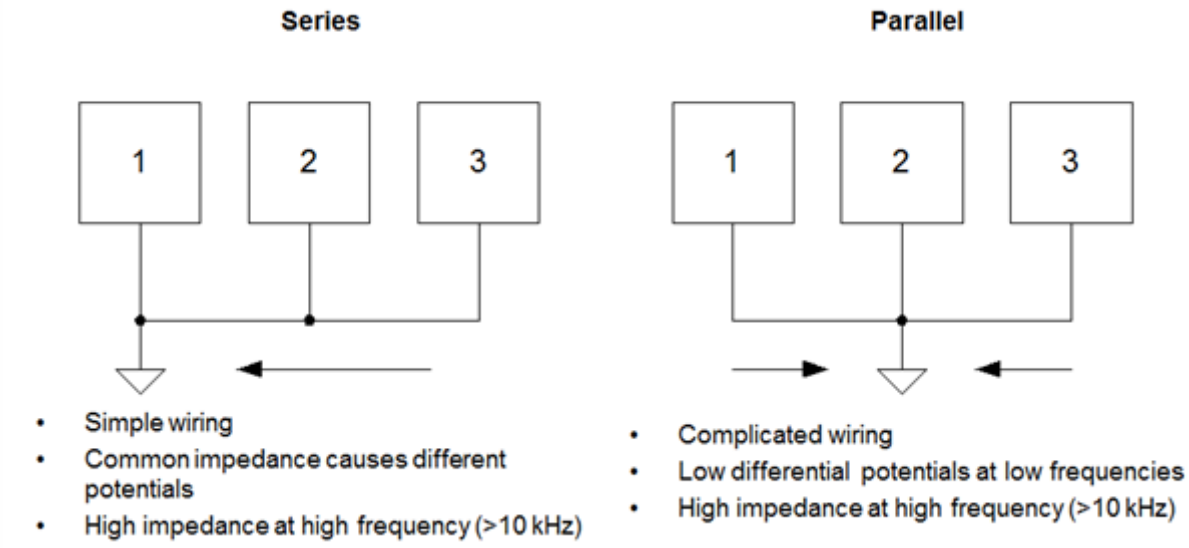

Figure 5. Series and Parallel Single-point Ground Connections

A better approach is to use multipoint grounding. As shown in Figure 6, multipoint grounding enables low impedance between circuits to minimize potential differences, and it also reduces circuit trace inductance. The objective is to contain high-frequency currents in individual circuits and keep them out of the ground plane.

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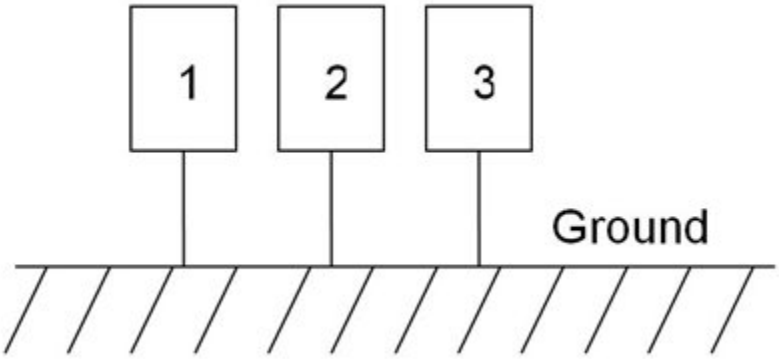

Figure 6. Multipoint Ground Connections

Many buck converter control ICs recognize the noise and quiet circuit areas, and the IC pinout is such that the layout and component placement around the IC pins is easier. Some even provide a separate pin for power and analog ground, as shown in the TPS40170 60V synchronous buck pulse-width modulation (PWM) controller pinout shown in Figure 7.

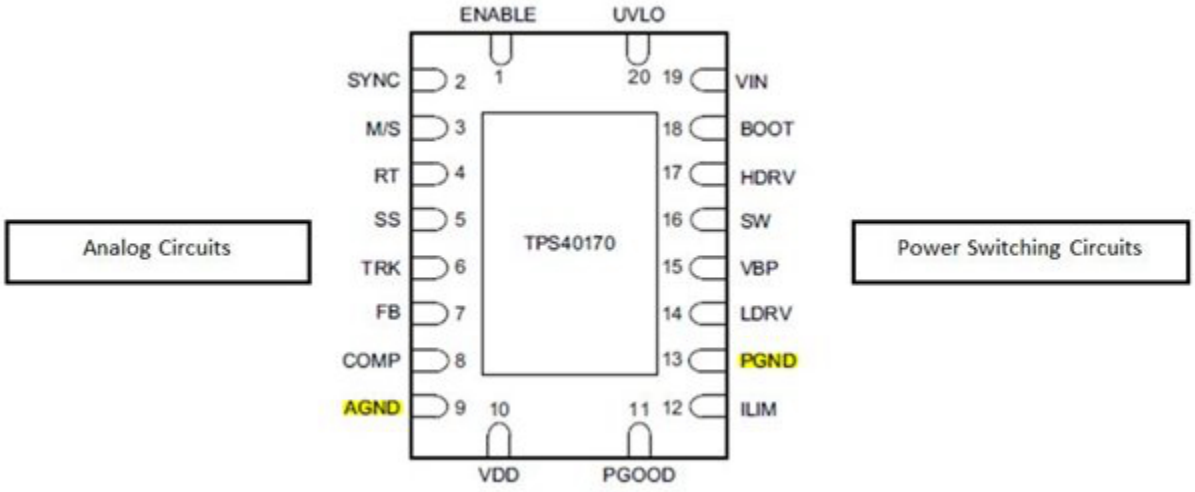

Figure 7. Buck Controller IC Pinout for Analog and Power Connections

So planning for the layout around the IC pinout and using the good layout practices mentioned in this post can help you get your buck converter design working right from the start, and avoid any headaches later. Check out TI's buck converter and buck controller selection tables for a variety of buck DC/DC solutions.

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