

Clock Tree Fundamentals: Finding the Right Clocking Devices for Your Design



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Finding the right devices to build your clock tree doesn't have to be difficult. Understandably, the plethora of options can be overwhelming. Also, selecting a less-than-ideal device may result in compromises, potentially increasing system cost or affecting performance. To help simplify device selection, this article explores key considerations when assessing both your system's clocking needs and available devices.

To visualize the clocking considerations in this article, we will refer to the [ultrasound scanner](#) clock tree in [Figure 1](#).

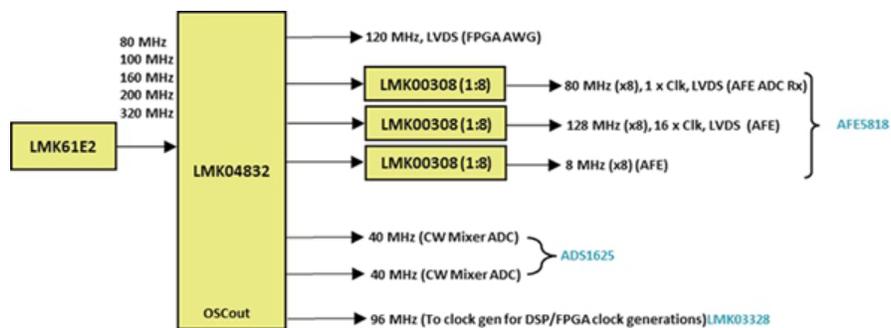


Figure 1. Clock Tree Diagram Example for an Ultrasound Scanner

Key System Clocking Considerations Include:

- Input type or format.** Typically, your clock tree will originate from a self-driving clock source – either an [oscillator](#), or perhaps a voltage-controlled crystal oscillator (VCXO) or XTAL (crystal). Determine what your input frequency is and its input format. The input is a starting point for defining the rest of the clock tree. It must be compatible with your first stage of devices. For example, if your input is a crystal, you must select a device with internal circuitry to accept a crystal input. Otherwise, there will be no outputs generated by that device and, if your clock tree has multiple stages, no inputs going to the rest of the devices. The [ultrasound scanner](#) clock tree example in [Figure 1](#) uses a [LMK61E2](#) ultra-low jitter oscillator. The LMK61E2 can generate a wide range of frequencies, including 80 MHz, 100 MHz, 160 MHz, 200 MHz and 320 MHz, which can meet most input frequency requirements.
- Frequencies.** If your system needs multiple copies of the same frequency, you'll likely only need a single [clock buffer](#). If it's more complex, with various frequencies supporting different receivers, you'll need a [clock generator](#) to generate different frequencies scaled from the same input source. The 16-channel [AFE5818](#) analog front-end shown in [Figure 1](#) requires 80 MHz, 128 MHz and 8 MHz frequencies. Similarly, the [ADS1625](#) analog-to-digital converter (ADC) and [LMK03328](#) clock generator require 40-MHz and 96-MHz inputs respectively. The [LMK04832](#) clock generator supports these devices by generating all the required frequencies.
- Number of outputs.** When designing your clock tree, it's important to note the total number of required outputs and how many need to be the same frequency. Extra buffers can help fan-out multiple copies of the same frequency, if necessary. Along with the input frequency and format, the number of outputs is also listed in the ultrasound clock tree example in [Figure 1](#). To provide eight 80-MHz clocks to the [AFE5818](#), the [LMK00308](#) 1-to-8 channel clock buffer is used to fan-out the 80 MHz output generated by the LMK04832.
- Output formats.** The output of your selected clocking device must be compatible with the input requirements of the devices receiving these clocks as inputs. Typical input requirements are associated with the voltage

limits needed for registering the high and low levels of the clock cycle, and how fast the rising and falling edges are. Additionally, some devices require a single-ended input such as a sine wave or low-voltage complementary metal-oxide semiconductor (LVCMOS) clock, while other devices require differential inputs such as low-voltage differential signaling (LVDS) or low-voltage positive-emitter coupled logic (LVPECL). In [Figure 1](#), the 80-MHz and 128-MHz clocks provided to the AFE5818 are in the LVDS format.

- **Noise performance.** The clocking devices in your clock tree will have different jitter and phase noise performances. Devices with low-input jitter requirements may not tolerate a noisy reference clock. A [jitter cleaner](#) can help clean up the jitter on the input before generating a low-noise reference for the receiver.
- **Power consumption.** Don't forget to budget power for the devices in your clock tree and ensure that all of the clocking devices you've chosen meet system temperature requirements. Overlooking the power consumption of the clocking devices could overload power-management integrated circuits (ICs) or cause you to go over your system's total power consumption budget.
- **Solution size.** Clocking devices may require supporting components such as power-supply filtering passives, crystal or an external voltage-controlled oscillator (VCXO). The total solution size for a clocking device is the sum of the areas required by the device and its supporting components. Additionally, there will be traces on your printed circuit board (PCB) to distribute these clocks. Always consider the size and space available on your PCB, as it'll determine whether an integrated solution or multichip solution is better for your design. Increased size and power consumption often correlate to better noise performance, a larger number of generated output clocks or both.

This isn't meant to be a comprehensive list. Rather, it's a starting point. Additional system requirements may include [high-frequency radio-frequency clocks](#), clocks with a phase-deterministic relationship, status outputs, hitless switching, output enable pins on devices or a specific clock-to-clock skew. I recommend recording these requirements in your notes while you're outlining your clock tree.

Designing a clock tree using the requirements outlined in this article can help simplify your design process. Proper organization is important, especially when designing for larger systems requiring many clocks. For any additional clocking IC or clock tree questions, you can connect directly with our engineers in the [Clock & Timing forum on TI E2E](#)™.

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