TMS320LF2401A, TMS320LC2401A

DSP Controller

Silicon Errata

SPRZ013G
December 2001
Revised June 2005

Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320LF2401A DSP Controller (silicon revisions 0, A, B, and C) and TMS320LC2401A DSP Controller. The updates are applicable to one or both of the following:

- TMS320LF2401A (32-pin LQFP, VF suffix)
- TMS320LC2401A (32-pin LQFP, VF suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature range and voltage range should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

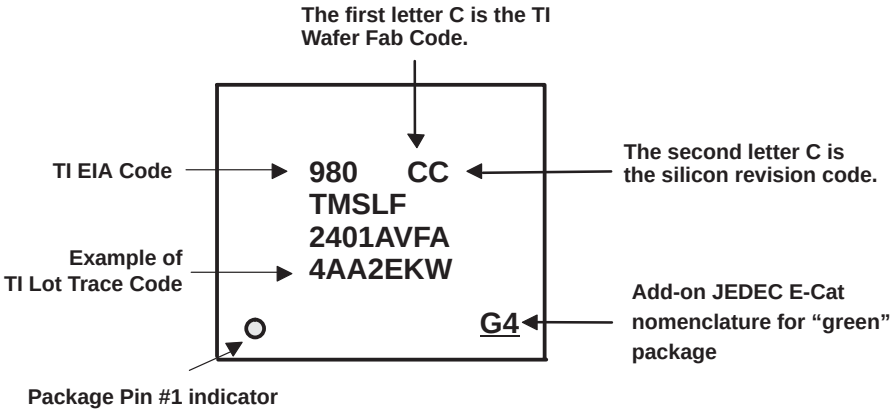
TMS Definition

Fully-qualified production device.

1.2 Revision Identification for TMS320LF2401A

The silicon revision can be determined by the second letter to the right of the TI EIA (Electronics Industries Association) code (980) as shown on the top of the package in Figure 1.

Figure 1. Example, Silicon Revision Code for TMS320LF2401A (VF)



Second Letter After TI EIA Code	Silicon Revision	Comments
Blank (no second letter)	Indicates Revision 0	This silicon revision is available as TMX only.
A	Indicates Revision A	This silicon revision is available as TMX only.
B	Indicates Revision B	This silicon revision is available as TMX only.
C	Indicates Revision C	This silicon revision is available as TMS.

2 Known Design Marginality/Exceptions to Functional Specifications

Advisory	*Maximum CLKIN frequency while using boot-ROM SCI loader*

Revision(s) Affected: TMS320LF2401A − Revisions 0, A, B, and C
TMS320LC2401A

Details: The SCI boot loader briefly sets the PLL to x4 prior to checking whether the PLL must be set to x2. If a CLKIN frequency greater than 10 MHz is used, this could result in operating the device at frequencies greater than 40 MHz.

Workaround: CLKIN frequency should not exceed 10 MHz if the boot-ROM SCI loader is used.

Advisory	*Internal Oscillator*

Revision(s) Affected: TMS320LF2401A − Revisions 0, A, B, and C

Details: The internal oscillator of the 2401A device has a design marginality that may prevent the internal oscillator from starting upon power-up under certain conditions pertaining to board layout, ground bounce, and power-supply ramp rate. This is a concern only when the internal oscillator is used in conjunction with an external quartz crystal/ceramic resonator and not with an external oscillator.

Workaround: Use of a 1M-Ω resistor in parallel with the crystal across the XTAL1 and XTAL2 pins removes this condition.

Advisory	*ADC Sequencer Operation*

Revision(s) Affected: TMS320LF2401A − Revisions 0, A, B, and C
TMS320LC2401A

Details: The ADC sequencer operation has an issue when CPS = 1 *and* ACQ_Prescaler = 0. When an ADC sequence is started, the sequence stops after performing the first conversion. For example, if there are five conversions programmed for a sequence, the sequencer may stop after performing the first conversion. When CPS = 0, all the conversions are performed. The issue surfaces only when CPS = 1 **and** ACQ_Prescaler = 0. CPS can be 1 for any other ACQ_Prescaler value.

Workaround: ACQ_Prescaler = 0 should not be used in conjunction with CPS = 1.

Advisory	*XF/TMS Pin Function*

Revision(s) Affected: TMS320LF2401A − Revisions 0, A, B, and C

Details: The XF output function is multiplexed with the JTAG TMS input function onto the same pin. When the $\overline{\text{TRST}}$ pin is high, the XF/TMS pin is configured as a TMS input and when the $\overline{\text{TRST}}$ pin is low, it is configured as an XF output pin. The problem arises in that at certain times, it is legal for a scan controller to drive the TMS pin while pulling $\overline{\text{TRST}}$ low to reset the JTAG logic. If the state of the XF output function is opposite the state that the scan controller drives onto TMS, a drive conflict will arise between the device and the scan controller. Over time, this can potentially degrade the reliability of the output buffer on the XF/TMS pin, as well as potentially damaging the scan controller.

Workaround: This has been fixed in the C revision of the silicon. An XF-enable bit was added to the design as bit 0 of address 0x701B. This register is labeled SCSR4. The bit will come up out of reset as a zero, with XF output disabled. If you write a one to this bit, the XF output will be enabled (assuming $\overline{\text{TRST}}$ is low). This bit is not readable.

3 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Click on **DSP Product Tree**
3. Click on the **C2000** tab
4. Click on **TMS320C24x DSP Generation**
5. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320LF2401A, please refer to the following publications:

- *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357)
- Manual Update Sheet for *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (SPRU357B) [literature number SPRZ015]
- *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set* (literature number SPRU160)
- *3.3V DSP for Digital Motor Control* application report (literature number SPRA550)
- *TMS320LF2401A, TMS320LC2401A DSP Controllers* data sheet (literature number SPRS161)

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