Very large FFT for TMS320C6678 processors

Xiaohui Li
Applications Engineer
Processors

Ellen Blinka
Marketing engineer
Processors

Texas Instruments

Introduction

This white paper discusses the very large FFT (VLFFT) demo, which implements one-dimensional complex single-precision floating-point FFTs of size 16K to 1024K samples on 1, 2, 4 and 8 DSP cores of TI's TMS320C6678 8-core fixed- and floating-point DSP in order to demonstrate the capabilities of the C66x DSP core as well as the capability of the architecture to accommodate parallelization across multiple cores with performance boosts proportional to the number of cores added. The FFT was chosen as the algorithm for this demo as FFTs are common signal processing building blocks used in applications such as medical imaging, communications, and military and commercial radars, and electronic warfare (jammers, anti-jammers). The 1024K sample FFT is shown to take only 6.4 ms when the algorithm is run on all eight DSP cores of the TMS320C6678 device at 1 GHz.

TMS320C6678 SoC

The TMS320C6678 device is an eight-core DSP based on TI's C66x fixed- and floating-point DSP core and built on TI's innovative KeyStone™ architecture which enables full multicore entitlement. It is capable of operating at up to 1.25 GHz, at which speed it can produce 160 GFLOPS and consumes less than 10 W in typical use cases. It also features 512 KB of L2 memory per DSP core and 4 MB of shared memory for a total of 8 MB of on-chip memory, all with ECC. The DDR3 interface is capable of running up to 1600 MTPS, can access up to 8 GB of external memory and is a 64-bit + 8-bit ECC interface. Peripherals include PCIe, Serial RapidIO® and Gigabit Ethernet, as well as TI's HyperLink interface which provides up to 50-Gbps connection to other TI DSP, ARM®, and ARM+DSP processors, as well as to FPGAs though third-party IP blocks.

In the VLFFT demo, the TMS320C6678 device operates at 1 GHz, using DDR3 transfers at 1333 MHz.

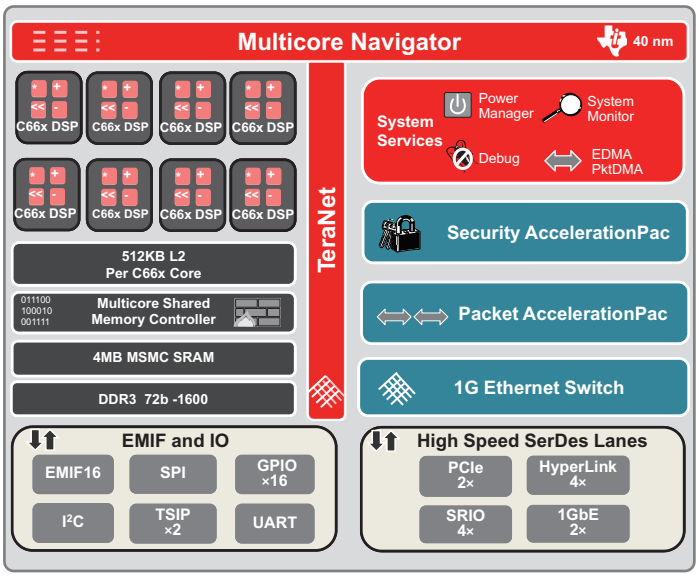

Figure 1: TMS320C6678 block diagram

VLFFT demo

The VLFFT algorithm requires input data to be placed in the device's external memory. During the demo, data is accessed, distributed to and processed by the DSP cores, and then the output is placed into external memory. The cycle counts and times measured incorporate this entire process. The software can be configured to use different numbers

of cores (1, 2, 4, or 8) to do the computation on FFTs of the following sizes:

- **16K**
- **32K**
- **64K**
- **128K**
- **256K**
- **512K**
- **1024K**

The FFT implementation is designed to achieve maximum performance by distributing the computational load across multiple cores, and by fully utilizing the high-performance computational power of the C66x DSP cores. The basic decimation-in-time approach is used to formulate a one-dimensional very large FFT computation into a form similar to a two-dimensional FFT computation. For very large N, it can be factored into N = N1*N2. If it is very large, a one-dimensional input array can be represented as a two-dimensional array of N1 rows and N2 columns and then the following steps can be taken to compute a one-dimensional very large FFT from this representation:

1. Compute N2 FFTs of N1 size in the column directions
2. Multiply by twiddle factor
3. Store N2 FFTs of N1 size in row directions to form a N2 by N1 two-dimensional array
4. Compute N1 FFTs of N2 size in the column direction
5. Store data in column direction to form a N2 by N1 two-dimensional array

This algorithm is described fully by Takahashi in "High-performance parallel FFT algorithms for the Hitachi SR8000."[1]

In multicore implementation, step one is accomplished by computing N2/(number of cores) FFTs of size N1 on each core, and step 4 by computing N1/(number of cores) FFTs of size N2 on each core. Core 0 is used as a master core and is responsible for synchronizing all the cores, and the rest of the cores are used as slave cores. On each core, depending on the sizes of N1 and N2, the total number of FFTs on each core is divided into several smaller blocks in order to accommodate the size of the L2 SRAM per core. Each block of data is prefetched by DMA from external memory into L2 SRAM and the FFT results are written back to external memory by DDR. Two DMA channels are used by each core to transfer input and output samples between external memory (DDR3) and internal memory (L2 SRAM).

Results

The results from running the FFT code on a TMS320C6678 evaluation board (TMDSEVM6678LE) are listed in Table 1 on the following page in both DSP cycles and in milliseconds. Ideally when the number of cores used for the calculation is doubled, the cycle count should be cut in half, but this is rarely achieved in real-world situations due to overhead from data movement, memory block sizing, and non-infinite bandwidths of data input mechanisms (here, external memory). In this example, when two cores are used instead of one the time to run the FFT is reduced on average by 49.3 percent (1.97×), nearly reaching the ideal halving of cycle count. When four cores are used instead of one the time to run the FFT is reduced on average by 72.5 percent (3.67×), and when eight cores are used the time is reduced on average by 81.6 percent (5.7×).

FFT size	Performance of Computing Very Large FFT (DSP cycles) TMS320C6678-1 GHz, DDR-1330 MHz			
	1 core	2 cores	4 cores	8 cores
16K	473175	261457	159063	131405
32K	914699	478129	278405	197939
64K	1856711	922285	507845	314560
128K	4099502	2004217	1059706	640926
256K	8794604	4323499	2227541	1185959
512K	18669157	9291431	4703590	3102933
1024K	38556557	19328150	9605249	6403155

FFT size	Performance of Computing Very Large FFT (time, ms) TMS320C6678-1 GHz, DDR-1330 MHz			
	1 core	2 cores	4 cores	8 cores
16K	0.473	0.261	0.159	0.131
32K	0.915	0.478	0.278	0.198
64K	1.857	0.922	0.508	0.315
128K	4.100	2.004	1.060	0.641
256K	8.795	4.323	2.228	1.186
512K	18.669	9.291	4.704	3.103
1024K	38.557	19.328	9.605	6.403

Table 1: Results of FFT on one, two, four and eight DSP cores in cycles and milliseconds

It can be seen that the time reduction improves as FFT size increases from 16K to 256K for both the two- and the four-core use cases, and even more dramatically in the eight-core use case. This is because for these smaller FFTs, as more cores are added, the penalty from parallelizing the code is small relative to the improvement from adding the extra cores. Past 256K size FFTs, the improvement is either flat, having reached the 2× or 4× improvement for the two- and four-core use cases, or decreases in the case of eight cores being used. This decrease in improvement is due to a memory boundary being reached as the 8 cores are consuming data faster than they can be supplied with data from external memory. The time to calculate a 1024K FFT, a million point FFT, is shown to be 6.4 ms when using all eight DSP cores at 1 GHz.

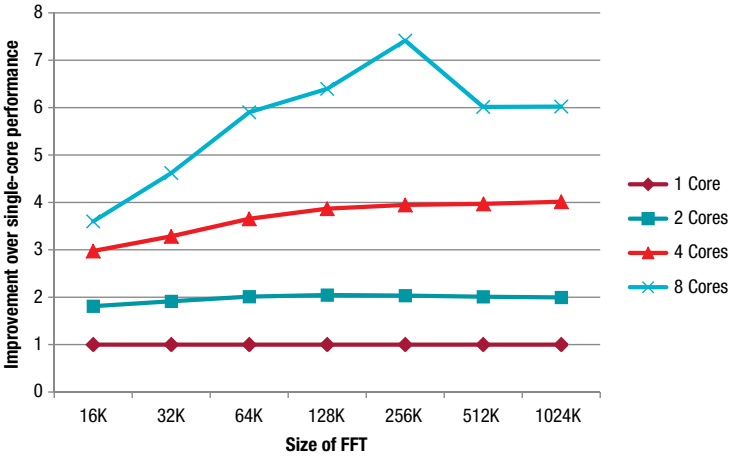

Figure 2: Performance improvement of multiple cores over single core

Conclusions

It is shown that a million point FFT can be executed by the TMS320C6678 device in as little as 6.4 ms when all eight cores are operating on the data in parallel, at 1 GHz. With these speeds, the DSP can be used for real-time operations in applications such as radar, electronic warfare, medical imaging, and more. Execution time could be improved even further by running the TMS320C6678 device at the maximum speed possible, 1.25 GHz, and using higher bandwidth DDR3, 1600 MTPS.

References

[1] D. Takahashi, “High-performance Parallel FFT algorithms for the Hitachi SR8000,” in *Proceedings of the Fourth International Conference/Exhibition on High-Perfomance Computing in the Asia-Pacific Region,* 2000.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265