User's Guide

Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family

ABSTRACT

The *Hardware Design Considerations for Custom Board Design* user's guide provides an overview of the design considerations that are recommended to be followed by the custom board designers while designing custom boards using AM62L (AM62L32, AM62L31) processor family. The user's guide can be used as guidelines at different phases of custom board design (by custom board designers).

Additionally, links (TI.com product page) are provided to processor product pages, processor related collaterals, FAQs related to processor and processor peripherals published on E2E, and commonly referenced documents during custom board design. The custom board designers can refer to the links during custom board design to minimize design errors, optimize the design efforts, reduce board build iterations and optimize the project timeline.

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1 Introduction

The *Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Processor Family* can be used as a starting point by custom board designers designing custom board using any of the above listed processors. The user's guide provides an overview of the design flow at different phases of custom board design and highlights important design requirements that are recommended to be addressed. Note that the user's guide does not include all the information required to complete the custom board design. In many cases, the document refers to the device-specific collaterals and various other documents for specific information.

The user's guide has been organized as a sequence of sections. The user's guide starts with decisions that are required to be made during the planning phase of the custom board design, selection of processor and attached devices, electrical and thermal requirements. Recommendations discussed in each of the section are recommended to be addressed before moving to the next section.

Note

The user's guide does not cover all aspects or phases of custom board design.

Note

The processor family has capabilities to address safety requirements.

The focus of the user's guide is non-safety applications.

See the following FAQ:

[FAQ] AM62L: Commonly Asked Questions

1.1 Before Getting Started With the Custom Board Design

The processor family includes a number of peripherals supporting multiple functions (memory, communication) and processing capabilities (all the peripherals and processing capabilities may not used in all the custom board designs). The functional and performance requirements for different custom board designs using the same processor can vary depending on the end application. Custom board designers are expected to understand the requirements before selecting the processor and determining the board level implementation requirements. Additional circuitry can be added to the custom board design to enhance functionality and operate correctly in the end application operating environment. For selecting the processor OPN and to finalize the below key requirements, see the device-specific data sheet, silicon errata, TRM, hardware design considerations for custom board design, schematic design guidelines and schematic review checklist, and EVM collaterals (latest, recommendation is to frequently check for updates to collaterals on TI.com):

- Expected operating conditions for the processor, target boot mode, storage type and interfaces
- Processing (Performance) requirements for each of the core in the selected processor
- External DDR memory type (DDR4 or LPDDR4), width, speed, size
- Processor peripherals used (interfaced to the attached devices)

During the custom board design, as a starting point for information on key devices (components) used on the EVMs and SKs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key devices (components) list

1.1.1 AM62Lx Processor Family Peripherals and IOs Change Summary (With Respect to AM62x Processor Family)

Below are some of the processor implementations to note during the AM62Lx-based custom board designs or changes to note when migrating from the AM62x design to the AM62Lx design:

1. The core supply voltage is fixed to 0.75V
2. Reset inputs and reset status outputs (numbers) have been optimized

3. Implementation of 1.8V only IOs in addition to dual-voltage 1.8V/3.3V IOs. The IO supply for IO groups rails have been named accordingly. 1.8V only (VDDS0, VDDS1, VDDS_RTC and VDDS_WKUP) and dual-voltage 1.8V/3.3V (VDDSHVx [x = 0-4])
4. Buffer Type 1P8-LVCMOS and RTC-LVCMOS supported (have been implemented) and Electrical Characteristics is added
5. Some of the processor peripherals including CPSW3G0 and OSPI0 support only 1.8V IO levels
6. DDR4 and LPDDR4 addressing range is reduced (supports single rank) and some of the DDRSS signals used for DDR4 interface have not been pinned out
7. OSPI0 interface supports connecting to x2 devices (OSPI0 module can be interface to 2 attached devices)
8. Integrated LDO for generating 1.8V/3.3V SD card interface IO supply to support UHS-I SD card
9. Integrated 1x 12-bit Analog-to-Digital Converter (ADC), Up to 4MSPS, 4x analog inputs (time-multiplexed)
10. Support for multiple boot mode configuration approaches - Reduced pin count - Using only 4 of the bootstrap pins BOOTMODE [15:12], Boot from eFuse configured with the reduced pin count configuration and Full pin count - Using all 16 of the bootstrap pins BOOTMODE [15:0]
11. Display interface is supported includes MIPI DSI (x4 lanes DPHY) or DPI (24-bit RGB LVCMOS) (Any one of the display interface is actively supported and supported display is required to be selected during boot)
12. RTC only and RTC + DDR Self-refresh low-power modes are supported (Partial IO for CAN/GPIO/UART wakeup are not supported)
13. EXT_WAKEUP0 and EXT_WAKEUP1 pins for External Wakeup Inputs
14. I2C interface instances including open-drain output type IO buffer I2C interface have been optimized. Open-drain output type IO buffer I2C interface needs a pullup only when the IO is used
15. Pin connectivity requirements for I2C interface with open-drain output type IO buffer I2C buffers has been updated. A pullup is required only when the IO is used
16. IOSETs have been added for multiple peripherals (see the device-specific data sheet)
17. One VTM temp sensor is provided (Temp Sensor 0: DDR/A53)
18. PMIC_LPM_EN0 has a special output cell that turns on a weak pullup as soon as power is applied. The weak internal pullup turns off at the same time the output is driven high on the rising edge of RTC_PORz input. (An external pull was required on AM62Lx processors because the PMIC_LPM_EN0 IO was turned off while reset was asserted. In this case, the PMIC can never turn on without the external pullup resistor)
19. Non Muxed interface (connection of address bus and data bus separately) using GPMC0 is not supported
20. Ethernet boot is not supported
21. Camera Serial Interface (CSI-2) is not supported
22. VMON_VSYS Voltage monitor pin is not supported
23. VMON_3P3_SOC Voltage monitor for 3.3V processor power supply and VMON_1P8_SOC Voltage monitor for 1.8V processor power supply are not supported
24. Configuring the ADC inputs (ADC0_AIN0-3) as digital inputs is not supported

1.2 Peripheral Circuit Implementation - Compatibility Between Processor Families

During custom board design, when implementing the required functionality (circuit) for peripheral interfaces, memory interface and IO interfaces, the recommendation is to review and follow the processor-specific recommendations including ROC, sequencing, IO level compatibility as per the processor-specific data sheet and other available collaterals on the product page. The interface connection requirements and circuit implementations may not be similar (or compatible) with the circuit implementations when compared to legacy Processors or MCUs (TI AM335x, AM437x or other TI processors or processors supported by other suppliers). Example peripheral interfaces include SD card interface including support for high-speed UHS-I, USB interface and IO interface implementation including reset (warm or cold) inputs or external IO interfaces (for slew rate, IO level compatibility, fail-safe operation).

1.2.1 AM62Lx Processor Family Specific Implementation

Some of the AM62Lx peripheral interface supports only 1.8V IO levels (AM62x does not support 1.8V only IOs).

The DDRSS does not support DDR0_ALERT_n, DDR0_PAR, DDR0_CKE1, DDR0_CS1_n, DDR0_ODT1 signals (pins).

1.2.2 Implementation Reference

AM64x and AM62x can be referenced for some of the implementation including DDRSS (DDR4 interface, VTT termination, DDR4 VTT LDO and LPDDR4).

1.3 Selection of Required Processor OPN (Orderable Part Number)

Selection of the required processor OPN is an important phase during custom board design. To get an overview of the processor family architecture and for selecting the required processor OPN (that can be used in the custom board) based on the required functionality and features, package (ANB) and speed grade, see the *Functional Block Diagram*, *Device Comparison*, *Device Naming Convention*, *Device Speed Grades* and *Packaging Information* sections of the device-specific data sheet.

See the *Device Comparison* chapter, *Device and Documentation Support* section of the device-specific data sheet to choose the required processor OPN.

The recommendation is to update the selected processor OPN in the schematics with the chosen OPN.

For the list of available packages for AM62Lx processor family, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A / AM62D-Q1 / AM62P / AM62L Custom board hardware design - Available Device Packages

1.4 Technical Documentation

A number of documents relevant to the selected processor (family) are available on the processor-specific product page on TI.com. The recommendation for custom board designers is to read the relevant collateral (listed in the below FAQ before starting the custom board design.

The following FAQ summarizes the collaterals that can be referred to when starting the custom board design:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – Collaterals to Get started

1.4.1 Updated EVM Schematic With Design, Review and Cad Notes Added

During custom board design, as part of the custom board design flow process, the custom board designers can reuse the EVM design and make the required edits. Alternatively, custom board designers can reuse the common circuit implementations, including processor, memory and communication interfaces. Since the EVM design is expected to have additional functions, custom board designers tend to optimize the EVM schematic design as per the custom board requirements. While optimizing the EVM schematics, errors can be introduced into the custom board design that can affect functionality, performance or reliability of the custom board. When optimizing, custom board designers can have queries regarding the EVM implementation. On many of the customer board reviewed, common design and optimization errors across multiple custom board designs were observed. Based on the customer queries, customer and internal inputs, and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) have been added near each section of the EVM schematic for custom board designers to review and follow (implement to minimize errors).

Additional files as part of the design downloads have been included to support optimizing the evaluation time for the selected processor during the custom board design evaluation phase. The EVM design includes the processor that support maximum functionalities.

TMDS62LEVM: https://www.ti.com/lit/zip/sprcal6

The downloadable documents are listed in the below FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Design notes and Review notes for Reuse of EVM TMDS62LEVM Schematics

The product overview document is in works. Review the FAQ or TI.com frequently for availability.

For information related to availability of design files in Altium CAD tool format, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Available design files and supported CAD tools format that can be used during custom board Schematic and PCB design

The following FAQ includes the PDF schematic (with D-Notes, R-Notes, CAD notes added) and additional information related to EVM TMDS62LEVM:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Design notes and Review notes for Reuse of EVM TMDS62LEVM Schematics

1.4.2 Collaterals on TI.com, Processor Product Page

The most recently updated collaterals including the data sheet, TRM, silicon errata, hardware design considerations user's guide and schematic design guidelines and schematic review checklist are available on the product page.

Additional collaterals that are in works (being edited or reviewed) are being added (updated) to the product page and the current collaterals are also being updated on a continuous basis. The recommendation is to review the collaterals on TI.com for updated revision or new collateral additions on a regular basis.

1.4.3 Updates to Hardware Design Considerations User's Guide

There can be changes to the *Hardware Design Considerations* user's guide with respect to the current revision published on TI.com (based on customer feedback, learnings, errors or improvements) that are updated during the next document revision.

The below FAQ lists the changes customer board designers are required to be aware and follow during custom board design before the release of the revised user's guide on TI.com:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Custom board hardware design - Updates to Hardware Design Considerations and Schematic Design Guidelines collaterals

1.4.4 Processor and Peripherals Related FAQs to Support Custom Board Designs

Based on interactions with multiple custom board designers, queries from a number of custom board designers and learnings from queries received from custom board designers, a number of FAQs have been created (related to (detailed explanation and example illustrations added) processor functioning, processor connections, processor peripherals and interface, processor evaluation EVM, common errors observed during customer board design reviews, data sheet and pin attributes and commonly asked E2E queries) to support custom board designers during the custom board design. Refer the following list of FAQs that can be used during custom board design along with other available design collaterals including *Hardware Design Considerations for Custom Board Design* and *Schematic Design Guidelines and Schematic Review Checklist*:

There is a FAQ master list that provides list of all available FAQs for the Sitara processor families:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM243x, AM335x) families

For guidelines and E2E query links for custom board designers to refer, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design – Guidelines and E2E query links for custom board designers to refer

To make it easy for custom board designers working on a specific processor family, processor family wise FAQs have been listed:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

See the following FAQ that provides list of all the available FAQs including software related FAQs for sitara family of processors:

[FAQ] AM6x: Latest FAQs on AM62x, AM62Ax, AM62D-Q1, AM62Px, AM62L, AM64x, AM24x, AM3x, AM4x Sitara devices

Note

The FAQs are updated frequently. The recommendation is to review the FAQs of interest on a regular basis for updated information.

1.5 Custom Board Design Documentation

The recommendation is to update custom board design documents periodically to capture the updates to custom board requirements and changes to design (observed while testing or review) during different phases of custom board design. The updated information can be the baseline for the documentation package (design document) required for review (external or internal) support.

1.6 Processor and Processor Peripherals Design Related Queries During Custom Board Design

During the custom board design, for queries related to processor and processor peripherals, the recommendation is to start an E2E query for the device experts to support. The recommendation is to include queries related to a specific section of the design or peripheral or topic in an E2E query to minimize assignment and reply delay.

2 Custom Board Design Block Diagram

Drawing a detailed block diagram, covering all the major (required) functional blocks and interfaces (to external attached devices (peripherals)) is recommended for designing a fully functional custom board.

2.1 Developing the Custom Board Design Block Diagram

The recommendation is to identify and review all the relevant end equipment use case requirements (features), functions and include all critical components (functional blocks), associated devices required for processor functioning (Example: PMIC) and include details of the attached devices interfaced to the processor as part of the block diagram. The recommendation is to draw separate blocks for each function or interface, connect blocks with arrows indicating the directions, label blocks and clearly indicate the interfaces and processor IOs used for connecting the processor and attached devices. The recommendation is to consider grouping of the blocks based on the implemented functions whenever possible. The recommendation is to review, refine and baseline the block diagram before starting the design.

The below resources can be used (as supporting documents) when preparing the detailed block diagram:

- *TMDS62LEVM* (AM62L evaluation module) and any other available EVMs.
- The link listed below to the processor-specific product page on TI.com includes Functional block diagrams, Data sheet, TRM, User guides, Silicon errata, Application notes, Hardware design considerations for custom board design, Schematic design guidelines and schematic review checklist, and other relevant documents. The design and development section include links to available EVM (EVM design files), design tools, simulation models and software. As part of information related to support and training, links to commonly viewed or searched E2E threads and E2E FAQs are available.

The processor product page link on TI.com is listed below:

AM62Lx [ANB]

- AM62L

2.2 Configuring the Boot Mode

The processor family supports reduced pin count (x4 pins) or full pin count (x16 pins) boot modes. The processor family additionally supports eFuse BOOTMODE1 and eFuse BOOTMODE2. Custom board designers have the flexibility to choose the required boot mode to optimize use of external components.

For supported boot mode configurations, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62Ax / AM62Px / AM62D-Q1 / AM62L - Supported bootmode configurations

The recommendation is to indicate the configured boot mode and the boot mode provisions provided in the block diagram. The recommendation is to include the boot configuration (reduced pin count or full pin count or eFuse), primary boot and backup boot.

The processor family supports multiple peripheral interfaces that support boot. For the available boot mode configurations and supported peripherals, see the device-specific TRM. The processor family supports primary boot mode and an optional backup boot mode configuration. If the primary boot (source) mode fails, the ROM switches on to the backup boot mode.

The device supports two different BOOTMODE pin mapping options:

1. Reduced Pin count - Using only 4 of the 16 bootstrap pins BOOTMODE [15:12]
2. Full Pin count - Using all 16 of the bootstrap pins BOOTMODE [15:0]

The reduced pin count option is implemented in hardware, and is transparent to the ROM code. Its implementation is a look-up table that uses four pins to select from either the full pin count option, or a set of commonly used boot modes selected as reduced pin count options. The selection determines what value is loaded into the Device Status register WKUP_CTRL_MMR_CFG1_DEVSTAT[15:0] on a POR. The boot mode configuration inputs are recommended to be stable before releasing (deassertion) the PORz input.

The reduced pin count boot mode configuration offers the advantage of requiring less boot mode configuration pins and external resistors, which can translate to fewer components (pullup or pulldown resistors) required. The reduced pin count boot mode comes at the cost of making fewer pin selectable boot mode options.

However, two (eFuse BOOTMODE1, eFuse BOOTMODE2) of the reduced pin count boot mode configuration options selectable from the *Reduced BOOTMODE Pin Mapping* table can be configured to any of the full 16-bit options by programming the required boot mode configuration the eFuse. To program the eFuse, a dedicated supply generated using an LDO with provision to enable only while writing the eFuse is required to be connected to the VPP pin.

Note

The recommendation is to provide provision to connect the VPP supply (Using on-board LDO or connect an external supply for production programming using a test point provided for the processor VPP pin along with on-board capacitors added and a processor IO used to control the VPP supply timing) to the processor VPP pin used for eFuse programming. For more information, see the Section 3.2.6.

To reduce the required pullup/pulldown resistors used for configuring the boot modes, the input buffers for BOOTMODE [11:0] pins are disabled during POR unless BOOTMODE [15:14] are set to '00'. Disabling the buffers avoids power consumption due to floating inputs on these pins when the reduced pin count boot mode configuration is used. For more information, see the device-specific TRM.

Reduced Pin Count Boot Mode:

Reduced pin count boot mode uses BOOTMODE [15:12] (x4 pins) and the configuration is summarized below:

BOOTMODE [13:12] – The boot mode pins are used to configure the required primary and secondary boot mode or eFuse BOOTMODE1/eFuse BOOTMODE2

BOOTMODE [15:14] – The boot mode pins are used to select the boot mode configuration (reduced or full pin count). For more information, see the device-specific TRM.

Note

BOOTMODE [11:00] – IO buffers are off during reset and after reset. The boot mode input (IOs) pins can be left unconnected when the IOs are not configured for alternate functions or can be configured for available alternate functions. The recommendation is to connect the boot mode input (IOs) pins to the alternate function through a 0Ω series resistor. Series resistor can be used to isolate the alternate function during testing.

Note

Leaving BOOTMODE [15:12] pins unconnected is not recommended or allowed option.

Full Pin Count Boot Mode:

Full pin count boot mode uses BOOTMODE [15:00] (x16 pins) and the configuration is summarized below:

PLL Config (Configuration): BOOTMODE [02:00] – PLL config pins are used to indicate the system clock (PLL reference clock selection) frequency (WKUP_OSC0_XI/XO) to ROM code for PLL configuration

Note

For supported crystal frequency see the processor-specific data sheet. Configure the boot mode to match the supported crystal or clock frequency. Wrong clock frequency configuration affects the processor performance including resetting of the board.

Primary Boot Mode: BOOTMODE [06:03] – The boot mode pins are used to configure the required primary boot mode, the peripheral/memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – The boot mode configuration pins support optional configurations for primary boot and are used in conjunction with the primary boot mode selection pins

Backup Boot Mode: BOOTMODE [12:10] – The boot mode pins are used to configure the required backup boot mode, the peripheral/memory to boot from, in case primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – The boot mode pin provides additional configuration options (optional - depends on the selected backup boot mode pins)

BOOTMODE [15:14] – The boot mode pins are used to select the boot mode configuration (reduced or full pin count). For configuration, see the device-specific TRM

Note

Leaving BOOTMODE [15:00] pins unconnected is not recommended or allowed option.

For more information on full and reduced pin count boot mode mappings, see the *Boot Mode Pin Mapping Options* section of device-specific TRM.

Key considerations when configuring boot mode:

- The recommendation is to always include provision to configure boot modes used during the custom board development phase, such as USB boot (USB0, DFU), UART boot (UART0) or no-boot/Dev boot mode for debug (using JTAG)
- Boot mode pins support alternate functions that can be configured after the boot mode configuration inputs are latched. The recommendation is to take into consideration the alternate function implemented when choosing pullup or pulldown resistors during custom board design. In case the boot mode inputs are being driven by external inputs to support test automation or remote configuration, the boot mode inputs are required to return to the required boot configuration value (level) whenever the processor is reset (indicated by the RESETSTATz output pin) to allow the processor to boot correctly.

For information related to supported boot modes, see the *Initialization* chapter of the device-specific TRM and device-specific silicon errata.

For implementing the required boot mode (reduced pin count or full pin count), see the EVM *TMDS62LEVM* schematic.

Note

Custom board designers are responsible for providing provision to set the required boot mode configuration (using pullups or pulldowns, or optionally using jumpers/switches (with provision for external ESD protection when set in uncontrolled ESD environment)). The recommendation is to provide provision for pullup and pulldown for the boot mode input pins that have configuration capability for increase design flexibility. Shorting of multiple boot mode input pins together, leaving any of the boot mode input pins unconnected or connecting the boot mode inputs directly to supply or ground is not recommended or allowed.

Note

When the full pin count boot mode option is configured, each of these balls (BOOTMODE [15:0]) are required to be connected to the corresponding power supply or VSS through separate external pull resistors to make sure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.

When the reduced pin count boot mode option is configured, each of these balls (BOOTMODE [15:12]) are required to be connected to the corresponding power supply or VSS through separate external pull resistors to make sure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.

Note

The recommendation is to connect the processor boot mode input pins (configured for alternate function) to the alternate function through a 0Ω series resistor. Series resistor can be used to isolate the alternate function during testing.

Note

Boot mode configuration resistors are recommended to be pulled to VDDSHV0.

Note

When boot mode configuration is set using eFuse, provision to connect the VPP supply is recommended.

Note

For reduced pin count boot mode configuration, 25MHz (Crystal or LVCMOS digital clock) is the only supported clock frequency.

For full pin count boot mode, see the device-specific data sheet for the supported clock frequencies and the device-specific TRM to configure the supported clock frequency.

For implementing the boot mode, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation with isolation buffers used

[FAQ] AM625 / AM623 / AM620-Q1 / AM64x / AM243x / AM62A / AM62P / AM62D-Q1 / AM62L - Bootmode implementation without isolation buffers

2.3 Configuring the Processor Pins Functionality (PinMux Configuration)

The processor family supports a number of peripherals, interfaces (memory, synchronous, asynchronous) and GPIOs. To optimize processor size, pin count and package while maximizing functionality, many of the processor pads (pins) provide provision to multiplex (up to eight) signal functions. All peripheral instances may not be configurable or used (on a specific custom board).

TI provides the SysConfig-PinMux Tool that can be used by custom board designers to configure the required functionality (peripherals, interfaces and IOs).

Note

The recommendation is to save the PinMux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After the selection of the processor OPN and updating the block diagram to include the processor part number, the next phase of the custom board design is the power supply architecture design.

3.1 Power Supply Architecture

The power supply architectures that can be considered are listed below:

3.1.1 Integrated Power Architecture

The integrated power architecture can be based on Multi-channel ICs (PMIC) such as TPS65214 or similar. Review the PMIC product page for the device status (preview or active), changes to the collaterals and addition of collaterals.

For more information on the AM62Lx power architecture using PMIC, see the EVM *TMDS62LEVM* schematic and *AM62L Power Supply Implementation* application note.

Note

PMIC MODE/RESET pin was configured as cold reset and connecting RESETSTATz to the pin is not an option. For applications using the “RTC only” low-power mode, customers can drive the pin with the “power-good” signal of the external DC/DC or LDO generating the RTC supply rails. The connection triggers a cold reset on the PMIC if there is a fault on VDD_RTC or VDDS_RTC.

It is allowed or acceptable (safe) to leave the pin floating since an internal (approximately 25nA) pulldown is available and enabled.

The recommendation is for PORz input to reach a valid logic low level before the supplies begin to ramp down. The PMIC based power architecture is designed (expected) to monitor (make sure) if all power rails have been turned off and decay below 300mV before initiating a new power-up sequence anytime any of the processor power rail drops below the minimum value defined in *Recommended Operating Conditions*.

When choosing an alternate (non-TI) PMIC, the recommendation for custom board designers is to review the relevant processor collaterals including the device-specific data sheet and *Maximum Current Ratings* application note and follow the requirements/recommendations. The recommendation is to review the slew rate requirements, *Power-Up Sequencing* and *Power-Down Sequencing* sections of the device-specific data sheet and confirm the selected PMIC based power architecture supports the requirements.

See the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design – Queries regarding power architecture including PMIC

3.1.2 Discrete Power Architecture

The power architecture can be based on discrete DC-DC converters and LDOs.

For information related to available or recommended discrete power architecture, see the device-specific (AM62L) product page on TI.com.

Processor-specific product page provides the updated information on the available power architecture.

When a custom (TI or Non-TI) discrete power architecture is implemented, take note of the supplies sizing, supplies sequencing, supplies slew rate and PORz input L->H delay (hold time) (for oscillator start-up and stabilization) requirements after all the supplies ramp and verify these requirements as per the device-specific data sheet are followed.

During power-down, the recommendation is for the PORz input to reach a valid logic low level before the supplies begin to ramp down. The discrete power architecture is expected to be designed to be able to turn off all power rails and monitor the power rails decay to less than 300mV before initiating a new power-up sequence anytime a power rail drops below the minimum value defined in *Recommended Operating Conditions*.

PORz input is recommended (required) to be held low (active) during power-up until all the processor supplies ramp and are valid (stable) plus minimum delay of 9.5ms (mentioned as 9500000ns in device-specific data sheet) for internal oscillator to start-up and stabilize (when using external crystal plus internal oscillator, see the device-specific data sheet) or PORz input is held low (active) until all the processor supplies ramp and are valid and external oscillator clock output is stable (when using external LVCMOS digital clock source (oscillator)) plus minimum delay of 1.2µs (mentioned as 1200ns in data sheet) (see the device-specific data sheet).

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to Discrete power Architecture

3.2 Processor Supply (Power) Rails (Operating Voltage)

For a complete list of processor power supply rails and recommended operating condition (ROC), see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

For more information about processor ROC, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62D-Q1 / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition

The processor family does not support dynamic voltage scaling (switching) for processor core, peripheral core and peripheral analog supplies after the processor cold reset input (PORz) has been released. Some of the IO supply for IO groups support dynamic voltage switching. Refer to the *IO supply for IO groups* description in the device-specific data sheet for the IO supply for IO groups that support dynamic voltage switching.

For more information about dynamic voltage scaling (DVS) and dynamic frequency scaling (DFS), see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling for SOC core (VDD_CORE), Peripheral Core and Analog supplies

Note

The recommendation is to verify that the supplies connected to the processor supply rails are within the *Recommended Operating Conditions* of the device-specific data sheet.

3.2.1 Supported Low-Power Modes

For the supported low-power modes, see the device-specific data sheet.

For implementation of RTC only or RTC + DDR Self-refresh low-power mode, see the EVM *TMDS62LEVM* schematic.

For additional explanation on the low-power modes and the functioning see the device-specific TRM.

PMIC_LPM_EN0 has a special output cell that turns on a weak pullup as soon as power is applied. The weak internal pullup turns off at the same time the output is driven high on the rising edge of RTC_PORz input. (An external pull was required on AM62x processors because the PMIC_LPM_EN0 IO was turned off while reset was asserted. In the case, the PMIC can never turn on without the external pullup resistor).

3.2.2 Core Power Supply

The processor family is specified to operate at a fixed core voltage of 0.75V.

Processor core supply VDD_CORE and peripheral core supplies VDDA_CORE_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 are recommended to be powered from the same power source (specified nominal operating voltage as per the *Recommended Operating Conditions* (ROC) table).

For supply rails that includes a ferrite filter, a bulk capacitor is recommended on the load side of ferrite (connecting to the processor pins).

A 0.75V Fixed-voltage always-on power source is recommended to be connected to VDD_RTC (RTC Core Supply voltage) when low-power modes (including RTC only mode) are used.

The recommendation is to connect VDD_CORE and VDD_RTC to the same power source when low-power mode (including RTC only mode) is not used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Peripherals Power Supply

The processor family supports dedicated, peripheral supply (power) pins for USB (common for USB0 and USB1), PLLs, DSITX0 and ADC0. The nominal voltage is 1.8V. An additional 3.3V analog supply is recommended for USB.

For VDDS_DDR (DDR PHY IO supply), the recommended supply is 1.1V (when interfaced to LPDDR4 memory - attached device) or 1.2V (when interfaced to DDR4 memory - attached device) based on the memory used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.4 Processor IO Supply for IO Group Power Supply

The processor family supports the following:

- Dual-voltage IO supply for IO group power supply (3.3V or 1.8V)
- Fixed IO supply for IO group power supply (1.8V)

3.2.4.1 1.8V or 3.3V Dual-Voltage IO Supply for IO Group Power Supply

The processor family supports x5 (five) dual-voltage IO supply for IO group (VDDSHVx [x = 0-4]). Each group is connected (referenced) to a fixed set of IOs. Each IO supply for IO group can be connected to fixed (VDDSHV2, VDDSHV3, VDDSHV4 supports dynamic supply switching) 3.3V or 1.8V supply independently. The IO supply for IO group defines a common operating voltage for the entire set (fixed set) of IOs.

3.2.4.1.1 Additional Information

Most of the processor IOs are not fail-safe. For information on available fail-safe IOs, see the device-specific data sheet. The recommendation is to connect the IO supply of attached devices to the same power source connected to the respective processor dual-voltage IO supply for IO group (VDDSHVx) to make sure the custom board design never applies potential to any of the processor IO that is not powered. Applying input to the IOs that are not fail-safe when IO supply is not available can affect the processor functionality, performance and reliability.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe)

The FAQ is generic and can also be used for AM62Lx processor family.

Available IO supply for IO groups information are listed below:

- VDDSHV0 – Dual-voltage IO supply for GPMC0 IO group (Fixed)
- VDDSHV1 – Dual-voltage IO supply for General interface IO group (Fixed)
- VDDSHV2 – Dual-voltage IO supply for MMC0 IO group (Fixed or Dynamic supply switching)
- VDDSHV3 – Dual-voltage IO supply for MMC1 IO group (Fixed or Dynamic supply switching)
- VDDSHV4 – Dual-voltage IO supply for MMC2 IO group (Fixed or Dynamic supply switching)

Note

Dynamically switched supply 1.8V or 3.3V can be applied to IO supply for IO groups shown above as dynamic. A fixed 1.8V or 3.3V can be applied to IO supply for IO groups shown above as fixed. There is no IO supply voltage level dependency between 2 IO supply for IO groups.

3.2.4.2 1.8V Fixed IO Supply for IO Group Power Supply

The processor family supports x4 (four) Fixed-voltage 1.8V IO supply rails (VDDS0, VDDS1, VDDS_RTC and VDDS_WKUP). All attached devices (IOs) connected to these IOs are required to be powered from the same power source that is being used to power the respective processor supply rails.

A 1.8V Fixed-voltage an always-on power source is recommended to be connected to VDDS_RTC (IO supply for LFOSC0 and RTC IO group) when low-power modes (including RTC only mode) are used.

The recommendation is to connect VDDS_RTC (IO supply for LFOSC0 and RTC IO group) to a valid 1.8V IO power source when low-power modes (including RTC only mode) are not used.

Available IO supply for IO groups information is listed below:

- VDDS0 – IO supply for GENERAL0 IO group (RGMII1, RGMII2 IO groups)
- VDDS1 – IO supply for OSPI0 IO group
- VDDS_RTC – IO supply for LFOSC0 and RTC IO group
- VDDS_WKUP – IO supply for WKUP IO group

3.2.5 Integrated LDO for SD Card Interface (Dynamic Voltage Switching Dual-Voltage Power Supply)

The processor family supports an integrated LDO (SDIO_LDO) to power the SDIO interface IO supply for IO group and SD card interface pullups, capable of dynamically switching between 3.3V and 1.8V voltage. The recommendation is to connect the recommended output capacitor close to the LDO output pin (CAP_VDDSHV_MMC). For information on recommended, capacitor value and connection, refer to the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

V1P8_SIGNAL_ENA bit is used to control the LDO output level used for controlling the SD card interface IO (signaling). The output of the LDO can be connected to the processor IO supply for IO group used for SD card interface (VDDSHV3 or VDDSHV4 for UHS-I SD card support).

For connecting the LDO pins (SDIO_LDO and CAP_VDDSHV_MMC) when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

3.2.6 VPP (eFuse ROM Programming) Power Supply

VPP supply can be sourced from a separate on-board LDO supply or an external supply controlled by a processor IO.

VPP supply pin can be left floating (HiZ) or pulled to ground (ok to connect a resistor with a TP to isolate the ground and connect supply) during, processor power-up, power-down and normal operation.

The following hardware requirements are recommended to be taken care when programming eFuse ROM (OTP):

- The VPP power supply is recommended to be applied only after completion of processor power-up sequence and while programming the eFuse.
- The recommendation is to use a fixed output LDO with higher input voltage (2.5V or 3.3V) and enable input (control). The enable input is recommended to be controlled by the processor GPIO for timing the VPP supply.
- The VPP supply is expected to see high load current transients. Local bulk capacitor is recommended near to the processor VPP pin to support the current transient.
- Select LDO with quick discharge capability or use an external discharge resistor.
- A maximum current of 400mA is specified during eFuse programming.
- When an external power supply is used, the supply is recommended to be applied after the processor power supplies ramp and are stable.
- When an external power supply is used, recommend adding on-board bulk capacitor, decoupling capacitor and discharge resistor near to the processor VPP pin. Add a test point to connect external power supply and provision to connect one of the processor GPIO to control timing of the external supply.
- The recommendation is to disable the VPP supply (left floating (HiZ) or grounded) when not programming the eFuses.
- When an adjustable LDO is used, consider adding an external zener for over-voltage protection at the LDO output.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.2.7 Internal LDOs for IO Supply for IO Groups (Processor)

The processor family supports x5 (five) internal LDOs (CAP_VDDS_GENERAL1, CAP_VDDS_GPMC and CAP_VDDS_MMCx [x = 0-2]) and each of the LDO output connects to a separate ball (pin) for connecting an external capacitor. For information on recommended, capacitor value and connection, refer to the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

Follow the relevant EVM design for selection of the capacitor voltage rating and package. Selecting a capacitor (value, voltage rating) that does not follow the EVM or the data sheet recommendations can affect the LDO output stability and processor performance.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Queries related to CAP_VDDSx CAP_VDDS

3.3 Power Supply Filtering

For implementing filtering, decoupling and bulk capacitors for the supply rails, see the EVM *TMDS62LEVM* schematic.

For supply rails that includes a ferrite filter, a bulk capacitor is recommended on the load side of ferrite (connecting to the processor pins.

3.4 Power Supply Decoupling and Bulk Capacitors

To decouple the processor (and attached device) supplies from board noise, decoupling and bulk capacitors are recommended.

For information on optimizing and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

Note

The decoupling capacitor numbers and type on the SK or EVM are only intended to serve as a guideline for customers. The true pass or fail criteria is the target impedance published in the PDN application note.

3.4.1 Note on PDN Target Impedance

The PDN target impedance values are provided for specific supply (VDD_CORE). The PDN target impedance values are not provided for other (all) supply rails since the target impedance calculation includes reference to the maximum current on the power rails and is dependent on use case.

For updates on the PDN target impedance supplies and values, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – Collaterals to Get started

Look for PDN target impedance values (VDD_CORE).

For VDDS_DDR supply rail, using target impedance as the signoff criteria is not recommended. See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* which outlines all details of power aware SI/PI simulations that needs to be performed. The eye mask checks from the power aware simulations are the signoff criteria for VDDS_DDR.

3.5 Power Supply Sequencing

A detailed diagram of the recommended *Power Supply Sequencing* (power-up and power-down sequence for No Low-Power Mode, RTC Only Low-Power Mode, RTC + DDR self-refresh Low-Power mode) are provided in the device-specific data sheet. All associated processor power supplies are recommended to be designed to allow for controlled supply ramp (supply slew rate) and supply sequencing (using a PMIC-based power supply or using on-board logic when discrete power architecture is implemented).

For more information, see the *Power Supply Requirements*, *Power Supply Slew Rate Requirement* and *Power Supply Sequencing* sections of the device-specific data sheet.

The sequence diagrams are updated based on customer inputs and internal analysis. The recommendation is to review the power sequence diagrams when updated revision for device-specific data sheet is available.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Custom board hardware design – Processor power-sequencing requirements for power-up and power-down

The FAQ is generic and can also be used for AM62Lx processor family.

3.6 Power Supply Diagnostics (Using Processor Supported External Input Voltage Monitors)

Voltage monitors internal to the processor are not supported.

3.7 Power Supply Diagnostics (Monitoring Using External Monitoring Circuit (Devices))

For enhancing custom board performance and based on the application requirements, the recommendation is to provide provision for external monitoring circuit (devices) for all the on-board processor and peripheral supply rails voltage and current draw from supply rails.

For more information, see the EVM *TMDS62LEVM* schematic.

Now that the power supply architecture and the required devices for generating the supply rails (based on power architecture) have been finalized, the recommendation is to update the block diagram to include the power architecture (include rail voltage value in the supply rail name) and connections. The recommendation is to generate a Power Supply Sequencing (power-up and power-down sequence based on No Low-Power Mode, RTC Only Low-Power Mode, RTC + DDR self-refresh Low-Power mode) diagram and verify the sequence with the device-specific data sheet.

3.8 Custom Board Current Requirements Estimation and Supply Sizing

The current (maximum and minimum) requirements for each of the supply rail are not provided in the device-specific data sheet. Current requirements are highly application dependent and are required to be estimated using TI provided tools and documents for a specific use case.

The recommendation is to take into account the maximum current rating (provided in the *Maximum Current Ratings* application note) for power supply sizing.

4 Processor Clock (Input and Output)

The next phase of the custom board design is implementation of clock architecture for processor and attached devices. The processor clock can be generated using internal oscillator with an external crystal connected or an external oscillator that generates an LVCMOS compatible clock output. Follow the connection recommendations in the device-specific data sheet when using an external oscillator as the clock source. The below section describes the available processor clock sources and requirements.

4.1 Processor Clocking (External Crystal or Oscillator)

The recommended processor clock sources and connections are shown in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25MHz external crystal connected directly to XI and XO pins that connects to the internal high frequency oscillator through WKUP_OSC0_XI / WKUP_OSC0_XO or external LVCMOS digital clock connected to through WKUP_OSC0_XI is, the main clock input source for the processor internal operations.

Follow the device-specific data sheet for the selection of the load capacitors when crystal is used to generate the processor clock.

The device-specific data sheet provides a recommended delay for clock to start-up and be stable.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Queries regarding crystal (MCU_OSC0) Start-up Time

The FAQ is generic and can also be used for AM62Lx processor family.

Spread Spectrum Clocking (SSC) (Clock source (input), internal clocks, PLLs) is not currently supported on AM62Lx processor family.

For information related to SSC support, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP : Enabling spread spectrum core clock on PRUSS

The FAQ is generic and can also be used for AM62Lx processor family.

The recommendation is to use a 32.768kHz crystal as clock source for low frequency oscillator (LFOSC0).

For more information, see the following FAQ:

[FAQ] AM62L (AM62L32, AM62L31): Custom Board Hardware design - LFOSC usage in the processor

Note

MCU_OSC0 (High frequency oscillator) for AM62x is WKUP_OSC0 for AM62Lx.

WKUP_LFOSC0 (Low frequency (32.768kHz) oscillator) for AM62x is LFOSC0 for AM62Lx.

4.1.1 LFOSC0 Connection When Unused

For information on the recommended connections for unused LFOSC0, see the *LFOSC0 Not Used* section in the *Specifications* chapter of the device-specific data sheet.

4.1.2 WKUP_OSC0 and LFOSC0, Crystal Selection

When selecting crystal for WKUP_OSC0 or LFOSC0, the recommendation is to consider the temperature and aging characteristics based on the worst case operating environment and expected life expectancy of the custom board or the end equipment. Verify the crystal load and the crystal load capacitor value used (including addition of the PCB capacitance (for WKUP_OSC0)) matches the device-specific data sheet recommendations. The recommendation is to select crystal load which allows selection of a standard capacitor value. Mismatch in value can introduce clock frequency PPM errors.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding Crystal selection and clock specifications

For more information, see the *WKUP_OSC0 Crystal Circuit Requirements* and *LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

The recommendation is to connect the WKUP_OSC0 crystal directly to the processor as per device-specific data sheet.

The recommendation is to verify the crystal selection with the crystal manufacturer (as required).

4.1.3 LVCMOS Compatible Digital Clock Input Source

The WKUP_OSC0_XI and LFOSC0_XI clock inputs can be sourced from an external 1.8V LVCMOS square-wave digital clock source. For more information, see the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators*, *WKUP_OSC0 LVCMOS Digital Clock Source* section in the *Specifications* chapter of the device-specific data sheet.

For more information, See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1/ AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 / AM62L Custom board hardware design – Queries regarding LVCMOS Digital Clock Source for, MCU_OSC0 (WKUP_OSC) or WKUP_LFOSC0 (LFOSC0)

Note

Follow the device-specific data sheet recommendations for connecting WKUP_OSC0_XO and LFOSC0_XO pins when LVCMOS digital clock is connect to the XI input.

Note

For more information, refer to the Notes provided in the *WKUP_OSC0 LVCMOS Digital Clock Source* section of device-specific data sheet.

4.2 Processor Clock Outputs

Processor IOs (pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for attached devices (External peripherals - Example: EPHY).

When CLKOUT0 and WKUP_CLKOUT0 are used to source more than x1 attached devices, buffering the CLKOUT0 and WKUP_CLKOUT0 is recommended.

Jitter profile is not defined on any of the clock outputs because there are many custom board specific variables that can impact jitter. Custom board designer is expected to measure clock output jitter of the specific custom board implementation across all operating conditions expected for the final product.

For more information, see the device-specific data sheet and TRM.

4.2.1 Observation Clock Outputs

The processor provides provision to output a MAIN domain observation clock and/or WKUP domain observation clock based on the processor family. OBSCLK0, OBSCLK1, WKUP_OBSCLK0 are observation clock outputs for test and debug purposes only. Observation clocks can be used to select one of the several different clocks as output. The observation clock is not expected to be used as a clock source for any external device. As stated in the device-specific data sheet, OBSCLK0, OBSCLK1 and WKUP_OBSCLK0 signals are provided for test and debug purposes only.

4.3 Clock Tree Tool

Clock Tree Tool (CTT) can be used to visualize the processor clock tree. Being an interactive visual tool, the CTT gives the user a global view of the device clock tree architecture and can be used to determine the register settings to obtain a specific configuration.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – Clock Tree Tool

5 Joint Test Action Group (JTAG)

The processor family supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV, ALX) Custom board hardware design – JTAG

Although JTAG is considered optional for normal board functioning, the recommendation is to include JTAG connections on the custom board design. The recommendation is to add provision for recommended pulls as per pin connectivity requirements and external ESD protection to populate when JTAG interface is used.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*

- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires five standard JTAG signals.
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in the mode.
- Trace port: the trace port allows real-time dumping of certain internal data. The trace port uses the EMUx pins to output the trace data.

For supported JTAG clocking rates, see the device-specific TRM.

Processor JTAG interface signals can be used to perform for boundary scan tests. The BSDL file for boundary scan testing can be downloaded from the below section on the processor-specific product page:

5.1.1.1 BSDL File

- AM62L BSDL

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation signals are referenced to the same IO supply for IO group. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 signals are referenced to VDDS0.

The recommendation is to use the TI recommended, defined and supported 20-pin connector rather then the 10-pin ARM connector. The 10-pin JTAG connector does not include the TRSTn signal or the EMU0, EMU1 signals.

For implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 Connection Recommendations for JTAG Interface Signals

For connection recommendations of JTAG interface signals, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

The recommendation is to always provide provision for TPs for the processor JTAG signals to be able to connect to external JTAG (When JTAG interface is not part of the custom board design) interface signals or debugger. The recommendation is to add the recommended pulls near to the processor JTAG signals as per the *Pin Connectivity Requirements* section of the processor-specific data sheet. Adding provision for external ESD protection and mounting the ESD components when the JTAG interface is used is recommended.

5.1.4 Debug Boot Modes and Boundary Scan Compliance

For supported debug functionalities, see the *On-Chip Debug* chapter of device-specific TRM.

Refer to the below sections of the of the *On-Chip Debug* chapter:

- JTAG Interface, JTAG Interface Signals
- Trace Port Interface, Trace Port Signals
- Debug Boot Modes and Boundary Scan Compliance

Emulation control inputs EMU0 and EMU1 are used to configure the debug boot mode behavior. Emulation control inputs EMU0 and EMU1 can be used to enable the boundary scan test capability.

Debug Boot Mode

Emulation control inputs EMU0 and EMU1 are sampled when PORz input is deasserted and the decoded value determines the debug boot mode behavior as detailed in Table *Debug Boot Modes* of the *On-Chip Debug* chapter of device-specific TRM.

Boundary Scan Compliance

Emulation control inputs EMU0 and EMU1 are sampled when TRSTn is deasserted and the decoded value determines the debug boot mode behavior as detailed in Table *Boundary Scan Compliance* of the *On-Chip Debug* chapter of device-specific TRM.

Debug or boundary scan functionalities does not have any dependency on boot mode configuration.

6 Configuration (Processor) and Initialization (Processor and Device)

The recommendation is to deassert (release) the processor cold reset input (for WKUP domain (PORz)) only after all the recommended processor supplies ramp plus the recommended delay (reset hold time) for the clock (crystal plus internal oscillator or external oscillator) to start-up and stabilize (see device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor family supports x3 (three) external reset inputs (pins) including cold reset input (PORz), MAIN domain warm reset input (RESETz) and RTC Power-on Reset input (RTC_PORz).

For connecting the warm reset input, follow the *Pin Connectivity Requirements* section of the device-specific data sheet.

See the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31): Custom Board Hardware design - PORz and RTC_PORz slew rate

The supported processor reset signals (Reset inputs, Reset status output) are described in the device-specific data sheet and device-specific TRM.

The processor family provides x1 (single) reset status output (pin) (MAIN domain warm reset status output (RESETSTATz)). RESETSTATz output reflects the internal reset state of the processor, and is low when either cold reset PORz input or warm reset RESETz input is low, and goes high after (see the device-specific data sheet) after PORz input or RESETz input is deasserted.

Processor reset status output when not used can be left unconnected. The recommendation is to provide provision for a test point for testing or future enhancements. An optional pulldown is recommended.

For the PORz input, LVCMOS IO input (3.3V tolerant, fail-safe input), a 3.3V input can be applied. The input thresholds follow the 1.8V IO supply voltage (VDDS_OSC0).

Follow the recommended PORz input timing recommendations in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset options are available through processor internal registers and emulation.

For more information, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design - Processor Reset inputs, Reset Status Output and Connection recommendations

6.1.1 RTC Power-on Reset (RTC_PORz)

RTC_PORz input is not recommended or allowed to float. RTC_PORz input IO level is 1.8V and is not fault tolerant. RTC_PORz input pin is required to be connected as described below:

1. The RTC_PORz input needs to be sourced from the PG output of VDD_RTC and VDDS_RTC power sources when operating in RTC Only mode. The PG open-drain outputs are released once both supplies are valid and the RTC domain is released from reset.

2. The RTC_PORz input needs to be sourced from a PMIC GPO (follow the power sequence diagrams in the device-specific data sheet when alternate power architecture is used) when operating in RTC + DDR Self-refresh mode. The PMIC is sourcing both the RTC power supplies. One of the PMIC's open-drain output is released at the appropriate time in the power-up sequence (check the PMIC used and the supported implementation).
3. The recommendation is to connect RTC_PORz input to the same signal connected to PORz input (1.8V level) when not using low-power modes. Assumes VDD_RTC is connected to the same source as VDD_CORE, and VDDS_RTC is connected to the same source as VDDS0, VDDS1.

The potential applied to the VDD_RTC power supply rail must always be greater than or equal to the potential applied to VDD_CORE. The only power supply (rail) sequence requirement for VDD_RTC.

The RTC_PORz input must be held low until the RTC power rails are valid.

6.2 Latching of Processor Boot Mode Configuration Inputs

For information on the available processor boot options, see above Section 2.2.

Processor boot mode configuration inputs are latched at the rising edge of PORz input. After the status (level) on the boot mode inputs (pins) are latched, the boot mode input pins are available to be configured for alternate functions (multiplexed). RESETSTATz output optionally can also be used for latching the pin strap configuration for attached devices.

6.3 Resetting of the Attached Devices

Using an ANDing logic (implemented using a 2-input AND gate) to reset the attached devices as applicable (on-board media and data storage devices, and other peripherals) is recommended since the ANDing logic can cover all processor external reset conditions. Any of the processor general purpose input/output (GPIO) pin (select an AM62Lx pin with a GPIO multiplexing option that is turned off by default) is connected to one of the AND gate input with provision for 0Ω to isolate the GPIO input to the ANDing logic for testing or debug. MAIN domain warm reset status output (RESETSTATz) can be connected as the other input to the AND gate. Make sure the processor IO supply and the pullup supply connected to the AND logic input are sourced from the same power source. Processor IO buffers are off during reset. The recommendation is to add a pullup near to the ANDing logic AND gate input (input that is connected to the processor GPIO, RESETSTATz output has a pulldown near the processor pin and driven high by the processor reset logic) to prevent the AND gate input from floating and to enable the reset logic controlled by the processor IO during power-up (Example: eMMC flash or OSPI flash comes out of reset as soon as the RESETSTATz output goes high).

An ANDing logic is recommended to reset the attached devices since the ANDing logic provides the flexibility to be able to reset the attached device in all processor reset condition.

In case only the processor MAIN domain warm reset status output (RESETSTATz) is used (without ANDing logic) to reset the attached device, the recommendation is to match the IO voltage levels of the attached device and RESETSTATz output. A level translator is recommended to match the IO voltage levels. The implementation reduces the attached device reset options flexibility.

For SD card interface, to support UHS-I SD card, the recommendation is to provide provision for a software enabled (controlled) power switch (load switch) that sources the power supply (VDD) to the SD card. A fixed 3.3V supply (processor IO supply) is connected as supply input to the power switch.

Use of power switch allows power cycling of the SD card configured for UHS-I speed (since resetting the power switch is the only way to reset the SD card) to the default speed.

For more information on implementing attached device reset and power switch enable reset logic for SD card power supply, see the EVM *TMDS62LEVM* schematic.

6.4 Watchdog Timer

Use of watchdog timer is application dependent. Consider using internal or external watchdog timer.

7 Processor - Peripherals Connection

The processor peripherals connection section covers the supported processor peripherals and is intended to be used along with the information provided in the device-specific data sheet, TRM, and relevant application notes. The documents type available that can be used include:

- Data Sheet: Pin diagrams, Pin function description, Pin attributes, Processor operating modes (MUX modes), configuration during and after reset, Electrical characteristics, AC Timings
- TRM: Functional description of processor and supported functionalities for the core and peripherals, Programming Guide, Information regarding registers and supported configuration
- Application Notes: Description of specific feature or peripheral, and description of commonly observed issues

Note

Additionally, FAQs and relevant E2E threads (newly created or previously answered) can be leveraged or used.

7.1 Selecting Peripherals Across Domains

The processor architecture includes multiple domain, each domain includes specific processing cores and peripherals:

- MAIN Domain
- RTC Domain
- Wakeup (WKUP) Domain

7.2 Memory Controller (DDRSS)

The DDRSS interface supports DDR4 or LPDDR4 memory interface. Choice of DDR4 or LPDDR4 memory is application or customer dependent as there are differences in latency and burst lengths in each of the memory type.

For additional information, refer below application note:

Sitara AM62Lx Benchmarks

Refer *DDR Electrical Characteristics* section of the device-specific data sheet for information related to JEDEC compliance. Refer note below from the device-specific data sheet:

Note

The DDRSS interface is compatible with DDR4 devices that are JESD79-4B standard-compliant, and LPDDR4 devices that are JESD209-4B standard-compliant.

For data bus width, inline ECC support, speed and max addressable range selection, see the *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter of device-specific data sheet.

The allowed memory configurations for DDR4 interface are 1x 16-bit or 2x 8-bit. 1x 8-bit memory configuration is not allowed or valid configuration.

The allowed memory configuration for LPDDR4 interface is 1x 16-bit.

When using LPDDR4 memory interface, based on the application requirements, same memory device can be used with the AM625 / AM623 / AM620-Q1 / AM625-Q1, AM62A7 / AM62A7-Q1 / AM62A3 / AM62A3-Q1 / AM62A1-Q1, AM62D-Q1, AM62P / AM62P-Q1 and AM62Lx processors due to the availability of 16-bit configuration.

LPDDR4 memory is used in the current EVM design. The below FAQ lists the SK / EVM that can be referenced in case DDR4 memory interface is required.

For connecting the DDRSS signals when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information on DDR4 or LPDDR4 memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x (ALV) Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDRSS : DDR4 / LPDDR4 MEMORY Interface

For more information, see the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDRSS controller and DDRSS PHY have a number of parameters to configure. To support the configuration, an online tool *(SysConfig tool)* is provided that generates an output file that is consumed by the driver. Choose the *DDR Subsystem Register Configuration* from the *Software tool* pulldown menu and choose the processor. The SysConfig tool takes board information, timing parameters from DDR device-specific data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then initiates the full training sequence.

The SDK includes configuration file for the memory (LPDDR4) device mounted on the EVM. In case a new configuration is required for a different memory (DDR4 or LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see the following FAQ:

[FAQ] AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 Custom board hardware design – Processor DDR Subsystem and Device Register configuration

The FAQ is generic and can also be used for AM62Lx processor family.

7.2.2 Calibration Resistor Connection for DDRSS

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations (including value and tolerance) as per the device-specific data sheet.

7.2.3 Attached Memory Device ZQ and Reset_N (Memory Device Reset) Connection

Follow the EVM schematic for connecting the recommended resistors (ZQ (Impedance calibration) and Reset_N (attached memory reset input)) to the memory device including recommended value and tolerance.

7.2.4 Unused Signals (Pins) on the Memory Device

The DDRSS does not support DDR0_ALERT_n, DDR0_PAR, DDR0_CKE1, DDR0_CS1_n, DDR0_ODT1 signals (pins). The recommendation is to follow the memory data sheet recommendations to connect any of the available signals that are not interfaced to the processor DDRSS.

7.3 Media and Data Storage Interfaces (MMC0, MMC1, MMC2, OSPI0/QSPI0 and GPMC0)

The processor family supports below memory interfaces:

7.3.1 Multi-Media Card/Secure Digital (MMCSD) Interface (MMC0, MMC1, MMC2)

The processor family supports x3 (three) Multi-Media Card and Secure Digital (MMC/SD/SDIO) (8b + 4b + 4b).

MMC0 supports 8-bit eMMC (embedded Multi-Media Card) interface. For supported speeds, see the *MMC0 - eMMC/SD/SDIO Interface* section of device-specific data sheet, refer EVM for implementation. Alternatively, the MMC0 signals can be used as IOs or other supported muxed functions, or for on-board SDIO interface. Interfacing SD card to MMC0 port is not recommended. MMC0 is the recommended interface for eMMC interface.

For more information on eMMC memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

For information on the supported speeds, see the following FAQ:

[FAQ] AM623: Can eMMC0 support DDR50 mode

For information on supported interface on the MMC0 port, see the following FAQ:

[FAQ] AM62A3: Any way to get 2 eMMC interfaces?

For information related to eMMC pulls, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: eMMC0_DAT0 not enabled pull up by ROM

For information related to eMMC capability to pause the clock when there are no transfers, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Is the eMMC clocks maintained when read and write operations are finished ?

The FAQ is generic and can also be used for AM62Lx processor family.

Refer to the silicon errata for eMMC related erratas.

MMC1/MMC2 supports 4-bit SD card interface including support for UHS-I SD card. MMC1 is recommended for implementing SD card interface (SD card boot mode, MMC1 peripheral was timing closed for operating with SD cards). MMC1 CLK, CMD, and DAT[3:0] signal functions are implemented with SDIO buffers on pins powered from (referenced to) VDDSHV3, which can be operated at 1.8V or 3.3V (dynamically switched) and MMC1 SDCD and SDWP signal functions are implemented with LVCMOS buffers on pins powered from (referenced to) VDDSHV1, which can be operated at 3.3V or 1.8V. The logic state of the MMC1_SDCD and MMC1_SDWP inputs to the host is not recommended to be changed when IO operating voltage for SD card changes to support UHS-I SD card.

Refer to the silicon errata for MMC1 SD card interface related erratas.

MMC1/MMC2 supports 4-bit embedded SDIO interface. MMC2 is recommended for implementing embedded SDIO interface. The MMC2_SDCD and MMC2_SDWP pins are powered from the same power rail as the other MMC2 pins. The MMC2 assignments are different because MMC2 is expected to be used with on-board fixed operating voltage SDIO devices similar to Wi-Fi or Bluetooth transceivers. For supported speeds, see the *MMC1/MMC2 -SD/SDIO Interface* section of device-specific data sheet, refer EVM for implementation.

For more information, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Why is MMC1 powered by two different voltage supplies, VDDSHV1 and VDDSHV3 ?

For MMC1/MMC2, UHS-I SDR50, UHS-I SDR104 receive modes require data training to center the data capture to the center of the data valid window. The timing requirements are not fixed to specific values. The required DLL software configuration settings for MMC1/2 timing modes is provided in the below table:

MMC1/MMC2 DLL Delay Mapping for all Timing Modes of device-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: UHS-I SDR104 Receive mode timing

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *Multi-Media Card Secure Digital (MMCSD) Interface* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3.2 Octal Serial Peripheral Interface (OSPI0) / Quad Serial Peripheral Interface (QSPI0)

The processor family supports connecting x1 memory device (1x Octal Serial Peripheral Interface (OSPI0) or Quad Serial Peripheral Interface (QSPI0)) or connecting up to x2 memory (Example: x1 OSPI + x1 QSPI) devices over the OSPI0 interface. The OSPI0 IOs are referenced to VDDS1 and support fixed 1.8V IO level.

Below are the valid combinations:

- OSPI + OSPI (Faster - DQS)
- QSPI + OSPI (Faster - DQS)
- OSPI (Faster - DQS)
- QSPI (Faster - LBCLKO)

Follow the EVM schematic implementation to interface the OSPI0 interface to memory devices, addition of series resistor for OSPI0_CLK, pulldown for OSPI0_CLK, pullup for data and CS signals, and implementation of memory devices reset logic.

Refer to the device-specific TRM to connect the supported CS (chip select) to the attached memory device when boot functionality is required to be supported.

OSPI0 supports two data capture modes, PHY mode and Tap mode. To better understand the supported modes, refer to the OSPI, *OSPI0* sub-section in the *Timing and Switching Characteristics* section in the *Specifications* chapter of the device-specific data sheet.

For more information on OSPI or QSPI memory interface, see the following FAQs:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – OSPI0 interface implementation (on TMDS62LEVM) guidelines

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

[FAQ] OSPI FAQ for Sitara/Jacinto devices

For more information, see the *Octal Serial Peripheral Interface (OSPI)* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3.3 General-Purpose Memory Controller (GPMC0) Interface

The processor family supports x1 General-Purpose Memory Controller (GPMC0) up to 133MHz interface.

For supported memory interfaces, see the *Media and Data Storage* section in the *Features* chapter, *Device Comparison* table in the *Device Comparison* chapter and *GPMC0 Signal Descriptions* table in the *Terminal Configuration and Functions* chapter of device-specific data sheet.

The GPMC0 IOs are referenced to VDDSHV0.

Supported GPMC0 configuration includes 16-bit (GPMC, Raw NAND, Muxed-NOR). The GPMC0 signal names are representative of the IP functionality rather than the supported functionality.

For more information, see the *General-Purpose Memory Controller (GPMC)* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Ethernet Interface

The processor family supports x2 (two) independent Ethernet interface with independent MAC ID (using CPSW3G0 peripheral). Each of the MAC interface supports RGMII or RMII interface.

For more information on the Ethernet interface, see the following FAQs:

[FAQ] AM6442, AM6441, AM6422, AM6421, AM6412, AM6411 and AM2434, AM2432, AM2431 (ALV, ALX) Custom board hardware design - Ethernet

The FAQ is generic and can also be used for AM62Lx processor family.

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RGMII interface and RGMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to RMII interface and RMII TI EPHY

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Ethernet PHY RGMII synchronous clock

The FAQ is generic and can also be used for AM62Lx processor family.

7.4.1 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G0)

The processor family supports x1 CPSW3G0 Ethernet switch (2 external ports). The CPSW3G0 can be configured either as a 3-port switch (interfaces to 2 external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having individual MAC address.

The CPSW3G0 interface IOs are referenced to VDDS0 and supports fixed 1.8V IO level.

CPSW3G0 supports RGMII (10/100/1000) or RMII (10/100) interface for each of the external Ethernet interface port.

For implementation of RMII interface, see the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G0 when configured for RMII interface supports processor connections to Ethernet PHY (EPHY) configured as controller (master) or device (slave).

CPSW3G0 when configured for RMII interfaces, interfaces to EPHY configured for an external 50MHz (connected to a buffered external oscillator or processor clock output CLKOUT0) clock input (one of the buffered clock output connects to processor MAC) or EPHY configured for 25MHz crystal or clock input with 50MHz clock output from EPHY connected to the processor MAC clock input.

One of the CPSW3G0 port is an internal CPPI (Communications Port Programming Interface) host port. CPPI is a streaming interface to provide data from DMA to CPSW3G0 peripheral and vice-versa.

CPSW3G0 allows using mixed RGMII/RMII interface topology for the x2 external interface ports.

RGMII_ID is enabled by default for Transmit data (TDn). RGMII_ID is not timed, tested, or characterized. Processor MAC does not implement internal delay for the Receive data (RDn) path.

For more information on the CPSW3G0 Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Programmable Real-Time Unit Subsystem (PRUSS)

The processor family does not support PRUSS.

7.6 Universal Serial Bus (USB) Subsystem

The processor family supports x2 (two) USB 2.0 interface ports. The USB interfaces (USB0, USB1 ports) can be configured as host or device or Dual-Role Device (DRD). USBn_ID (identification) functionality can be implemented (supported) using processor GPIO.

Follow the *USB (USB VBUS Detect Voltage Divider / Clamp Circuit) VBUS Design Guidelines* section of the device-specific data sheet to scale the external USB VBUS voltage (supply near the USB interface connector) and connecting to USBn_VBUS [n = 0, 1] pins.

Connecting the scaled VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) input is recommended when the USB interface is configured for device mode. Connection of scaled VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) is optional when the USB interface is configured for host mode.

Connecting 3.3V or a permanent supply equivalent to the processor supply to the USB VBUS is not recommended or allowed. The USB VBUS supply needs to be switched. The fail-safe input condition is valid only when the supply is connected through the recommended VBUS voltage divider and zener diode.

A USB power switch with OC (over current) output indication is recommended when the USB interface is configured as host for VBUS output voltage control. The USBn_DRVVBUS [n = 0, 1] (internal pulldown enabled during and after reset) controls the power switch. The recommendation is to connect the OC output to a processor IO (input) to detect VBUS over load.

For information related to USB connections and On-The-Go feature support, see the device-specific TRM.

When both USB0 and USB1 interfaces are not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the USB supply pins.

When USB0 or USB1 interface is not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the interface signals and USB supply pins.

The recommendation is to always provision for USB0 DFU boot for early board builds for board bring-up and debug.

For more information on USB2.0 interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – USB2.0 interface

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.7 General Connectivity Peripherals

The processor family supports multiple, general connectivity peripherals and instances. The processor family supports the following peripherals:

The following peripherals (UART, MCAN, MCSPI, MCASP, I2C) implements IOSET. Make sure the usage of the correct IOSET in the custom board design. Timing closure is based on the IOSETs.

Multichannel Serial Peripheral Interface (MCSPI):

The processor family supports x4 (four) (x4 MAIN domain) instances of MCSPI. The MCSPI module is a multichannel transmit/receive, synchronous serial bus and can operate in controller mode or peripheral mode. In controller mode, the processor SPI interface sources the clock to the attached device. In peripheral mode, the attached device is required to source the SPI clock to processor.

A series resistor 22Ω is recommended (as a starting point) for the MCSPI clock output signals. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown is recommended close to the attached device clock input pin.

A pullup is recommended for the chip select (CS) pin close to the attached device.

The MCSPI peripheral does not support boot. The OSPI0 supports SPI boot.

For the MCSPI SPIx_D0 and SPIx_D1 are the data lines. The data lines support programming the signals either to transmit data (transmission, output) or receive data (reception, input). A parallel pull is recommended for the processor or attached device data lines that can float.

The recommendation is to connect the SPI to x1 (single) memory device. When connecting to multiple memory devices, the recommendation is to follow high-speed design practices and perform simulations to make sure the layout is not going to generate non-monotonic clock transitions when the single clock source is connected to multiple SPI attached devices.

See the following FAQs:

[FAQ] SK-AM64B: MCSPI Integration Guide

[FAQ] AM6412: AM64x SPI D0 and D1 - MISO/MOSI

The FAQ is generic and can also be used for AM62Lx processor family.

Inter-Integrated Circuit (I2C):

Refer below Section 7.7.1.

Universal Asynchronous Receiver/Transmitter (UART):

The processor family supports x8 (eight) (x7 MAIN domain, x1 WKUP domain) instances of UART interface. Supported UART functions include data transfer (TXD, RXD), Modem control functions (CTS, RTS) and extended modem control signals (DCD, RI, DTR, DSR - supported by MAIN domain UART1).

When external UART interface signals are directly connected to the processor UART interface signals, verify IO level compatibility and fail-safe operation. The recommendation is to provide provision for external ESD protection.

The recommendation is to provision for UART boot (UART0) for early board builds for board bring-up and debug.

General Purpose Input/Output (GPIO):

Processor GPIOs include LVCMOS and SDIO buffer types and are push-pull type outputs. Some of the specific IOs support open-drain output type IO buffer interface. LVCMOS IOs when configured as I (input) have input slew requirements and O (output) has capacitor loading requirements. Perform simulation with the connected load capacitor to make sure the output is within the ROC as per device-specific data sheet electrical characteristics.

For more information, see the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to GPIO

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62Ax / AM62D-Q1 / AM62Px / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – Queries related to LVCMOS input Hysteresis

Audio Peripheral - Multichannel Audio Serial Port (MCASP):

The processor family supports x3 (three) (x3 MAIN domain) instances of Audio peripheral - Multichannel Audio Serial Port (MCASP). MCASP supports up to 4/6/16 Serial Data Pins (serializer) across x3 MCASP with Independent TX and RX Clocks. MCASP supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats. A series resistor 22Ω is recommended (as a starting point) for the MCASP clock output. The resistor is recommended to be placed near to the processor clock output pin (used for retiming). A pulldown is recommended close to the attached device clock input pin.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (interface signals) that can float.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L Design Recommendations / Custom board hardware design - Queries related to MCASP

Industrial and Control Interfaces:

The processor family supports multiple instances (see the *Device Comparison* table of the device-specific data sheet) of Industrial and Control Interfaces.

1. Modular Controller Area Network (MCAN) with Full CAN-FD support
2. Enhanced Pulse Width Modulator (EPWM)
3. Enhanced Quadrature Encoder Pulse (EQEP)
4. Enhanced Capture (ECAP)

Modular Controller Area Network (MCAN) with Full CAN-FD support:

The processor family supports x3 (three) (x3 MAIN domain) instances of Modular Controller Area Network (MCAN) with Full CAN-FD support.

The MCAN module supports both classic CAN and CAN-FD (CAN with Flexible Data-Rate) specifications.

Processor IO buffers are off during reset and after reset. Parallel pulls are recommended for any of the processor IOs (MCAN interface signals) that can float.

The required interfaces can be configured using the *SysConfig-PinMux* tool.

For more information on the supported peripherals, see the *Peripherals* chapter of the device-specific TRM.

7.7.1 Inter-Integrated Circuit (I2C) Interface

The processor family supports x5 (five) (x1 (single) I2C compliant, fail-safe open-drain output type IO buffer and x4 (four) LVCMOS buffer type IO based emulated) I2C interfaces. The supported I2C interfaces include x4 MAIN domain, x1 WKUP domain I2C interfaces.

An external pullup is recommended for the I2C interface (I2C2 with I2C OD FS IO buffers) with open-drain output type IO buffer **only** when the IOs are configured for I2C interface or IOs. A pullup is not required in case the IOs (inputs) are being actively driven.

When open-drain output type IO buffer I2C interface (I2C2) is pulled to 3.3V supply, the inputs have slew rate requirements specified. An RC is recommended to limit the slew rate. For RC implementation, see the EVM *TMDS62LEVM* schematic and see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

An external pullup is recommended for LVCMOS IOs when configured as emulated open-drain output type IO buffer I2C interface (I2C0, I2C1, I2C3 and WKUP_I2C0). For the available emulated open-drain output type IO buffer I2C instances, see the device-specific data sheet.

Pullup values in the EVM can be used as starting point. The pullup value depends on the I2C interface implementation and loading of the I2C bus. The recommendation is to measure the I2C waveforms and reduce (adjust) the pullup value as required.

For more information, see the following FAQ:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design – I2C interface

Note

Verify the *Exceptions* sub-section in the *Timing and Switching Characteristics, I2C* section of the device-specific data sheet during the custom board design. Take note of the exceptions for the emulated I2C interface. The recommendation is to add a series resistor to control the fall time.

For more information, see the *Inter-Integrated Circuit (I2C) Interface* section in the *Peripherals* chapter of the device-specific TRM.

7.8 Analog-to-Digital Converter (ADC0)

The processor family supports 1x 12-bit Analog-to-Digital Converter (ADC), Up to 4MSPS, x4 (four) analog inputs (time-multiplexed).

For the allowed ADC0 input range and electrical characteristics, see the *ADC Electrical Characteristics* section of device-specific data sheet.

Note

ADC0 inputs are not fail-safe. The recommendation is to apply the ADC0 inputs only after the ADC0 supply ramps.

Take note of the allowed ADC0 input range while connecting the external inputs.

For connecting the ADC0, supply and inputs when entire ADC0 or any of the ADC0 inputs are not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM62L, AM64x, AM243x (ALV, ALX) Custom board hardware design – ADC0 design guidelines

For more information, see the *Analog-to-Digital Converter (ADC)* section in the *Peripherals* chapter of the device-specific TRM.

7.9 Display Subsystem (DSS)

The processor family provides pin outs (pin attributes defined) for DPI and DSI interfaces. The processor (hardware) supports configuring (using) either MIPI DSI (x4 lanes D-PHY (DPHY)) or DPI (24-bit RGB LVCMOS) display (external). The selection of the processor display interface is required to be done at boot time.

DSI MIPI D-PHY (DPHY) display interface:

The processor family supports display interface with x4 (four) data lanes and x1 (single) clock lane.

For connecting DSITX0 signals when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

DPI display interface:

The processor family supports 24-bit per pixel, RGB/YUV422 modes, LVCMOS output, DPI (parallel) display interface.

DPI does not currently support SSC. Start an E2E thread or review available collaterals on the processor-specific product page to check on the status of SSC support for DPI.

For more information on DPI, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB- display interface

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *Display Subsystem and Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

7.10 Connection of Processor Power Supply Pins, IOs and Peripherals When not Used

All the processor supply (power) pins are recommended to be supplied (connected) with the supply voltages as per *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified in the *Pin Connectivity Requirements* section of the device-specific data sheet.

The recommendation is to read the notes at the beginning and end of the *Pin Connectivity Requirements*.

The processor family includes pins (package balls) that have specific connectivity requirements and pins that are recommended to be left unconnected.

For information on connecting unused processor peripherals and IOs, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

For more information on connection of unused processor peripherals and IOs, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC peripherals and IOs connection when not used

7.10.1 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type fail-safe IO buffer. The recommendation is to connect external pullup when a PCB trace is connected and an external input is not being actively driven. Open-drain output type IO buffer has slew rate requirements specified when pulled up to 3.3V. An RC (delay) is recommended to limit the slew rate.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62L / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection

7.10.2 External Wakeup Inputs (EXT_WAKEUP0 and EXT_WAKEUP1)

EXT_WAKEUP0 and EXT_WAKEUP1 signals are the External Wakeup Inputs. External Wakeup Inputs are active low inputs.

For connecting the EXT_WAKEUP0 and EXT_WAKEUP1 inputs, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

7.10.3 RSVD Reserved Pin (Signal)

Pin named RSVD is Reserved. The recommendation is to leave the RSVD pin unconnected (no test point (TP)) as recommended in the device-specific data sheet.

The recommendation is to leave the RSVD pin unconnected (do not connect any PCB trace or test point).

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP: Custom board hardware design – Connection recommendations for RSVD pins

The FAQ is generic and can also be used for AM62Lx processor family.

8 Interfacing of Processor IOs (LVCMOS or SDIO or Open-Drain, Fail-Safe Type IO Buffers) and Performing Simulations

An important consideration during the custom board design before start of the schematic capture is to analyze compatibility (Electrical characteristics, IO level, fail-safe operation) between the processor and attached devices.

- The device-specific (processor) data sheet includes information with regards to timing and electrical characteristics.
- For high-speed interfaces, the recommendation is to run simulations using IBIS model.

For more information, refer to the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

For information related to drive strength configuration support, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Drive Strength Configuration for SDIO and LVCMOS I/Os

The IBIS and IBIS-AMI models can be downloaded from the below sections on the processor-specific product page:

8.1 IBIS Model

- AM62L IBIS Model

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62A / AM62P / AM62D-Q1 / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Queries related to IBIS model

8.2 IBIS-AMI Model

- AM62L IBIS-AMI Model

Note

The recommendation is to double click on the .exe file to install the IBIS-AMI models. Installing IBIS-AMI model is the only supported option to use IBIS-AMI model.

9 Processor Current and Thermal Analysis

The custom board current requirements depends on selected processor, peripherals used, end equipment features implemented, application environment, operating temperature requirements, and temperature/operating voltage variations.

9.1 Power Estimation

For estimating the processor current (power) based on the use case, use below:

AM62Lx Power Estimation Tool

Check the device-specific (AM62L) product page on TI.com for availability.

9.2 Maximum Current Rating for Different Supply Rails

For information on the maximum current rating at the processor power terminals for power supply groups, see the *AM62L Maximum Current Ratings* application note. The recommendation is to follow the *Maximum Current Ratings* application note for power supply sizing.

9.3 Supported Power Modes

For information on the supported power modes (including RTC only, DeepSleep), see the *Power Modes* sub-section, *Power* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application note provides guidance for implementation of a thermal option for custom board designs using Sitara family of processors. The application note provides background information on common terms and methods. Any follow-up design support that can be required is provided only for board designs that follow thermal design guidelines contained in the application note.

The Thermal model can be downloaded from the below section on the processor-specific product page:

9.4.1 Thermal Model

- AM62L Thermal Model

9.4.2 Voltage Thermal Management Module (VTM)

A x1 (single) temperature sensor is supported. The device-specific data sheet provides the VTM accuracy and the device-specific TRM provides information on the location of the temperature sensors.

See the following FAQ:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62D-Q1 / AM62Px / AM62L / AM64x / AM243x (ALV, ALX) Custom board hardware design – Voltage and Thermal Manager (VTM)

10 Schematic:- Capture, Entry and Review

The schematic, capture and entry can now be started for the custom board design.

The below FAQ summarizes key collaterals that can be referenced during custom board schematic design and custom board schematic review:

[FAQ] AM64x, AM243x (ALV, ALX), AM62x, AM62Ax, AM62Px, AM62D-Q1, AM62L Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

For guidelines on component selection, schematic capture and review, see the following sections:

10.1 Custom Board Design Passive Components and Values Selection

When selecting passive components, the recommendation is to follow the device-specific data sheet (as applicable) for the values including the tolerance and voltage rating. The recommendation is to follow the derating guidelines (generic or company specific for passives (Example: resistor wattage and capacitor voltage rating)).

Note

Component values, package size and voltage rating in the EVM have been provided as a good starting point for the custom board designer.

During custom board design, the recommendation is for the custom board designers to validate if the TI recommended values, tolerance, package size and voltage rating are appropriate for the specific custom board design (end equipment) implementation and make required updates.

10.2 Custom Board Design Electronic Computer Aided Design (ECAD) Tools Considerations

Orcad is the Electronic Computer Aided Design (ECAD) tool used for EVM schematics.

Allegro is the ECAD tool used for EVM layout.

For information on the ECAD tools used for EVM design, see the following FAQ:

[FAQ] AM625 / AM623 / AM62L / AM625-Q1 / AM62A7 / AM62A3 / AM62A1 / AM62P-Q1 / AM62D-Q1 Custom board hardware design – processor evaluation modules or starter kits information including Board Design CAD tools version

A .alg file is provided for translating the Allegro design file to Altium. In case an altium converted design files are required, the recommendation is to check the relevant EVM or processor product page for availability or add an E2E query.

10.3 Custom Board Design Schematic Capture

The next phase of the custom board design after completing the schematics design is the schematics capture. During the schematic capture phase, the custom board schematics can be newly drawn or the EVM schematic design can be used (reused as a starting point) to make the updates.

For more information, see the EVM *TMDS62LEVM* schematic.

During schematic capture, follow below checklist:

AM62L (AM62L32, AM62L31) Processor Family Schematic Design Guidelines and Schematic Review Checklist

Additionally, the below FAQ can be used that includes schematic review checklist for AM62x processor families:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

The below FAQ summarizes the considerations when EVM schematics design files are reused for custom board designs:

[FAQ] AM62L (AM62L32 , AM62L31) Custom board hardware design - Reusing TI EVM design files

Note

When the EVM design (schematic) is reused, take care of implementation completeness of the required functionalities (implemented on multiple pages) and change in net names due to design changes or optimization are reviewed and updated. Review and follow the notes (Design, Review and CAD) added on the schematic pages close to the circuit before implementation.

When the EVM design (schematic) is reused, the DNI settings for all the components can reset. Make sure the DNIs are reconfigured (populating DNIs can affect the functionality). Review the DNI notes added on the schematic pages close to the circuit implementation.

10.4 Custom Board Design Schematic Review

After the completion of the schematic capture, the recommendation is to perform a self review using the *AM62L (AM62L32, AM62L31) Processor Family Schematic Design Guidelines and Schematic Review Checklist*.

The below FAQ lists the collaterals and steps that can be followed for performing self-review of the custom board schematic design:

[FAQ] AM62L (AM62L32 , AM62L31) Design Recommendations / Custom board hardware design - Custom board schematics self-review

Additionally, the below FAQ can be used that includes schematic review checklist for AM62x processor families:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L / AM64x / AM243x (ALV) / AM335x Design Recommendations / Custom board hardware design - Schematics review checklists

Refer below FAQ for information related to some of the common errors observed during schematic updates:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62Ax / AM62Px / AM62D-Q1 / AM62L Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics updates for Design Update Note

For information on connecting used/unused processor pins, and peripherals, see the following FAQ:

[FAQ] AM62x, AM62Ax, AM62D-Q1, AM62L, AM62Px, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals and add pullup or pulldown? (e.g. GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSx, ...)

The recommendation is to plan a formal schematic review internally to review the custom board schematics with reference to the *Schematic Design Guidelines and Schematic Review Checklist*. The recommendation is to review custom board design implementation for possible design errors, change in component values, connection errors, missing net connections, and other design recommendations not being followed.

The recommendation is to review the custom board schematic follows the recommendations as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers and Simulation

After the schematic capture and reviews (self, team and external (review by attached device silicon suppliers)) have been planned, completed and required updates are made, the recommendation is to perform component placement analysis (floor plan) for the custom board design to determine the optimal component placement approach and the interconnect distances between processor and various ICs (attached devices), determine board dimensions and outline.

The next phase of the custom board design is board layout (placing the components, finalizing the form-factor and board layout).

See the following sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

The *AM62Lx Escape Routing for PCB Design* provides a sample PCB escape routing for the AM62Lx processor family that can be referenced during custom board layout.

See the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Layout guidelines maximum trace length, length matching tolerance, impedance, trace spacing requirements for EMMC, RMII, OLDI interfaces

The FAQ is generic and can also be used for AM62Lx processor family.

11.2 DDR Design and Layout Guidelines

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*. Use of guidelines simplifies DDR4 or LPDDR4 board layout. Layout guidelines and requirements have been captured as a set of layout (placement and routing) recommendations that allow custom board designers to implement a custom board design that support the required functionality for the memory connection topologies supported by the processor. Any follow-up design support that can be required are provided only for board designs that follow the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for the recommended trace impedance for routing the DDRSS (DDR4 or LPDDR4) signals.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for supported, DDR4 data rate, device bit width, device count, Channel Width, Channels, Die, Ranks.

For the propagation delay, the delay to be considered for DDR4 or LPDDR4 is the delay related to the traces on the board. On a need basis, the package delay that has been included in the *Additional Information: Package Delays* section of *AM62x, AM62Lx DDR Board Design and Layout Guidelines* can be added.

AM62x, AM62Lx DDR Board Design and Layout Guidelines includes guidelines for bit swapping.

The recommendation is to perform signal integrity (SI) simulations during custom board schematic design and the board layout phase.

Note

DDR2 and DDR3 interfaces are not supported.

11.3 High-Speed Differential Signals Routing Guidelines

The *High-Speed Interface Layout Guidelines* application note provides guidelines for routing the high-speed differential signals. Guidelines include PCB layer stack-up, PCB material selection guidance as well as routing skew, length, and spacing guidelines. Any follow-up design support that can be required is provided for custom board designs that follow *High-Speed Interface Layout Guidelines*.

Note

Consider using the EVM *TMDS62LEVM* EVM layout for reference during custom board design.

11.4 Processor-Specific EVM Board Layout

The processor-specific EVM board layout can be used as reference when doing a custom board layout or the EVM board layout can be reused and required modifications can be made. The required simulations has been performed for all the high-speed interfaces on the EVM board.

11.5 Custom Board Layer Count and Layer Stack-up

One of the important requirement to be considered in determining layer count is the number of layers required to implement the high-speed DDR4 or LPDDR4 memory interface. Following the recommended layout guidelines typically requires the number of layers used in the EVM (TI recommended) or the layers recommended in the *Escape Routing for PCB Design* application note. Optimization of layer count can be considered based on the custom board design functionalities.

See the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* for further guidance and recommendations for implementing the DDR4 or LPDDR4 memory interface.

AM62Lx Escape Routing for PCB Design application note can be used as a guideline during custom board layout. Use of TI Via Channel Array (VCA) technology supports layer optimization.

11.5.1 Simulation Recommendations

Simulation is recommended for any layout changes or optimizations done with respect to the EVM layout.

11.6 DDR-MARGIN-FW

The DDR margin firmware and supporting scripts allow visualization and measurement of system margin in the DDR interface on board. These tools enable probe-less measurement of critical data signals to understand if the custom board design follows the recommended design guidelines of the interface.

DDR-MARGIN-FW - Firmware and scripts to measure system DDR margin

Check the device-specific (AM62L) product page on TI.com for availability.

For more information, see the following FAQ:

[FAQ] PROCESSOR-SDK-AM62X: Question about AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP DDR MARGIN TEST Tool

The FAQ is generic and can also be used for AM62Lx processor family.

11.7 Reference for Steps to be Followed for Running Board Simulation

To get an overview of the board extraction, simulation, and analysis methodologies for LPDDR4 memory interface, see the *LPDDR4 Board Design Simulations* chapter of the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

See the following FAQs:

[FAQ] AM625 / AM623 / AM620-Q1 / AM625-Q1 / AM625SIP / AM62A7 / AM62A3 / AM62A1-Q1 / AM62D-Q1 / AM62L / AM62P / AM62P-Q1 / AM64x / AM243x Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM243x (ALV), AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px

12 Custom Board Assembly and Testing

The next phase of custom board design is board, assembly and bring-up, functional testing, software integration testing and performance testing.

The recommendation is to, verify that components marked as DNP or DNI in the design are not populated before applying power supply to the custom board.

The recommendation is to not connect any external inputs to the processor IOs before the processor IO supplies ramp (most processor IOs are not fail-safe, refer device-specific data sheet for available fail-safe IOs).

The recommendation is to verify the IO level compatibility when external inputs are directly connected to processor inputs. The recommendation is to provide provision to add an external ESD protection (as required) on-board or on the interface board.

The recommendation is to verify that none of the processor IO pullups have the supply rail referenced to the power source that is available before the processor IO supplies ramp.

12.1 Custom Board Bring-up Tips and Debug Guidelines

See the following FAQs during board bring-up:

[FAQ] AM625 / AM623 / AM620-Q1 / AM62L / AM62A / AM62D-Q1 / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Circuit Optimization of Custom board hardware design

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62L, AM62Ax, AM62D-Q1, AM62Px)

13 Processor (Device) Handling and Assembly

Moisture Sensitivity Level (MSL) rating/peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, lead finish/ball material and the recommended MSL rating/peak reflow to be followed.

For more information, see the following link:

- AM62L Ordering & quality

13.1 Processor (Device) Soldering Recommendations

Note the MSL rating/Peak reflow recommendation on TI.com for the selected processor.

13.1.1 Additional References

For information on Moisture sensitivity level, see the following:

- *MSL Ratings and Reflow Profiles*
- *Moisture sensitivity level search*

14 Terminology

ADC	Analog-to-Digital Converter
BSDL	Boundary-Scan Description Language
CAN-FD	Controller Area Network Flexible Data-Rate
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
DPI	Display Parallel Interface
DSI	Display Serial Interface
DSITX	Display Serial Interface Transmitter
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECAD	Electronic Computer Aided Design
ECAP	Enhanced Capture
ECC	Error-Correcting Code
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EPWM	Enhanced Pulse-Width Modulator
EQEP	Enhanced Quadrature Encoder Pulse
FAQ	Frequently Asked Question
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High-Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MAC	Media Access Controller
MCAN	Modular Controller Area Network
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interfaces
MCU	Micro Controller Unit
MMC	Multi-Media Card
MSL	Moisture Sensitivity Level
OSPI	Octal Serial Peripheral Interface
OTP	One-Time Programmable
PCB	Printed Circuit Board
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface

RMII	Reduced Media Independent Interface
ROC	Recommended Operating Condition
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select Input
TRM	Technical Reference Manual
TRSTn	Test Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCA	Via Channel Array
VTM	Voltage Thermal Management Module
WKUP	Wakeup
XDS	eXtended Development System

15 References

15.1 Processor-Specific (AM62Lx)

- Texas Instruments: *AM62Lx Sitara Processors Data Sheet*
- Texas Instruments: *AM62L Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Lx Sitara Processors Silicon Errata*
- Texas Instruments: *AM62L32, AM62L31 Processor Family Schematic Design Guidelines and Schematic Review Checklist*
- Texas Instruments: *EVM TMDS62LEVM*
- Texas Instruments: *AM62x, AM62Lx DDR Board Design and Layout Guidelines*
- Texas Instruments: *AM62Lx Escape Routing for PCB Design*
- Texas Instruments: *AM62L Maximum Current Ratings*
- Texas Instruments: *AM62L Power Supply Implementation*
- Texas Instruments: *AM62L Product Overview*
- Texas Instruments: *Sitara AM62Lx Benchmarks*

15.2 Common

- Texas Instruments: *AM625, AM623, AM620-Q1, AM625-Q1, AM625SIP, AM62A3, AM62A7, AM62A7-Q1, AM62A1-Q1, AM62D-Q1, AM62P-Q1 Schematic, Design Guidelines and Review Checklist*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*
- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*

- Texas Instruments: *Jacinto 7 DDRSS Register Configuration Tool*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Using IBIS Models for Timing Analysis*
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*

16 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (June 2025) **Page**

- (Thermal Model): Updated the thermal model link 32
- (Custom Board Design Passive Components and Values Selection): Added Note 32
- Added section Custom Board Design Electronic Computer Aided Design (ECAD) Tools Considerations 33
- (Custom Board Design Schematic Capture): Added Schematics review checklists FAQ 33
- (Custom Board Design Schematic Review): Added Custom board schematics self-review and SK Schematics updates for Design Update Note FAQs 33
- Added section Processor-Specific EVM Board Layout 35
- Added section DDR-MARGIN-FW 35
- (Custom Board Assembly and Testing): Added more information about board assembly and testing recommendations 36

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