User's Guide

Jacinto7 EVM Quad Port Ethernet Expansion Board User's Guide

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Trademarks

1 Introduction

The Jacinto7 EVMs are development and evaluation systems that enable developers to write software and develop hardware around the Jacinto7 family of processors. The main elements of the system are available on the EVM system itself. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto7 processor.

Beyond the basic resources provided, additional functionality can be added via expansion cards.

This Technical User's Guide describes the hardware architecture of the Jacinto7 EVM – Quad Port Ethernet Expansion board (QP-ENET), which is interfaced with J7 EVM boards through Serial Ethernet Expansion Connector.

1.1 Key Features

Key features of QP-ENET:

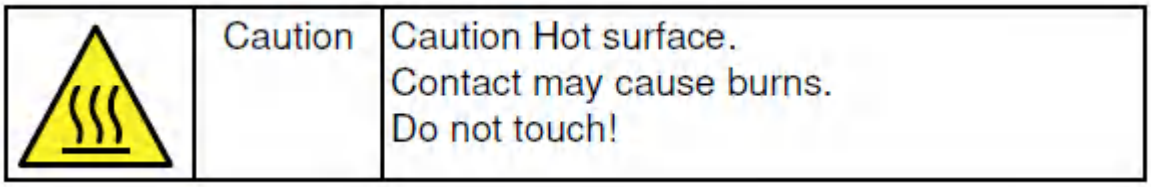
- Ethernet
  - 4x 10/100/1000Mbps - SGMII ports (VSC8514XMK-11)
- Board ID EEPROM
- Programmable Clock Generator

The orderable part number is provided in the table below:

Jacinto7 EVM Add-on Module	
Quad Port Ethernet Expansion	J721EXENETXPANEVM

1.2 Thermal Compliance

There is elevated heat on the processor/heatsink: use caution, particularly at elevated ambient temperatures. Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink.



1.3 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). TI recommends that this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the build-up of ESD. TI also recommends using ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per EN IEC 61326-1:2021.

2 QP-ENET Board Identification and Installation

2.1 QP-ENET Board Component Identification

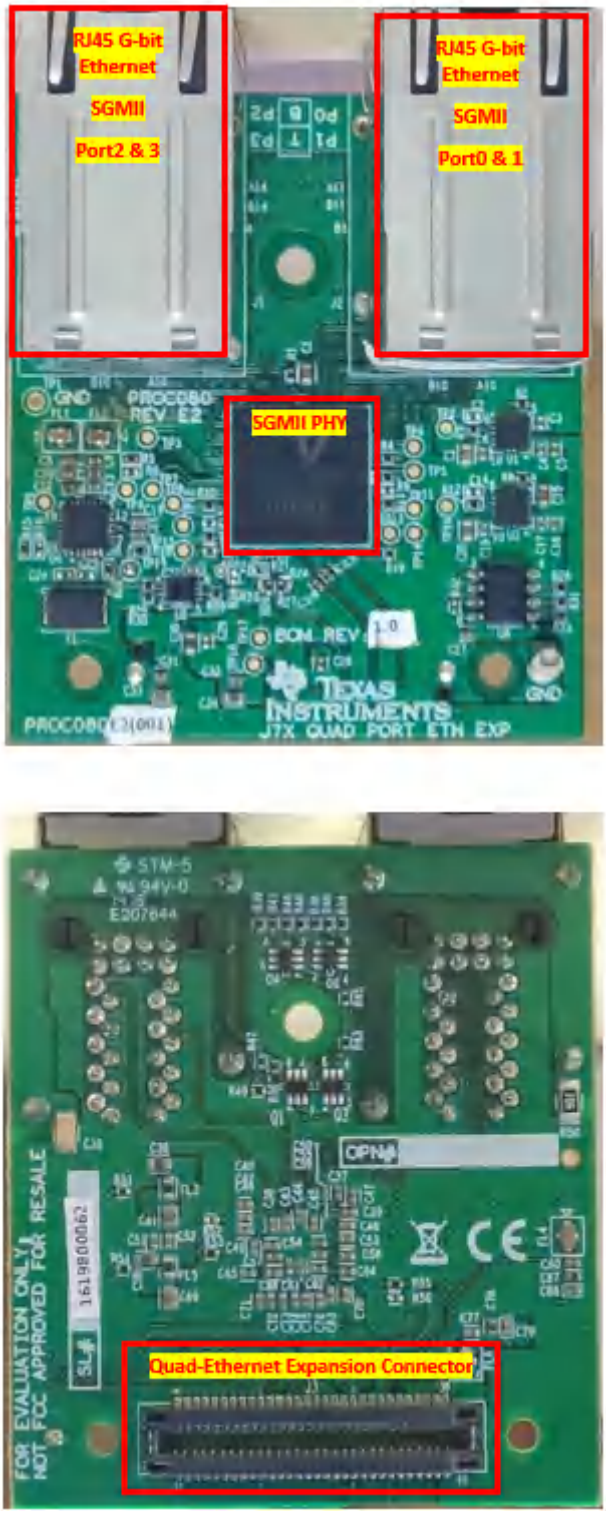


Figure 2-1. QP-ENET Expansion Board Component Identification

2.2 Interfacing QP-ENET Expansion Board with J784S4XG01EVM Board

QP-ENET Expansion boards shall be interfaced with Jacinto7 J784S4XG01EVM in bottom mating configurations. The images below show the J7AHP EVM board connectors **J51 and J52**, which mate with the QP-ENET board as an example, with expansion connectors **J3** on the QP-ENET mated to the SGMII Expansion connectors on the J7AHP EVM. It is valid to support/install on only one QP-ENET board, and in either location.

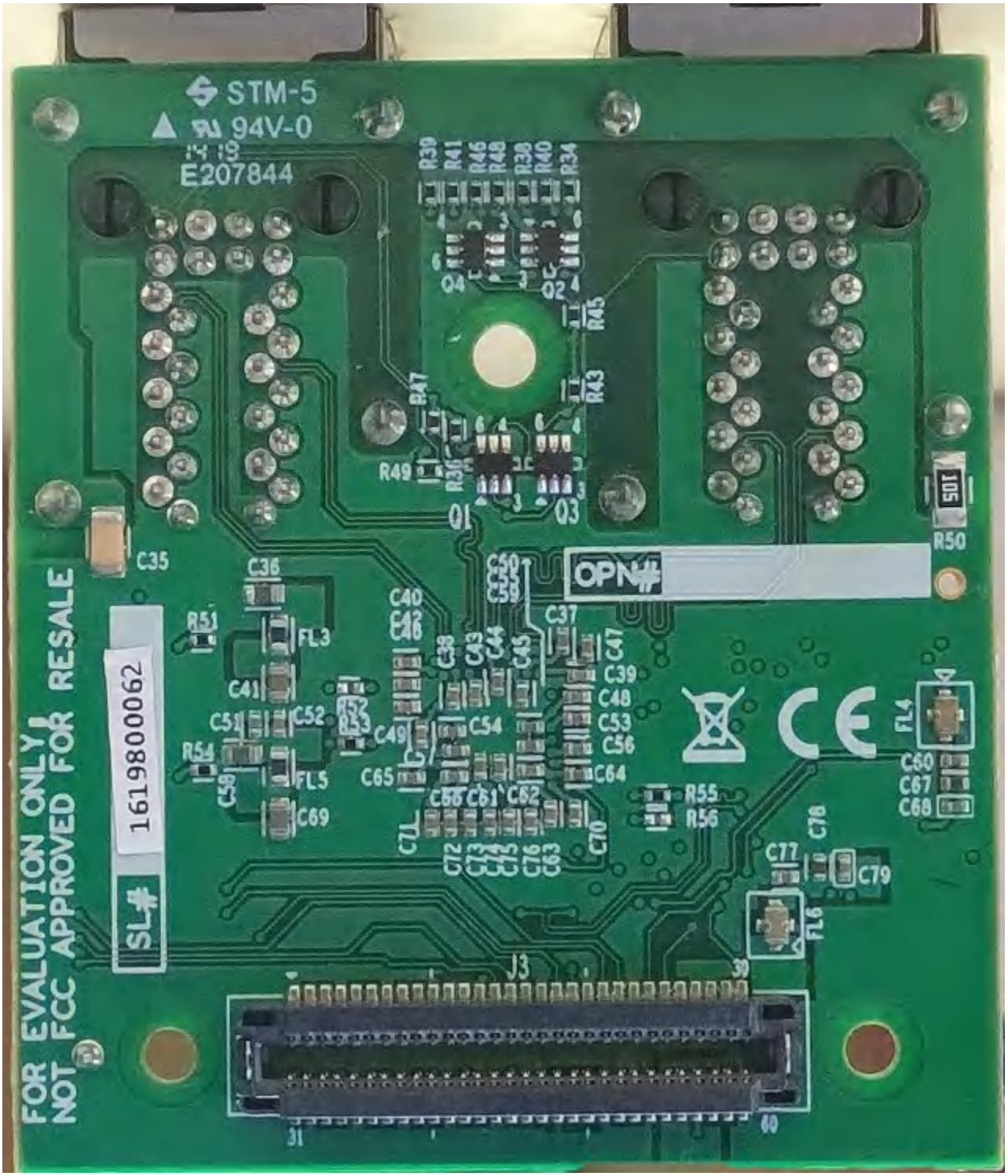


Figure 2-2. QP-ENET Expansion Board Bottom Side

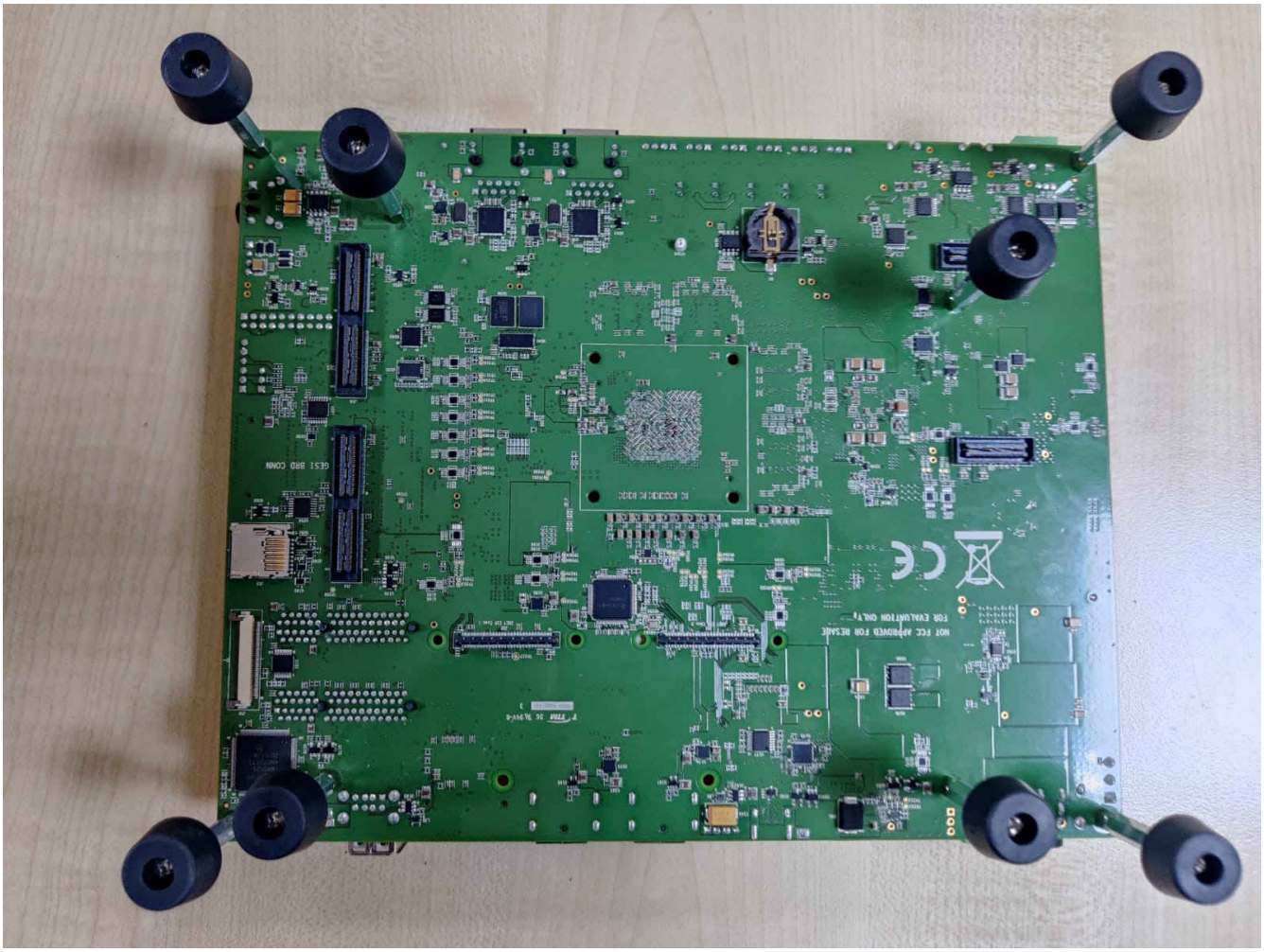


Figure 2-3. Q/SGMII Expansion Connector on J784S4XG01EVM Bottom Side

2.2.1 Detailed Board Assembly Procedure (J784S4XG01EVM)

This assembly procedure example is given for mating the QP-ENET board with the J784S4XG01EVM board.

1. Take the Assembled J784S4XG01EVM Board
2. Add M2.5 x 5mm hex spacers on each mounting holes provided on either sides of the J51 & J52 connector of the J784S4XG01EVM and secure it with M2.5 x 4 mm Phillips screws from the bottom sides to hold the spacer in place.
3. Add M3 x 12mm Phillips screws through the mounting hole provided between the Ethernet connectors on the QP ENET board (shown in the picture below) and secure it with a M3 x 5mm hex spacer from the other side (this step is done only on the QP ENET board).
4. Mount the QP board onto the J784S4XG01EVM connectors J51 & J52, making sure the connectors are seated evenly.
5. Add M2.5 x 4 mm Phillips screws from the top side of the QP to secure the QP mating with the J784S4XG01EVM board.
6. Add the M2.5 x 5 mm male to male spacer from the top side of the J784S4XG01EVM board to secure the remaining M3 screw protruding from the QP.
7. Add a M3 x 5mm spacer from the top side of the J784S4XG01EVM board to lock the other end of the M3 x12mm Phillips screw.

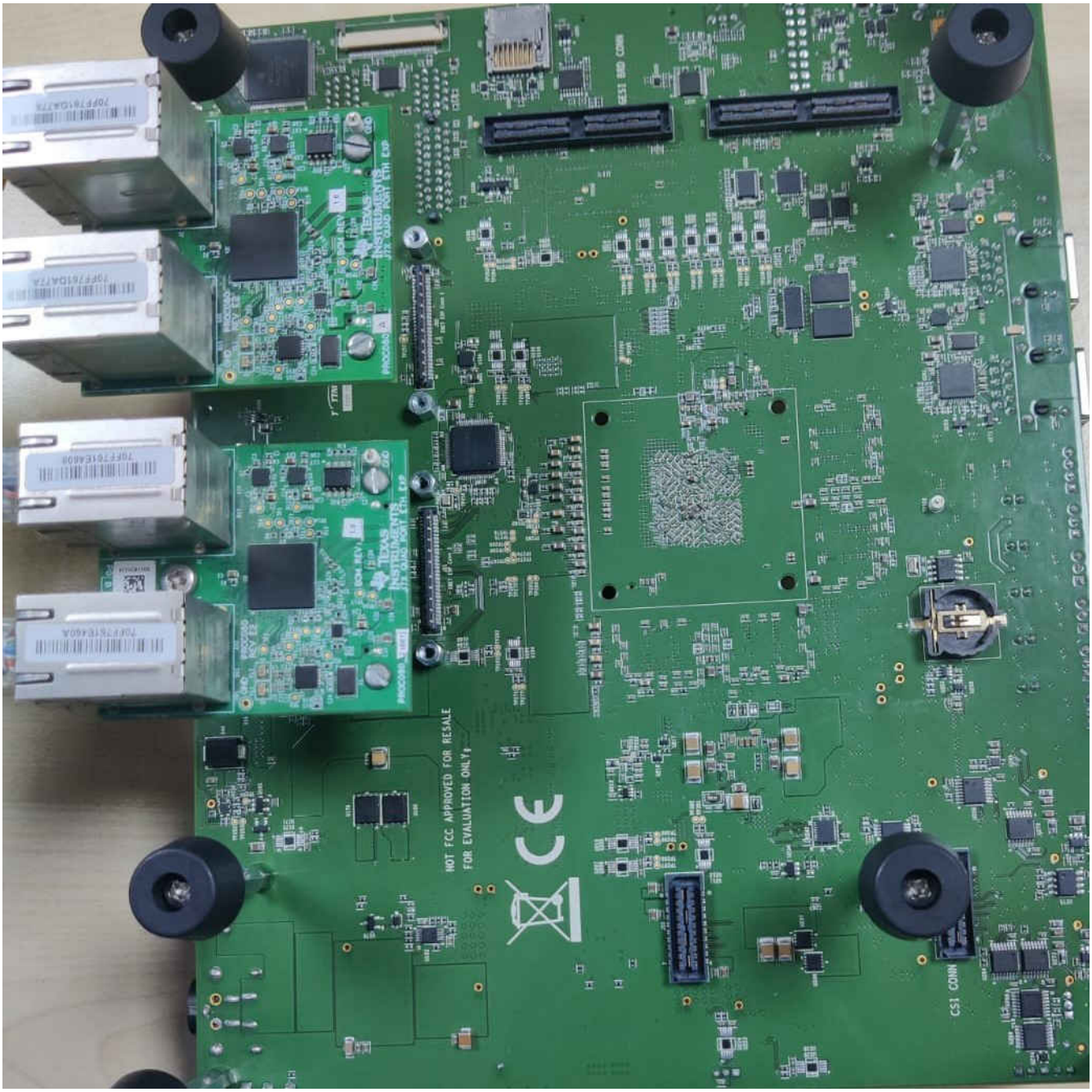


Figure 2-4. QP ENET Board

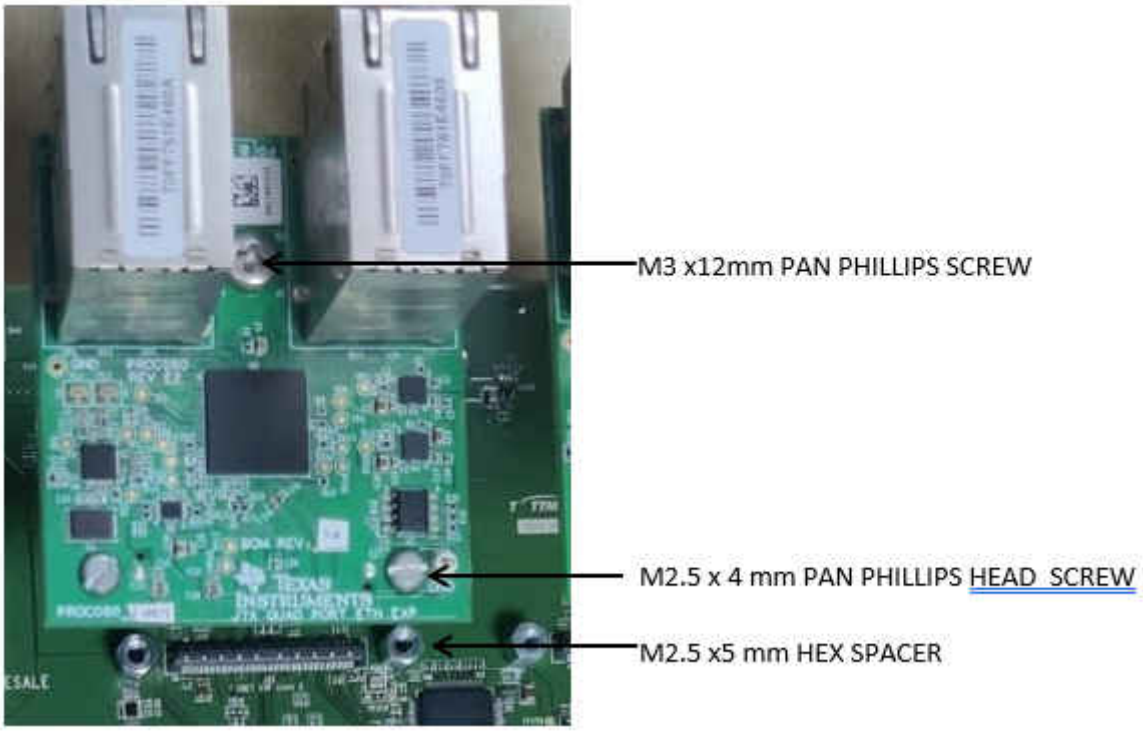


Figure 2-5. Bottom Side of J784S4XG01EVM

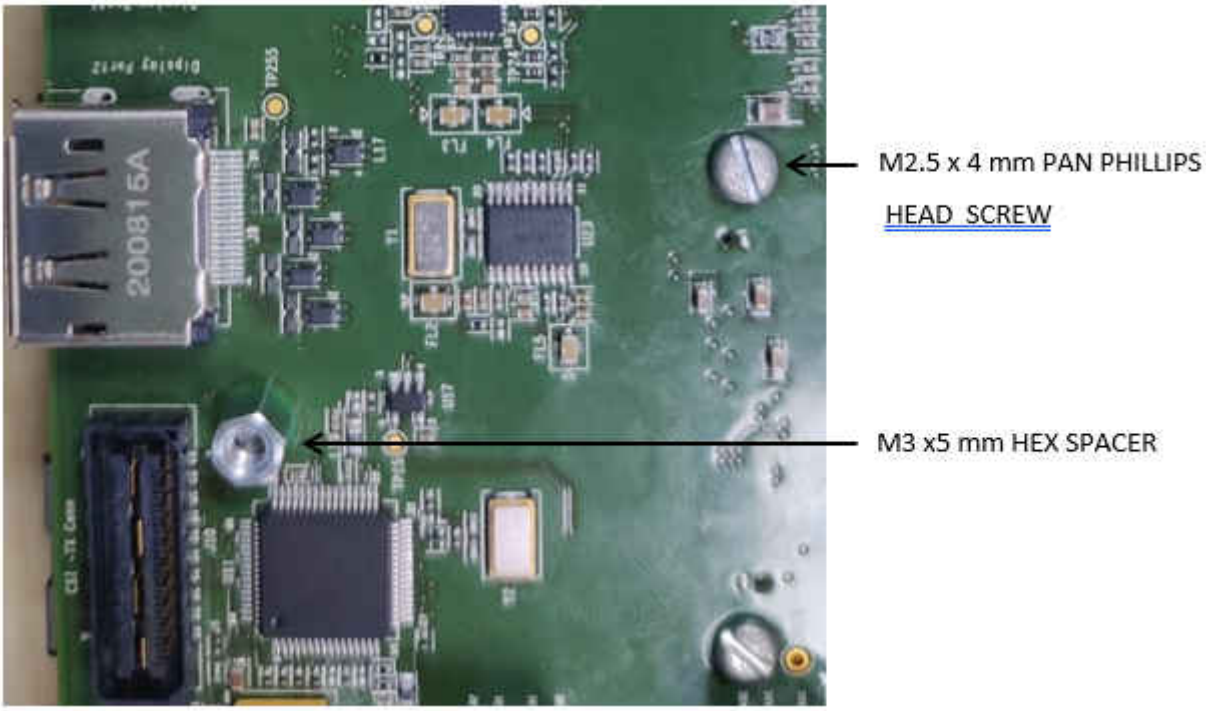


Figure 2-6. Top Side of J784S4XG01EVM

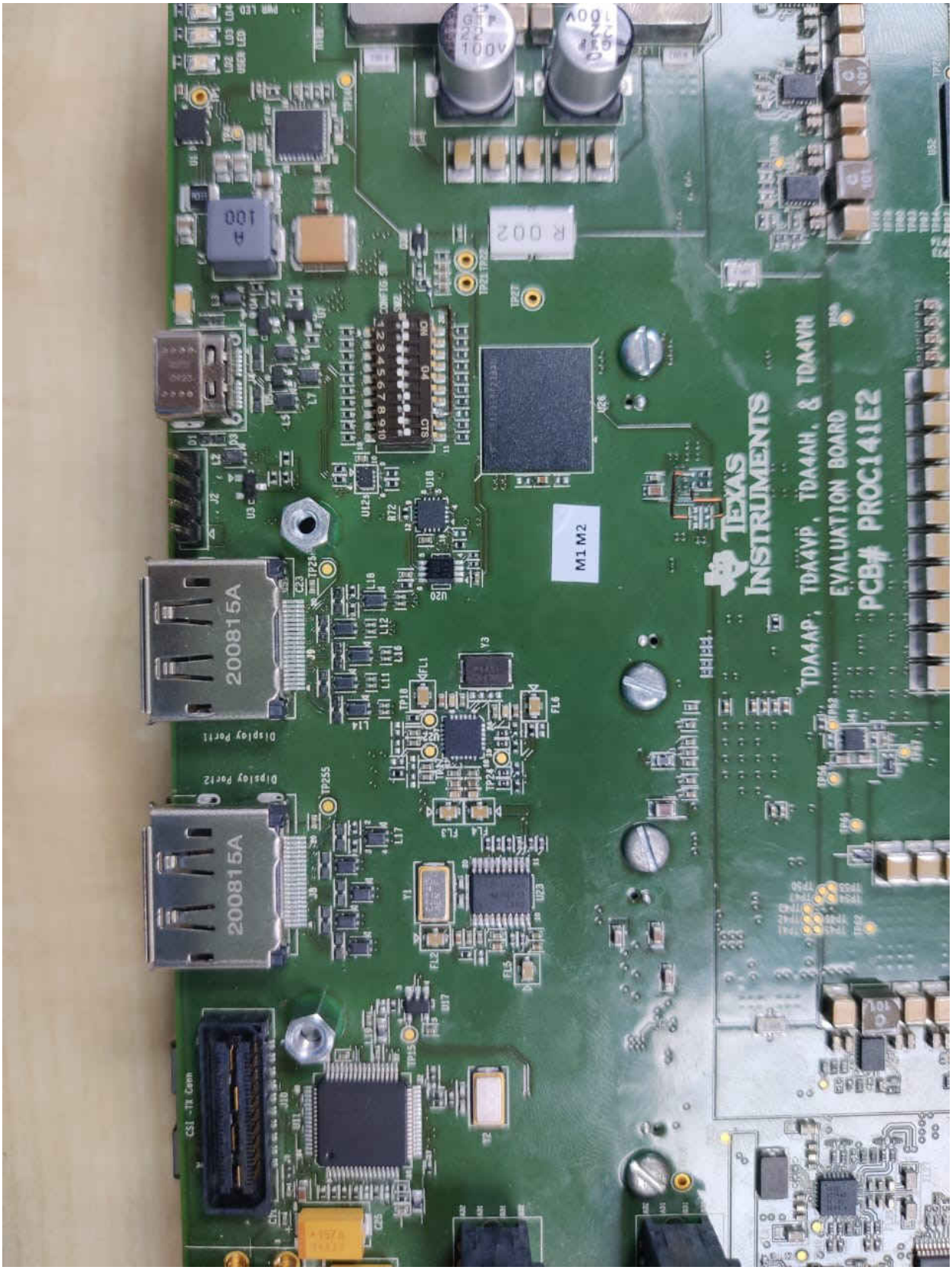


Figure 2-7. J784S4XG01EVM - QP ENET Board Assembly Procedure

3 QP-ENET Expansion Board Hardware Architecture

This section explains the Hardware Architecture of QP-ENET Expansion Board in detail.

3.1 QP-ENET Expansion Board Hardware Top Level Diagram

The generic functional block diagram of the QP-ENET Expansion Board is shown below.

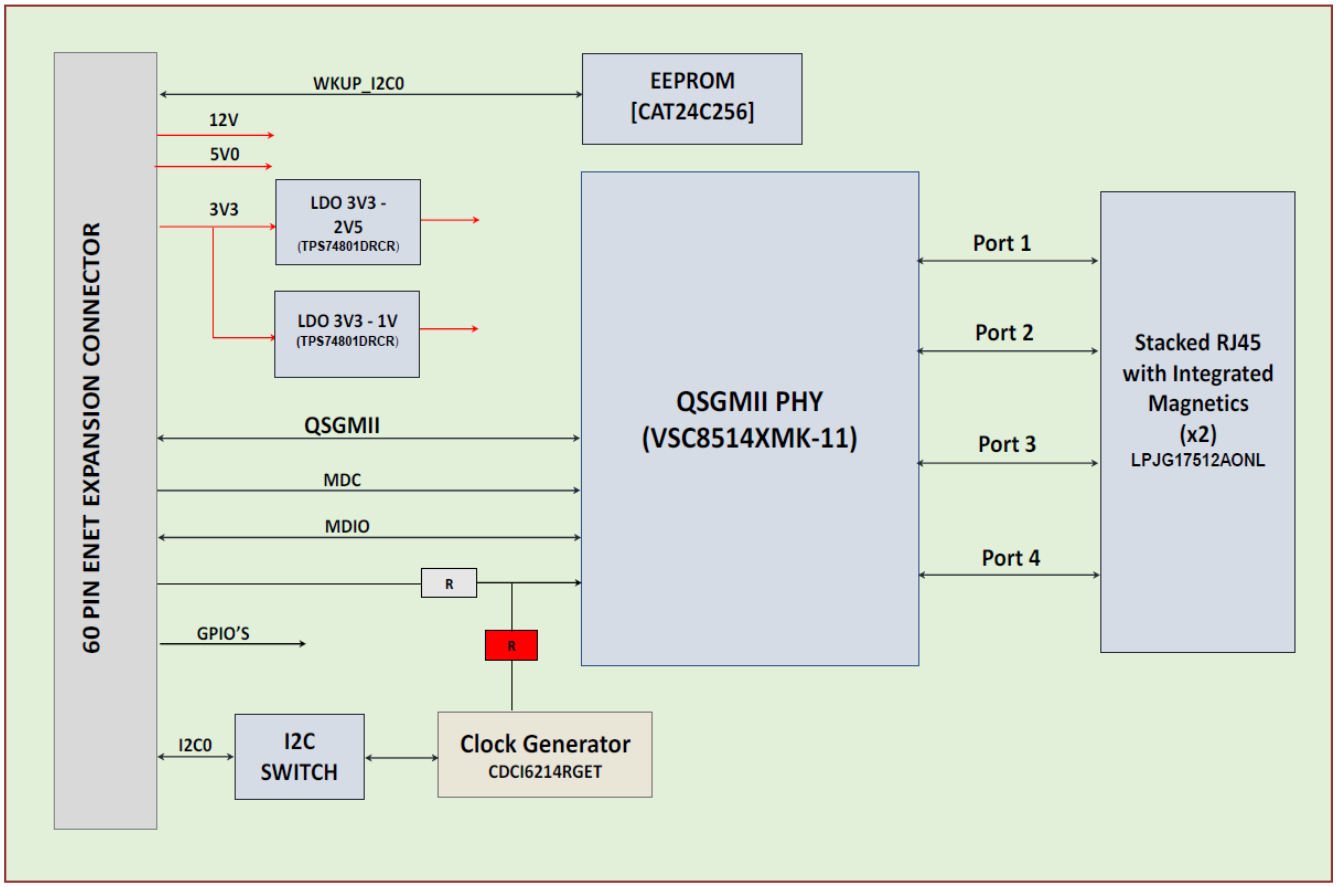


Figure 3-1. Functional Block Diagram of QP-ENET Expansion Board

3.2 Expansion Connectors

The J784S4XG01EVM board includes two Serial Ethernet Expansion connectors of 171446-1109 with 5-mm mating height, allowing the ENET expansion board (Quad-Port Ethernet Expansion) to be stacked on bottom side of the board.

This section provides an overview of the different interfaces and circuits on the Quad port Ethernet Expansion Board. The following table contains the Pin out/Signal mapping for the ENET Expansion connector.

Table 3-1. ENET Expansion Connector J3 Pinouts

PIN	Net Name	PIN	Net Name
1	DGND	31	QSGMII_INTN
2	NC	32	DGND
3	NC	33	QSGMII4_TX_P
4	DGND	34	QSGMII4_TX_N
5	NC	35	DGND
6	NC	36	QSGMII4_RX_P
7	DGND	37	QSGMII4_RX_N
8	NC	38	DGND
9	NC	39	QSGMII_PHY_REFCLK_N

Table 3-1. ENET Expansion Connector J3 Pinouts (continued)

PIN	Net Name	PIN	Net Name
10	DGND	40	QSGMII_PHY_REFCLK_P
11	VSYS_IO_3V3	41	DGND
12	VSYS_IO_3V3	42	QSGMII_MDC
13	DGND	43	QSGMII_MDIO
14	EEPROM_A0	44	DGND
15	EEPROM_A1	45	QSGMII_RESETN
16	EEPROM_A2	46	CDCI_I2C_SEL
17	DGND	47	ENET_EXP_SPARE
18	EEPROM_WP	48	DGND
19	REFCLK_25MHZ	49	VSYS_5V0
20	DGND	50	VSYS_5V0
21	WKUP_I2C0_SCL	51	DGND
22	WKUP_I2C0_SDA	52	NC
23	DGND	53	NC
24	I2C0_SCL	54	DGND
25	I2C0_SDA	55	VCC_3V3
26	DGND	56	VCC_3V3
27	VCC_12V0	57	DGND
28	VCC_12V0	58	NC
29	DGND	59	NC
30	ENET_EXP_PWRDN	60	DGND
SH1	DGND	SH2	DGND

3.3 Board ID EEPROM

The Quad port Ethernet Expansion Board is identified by its version and serial number, which are stored in the onboard EEPROM. On the J784S4XG01EVM, there are two QP-ENET expansion connectors available: one QP-ENET is set to address 0x54, the other one is set to 0x51, which are accessible on WKUP_I2C0.

The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

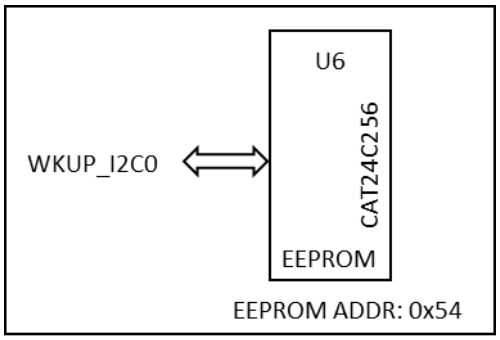


Figure 3-2. Board ID EEPROM

Table 3-2. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Description
	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	Payload type

Table 3-2. Board ID Memory Header Information (continued)

Header	Field Name	Size (bytes)	Description
	Length	2	Offset to next header
	Board_Name	16	Name of the board
	Design_Rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	First software release number
	VendorID	2	Vendor ID
	Build_Week	2	Week of the year of production
	Build_Year	2	Year of production
	BoardID	6	Reserved. Not populated with any value
	Serial_Nbr	4	Incrementing board number
MAC_ADDR	TYPE	1	payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_addrs	192	MAC address Contains 5 valid MAC addresses. Four MAC addresses for RGMII ports and one MAC address for RMII port.
END_LIST	TYPE	1	End Marker

These board ID details are programmed on the EEPROM from the address 0x0h.

3.4 Ethernet Interface

The Jacinto7 EVM – QP-ENET Expansion board provides an option for users to validate the Jacinto7 SoC's SGMII controllers.

The J7 EVM includes an SGMII connection between the VSC8514XMK Quad Port SGMII PHY and the network subsystem (NSS) of the processor. One channel of SGMII interfaces from the SERDES domain of the J7 processor used on the QP ENET board.

3.4.1 Quad Port SGMII PHY Default Configuration

The QP-ENET uses the PHY of the 138-pin QFN package, designated with the XMK suffix, which supports only the SGMII interface.

The VC8514 device includes three external PHY address pins, PHYADD [4:2] to allow control of multiple PHY devices on a system board sharing a common management bus. These pins set the most significant bits of the PHY address port map. The lower two bits of the address for each port are derived from the physical address of the port (0 to 3) and the setting of the PHY address reversal bit in register 20E1, bit 9.

Table 3-3. RGMII PHY Strap Configuration

Ports	SGMII Port1	SGMII Port2	SGMII Port3	SGMII Port4
Connectors	**J1A**	**J1B**	**J2A**	**J2B**
PHY Address	10010	10011	10000	10001
Auto Negotiation	Enabled	Enabled	Enabled	Enabled
ANEGSel	10/100/1000	10/100/1000	10/100/1000	10/100/1000
CLK_SQUELCH	No RCVRD Clock	No RCVRD Clock	No RCVRD Clock	No RCVRD Clock

3.4.2 SGMII Clocking Scheme

3.4.2.1 Main Clock

The reference clock to the PHY is generated from TI's Clock Generator Mfr. Part Number# CDCI6214RGET, which is placed on the J7AHP EVM Board. Clock inputs are AC coupled and LVDS compliant. The clock generator can be configured by I2C0 of the J7AHP SoC. The I2C address of this clock generator is 0x77.

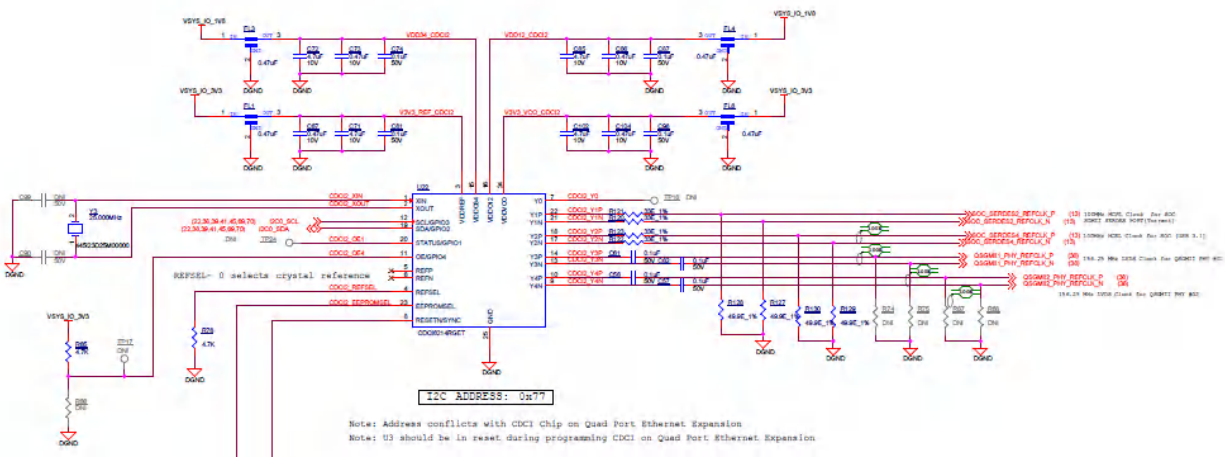


Figure 3-3. Default Clock Source on J7AHP EVM Board

3.4.2.2 Optional Clock

Optionally, the reference clock can be supplied by the SERDES clock generator Mfr. Part Number# CDCI6214RGET located on QP-ENET Board, which can be configured by I2C0 of the J7 SOC. The I2C address of this clock generator is 0x77, and this address conflicts with the CDCI Chip on EVM Boards. An I2C switch on the Quad port Ethernet Expansion Board is used to remove the address conflict by connecting any one of the clock generators.

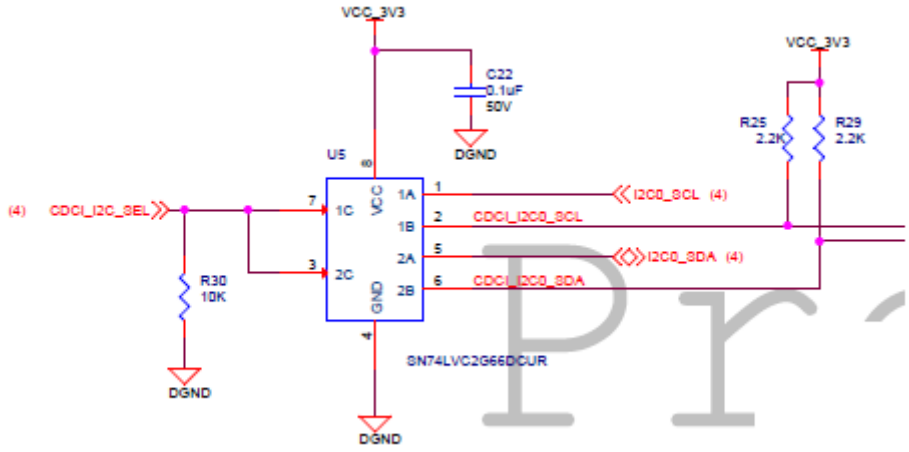


Figure 3-4. Clock Source I2C MUX

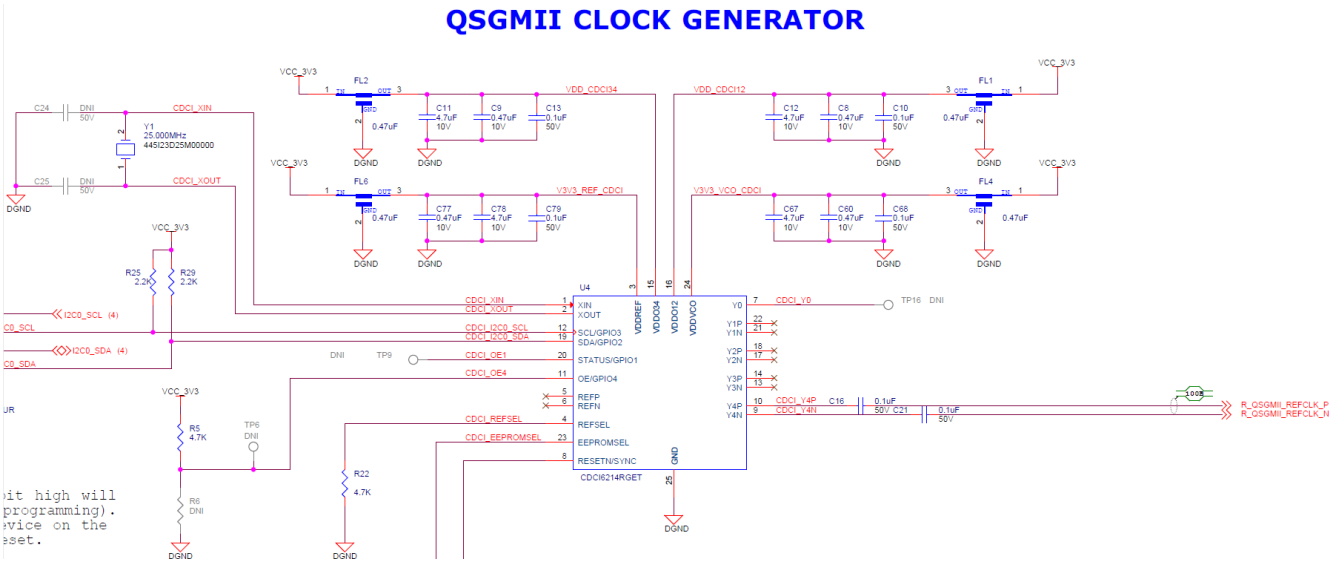


Figure 3-5. QP-ENET Optional Clock Source

Setting the CDCI_I2C_SEL IO EXP bit high will connect the I2C bus to CDCI (for programming) on the Quad Port Ethernet Expansion Board. During this time, the CDCI device on the EVM boards should be in reset mode. Also, there are resistor options provided that must be adjusted to reflect any change in source clock selection; this is given in the following images.

CLOCK SOURCE SELECTION

	Install	Remove	
From on board Clock Generator	R3,R4	R1,R2	
From CP Board	R1,R2	R3,R4	(default)

Figure 3-6. SGMII PHY Clock Input Source Path Selection

Reference Clock Selection

REFCLK_SEL1	REFCLK_SEL0	Frequency
0	0	125MHz
1	0	156.25MHz (default)

Figure 3-7. SGMII PHY Clock Configuration

3.4.3 Ethernet Port LED Indication

The following table shows the LED function of the SGMII ports RJ45 connectors. The Right LED gives the indication of link status and collision presence; if the LED is turned OFF then its means that the link is established in half-duplex mode, or no link established. If the LED is turned ON then the link is established in full-duplex mode. If the LED is blinking or pulse-stretching, then it means the link is established in half-duplex mode but collisions are present. The Left LED gives speed and activity status; if LED is blinking or pulse-stretching it denotes link activity and if not then no activity.

Table 3-4. SGMII Ports LED Function

RGMII Port RJ45-LED	FUNCTION
RIGHT - YELLOW	Duplex/Collision
LEFT - GREEN	10/1000Mbps Speed/Activity
LEFT - ORANGE	100Mbps Speed/Activity

3.4.4 Reset and Power-down Signals

The Reset signal on QP-ENET, QSGMII_RESETz is a reset signal sourced from EVM boards. This signal is used to reset the QSGMII PHY on the board.

QSGMII_RESETz is an AND output of the SOC PORz signal and ENET reset signal. The ENET reset signal is asserted by an I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) on the EVM boards.

The Power-down signal on QP-ENET, ENET_EXP_PWRDN is given by the I2C GPIO Expander2 (I2C ADD# 0x22, I2C0) on the EVM boards; this signal is used to put SGMII PHY on the QP-ENET board to inactive state. By default, this signal has a pull-up on the EVM board, i.e. the PHY is in active state all the time unless low is asserted on this signal.

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial Release

A Appendix

A.1 Appendix – I (Interface Mapping)

J721EXSOMG01EVM, J7200XSOMG01EVM, and J784S4XG01EVM Interface Mapping on QP-ENET Expansion is provided in the following table.

Table A-1. Interface Mapping

QP-ENET Peripheral	QP-ENET Interface	J721EXSOMG01EVM Connectivity	J7200XSOMG01EVM Connectivity	J784S4XG01EVM Connectivity
SGMII(U2)	SERDES Signals	SERDES0_TX/RX1 Port	SERDES0_TX/RX2 Port	SERDES2_TX/RX2 on ENET Conn1 , SERDES2_TX/RX3 on ENET Conn2
	MDIO Signals	MDIO0	MDIO0	MDIO1
Board ID EEPROM (U6)	Configuration I2C	WKUP_I2C0	WKUP_I2C0	WKUP_I2C0
CLOCK GENERATOR(U4)	Configuration I2C	I2C0	I2C0	I2C0

A.2 Appendix – II (QP-ENET Board GPIO Mapping)

QP-ENET GPIO Mapping is shown in the following table.

Table A-2. QP-ENET GPIO Mapping

QP-ENET Peripheral	Peripheral IO	Direction (for SoC)	Default	Active State	J721EXSOMG01EVM Connectivity	J7200XSOMG01EVM Connectivity	J784S4XG01EVM Connectivity
SGMII Port 0, Port1 Port 2 & Port3	Interrupt	Input	PU	Active Low	GPIO1_22	GPIO0_4	WKUP_GPIO0_84, WKUP_GPIO0_85
	Power Down	Output	PU	Active High	I2C GPIO EXPANDER2(U31.P20 , I2C0)	I2C GPIO EXPANDER2(U31.P20 , I2C0)	I2C GPIO EXPANDER2(U173.P20 , I2C0)
	Reset	Output	PD	Active Low	I2C GPIO EXPANDER2(U31.P21 , I2C0)	I2C GPIO EXPANDER2(U31.P21 , I2C0)	I2C GPIO EXPANDER2(U173.P20 , I2C0), I2C GPIO EXPANDER2(U173.P11 , I2C0)
	I2C MUX select	Output	PD	Select Signal	I2C GPIO EXPANDER2(U31.P22 , I2C0)	I2C GPIO EXPANDER2(U31.P22 , I2C0)	I2C GPIO EXPANDER2(U173.P22 , I2C0), I2C GPIO EXPANDER2(U173.P01 , I2C0)
	Spare GPIO	Input/ Output	NA	NA	I2C GPIO EXPANDER2(U31.P23 , I2C0)	I2C GPIO EXPANDER2(U31.P23 , I2C0)	I2C GPIO EXPANDER2(U173.P23 , I2C0), I2C GPIO EXPANDER2(U173.P12 , I2C0),

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