EVM User's Guide: TMDS273EVM, TMDS273GPEVM, TPR12REVM

AM273x Evaluation Module

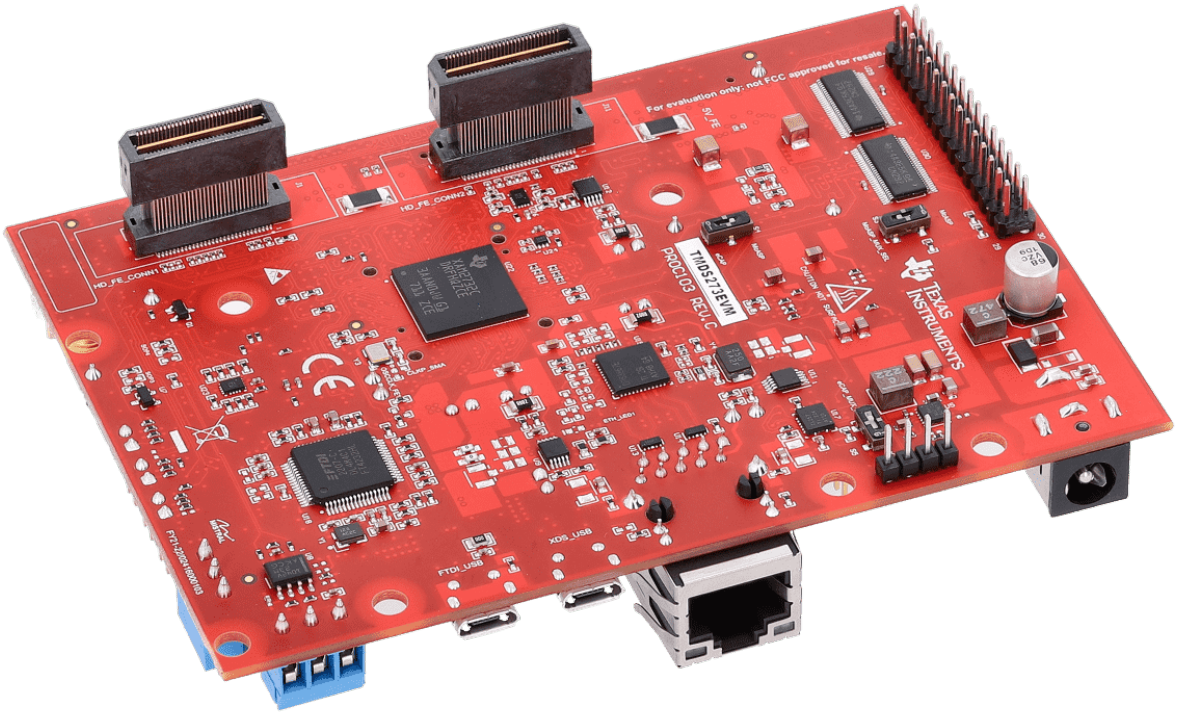
Description

The AM273x evaluation module (EVM) is a standalone test, development and evaluation platform that lets developers evaluate AM273x functionality and develop prototypes for a variety of applications.

The TMDS273EVM is equipped with a Sitara™ AM2732 microcontroller along with additional components to allow the user to make use of the various device interfaces including the CSI-2 RX, Ethernet™, dual CAN-FD and others to easily create prototypes. Onboard current measurement capabilities are available to monitor power consumption for power-conscious applications. The supplied USB cable paired with embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ (CCSTUDIO).

Features

- RJ45 Ethernet port capable of 100Mb or 10Mb speeds
- Dual CAN-FD interfaces
- Onboard XDS-110 emulator
- Onboard power measurement capabilities
- Contains AM2732 HS-FS device



TMDS273EVM

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1 Evaluation Module Overview

1.1 Introduction

The AM273xEVM is an evaluation module designed to develop software and evaluate the AM273x Radar Controller and Processor SoC from Texas Instruments. The AM273x is a multicore SoC designed to provide an integrated control and processing platform for TI AWR mmWave radar front-end devices in both single-device and cascaded modes of operation. The signal interface between the AM273x EVM and the AWR2243BOOST mmWave Radar EVM uses the 60-pin Samtec high density connector.

1.2 Preface: Read This First

1.2.1 If You Need Assistance

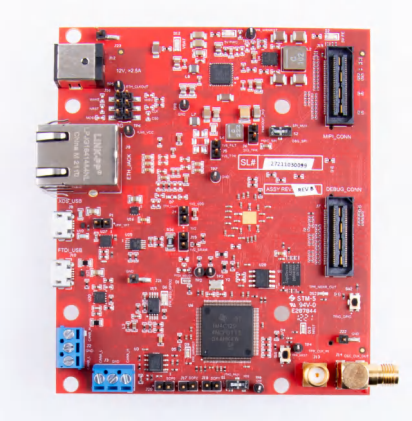
If you have any feedback or questions, support for Sitara MCUs and the AM273x EVM development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website.

1.2.2 Important Usage Notes

Note

A 12V, > 2.5A supply brick with a 2.1mm barrel jack (center positive) is not included in the kit and must be ordered separately. For more information on power requirements, go to Section 2.1.1.

1.3 Kit Overview



1.3.1 Kit Contents

The Sitara AM273x EVM Development Kit contains the following items:

- AM273x EVM
- Micro USB cable
- Ethernet Cable
- Samtec coax micro ribbon cable (HQCD-030-02.00-SEU-TBR-1)
- Spacers, screws, and washers

Note

The maximum length of the IO cables shall not exceed 3 meters.

1.3.2 Key Features

- Dual 60-pin high density (HD) connector interface with TI's front end radar device EVMs, such as the AWR2243BOOST
- XDS110-based JTAG emulation with Serial port for onboard QSPI flash programming
- UART to USB Debug port for terminal access using FT4232H
- External JTAG/ Emulator Interface with TRACE support over 60-pin MIPI connector
- Debug, SPI, I2C, and LVDS connected to 60-pin Debug connector
- Ethernet interface to stream the captured data over the network to the host PC
- Dual On-board CAN-FD transceiver
- One button and LED for basic user interface
- 12V power jack to power the board

1.3.3 Component Identification

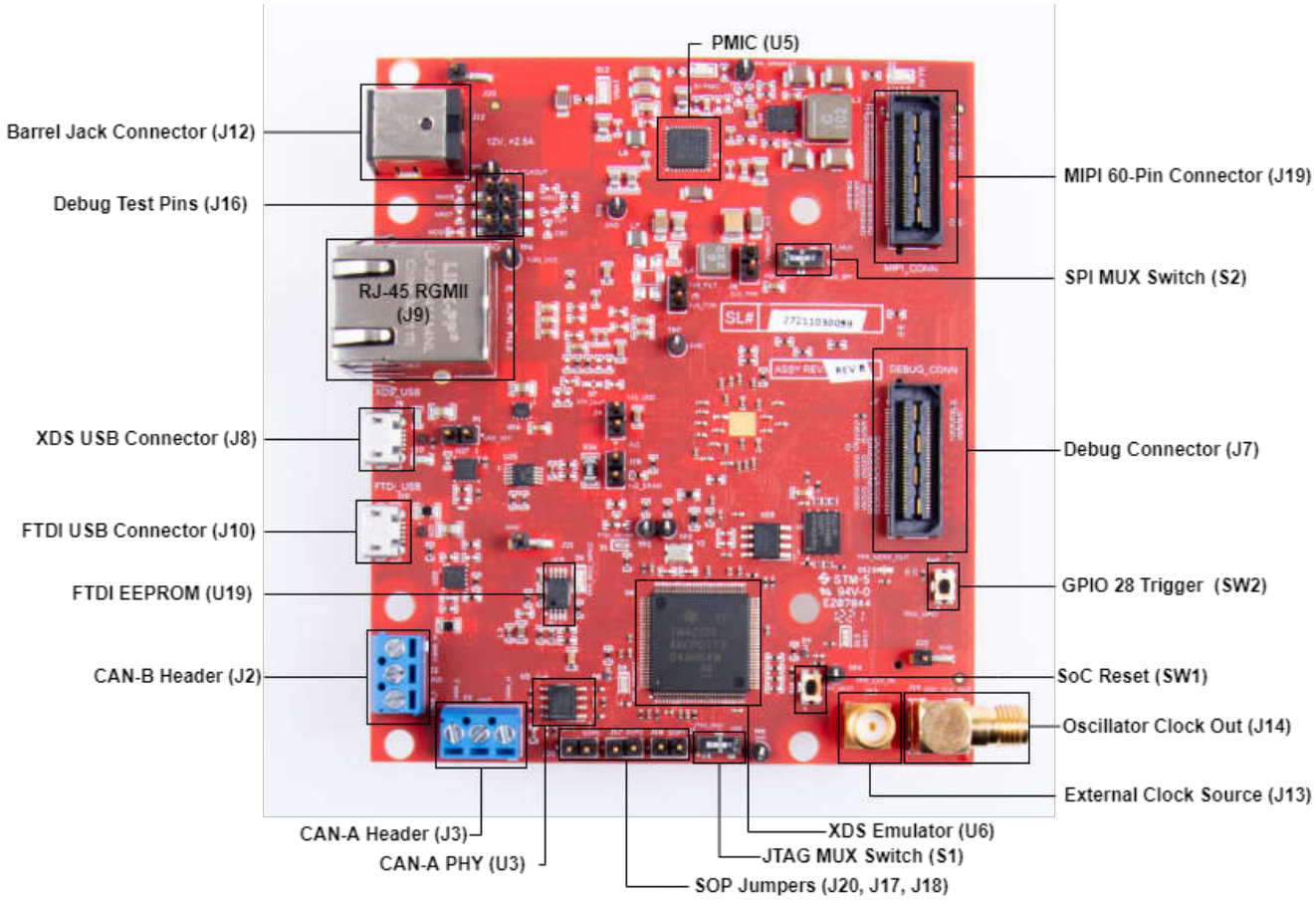


Figure 1-1. AM273x EVM Top Component Identification

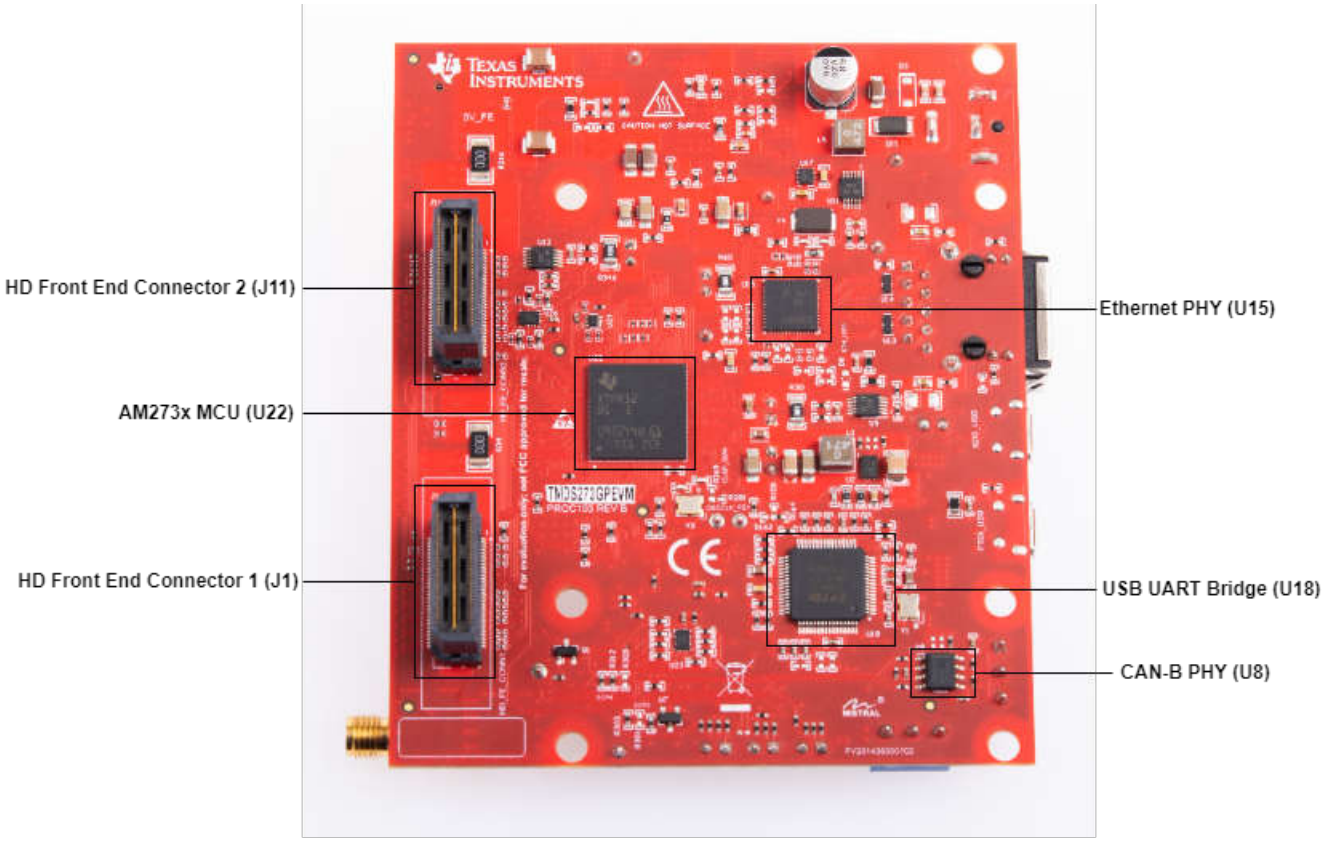


Figure 1-2. AM273x EVM Bottom Component Identification

1.3.4 Daughter Cards

The AM273x EVM development kit provides an easy and inexpensive way to develop applications with the AM273x Series microcontroller. Daughter cards are add-on boards that follow a pin-out standard created by Texas Instruments. The TI and third-party ecosystem of daughter cards greatly expands the peripherals and potential applications that you can easily explore with the AM273x EVM.

1.3.4.1 Connecting the AM273x EVM to the AWR2243BOOST EVM

The AM273x EVM can be connected to the AWR2243BOOST EVM for developing a complete radar system with front end and processor.

1.3.4.2 Connecting the AM273x EVM to the DCA1000

The AM273x EVM can be connected to the DCA1000 FGPA platform to allow for LVDS data streaming.

AM273x EVM and DCA1000 EVM can be connected with the help of a Samtec ribbon cable connected between Debug Connector J7 (see Table 2-14) on the AM273x EVM and DCA1000EVM 60-pin connector, as shown in Figure 1-3.

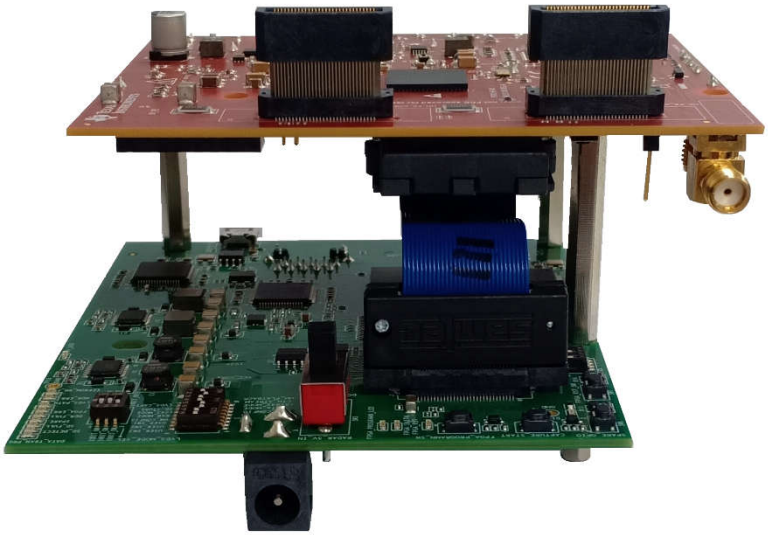


Figure 1-3. Interfacing DCA1000 EVM to Debug Connector of the AM273x EVM

1.3.5 Security

The AM273x EVM can have a Non-Secure (GP or General Purpose) or a Secure device (HS-FS). To determine if the device is secure, refer to field parameter for security: "y" of the Device name. If the Security Parameter is "H", then the device is a Secure device.

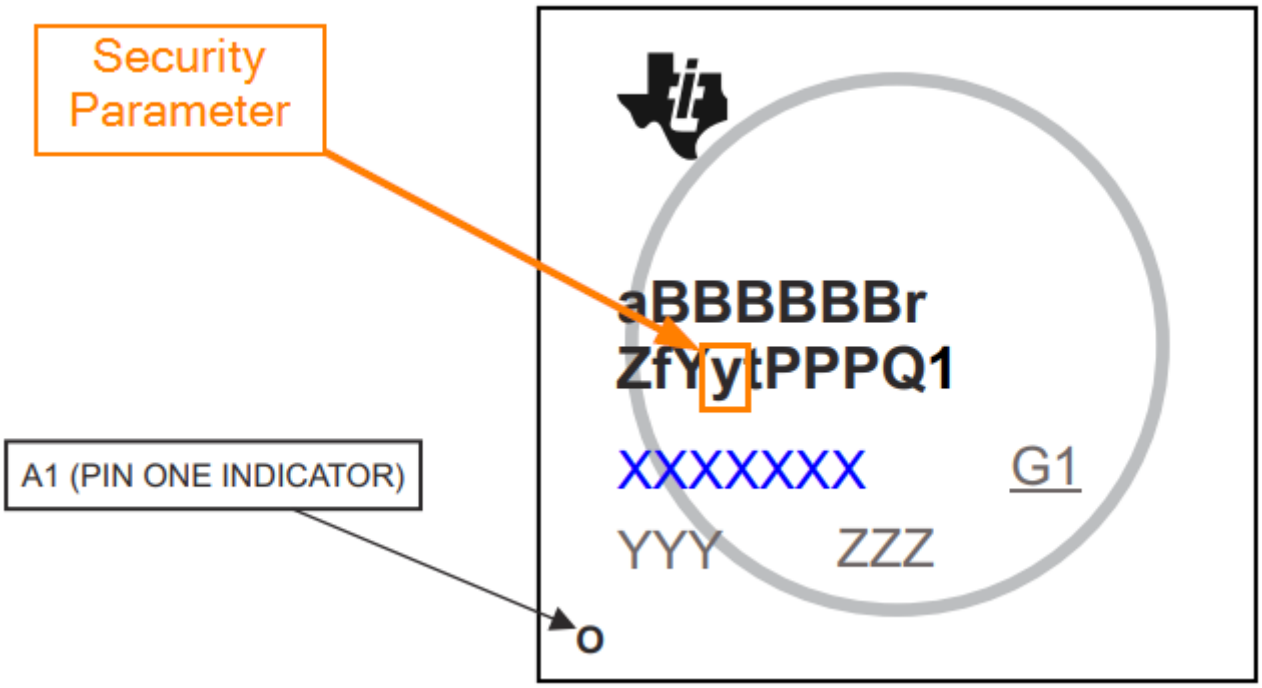


Figure 1-4. Security Field Parameter

The AM273x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted (optional) and signed using customer keys, which is verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security Subsystems and SoC Firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

1.3.6 Compliance

All components selected meet RoHS and REACH compliance.

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. An ESD controlled environment can include a temperature or humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection, such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment, such as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

2 Hardware

2.1 Board Setup

2.1.1 Power Requirements

The AM273x EVM is powered through a barrel jack connection. The power source must be capable of providing 2.5A at 12V. The length of the power cable must be < 3m.

External Power Supply or Power Accessory Requirements:

Nom Output Voltage: 12VDC

Max Output Current: 2500mA

Efficiency Level V

Note

TI recommends using an external power supply or power accessory which complies with applicable regional safety standards such as (by example) UL, CSA, CDE, CCC, PSE, etc.

The following power supply has been tested to work with the AM273x EVM:

https://www.digikey.in/product-detail/en/cui-inc/SDI65-12-U-P5/102-3417-ND/5277850

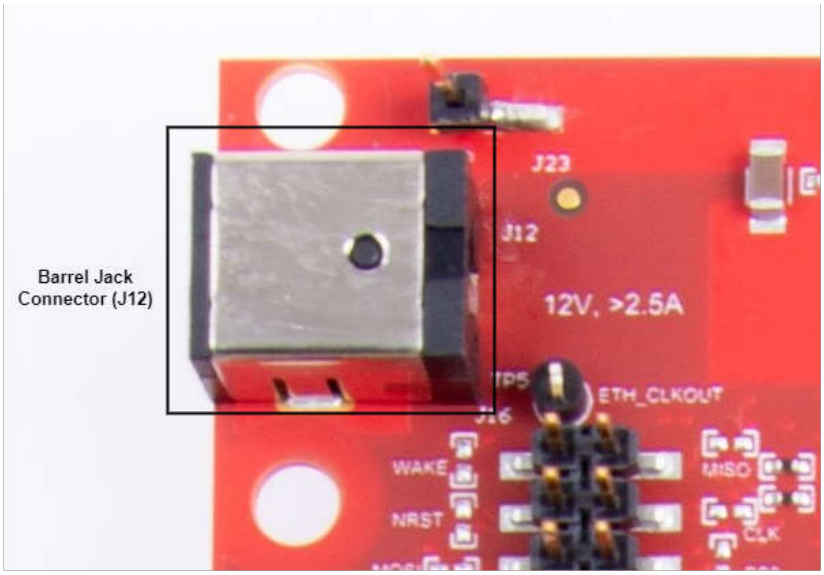


Figure 2-1. Barrel Jack Connector (J12)

The AM273x EVM includes a power design based on a power management integrated circuit (PMIC) to bring up the power rails according to the power on timing specifications and a LM61460 step-down converter to power the radar front end connector supplies

2.1.1.1 Power Status LEDs

Multiple power-indication LED's are provided on-board to indicate to users the output status of major supplies.

Table 2-1. Power Status LED's

Name	Default Status	Operation	Function
D12	ON	VBAT_INT	Power indicator for 12V barrel jack supply input
D16	ON	PMICOUT_5V0	Power indication for 5V PMIC output
D13	ON	nRESET	Indication of nRESET pin. If LED is glowing, the device is out of reset
D2	ON	5V_FE	Power indicator for 5V FE connectors

For further information on the TMDS273GPEVM LEDs, please see Section 2.1.4.

2.1.2 Push Buttons

The EVM supports two buttons that provide a reset and user input to the controller.

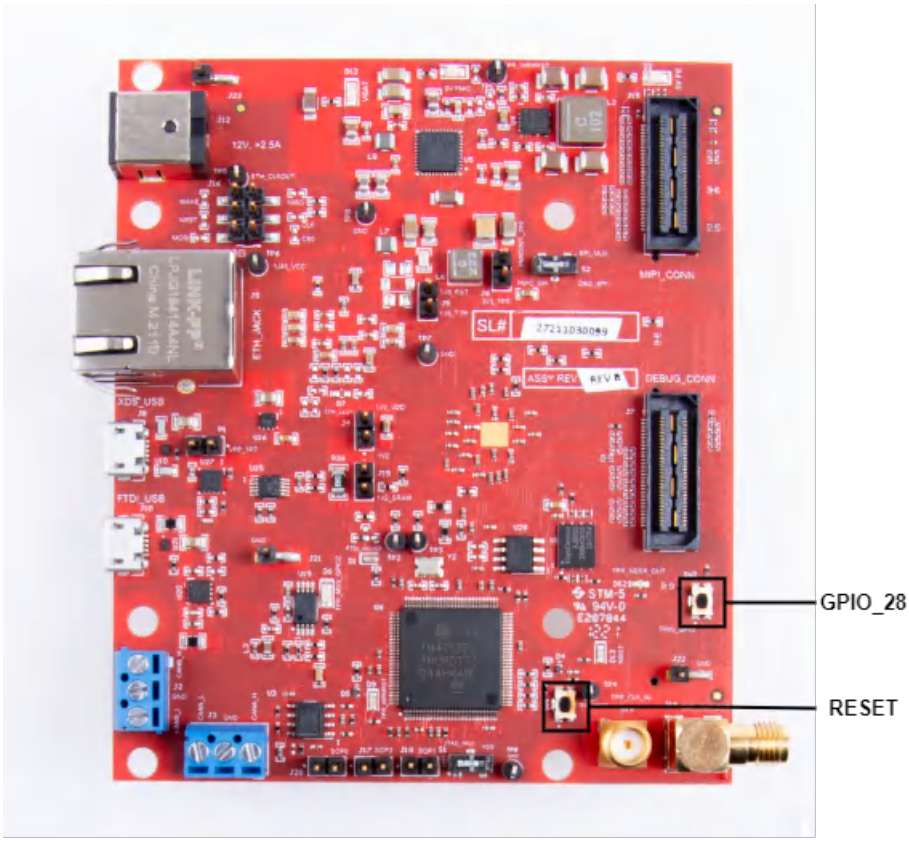
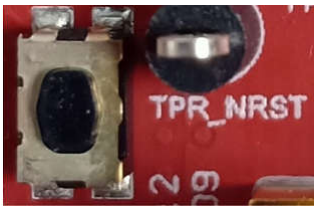


Figure 2-2. AM273x EVM Push Buttons

Table 2-2. EVM Push Buttons

Push Button	Signal	Function
SW1	TPR_NRST	AM273x, PMIC, and FTDI device reset
SW2	MSS_GPIO_28	User interrupt input

Table 2-3. Push Buttons Switches Information

Reference	Usage	Comments	Image
SW1	RESET	This Switch is used to RESET the AM2732, PMIC, and FTDI device.	
SW2	GPIO_28	When pushed, the GPIO_28 (net MSS_GPIO_28) is pulled high to PMICOUT_3V3. When idle (not pushed), GPIO_28 (net MSS_GPIO_28) is pulled to ground via a 10 kilo ohm resistor.	

2.1.3 Switches

The AM273x EVM contains two switches to mux various interfaces to different connectors on the EVM.

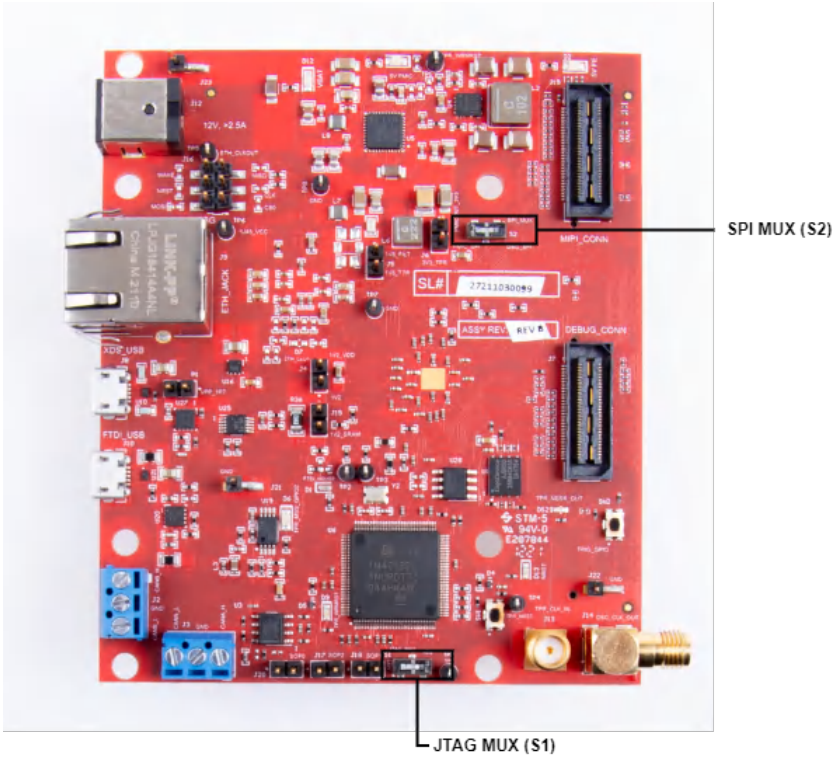


Figure 2-3. AM273x EVM Switches

Table 2-4. Switches Information

Reference	Usage	Comments	Image
S1	JTAG	When set to 'MIPI' position, the JTAG interface is routed to the MIPI 60-pin connector (J19). When set to 'XDS' position, the JTAG interface is routed to the XDS110 USB interface (J8).	
S2	SPI	When set to 'PMIC_SPI' position, the MSS_SPIB interface is routed to the PMIC and to the J16 header.(1) When set to 'DBG_SPI', the MSS_SPIB interface is routed to the 60-pin debug header (J7).	

(1) DNP resistors R5, R61, R167, and R176 must be populated to bring the MSS_SPIB interface out to the J16 header.

2.1.4 LEDs

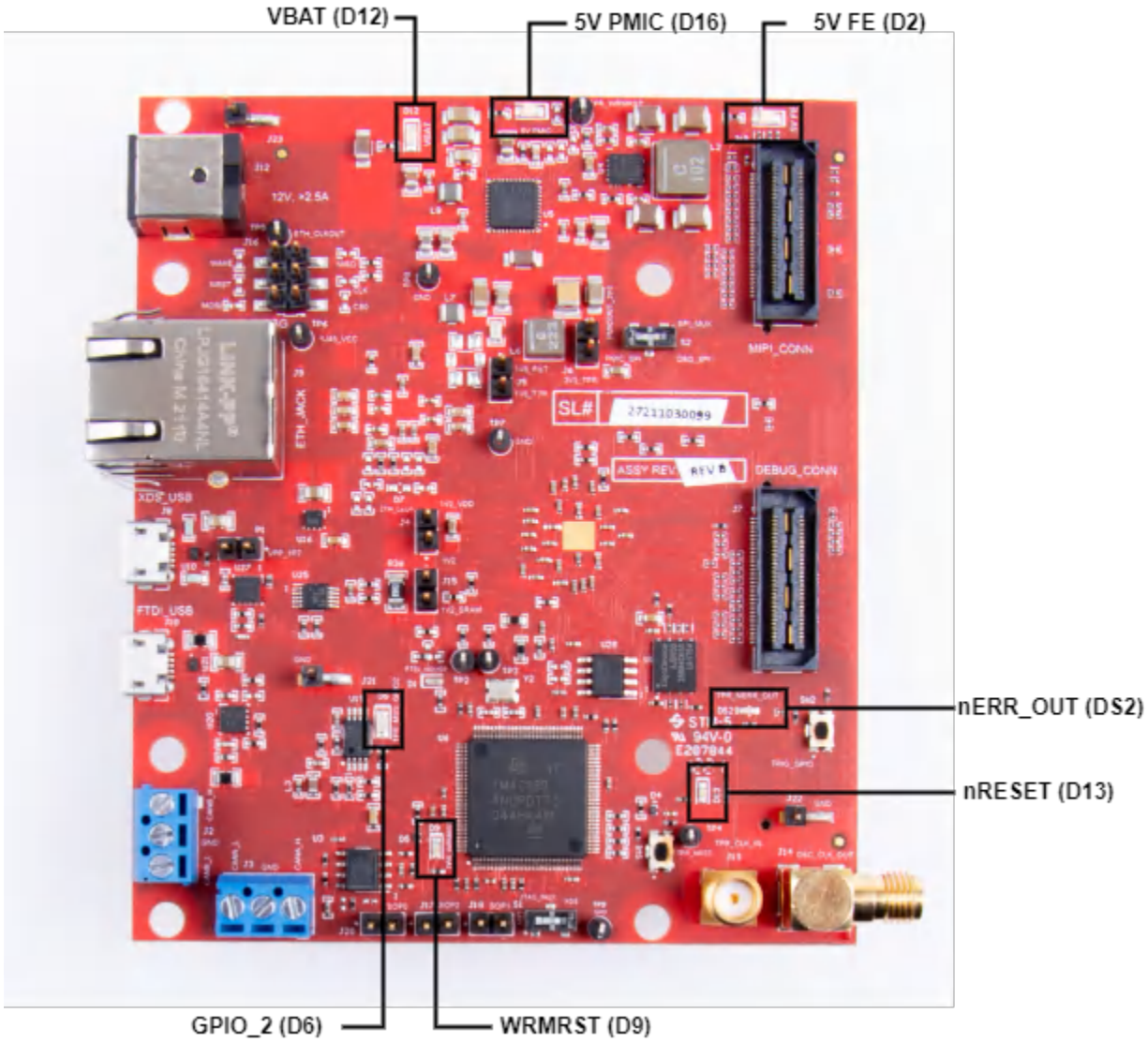


Figure 2-4. AM273x EVM LEDs

Table 2-5. LED Information

Ref	Color	Usage	Comments	Image
D12	Green	12V supply indication	This LED indicates the presence of 12V supply input.	
D16	Green	5V PMIC Supply	This LED indicates the presence of 5V supply output from PMIC.	
D2	Green	5V FE Supply	This LED indicates the presence of 5V supply for FE connectors.	
D13	Yellow	nRESET	This LED is used to indicate the state of nRESET pin. If this LED is glowing, then the device is out of reset.	
DS2	Red	NERR_OUT	Glows if there is any HW error in the AM273x device.	
D9	Yellow	WRMRST	Open drain fail safe warm reset signal.	
D6	Green	GPIO_2	Glows when the GPIO_2 is logic-1.	

2.1.5 Boot Mode Selection

The TMDS273GPEVM can be set to operate in three different boot modes based on the state of the Sense On Power (SOP) [2:0] lines. These lines are sensed ONLY during boot up of the AM273x device. The state of the device is described in Table 2-6.

A closed jumper refers to a '1' and an open jumper refers to a '0' state of the SOP signal going to the AM273x device.

Table 2-6. Boot Mode Selection Table

Boot Modes Supported	SOP2 (J17)	SOP1 (J18)	SOP0 (J20)
Dev Management/UART Mode (SOP mode 5)	1	0	1
Functional/QSPI Mode (SOP mode 4)	0	0	1

Figure 2-5. SOP Jumpers

2.2 Hardware Description

2.2.1 Functional Block Diagram

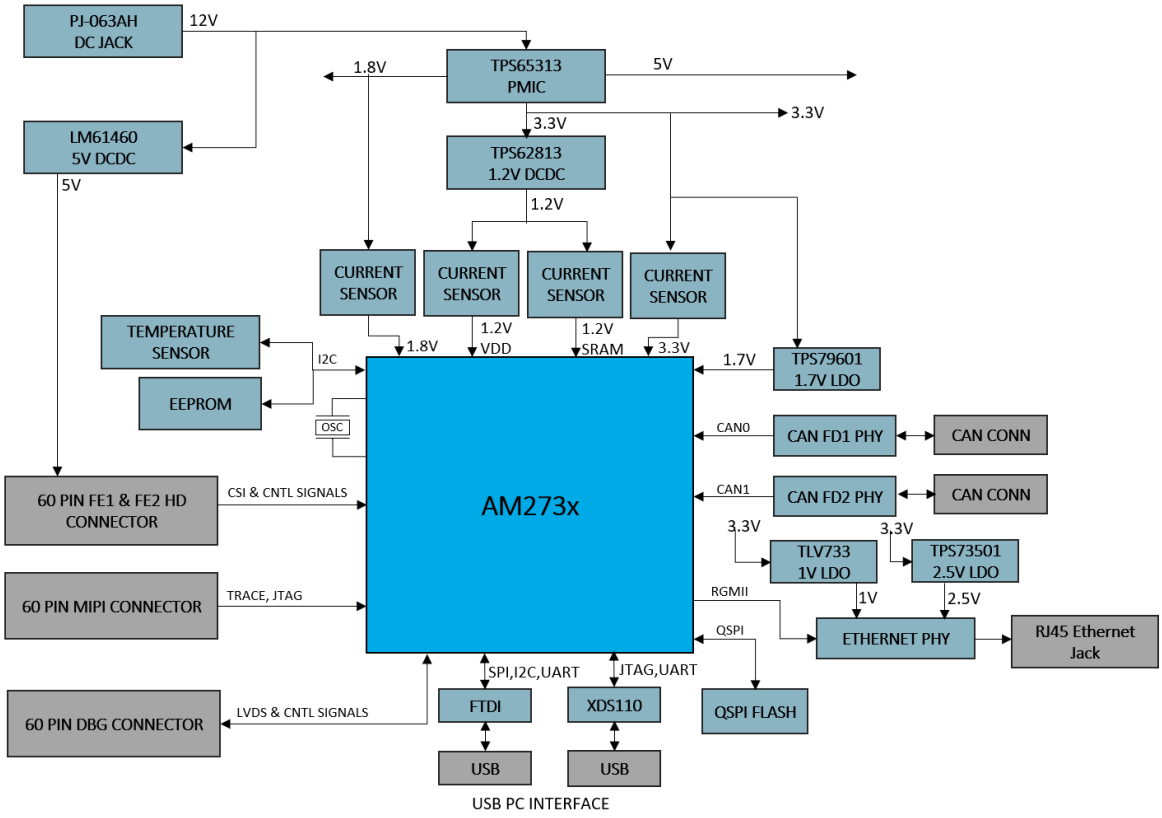


Figure 2-6. AM273x Functional Block Diagram

2.2.2 Memory Interface

2.2.2.1 QSPI Interface

The TMDS273GMEVM board has a 64 Mbit QSPI memory device (GD25B64CWAG from GigaDevice), which is connected to the MSS_QSPI interface of the AM273x SoC. This flash device is primarily meant to store the boot image, but can also serve as storage for other data if another boot mode is used.

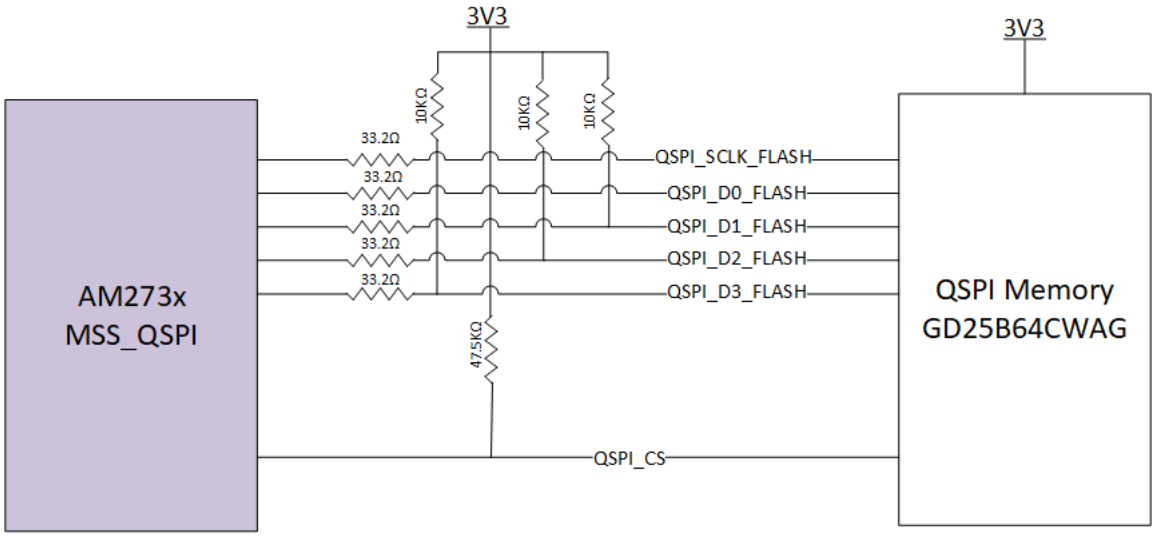


Figure 2-7. QSPI Interface

2.2.2.2 Board ID EEPROM

The AM273x EVM is a 2 Kbit I2C EEPROM for board ID information. The board ID memory is configured to respond to I2C address 0x50. This EEPROM (CAV24C02WE-GT3 from Onsemi) interfaces with the SoC via the MSS_I2CA port.

As seen in Figure 2-8, pins WP is allowed to float while A0, A1, and A2 are pulled to ground. These pins are pulled low internally. Pins A0, A1, and A2 configure the device address. The WP pin is the Write Protect input. When pulled high, this pin prevents write operations.

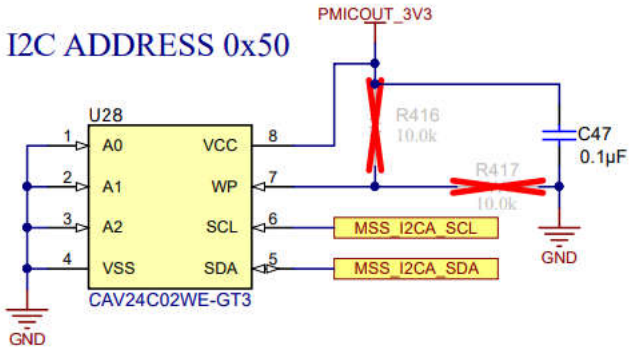


Figure 2-8. Board ID EEPROM

2.2.3 Ethernet Interface

The AM273x EVM supports an RGMII Ethernet port to provide the connection to the network. This interface is intended to operate primarily as a 100Mbps ECU interface and can also be used as an Instrumentation Interface.

The AM273x EVM supports following features:

- Full Duplex 10Mbps/100Mbps wire rate Interface to Ethernet PHY over RGMII, parallel interface
- MDIO Clause 22 and 45 PHY management interface
- IEEE 1588 Synchronous Ethernet support

The Ethernet port is interfaced to the AM273x through the Ethernet PHY DP83867ERGZR, and is used to stream the captured data over the network to the host PC.

Figure 2-11 shows the Ethernet RJ45 Mag-Jack connector, and Table 2-7 provides the connector pin details.

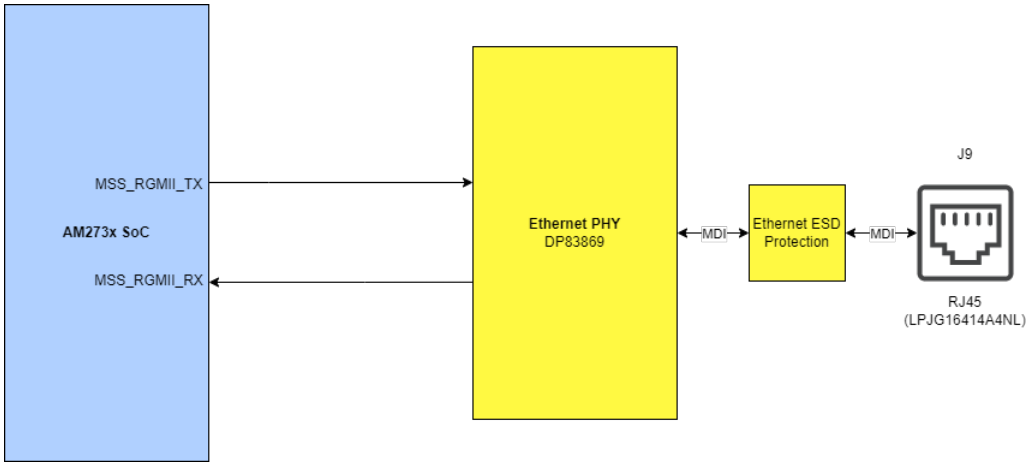


Figure 2-9. Ethernet Interface Block Diagram

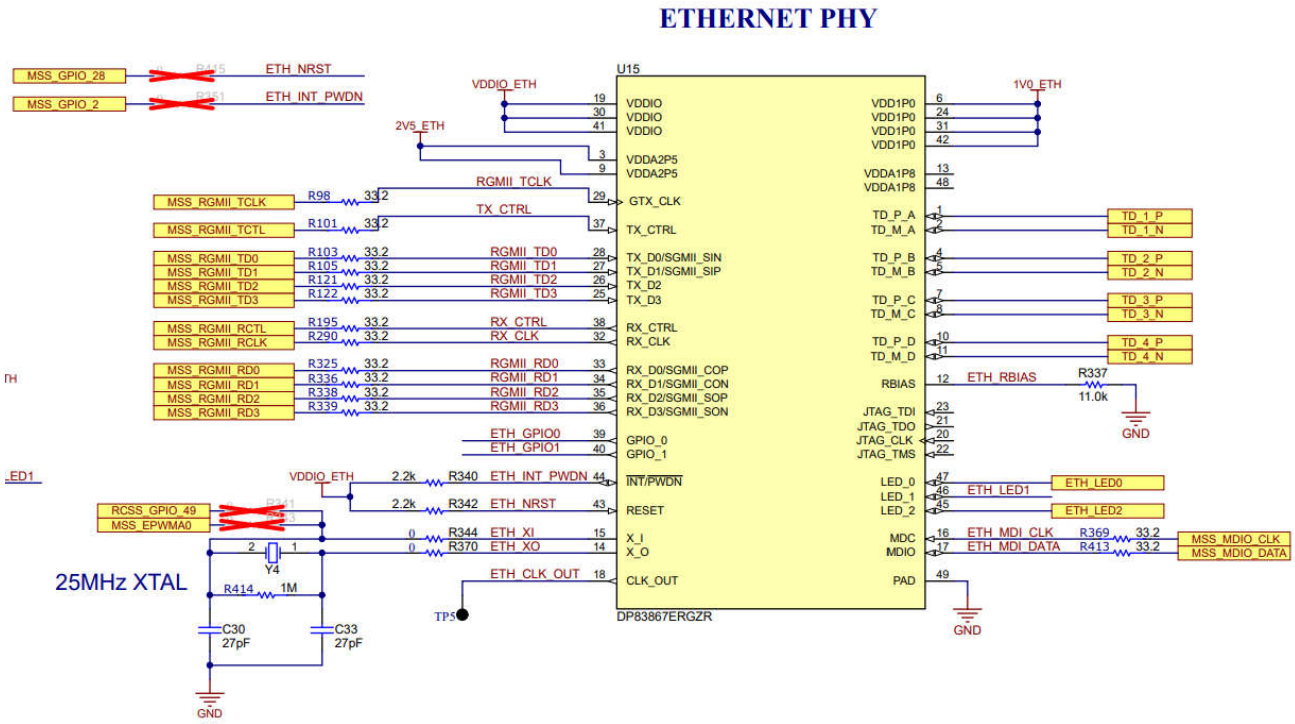


Figure 2-10. Ethernet PHY Schematic

Table 2-7. J9 Connector Pin

Pin Number	Description	Pin Number	Description
1	GND	2	Test point
3	ETH_D4P	4	ETH_D4N
5	ETH_D3P	6	ETH_D3N
7	ETH_D2P	8	ETH_D2N
9	ETH_D1P	10	ETH_D1N
11	LED_ACTn	12	GND
13	GND	14	LED_LINKn
15	ETH_GND	16	ETH_GND

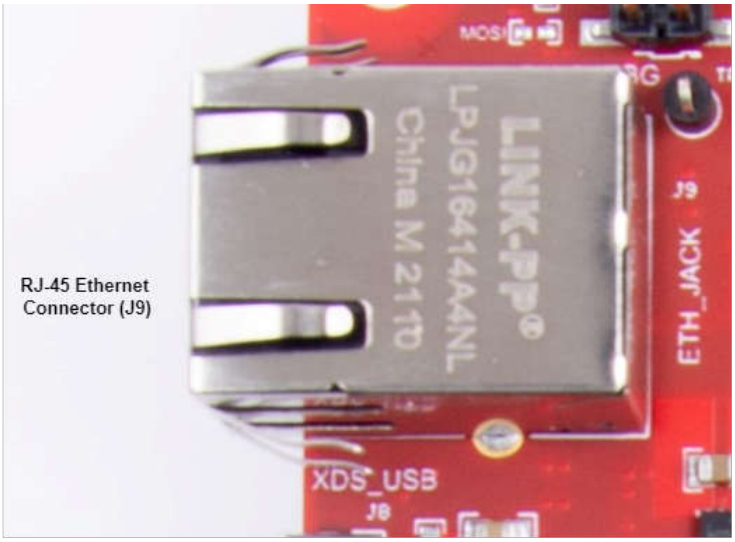


Figure 2-11. RJ45 Connector

2.2.4 Micro USB Interfaces

The AM273x EVM has two standard micro USB connectors.

Micro USB Connector J10 provides access to the AM273x UART, SPI, I2C, and SOP interfaces through the FTDI chip.

Micro USB connector J8 provides access to the JTAG, MSS_UARTA, and MSS_UARTB interfaces of the AM273x via the XDS110 emulator.

2.2.4.1 FTDI USB Interface

Micro USB Connector J10 provides access to the AM273x UART, SPI, I2C, and SOP interfaces through the FTDI USB Interface IC (the FT4232HL). The FTDI USB Interface IC is configured by the FTDI EEPROM as described in Section 2.2.4.1.1.

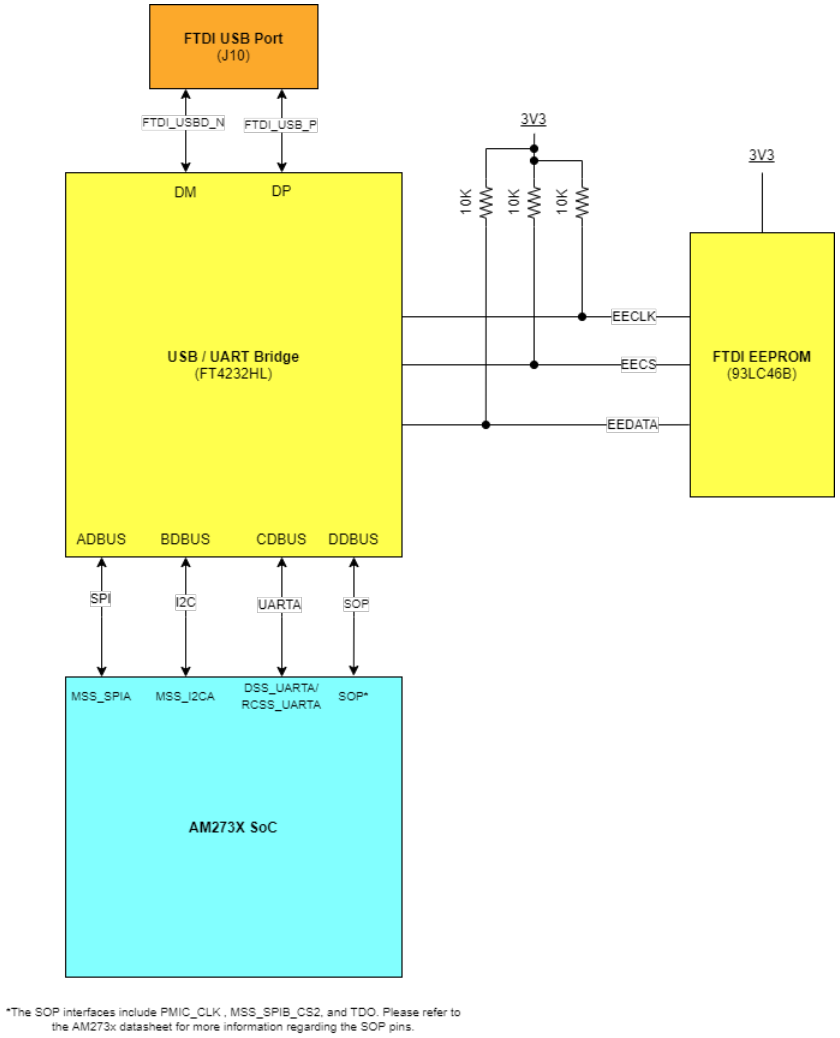


Figure 2-12. FTDI USB Block Diagram

Table 2-8. J10 Connector Pin

Pin Number	Description	Pin Number	Description
1	FTDI_VBUS	2	FTDI_USBD_N
3	FTDI_USBD_P	4	FTDI_USBID
5	GND	6	GND
7	GND	8	GND
9	GND	10	GND
11	GND		

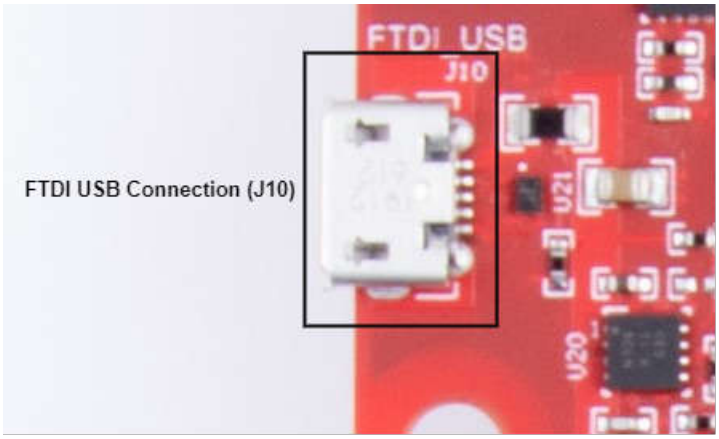


Figure 2-13. FTDI USB Connector

2.2.4.1.1 FTDI EEPROM Memory Device

The AM273x EVM contains a 1Kb serial EEPROM device (93LC46B from Microchip) that holds the programming information for the FT4232HL USB to UART bridge. By default the 93LC46B contains the power up data for the FT4232HL to boot into a UART configuration.

2.2.4.2 XDS USB Interface

Micro USB connector J8 provides access to the JTAG and MSS_UARTA interface with the MSS_UARTB transmission line of the AM273x via the XDS110 emulator.

This is the UART interface used to flash the binary to the onboard serial flash and for OOB demo.

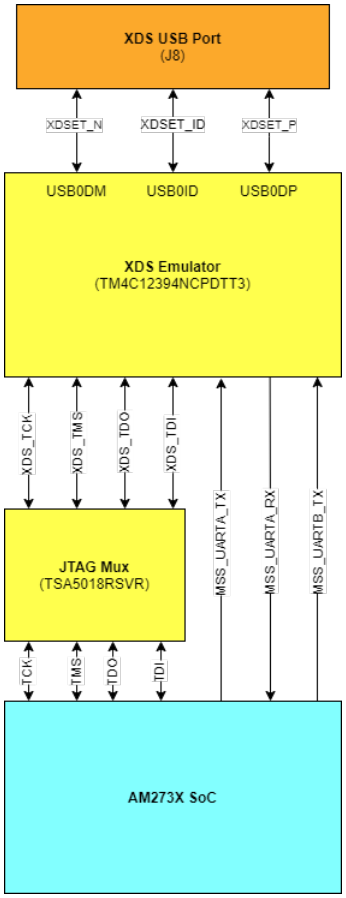


Figure 2-14. XDS USB Interface Block Diagram

Table 2-9. J8 Connector Pin

Pin Number	Description	Pin Number	Description
1	XDSET_VBUS	2	XDSET_D_N
3	XDSET_D_P	4	XDSET_ID
5	GND	6	GND
7	NC	8	NC
9	GND	10	GND
11	GND		

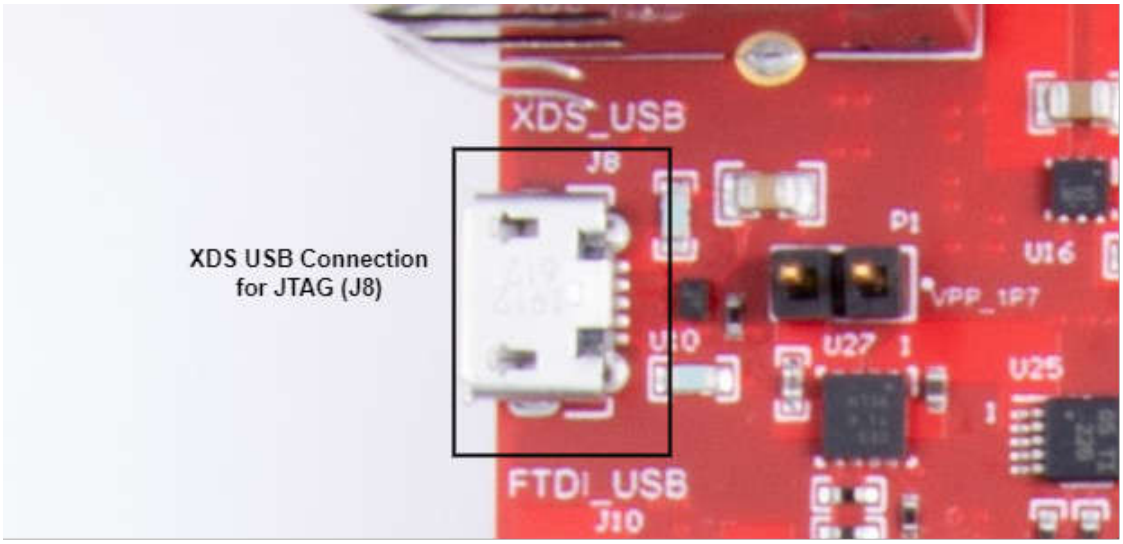


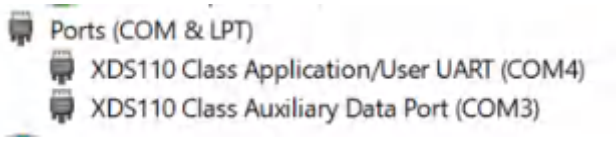
Figure 2-15. XDS USB Connector

2.2.4.3 PC Connection

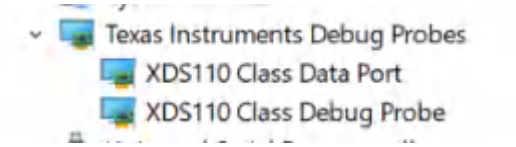
The connectivity is provided through the micro USB connector over the onboard XDS110 (TM4C1294NCPDT) emulator. This provides the following interfaces to the PC:

- JTAG for CCS connectivity
- MSS logger UART. This can be used to get MSS code logs on the PC

When the USB is connected to the PC, the device manager recognizes two XDS110 COM ports under Ports (COM and LPT).



XDS110 debug probe and data port are detected under Texas Instruments Debug Probes.



If the PC is unable to recognize the above COM ports, then install the EMU pack available at the following link:

https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_xds_software_package_download.html

2.2.5 I2C Interface

The AM273x SoC supports three I2C interfaces: MSS_I2CA, RCSS_I2CA, and RCSS_I2CB. The MSS_I2CA lines are muxed out of the controller by default, while the RCSS_I2CA and RCSS_I2CB lines require pin muxing to be accessible. Information regarding the locations of the I2C modules for the AM273x can be found in the Pin Attributes section of the AM273x data sheet.

- **MSS_I2CA Interface**:
  - Default pins:
    - MSS_I2CA_SDA: F16
    - MSS_I2CA_SCL: F18
  - Identify the EVM through the Board ID memory device (CAV24C02WE-GT3)
  - Read 1.2V, 1.8V, and 3.3V digital supply current sensors
  - Read 1.2V SRAM supply current sensor
  - Read temp sensor
  - Interface with 60 pin debug connector

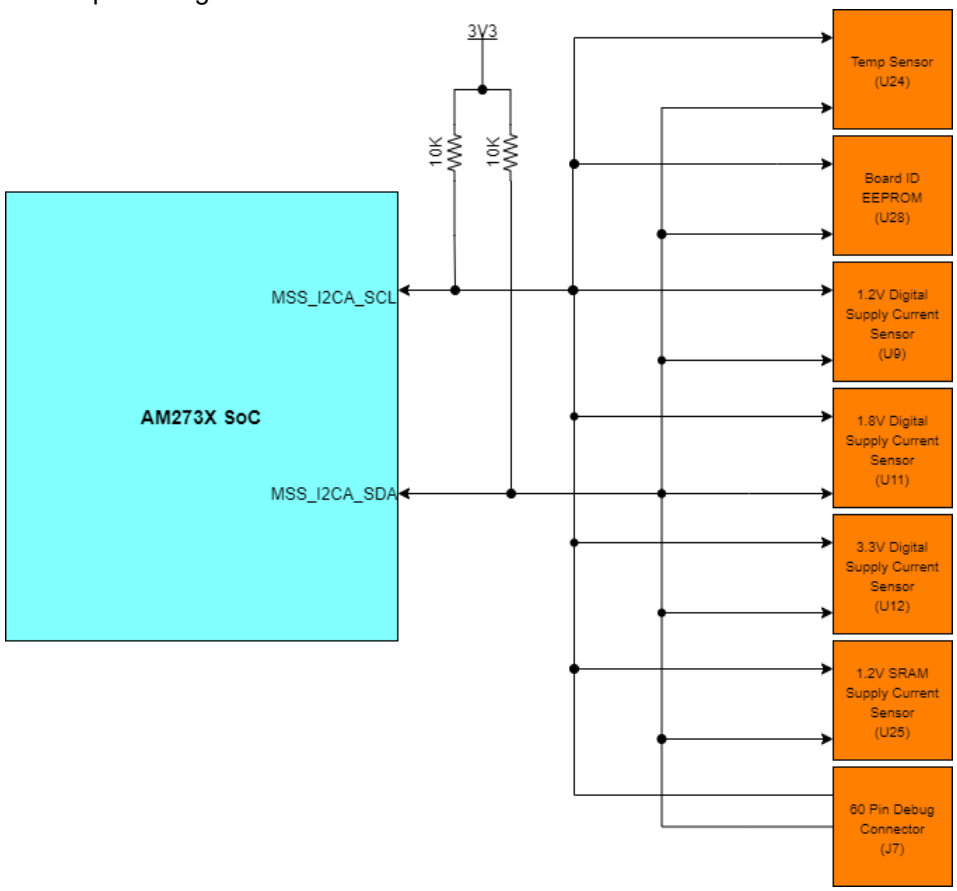


Figure 2-16. MSS_I2CA Block Diagram

- **RCSS_I2CA:**
  - Not available on the AM273x EVM by default
- **RCSS_I2CB:**
  - Not available on the AM273x EVM by default

2.2.5.1 I2C Connections

The board features temperature sensor for measuring onboard temperature, current sensors for current measurement for 1.2V, 1.8V, and 3.3V AM273x supply rails, and EEPROM for storing board ID. These are connected to the AM273x EVM through the I2C bus.

Table 2-10 shows the list of I2C devices available in the AM273x EVM board and the address.

Table 2-10. I2C Devices and Addresses

Sensor Type	Reference Designator	Part Number	Peripheral Address
Temp sensor	U24	TMP112AIDRLR	0x49
Current sensor for 3.3V rail	U12	INA226AIDGSR	0x44
Current sensor for 1.8V rail	U11	INA226AIDGSR	0x41
Current sensor for 1.2V Digital rail	U9	INA226AIDGSR	0x40
Current sensor for 1.2V SRAM rail	U25	INA226AIDGSR	0x45
EEPROM	U28	CAV24C02WE-GT3	0x50

2.2.6 UART Interface

The AM273x is composed of four UART interfaces:

- Two Main Subsystem Modules (MSS_UARTA and MSS_UARTB)
  - MSS_UARTA_RX and MSS_UARTA_TX are accessible through the XDS110 USB port (J8) via the XDS emulator.
  - MSS_UARTB_TX is available via the XDS110 USB port (J8) via the XDS emulator while MSS_UARTB_RX is not accessible by the default pin mux on the AM273x EVM.
- One Radar Controller Subsystem Module (RCSS_UARTA)
  - RCSS_UARTA is not available in the standard hardware configuration of the AM273x EVM. However, this port can be accessed if resistors R160 and R164 are depopulated with resistors R156 and R159 populated with 0 ohm resistors. This alteration makes RCSS_UARTA_RX and RCSS_UARTA_TX accessible via the FTDI USB port (J8) as replacements of the DSS_UART interface.
- One DSP Subsystem Module (DSS_UARTA)
  - DSS_UARTA_RX and DSS_UARTA_TX are accessible through the FTDI USB port (J10) via the FT4232HL UART - USB Bridge.

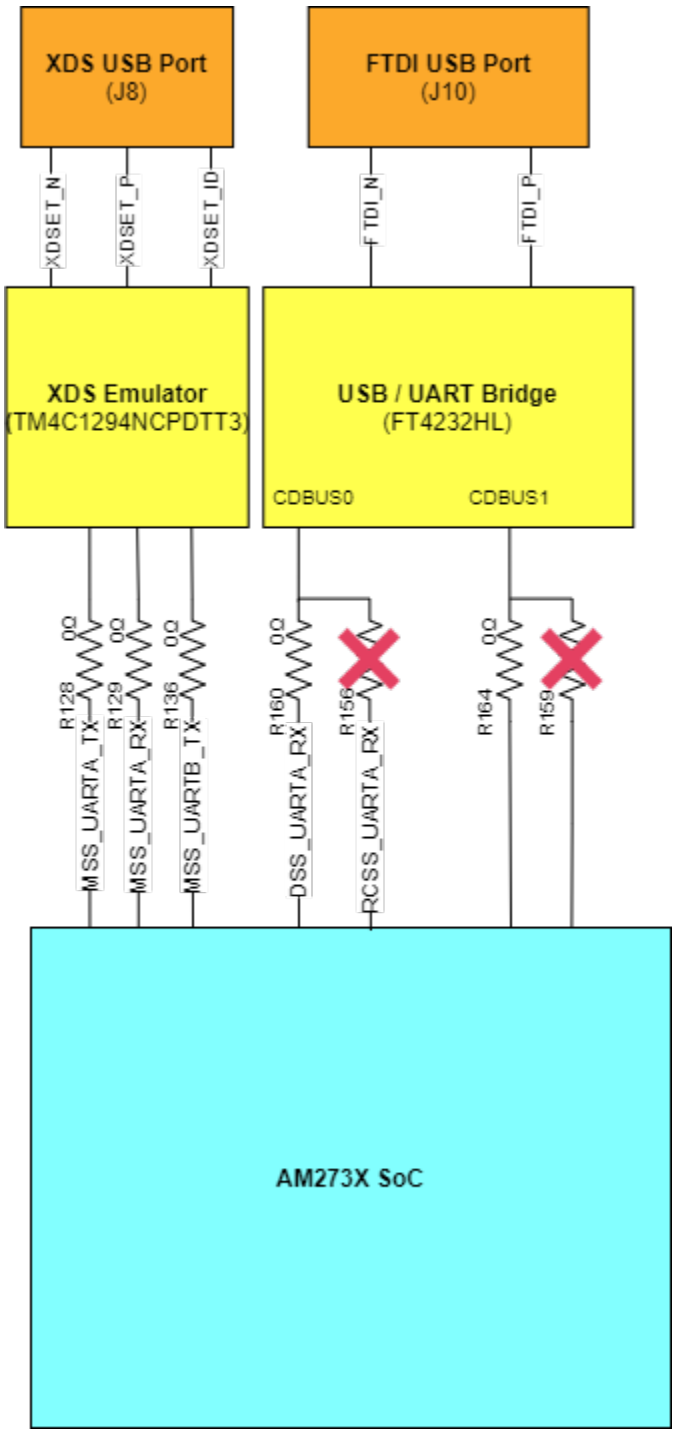


Figure 2-17. UART Interface

2.2.7 CAN Interfaces

2.2.7.1 CAN-A Interface

The J3 connector provides the CANA_L and CANA_H signals from the onboard can CAND-FD transceiver (TCAN1042HGVDRQ1). These can be directly wired to the CAN bus.

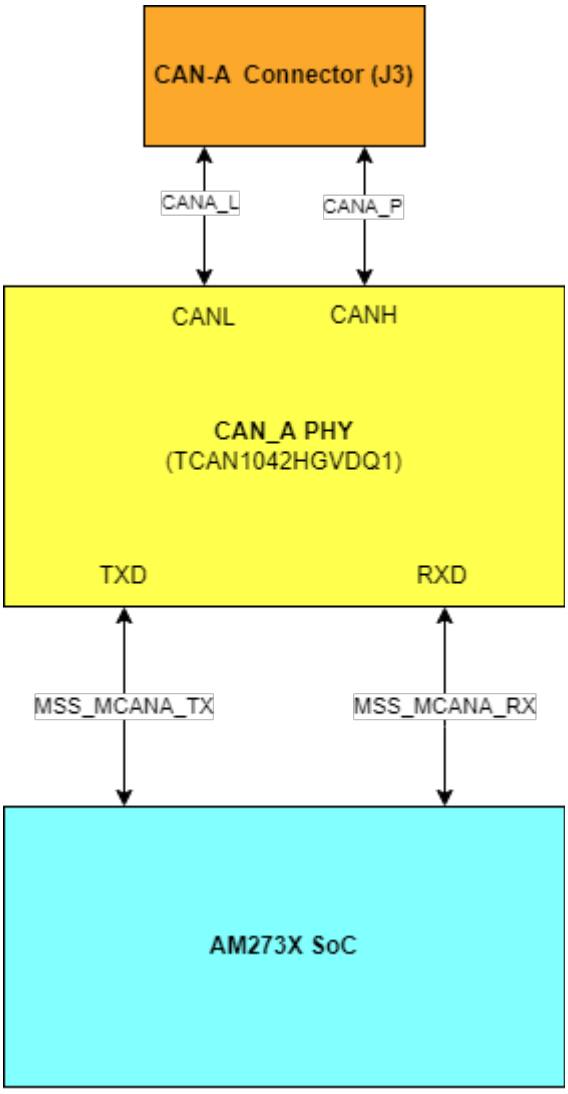


Figure 2-18. CAN-A Interface Block Diagram

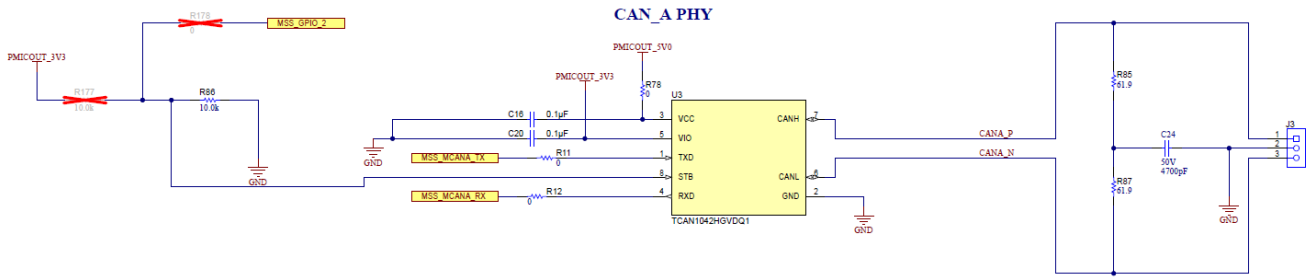


Figure 2-19. CAN-A Schematic

2.2.7.2 CAN-B Interface

The J2 connector provides the CANB_L and CANB_H signals from the onboard can CAND-FD transceiver (TCAN1042HGVDRQ1). These can be directly wired to the CAN bus.

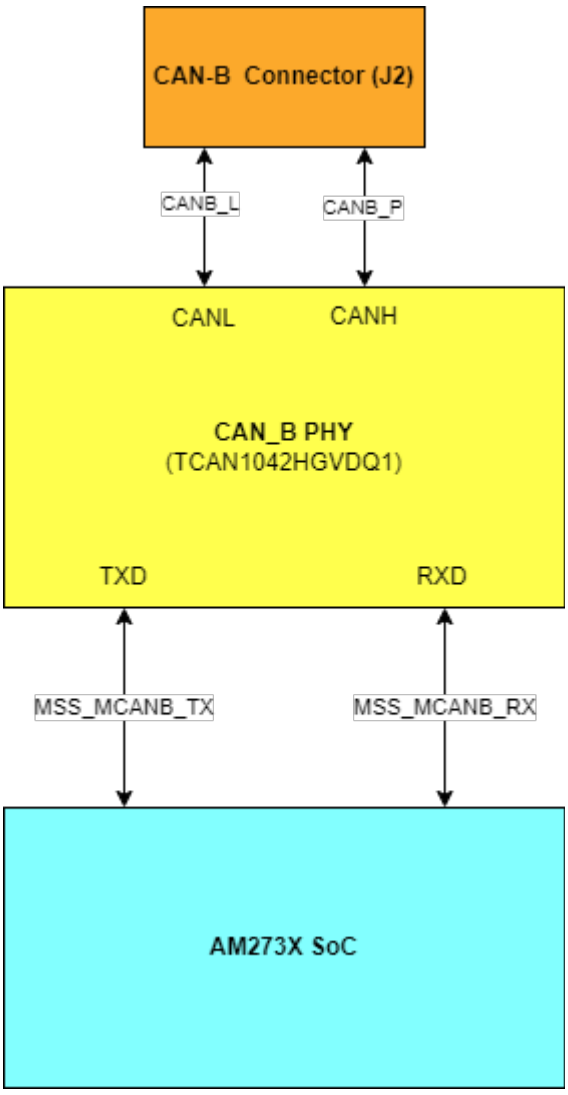


Figure 2-20. CAN-B Interface Block Diagram

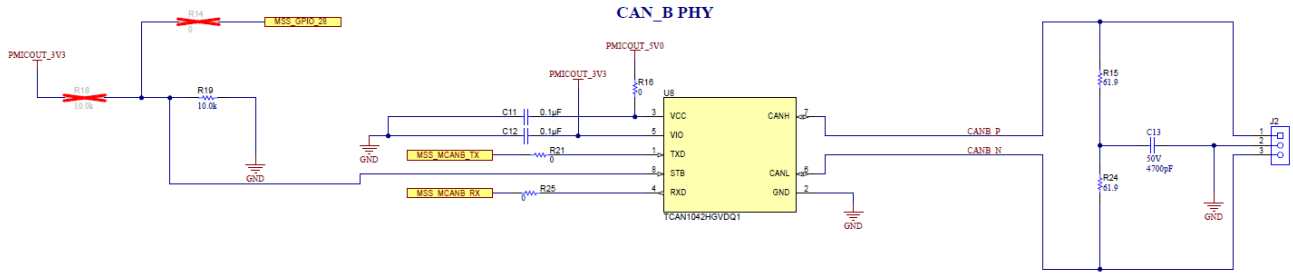


Figure 2-21. CAN-B Schematic

2.2.8 JTAG Emulation

The AM273x EVM includes the necessary circuitry for XDS110 emulation. The XDS110 class on-board emulation is used to support testing of software builds. The connection for the emulator uses a USB 2.0 micro-B connection (J8).

Alternatively, off-board emulation can be used to interface with the EVM through the MIPI 60 header (J19) or the 60 Pin Debug Header (J7). The XDS USB Port and the 60 pin headers are muxed at the TS3A5018RSVR analog switch (U23). The line for this mux selection is determined by the state of switch S1. When S1 is set to 'MIPI,' the signals are routed to the MIPI 60 Header (J19) and 60 Pin Debug Header (J7). When S1 is set to 'XDS,' the signals are routed to the emulator and XDS USB port (J8).

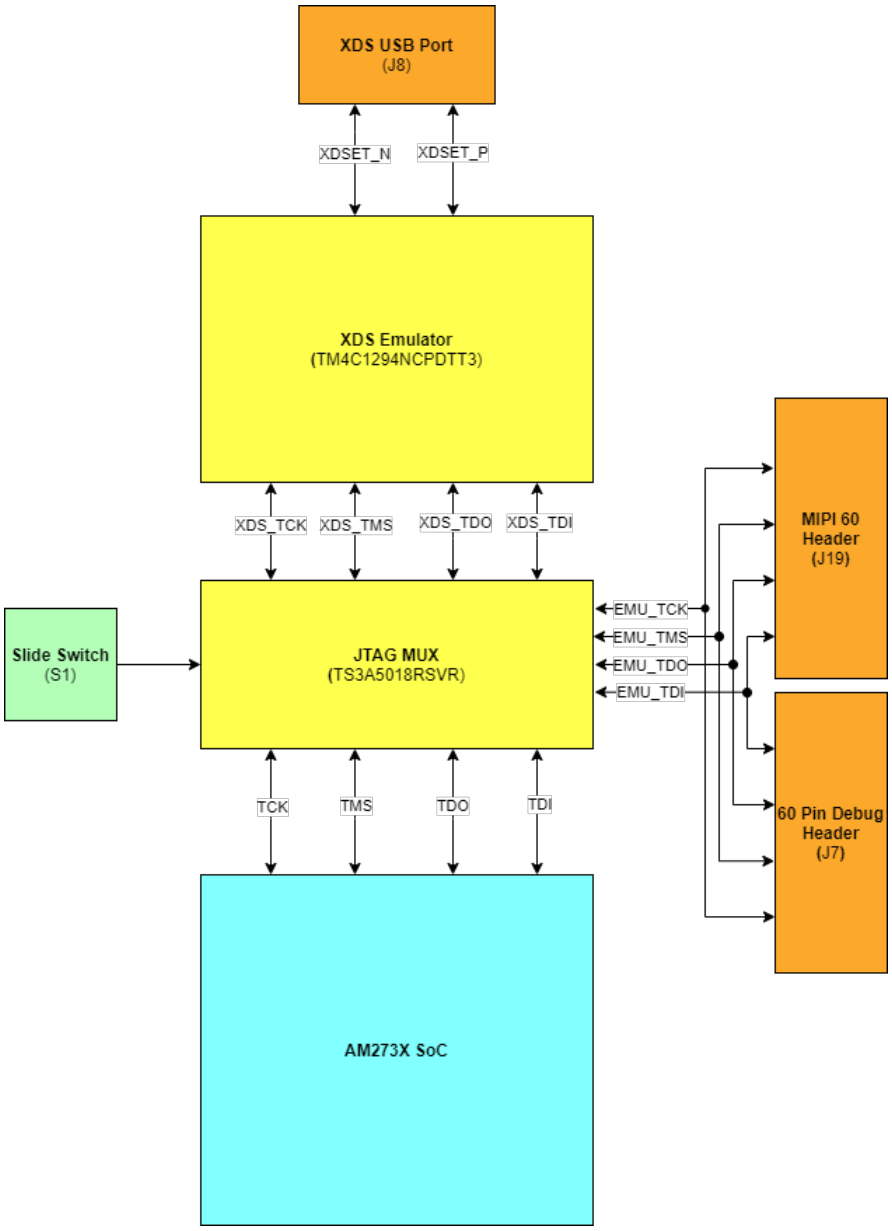


Figure 2-22. JTAG Emulation Block Diagram

2.2.9 SPI Interface

The EVM supports four SPIs:

- Two main subsystem interfaces:
  - MSS_SPIA is accessible through the FTDI USB port (J10) via the FT4232HL UART USB bridge.
  - MSS_SPIB is multiplexed out via the TS3A5018RSVR multiplexor to either the PMIC and debug test pins (J16) or the 60 Pin Debug Header (J7). The TS3A5018RSVR mutliplexor is driven by S2 which acts as a select line. When set to 'PMIC_SPI' position, the MSS_SPIB interface is routed to the PMIC and J16 header. When set to ‘DBG_SPI’, the MSS_SPIB interface is routed to the 60-pin debug header (J7). The CS1 line of the MSS_SPIB interface bypasses the multiplexor and is routed directly to the 60 Pin Debug Header.

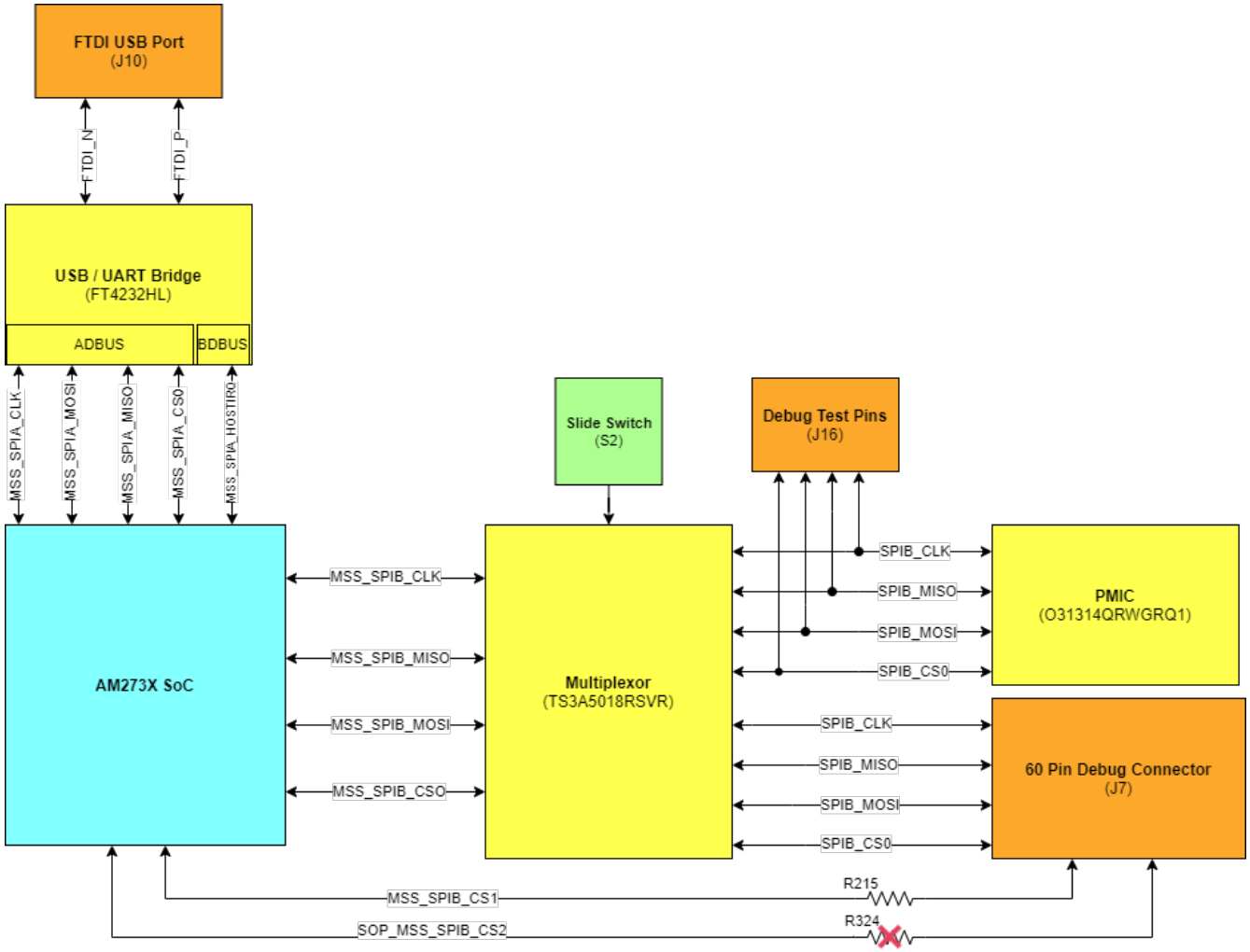


Figure 2-23. MSS SPI Interface

- Two radar control subsystem interfaces:
  - RCSS_SPIA is routed to the HD front end connector J1.
  - RCSS_SPIB is routed to the HD front end connector J11.

2.2.10 MDI Interface

The AM273x EVM has a two signal (clock and data) MDI interface. This purpose of the interface is to configure the Ethernet PHY. Since a PHY (TI's DP83867ERGZR) is established for the EVM, the software of the EVM is set to properly configure this PHY by default.

Please refer to Figure 2-10 for more detail on the Ethernet PHY design.

2.2.11 ePWM Interface

The AM273x EVM has one enhanced pulse-width modulator (ePWM) interface available on an external header. MSS_EPWMA0 is routed to pin 6 of the 60 pin debug header.

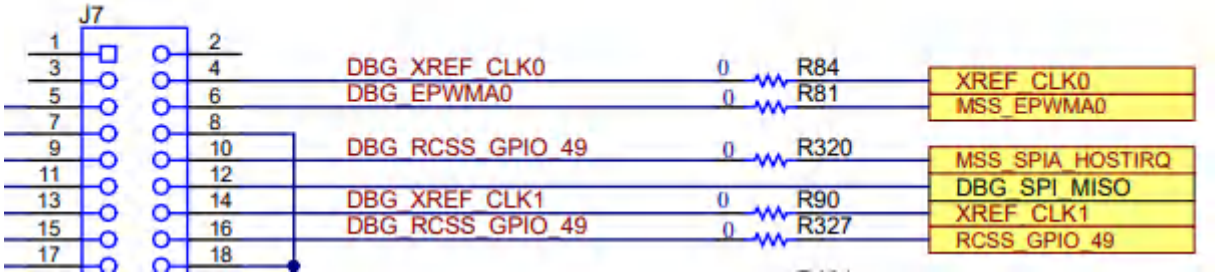


Figure 2-24. ePWM Debug Header Pin

Please see Section 2.3.4 for further detail on the Debug Connector pinout.

2.3 Connectors

2.3.1 60-Pin High Density (HD) FE Connector-1 (J1)

The 60-pin HD connector-1 provides the high speed 4-lane CSI interface, SPI, UART, I2C, and controls signals (NRST, NERR, WRMRST, REFCLK, OSCCLK, SOPs). This can be connected to the AWR2243BOOST EVM board to interface to the front end radar device.

Figure 2-25. High Density FE Connector-1 Schematic

Table 2-11. J1 Connector Pin

Pin Number	Description	Pin Number	Description
1	5V	2	5V
3	5V	4	NC
5	NC	6	NC
7	RCSS_SPIA_CS	8	NC
9	RCSS_SPIA_CLK	10	RCSS_SPIA_HOSTINT
11	RCSS_SPIA_PICO	12	RCSS_SPIA_POCI
13	NC	14	NERRIN_FE1
15	NC	16	HW_SYNC_FE1
17	NC	18	GND
19	NC	20	NC
21	NC	22	NC
23	NC	24	GND
25	NC	26	NC
27	NC	28	NC
29	NC	30	GND
31	NC	32	CSI2_RX0_3P
33	SOP0_FE1	34	CSI2_RX0_3N
35	SOP1_FE1	36	GND
37	SOP2_FE1	38	CSI2_RX0_2P
39	WRMRST_FE1	40	CSI2_RX0_2N
41	GND	42	GND
43	REFCLK_FE1	44	CSI2_RX0_CLKP
45	GND	46	CSI2_RX0_CLKN
47	OSCCLK_FE1	48	GND
49	GND	50	CSI2_RX0_1P
51	I2CA_SDA	52	CSI2_RX0_1N
53	I2CA_SCL	54	GND
55	NC	56	CSI2_RX0_0P
57	NC	58	CSI2_RX0_0N
59	nRESET_FE1	60	GND

2.3.2 60-Pin High Density (HD) FE Connector-2 (J11)

The 60-pin HD connector-2 provides the high speed 4-lane CSI interface, SPI, UART, I2C, and controls signals (NRST, NERR, WRMRST, REFCLK, SOPs). This can be connected to the AWR2243BOOST EVM board to interface with the second front end radar device in cascade configuration.

Figure 2-26. High Density FE Connector-2 Schematic

Table 2-12. J11 Connector Pin

Pin Number	Description	Pin Number	Description
1	5V	2	5V
3	5V	4	NC
5	NC	6	NC
7	RCSS_SPIB_CS	8	NC
9	RCSS_SPIB_CLK	10	RCSS_SPIB_HOSTINT
11	RCSS_SPIB_PICO	12	RCSS_SPIB_POCI
13	NC	14	NERRIN_FE2
15	NC	16	HW_SYNC_FE2
17	NC	18	GND
19	NC	20	NC
21	NC	22	NC
23	NC	24	GND
25	NC	26	NC
27	NC	28	NC
29	NC	30	GND
31	NC	32	CSI2_RX1_3P
33	SOP0_FE2	34	CSI2_RX1_3N
35	SOP1_FE2	36	GND
37	SOP2_FE2	38	CSI2_RX1_2P
39	WRMRST_FE2	40	CSI2_RX1_2N
41	GND	42	GND
43	REFCLK_FE2	44	CSI2_RX1_CLKP
45	GND	46	CSI2_RX1_CLKN
47	NC	48	GND
49	GND	50	CSI2_RX1_1P
51	I2CB_SDA	52	CSI2_RX1_1N
53	I2CB_SCL	54	GND
55	NC	56	CSI2_RX1_0P
57	NC	58	CSI2_RX1_0N
59	nRESET_FE2	60	GND

2.3.3 MIPI 60-Pin Connector (J19)

This connector provides the standard MIPI 60-pin interface for JTAG and trace capability through emulators such as the XDS560pro. Further information on the emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.

To use this interface, the JTAG lines from the TMDS273GPEVM must be muxed to MIPI 60-pin connector.

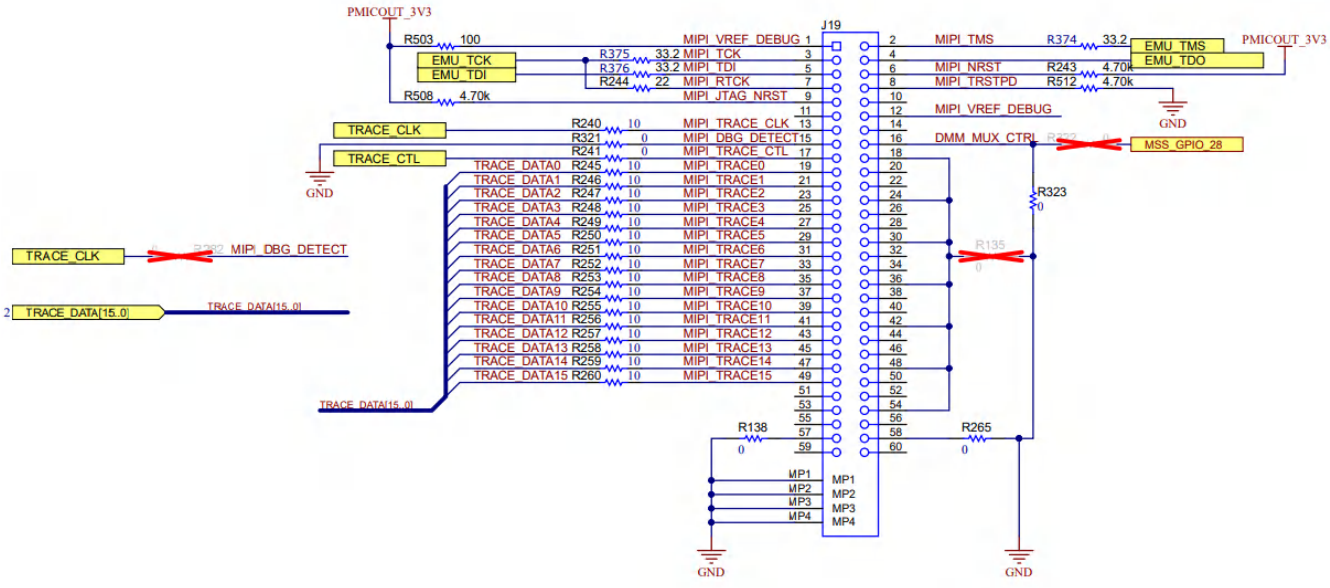


Figure 2-27. MIPI 60 Connector Schematic

Table 2-13. J19 Connector Pin

Pin Number	Description	Pin Number	Description
1	MIPI_VREF	2	MIPI_TMS
3	MIPI_TCK	4	MIPI_TDO
5	MIPI_TDI	6	MIPI_NRST
7	MIPI_RTCK	8	MIPI_TRSTPD
9	MIPI_JTAG_NRST	10	NC
11	NC	12	MIPI_VREF
13	MIPI_TRACE_CLK	14	NC
15	MIPI_DBG_DETECT	16	GND
17	MIPI_TRACE_CTL	18	NC
19	MIPI_TRACE0	20	NC
21	MIPI_TRACE1	22	NC
23	MIPI_TRACE2	24	NC
25	MIPI_TRACE3	26	NC
27	MIPI_TRACE4	28	NC
29	MIPI_TRACE5	30	NC
31	MIPI_TRACE6	32	NC
33	MIPI_TRACE7	34	NC
35	MIPI_TRACE8	36	NC
37	MIPI_TRACE9	38	NC
39	MIPI_TRACE10	40	NC
41	MIPI_TRACE11	42	NC
43	MIPI_TRACE12	44	NC

Table 2-13. J19 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
45	MIPI_TRACE13	46	NC
47	MIPI_TRACE14	48	NC
49	MIPI_TRACE15	50	NC
51	NC	52	NC
53	NC	54	NC
55	NC	56	NC
57	GND	58	GND
59	NC	60	NC

2.3.4 Debug Connector 60-Pin (J7)

This connector enables interfacing of LVDS signals to the DCA1000 EVM for data capturing purposes as well as SPI, I2C, JTAG, GPADC, and other control signals from the AM273x EVM for debug purposes.

The SPI interface must be muxed to the Debug Connector. For more details, refer to Section 2.1.3.

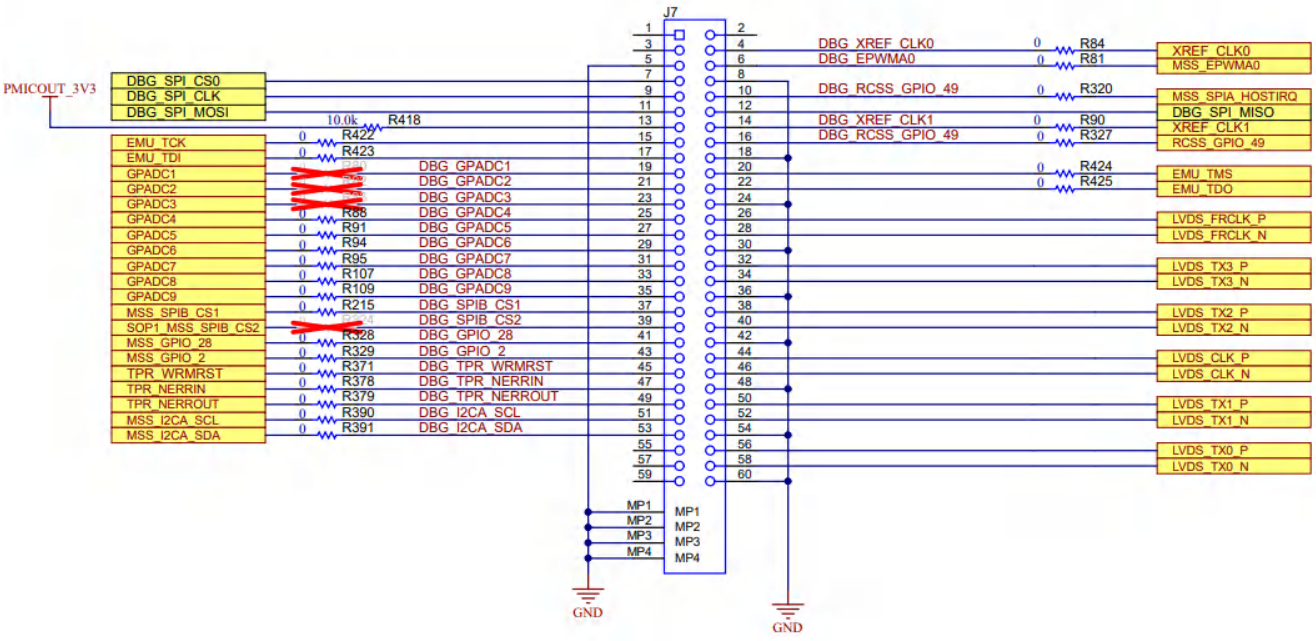


Figure 2-28. Debug Connector Schematic

Table 2-14. J7 Connector Pin

Pin Number	Description	Pin Number	Description
1	NC	2	NC
3	NC	4	XREF_CLK0
5	GND	6	MSS_EPWMA0
7	MSS_SPIB_CS0	8	GND
9	MSS_SPIB_CLK	10	MSS_SPIA_HOSTIRQ
11	MSS_SPIB_PICO	12	MSS_SPIB_POCI
13	3.3V PULL_UP	14	XREF_CLK1
15	EMU_TCK	16	RCSS_GPIO_49
17	EMU_TDI	18	GND
19	GPADC1	20	EMU_TMS
21	GPADC2	22	EMU_TDS

Table 2-14. J7 Connector Pin (continued)

Pin Number	Description	Pin Number	Description
23	GPADC3	24	GND
25	GPADC4	26	LVDS_FRCLK_P
27	GPADC5	28	LVDS_FRCLK_N
29	GPADC6	30	GND
31	GPADC7	32	LVDS_TX3_P
33	GPADC8	34	LVDS_TX3_N
35	GPADC9	36	GND
37	MSS_SPIB_CS1	38	LVDS_TX2_P
39	SOP1_MSS_SPIB_CS2	40	LVDS_TX2_N
41	MSS_GPI0_28	42	GND
43	MSS_GPI0_2	44	LVDS_CLK_P
45	TPR_WRMRST	46	LVDS_CLK_N
47	TPR_NERRIN	48	GND
49	TPR_NERROUT	50	LVDS_TX1_P
51	MSS_I2CA_SCL	52	LVDS_TX1_N
53	MSS_I2CA_SDA	54	
55	NC	56	LVDS_TX0_P
57	NC	58	LVDS_TX0_N
59	NC	60	GND

2.3.5 External Clock Option (J13, J1)

The AM273x SoC can operate with external clock source provided from J13 connector or clock provided from Radar FE via OSCK_FE1 on connector J1 (the HD Front End Connector).

The AM273x SoC supports externally driven clock (Square/Sine) at 40/50 MHz.

Note

To enable an external clock source from the J13 connector, the R269 resistor must be populated on board.

To enable an external clock from the J1 connector, the R281 resistor must be populated on board.

Refer to the AM273x data sheet for external clock specifications.

2.4 Mechanical Mounting of the PCB

The spacers and screws provided with the AM273x EVM kit help to arrest the AM273x EVM in the horizontal plane. Figure 2-29 shows the assembly of mechanical spacers to the board.

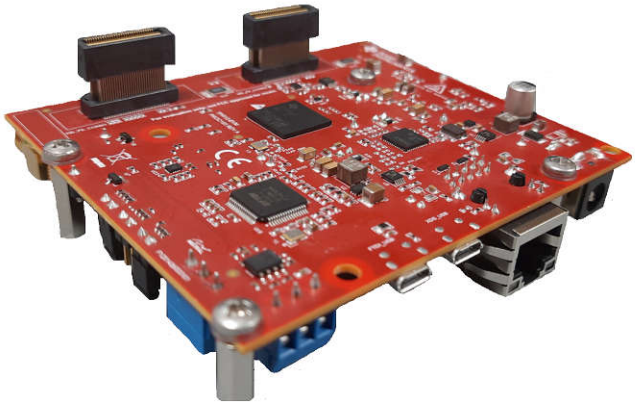


Figure 2-29. AM273x EVM Mechanical Assembly

The L-brackets provided with the AWR2443 EVM kit, along with the screws and nuts, help in the vertical mounting of the EVM. Figure 2-30 shows how the L-brackets can be assembled.

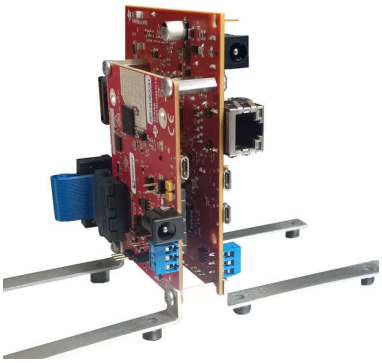


Figure 2-30. AM273x EVM Interfaced to the AWR2944BOOST EVM

The AM273x EVM is designed to interface with the DCA1000 EVM on Debug Connector (J7). Figure 2-31 shows how the AM273x EVM can be connected to the DCA1000 EVM.

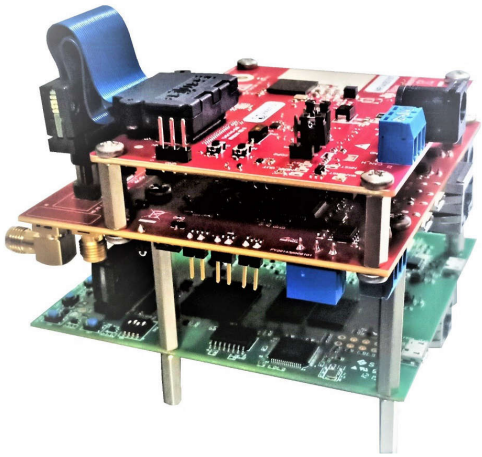


Figure 2-31. AM273x EVM Interfaced to the DCA1000 EVM

3 Additional Information

3.1 Trademarks

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3.A Rev. C Design Changes

The AM273x GPEVM had various design changes for the Revision C of the board. The changes are listed below:

1. **Power Supply Changes**
   a. The Rev. C GPEVM makes use of the LP877451 PMIC, which requires a 3.3V pre regulator but eliminate the need for additional external DC-DC converters.

Table A-1. Rev. C Power Solution Changes

Revision	External DC-DC Converters	Function	PMIC	Function
Rev B	TLV733	1.8V → 1.0V	TPS65313	12V → 5V, 3.3V, 1.8V
	TPS62813	3.3V → 1.2V		
Rev C	LM63625	12V→ 3.3V	LP877451	3.3V → 5V, 3.3V, 1.8V, 1.2V,1.0V

2. **Changes for McASP**
   a. The Rev C. routes out the McASP-A and McASP-C signals to a new 30 pin McASP header.
   b. Two additional 1:2 Muxes were added to support the signal path of the McASP A/C signals to the header where the select line logic comes from a single pole double throw switch.

Table A-2. McASP Mux Select

Switch Position	McASP_Mux_Select Logic	Function
Pin 1	Pulled down to ground	non-McASP signals are connected
Pin 3	Pulled up to 3.3V	McASP signals are connected to the 30-pin header

   c. The TRACE_DATA[0-6] signals from the AM273x were renamed to MUX_TRACE_DATA[0-6] to reflect that the signals are now inputs to a mux before being routed to MIPI 60 pin header.
3. **Changes for eCAP**
   a. The Rev C. routes out the eCAP signals to a new 4 pin eCAP header.
   b. 1:2 Mux added to give the option to route the eCAP signals to the eCAP header where the select line logic comes from a single pole double throw switch.

Table A-3. eCAP Mux Select

Switch Position	McASP_Mux_Select Logic	Function
Pin 1	Pulled down to ground	non-eCAP signals connected
Pin 3	Pulled up to 3.3V	eCAP signals connected to the 4-pin header

   c. An additional single pole double throw switch was added to choose between the McASP-A CLK return signal and the eCAP

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2024) to Revision D (August 2024)	Page
• (Compliance): Added Compliance note for ESD	9

Changes from Revision B (February 2024) to Revision C (April 2024)	Page
• Added note about IO cables	4

Changes from Revision A (October 2022) to Revision B (February 2024)	Page
• Changed all instances of legacy terminology to controller and peripheral where SPI is mentioned	4
• Changed all instances of legacy terminology to POCI and PICO where SPI is mentioned	4
• Updated all instances of *TMDS273EVM* to *AM273xEVM*	4
• Added *Security* section	8

Changes from Revision * (November 2020) to Revision A (October 2022)	Page
• Added *Rev C. Design Changes* section to detail revision changes from Rev B to Rev C	37

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