

## **AM570x BGA Escape Routing**

This document provides a sample Printed Circuit Board (PCB) escape routing for the AM570x System on Chip (SoC).

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## 1 Introduction

The AM570x has multiple functions assigned to each pin, making it impossible to provide a single escape routing for all permutations of pinmux definitions. The escape presented here is based on the AM570x six-layer reference design and the pinmux defined for that design.

The strategy provided in this document is designed to help ensure a successful escape. Care must be taken to escape signals with the most layout constraints early in the routing process. This document does not address those constraints. For additional information on routing these signals, refer to the [High-Speed Interface Layout Guidelines](#). Care must also be taken to ensure a robust Power Delivery Network (PDN) is provided.

## 2 BGA versus VCA Package Type

Most Ball Grid Array (BGA) devices include a full array of balls in a regular grid pattern. For these devices, the expectation is that each interior pad has an adjacent via to route the signal to an inner layer. This full array of vias creates tight channels that only allow one trace to be routed between the vias. As the number of balls increase, the number of layers required to escape signals increases.

Via Channel™ Array (VCA) packages remove a few balls, creating larger channels without vias. These channels allow more traces to be routed, thereby reducing the number of layers needed for 100% signal breakout. The AM570x is a 25x25 VCA package with a ball pitch of 0.65 mm.

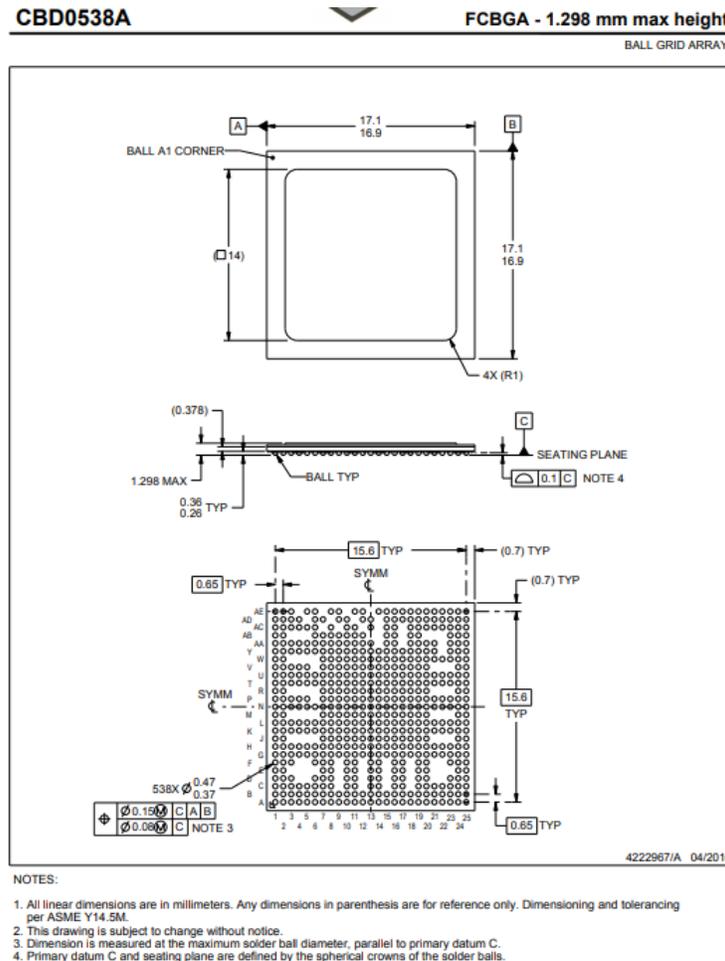


Figure 1. Package Drawing

### 3 Vias and Pads

#### 3.1 Ideal PCB Footprint

The ideal PCB footprint is described in the [nFBGA Packaging Application Report](#). The ideal ratio between the package via diameter on the package and the land diameter on the PCB is 1:1. The via diameter on the package is equivalent to the Solder Mask Opening (SMO) for the package, which is 0.350 mm for this device. Ideally, the diameter of the PCB pad would also be 0.350 mm.

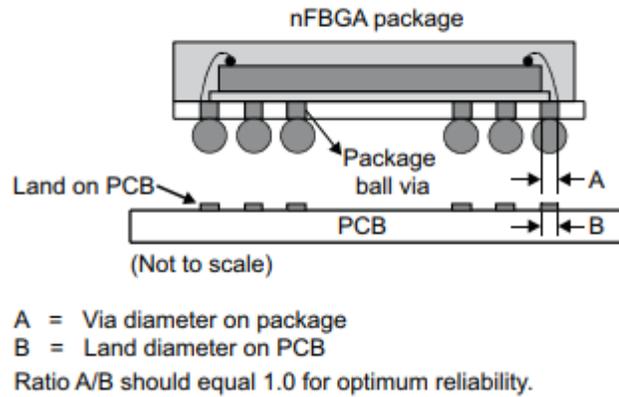


Figure 2. Package Via to Board Land Diameter Configuration

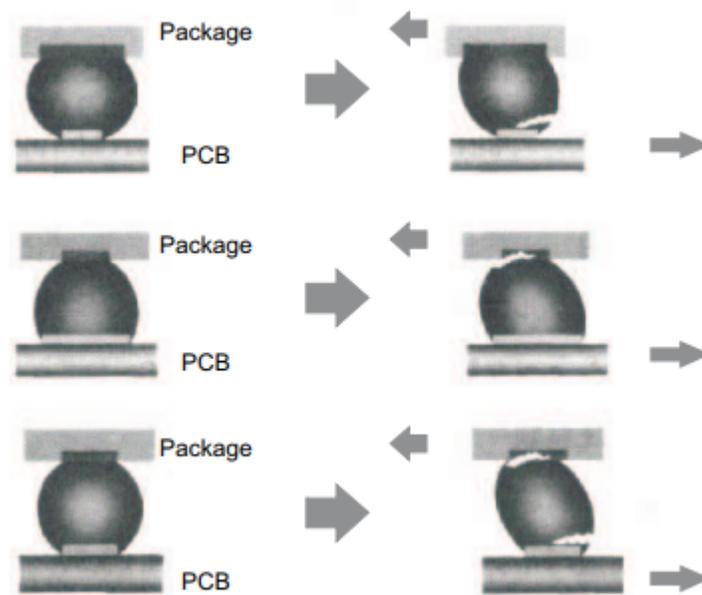


Figure 3. Effects of Via-to-Land Ratios

The ideal PCB pad size cannot be used with the 0.65-mm pitch if the signals must escape from under the part in six layers. If a 0.350-mm (13.77-mil) PCB pad is used, the space between the PCB pad and the annular ring for the via between the pads is reduced from 0.1065 mm (4.19 mil) to 0.0815 mm (3.19 mil). That requires reducing the spacing requirement to 0.0762 mm (3 mil) or requiring the use of a 6-mil drill. Either of these options would increase the cost of the PCB. This example presents a compromise to the ideal 1:1 package SMO to PCB pad ratio. Instead of a 0.350-mm PCB pad, a 0.300-mm pad is used. The 0.300-mm (11.8-mil) pad reduces the PCB pad size enough to allow the use of the 8-mil drill while maintaining the 0.1016-mm (4-mil) spacing.

### 3.2 *Via and Pad Properties for this Example*

The ball pitch of this device is 0.65 mm. To allow for a on-grid via placement, the following geometry is used for placing the vias and pads when creating the device PCB footprint. The following escape routing example described follows class 2 IPC performance classification for reliability and service expectations. The PCB via and pad properties for this example are shown in [Table 1](#).

Two spacing requirements must be maintained to support IPC class 2 reliability. 0.102-mm (4-mil) spacing must be present between all copper structures on the board. Copper structures include traces, pads, planes, and annular rings for vias. IPC class 2 does allow 90 degree breakout for vias. The 0.102-mm (4-mil) spacing between the via structure defined in [Table 1](#) allows sufficient tolerance to support this requirement. In addition, spacing between vias must be a minimum of 0.559-mm (22-mil) to accommodate the 90 degree breakout requirement.

**Table 1. Via and Pad Properties**

Items	Values [mm] (mil = 1/1000 inch)
BGA Package Ball Pitch	0.650 (25.6)
PCB Pad to Solder Mask Clearance, min	0.0508 (2.0)
Trace/Line Width, min	0.102 (4.0)
PCB SMO to PCB Land Diameter, Aspect Ratio	0.402/0.300 (15.8/11.8) 1:0.75
Via, Plated Through-Hole (PTH) Drill dia, min	0.203 (8.0)
Via, PTH Land dia, min	0.406 (16.0)
Via, PTH Anti-Pad (Plane Clearance) dia, min	0.965 (38.0)
Via, PTH Annular Ring Width, typ	0.102 (4.0)

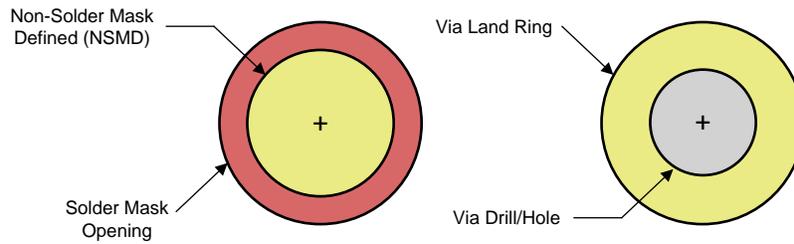
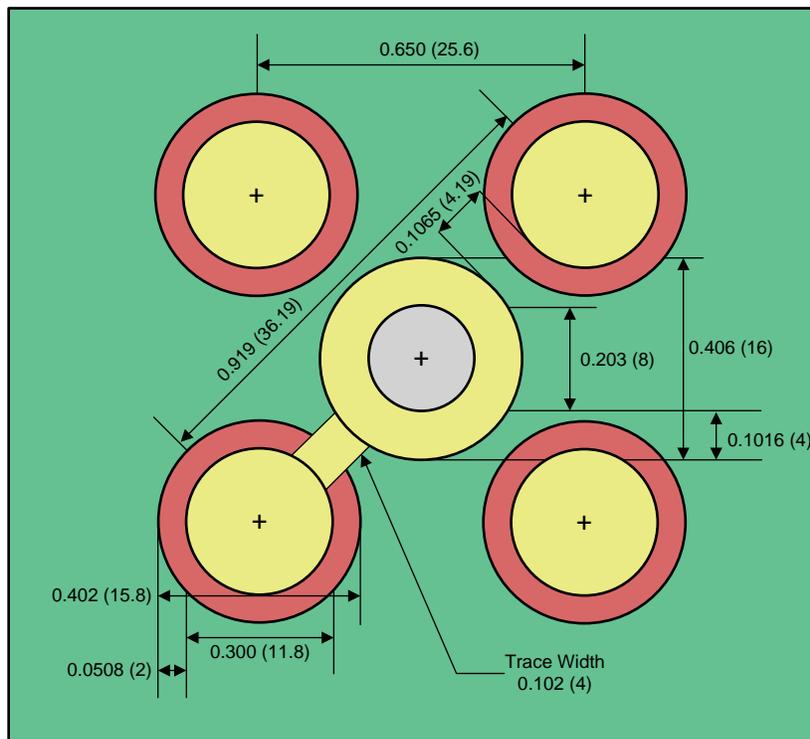


Figure 4. Via and Pad Dimensions

## 4 Stackup

The PCB layout designer must balance many different requirements when starting a PCB layout. The first is the board stackup. The AM570x device is available in a 17-mm × 17-mm package with a 0.65-mm pitch ball array of 25×25. The channels created by the VCA footprint allow the signals to be routed in a fewer number of layers. The example presented was routed using four signal layers and two power plane layers for a total of six layers, including the top and bottom of the board. This highly optimized route requires careful placement of components and uses portions of the internal routing layers for power planes needed by the AM750x. Some controlled impedance signals for the DDR are referenced to the ground plane and some are referenced to VDD\_DDR\_1V35 DDR I/O power plane. This complicates the DDR3 routing and requires additional simulation.

**Table 2. AM570x Reference Design Layers**

PCB Layer	Layer Use	Comments
Layer 1 – Top	Component Pads and Signal Routing	All signal escape for first two rows
Layer 2	Ground	
Layer 3	Signal Routing and Power	
Layer 4	Signal Routing and Power	
Layer 5	Power	Planes for multiple voltages
Layer 6 - Bottom	Signal Routing and Power	Capacitors and Connectors

A 6-layer stack-up similar to the one discussed here is extremely dense and requires more time to complete. When signals have escaped from the BGA array, the connected components must be spread apart to accommodate the lack of routing layers. Additional layers simplifies routing and allows components to be placed closer together, which may yield a smaller PCB with improved PDN and signal integrity.

It is not acceptable to violate routing rules to save money on reduced PCB layers or to reduce routing time. All requirements must still be met. In addition, creative routing increases design validation time for both simulation and bench testing. The AM570x reference design required careful simulation and numerous iterations to achieve success.

By contrast, the AM570x EVM is implemented in a 16-layer stack-up. That design has nearly every signal ball routed to circuitry or a connector. The additional layers were needed to meet the board requirements and the schedule available.

### 4.1 Floorplan Component Placement

Optimum trace routing has routes as short as possible with a minimum of cross-over while meeting all the constraints for length matching and timing associated with the peripheral interface. This requires careful placement of the components around the AM570x device. [Figure 5](#) shows the default arrangement of the signal balls and the power and ground balls. (It is understood that some of the interfaces can move to other locations due to pin multiplex choices, and that there are other interfaces not listed that are exposed through pin multiplex choices.) The PCB layout team must analyze the locations of the interfaces used and the associated components and connectors.

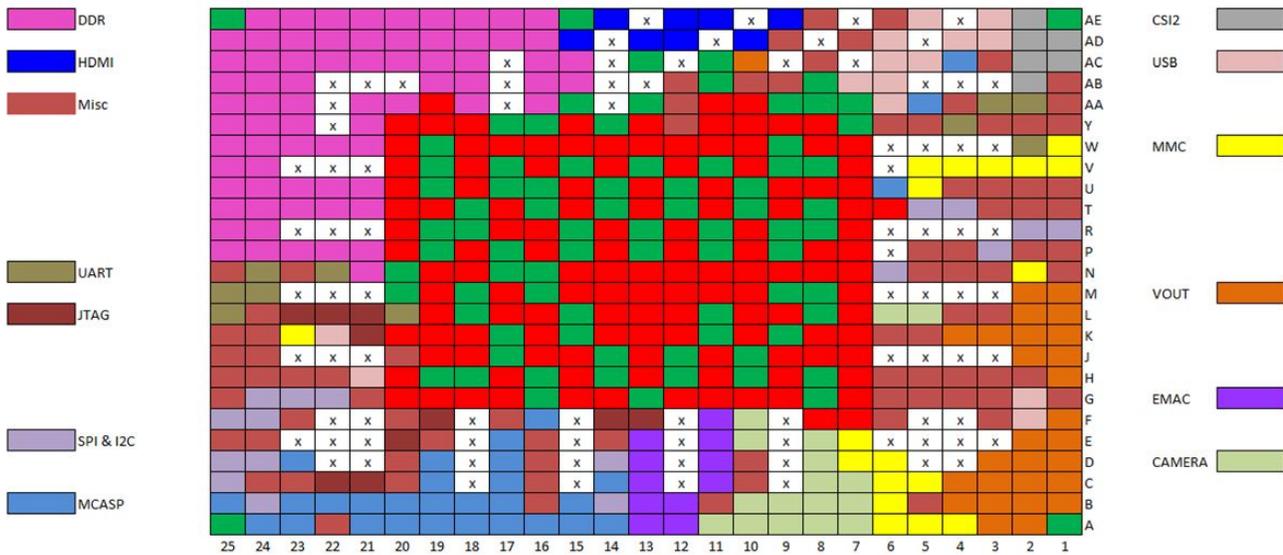


Figure 5. AM570x Floorplan

#### 4.2 Critical Interfaces Impact Placement

Placement of the AM570x device and some of the attached components or connectors is dictated by higher performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, routing distance limits may also determine component placement.

#### 4.3 Route Critical Interfaces

As indicated above, critical interfaces affect component placement options. When routing begins, these critical interfaces must be routed first. The design team must establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

Table 3 lists a recommended priority order for interfaces contained on the AM570x family of devices. Individual design requirements may cause this list to change somewhat but this provides a good baseline.

Table 3. Routing Priority

Interface	Routing Priority
USB, PCIE	10 (Highest Priority)
CSI2, HDMI	9
DDR	8
Power distribution	7
EMAC, MMC	6
Parallel Video, Camera	5
Clocks	5
SPI, McASP	4
EHRPWM	4
GPMP	2
GPIO	1
UART	1
I2C	1 (Lowest Priority)

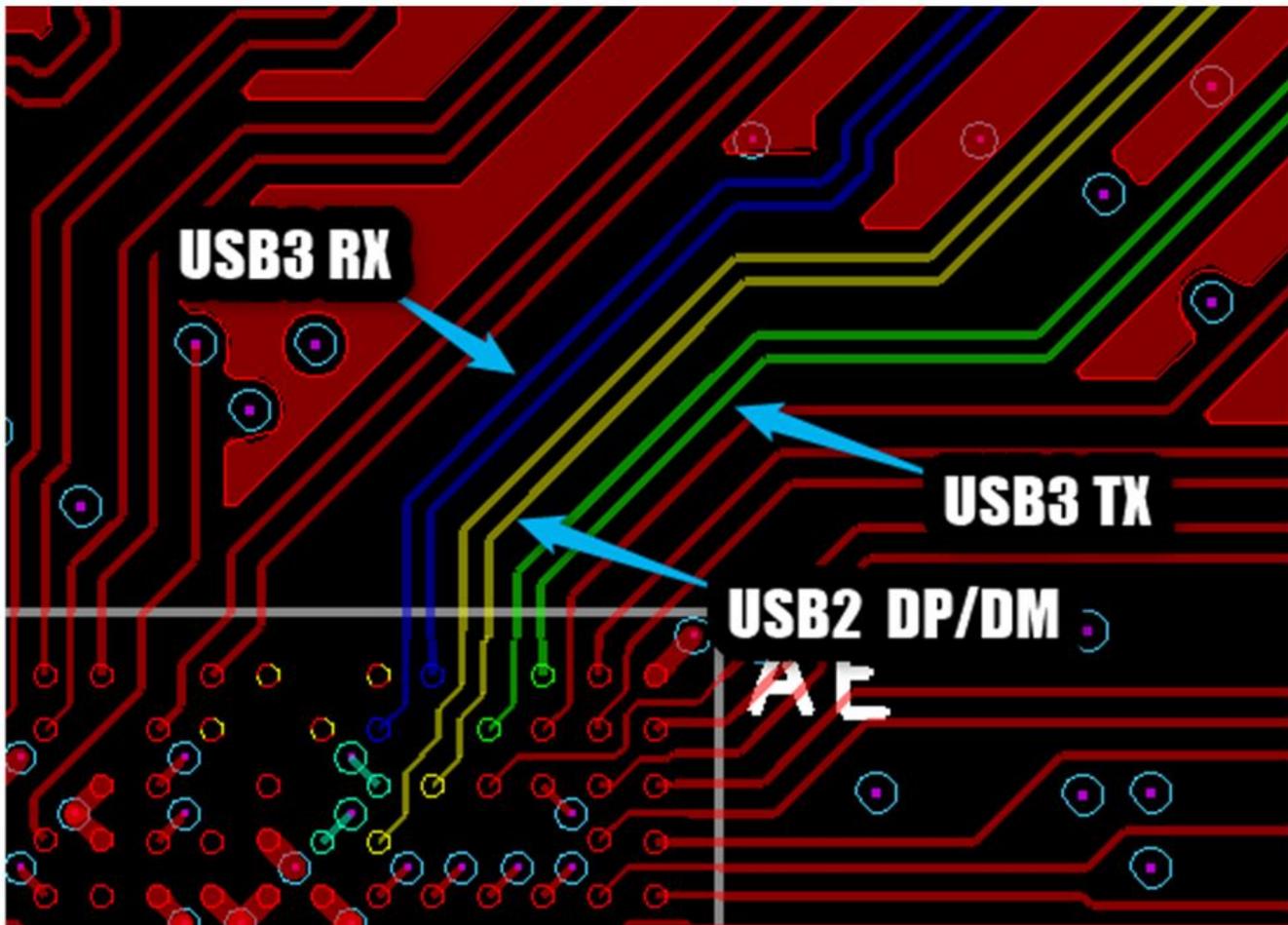
The placement of most of these should appear obvious. The multi-gigabit SERDES interfaces are the most critical due to their data rate and loss concerns. PCIe is at the top because it is sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the PCIe connector and the AM570x device. PCIe signals are assigned to balls along the edge of the BGA, allowing associated traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom of the priority list. This leaves synchronous and source-synchronous interfaces in the middle of the priority list, where they should be ordered by data rate. It is important to assign high priority to the PDN. Performance of the PDN is often ignored or given low priority, which can result in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry power and ground currents. Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.

#### 4.4 Route SERDES Interfaces

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. Most of the PCIe/USB3 SERDES interfaces are located on the outer two rings, allowing them to route away from the device without requiring vias. See below for the routing of the USB3 signals on the AM570x EVM on the top layer. The open channel provided by the missing balls for AE4 and AD5 allow the USB2 signals, needed for the USB3 connector, to be escaped on the top layer as well. The trace widths must narrow as they approach the device to allow them to pass between the pads. Wide traces limit signal loss, so trace width is dictated by signal loss and impedance requirements.

The PCIe signals are not routed as part of the reference design but the pads are highlighted. Some optimization of the surrounding signals would allow PCIe to route on the top layer as well.



**Figure 6. USB3 and PCIe Escapes**

## 5 CSI2 and HDMI Differential Pairs

In addition to the SERDES signals, the AM570x includes differential pairs for the HDMI interface and the CSI2 interface. These are also found on the outer two rings, and should be routed away from the device on the top layer. As with the SERDES signals, the traces for the differential pairs narrow when routing under the device, but should be widened as soon as they are escaped to achieve the desired signal loss and trace impedance. Because all the differential pairs and SERDES signals are controlled impedance, a ground layer must be placed on layer two to act as a reference. The pairs should be spread apart as soon as space allows to avoid crosstalk.

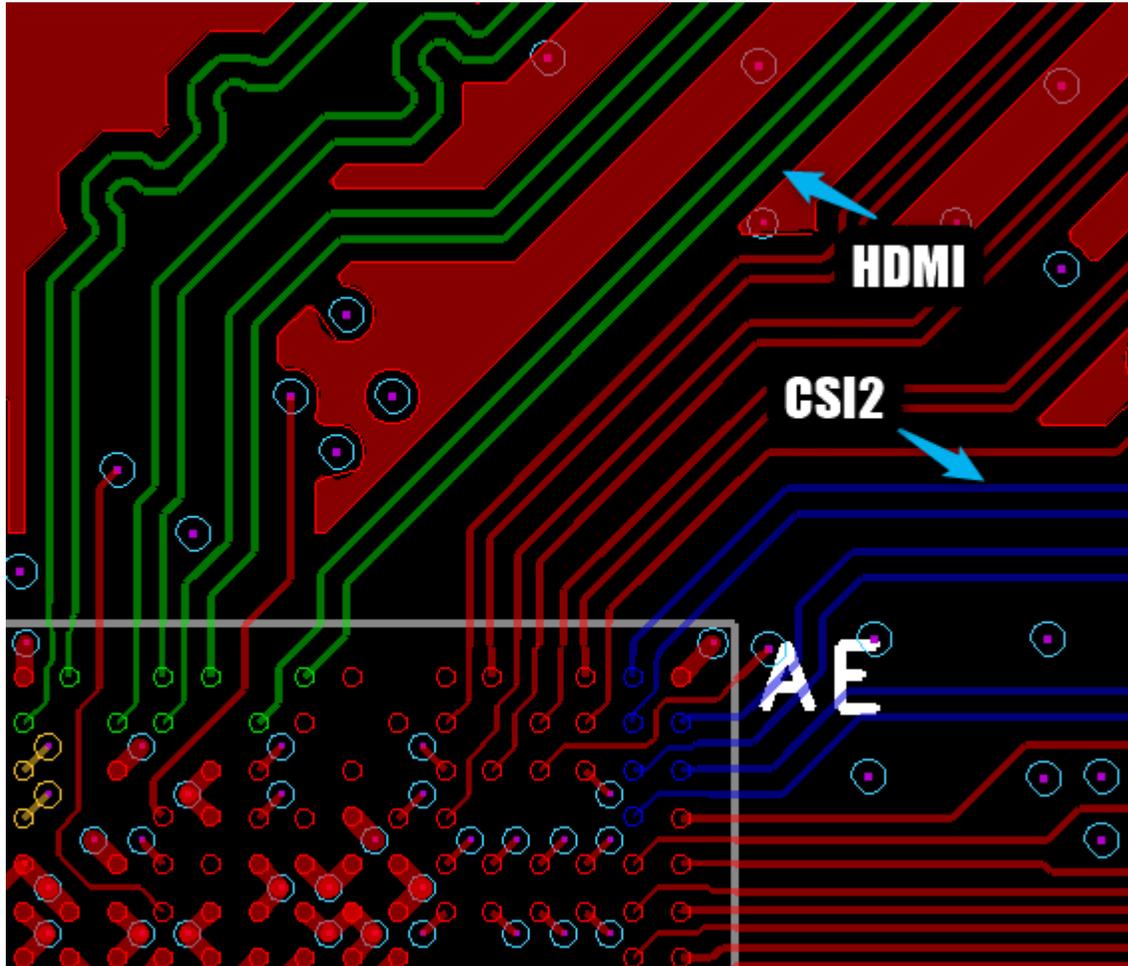
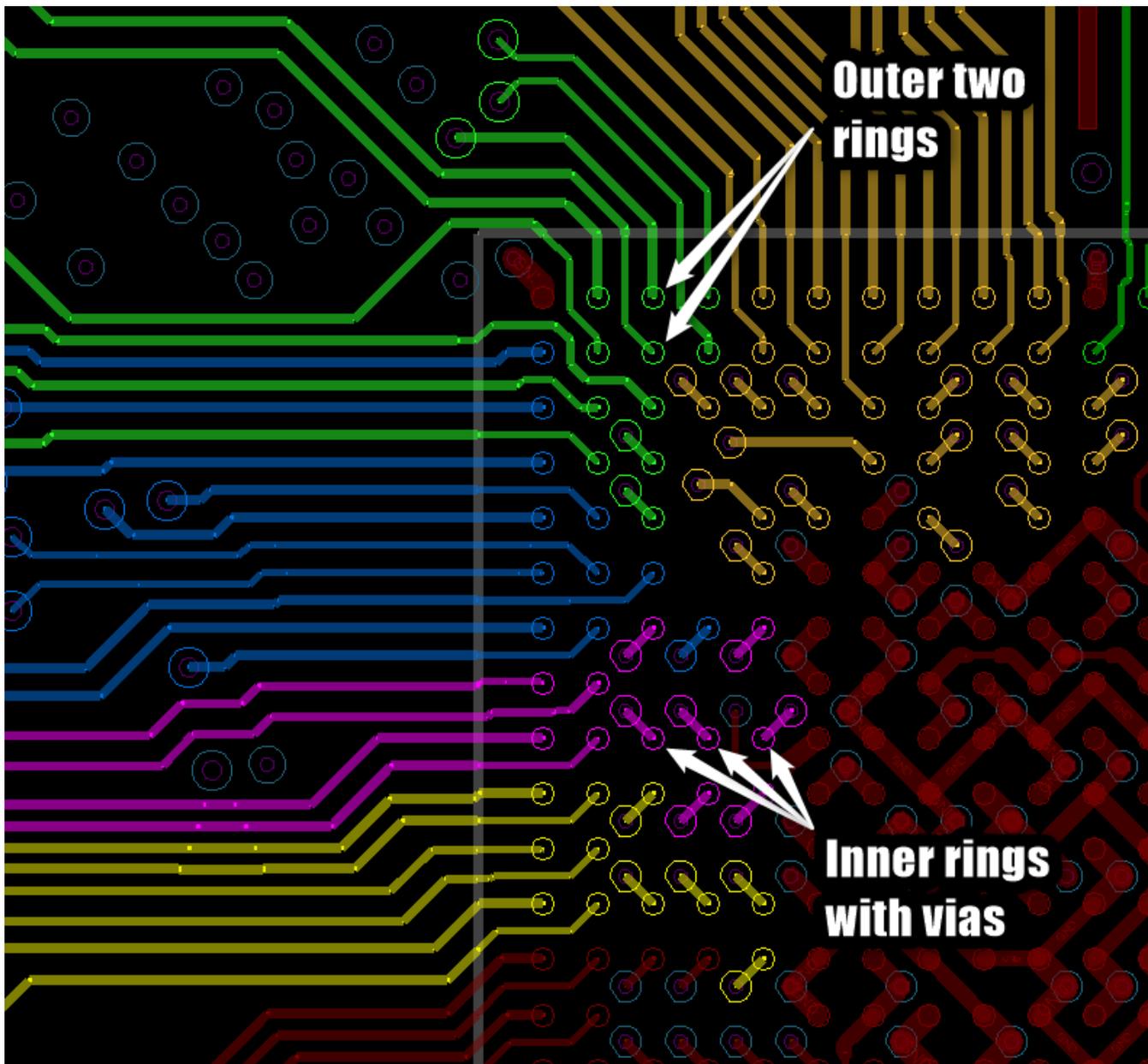


Figure 7. HDMI and CSI2 Escapes

## 6 Routing DDR Signals

The AM570x supports connection to DDR3 and DDR3L devices. The DDR signals must be routed next. Refer to the [AM570x data sheet](#) for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR3 on the AM570x reference design. The routing for DDR3 and DDR3L use an identical escape.

All signals on the first two rings should be routed away from the device on the top layer to a sufficient distance to provide routing channels for the interior rings. An example of the DDR routing for the top layer is shown in [Figure 8](#).



**Figure 8. Top Layer Signal Routing**

The interior rings use vias with the dimensions described above to route the signal to an inner layer. Positioning vias in areas where pads are not present creates a routing lane, which allows three traces to be escaped through the channel on each signal layer.

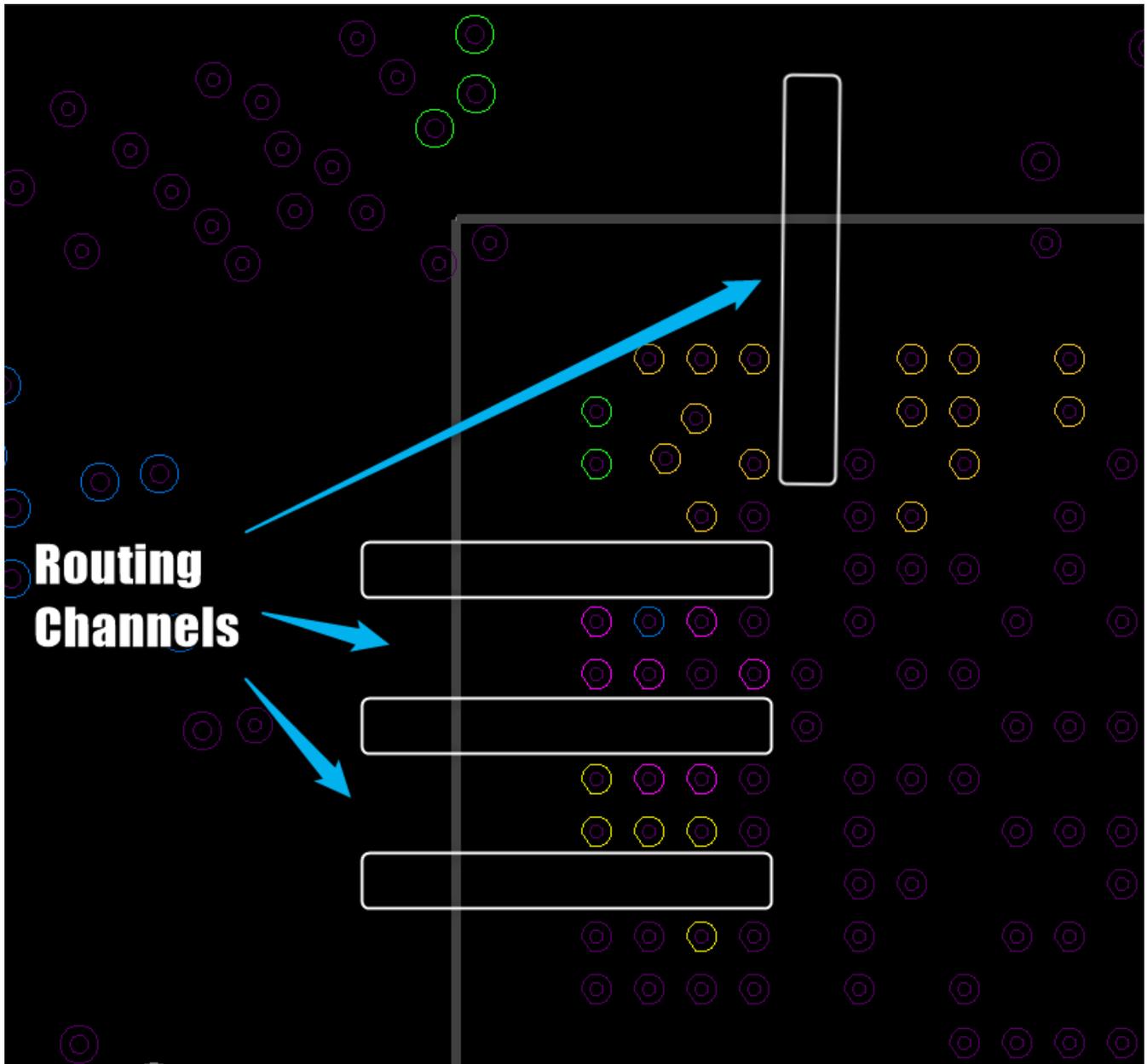
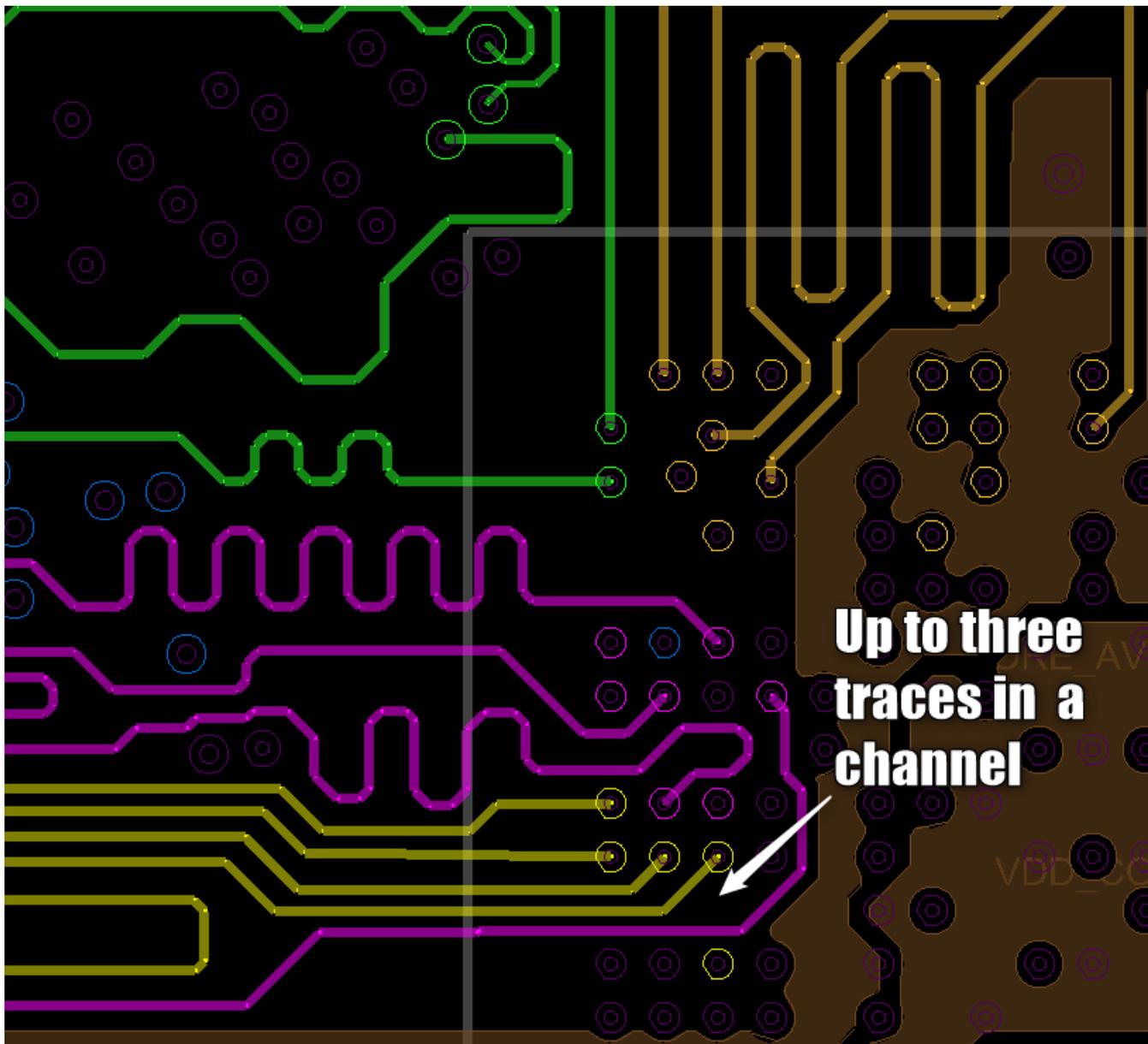


Figure 9. Via Placement and Routing Channels



**Figure 10. Inner Layer Routing**

### 6.1 Address/Command Routes

The DDR3 SDRAM memory devices should be arranged so that the data pins are closest to the AM570x device. This lets the data group nets have the shortest possible routing. The Address, Command, and Control signals operate at half the bandwidth of the data so they are expected to be longer. In the reference design, two 16-bit DDR3L devices are placed to the left of the device, with the data balls closest to the AM570x.

The address command signals are routed up from the AM570x and then across to the first memory device. Address/command signals are routed in a fly-by fashion from the AM570x, to the first device, then to the second device and finally to the terminating resistors. JEDEC allows Address, Command, and Control signals to be routed adjacent and referenced to the VDD\_DDR\_1V35 voltage plane based on the understanding that these nets operate at half the clock rate.

## 6.2 Data Group Routes

The data groups are routed point-to-point between the AM570x and respective pin of the memory device. Ideally all the signals in a data group should be routed on the same layer but that is not possible with a 6-layer design. The data group signals must be length matched as described in the data manual. You must compensate for the difference in propagation speed when some signal traces of a data group are routed as microstrips on a surface layer, while others are routed as stripline on an interior layer. Because individual data routing groups are dispersed onto multiple routing layers, the delay introduced by via barrels may also need to be included as part of length matching.

The next four images show DDR routing on four signal layers of the reference design. All DDR signals must be routed adjacent to a continuous reference plane, preferably a ground plane. The reference design uses a ground plane on layer 2 and a solid VDD\_DDR\_1V35 plane on layer 5. Using VDD\_DDR\_1V35 as a reference plane and using a combination of microstrip and stripline traces requires extensive simulation to ensure a positive result.

This example uses VDD\_DDR\_1V35 as a reference plane to implement a 6-layer PCB. This design approach may limit the maximum DDR data rate. Signal integrity is degraded when signals are referenced to the VDD\_DDR\_1V35 plane, because this increases the impedance of return current paths. The impedance of the return path can be minimized by placing decoupling caps between the VDD\_DDR\_1V35 and ground planes as close as possible to any via in the route where the reference shifts between VDD\_DDR\_1V35 and ground. This allows return current to transition back to the ground reference plane.

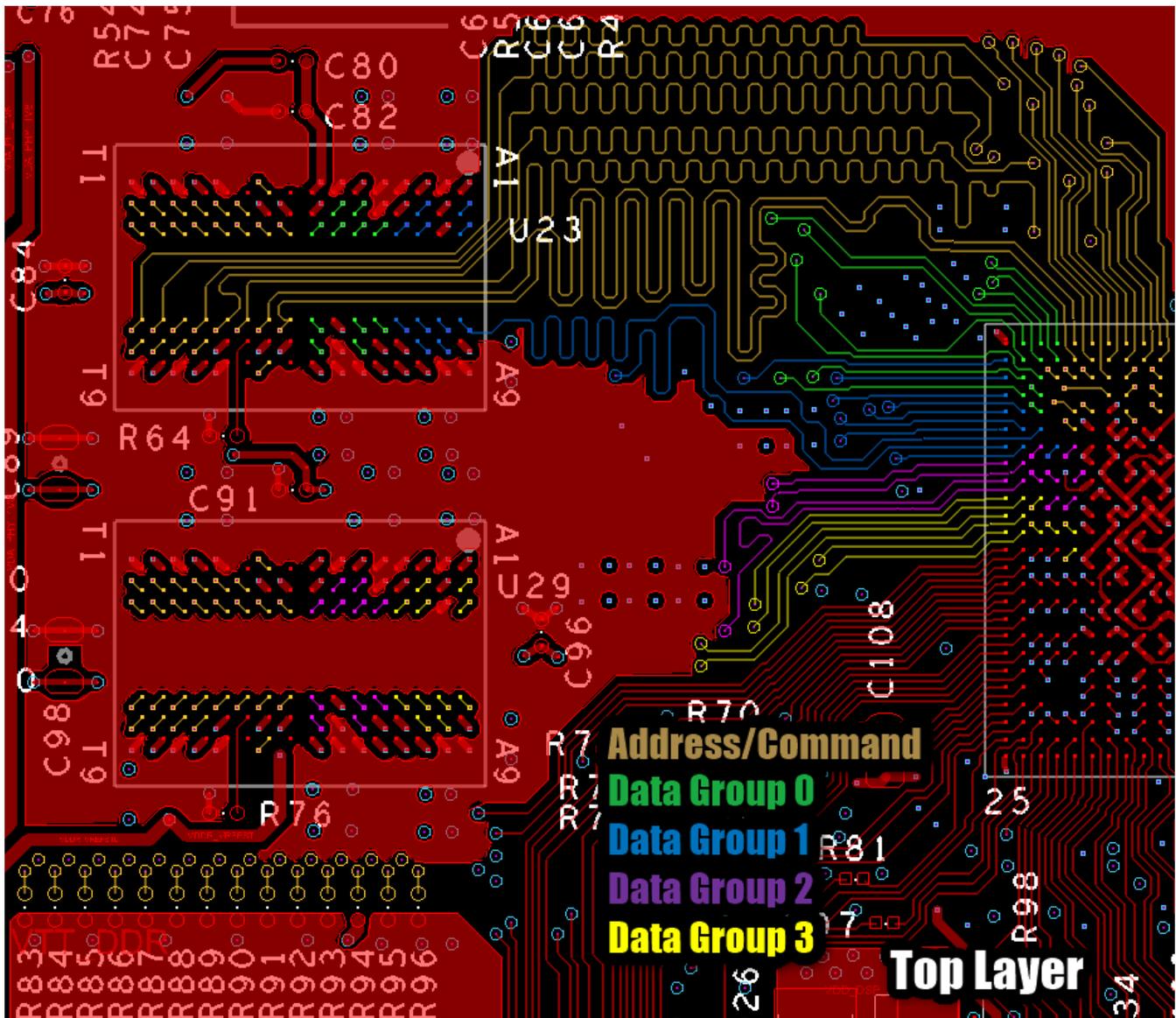


Figure 11. DDR Routing Top Layer



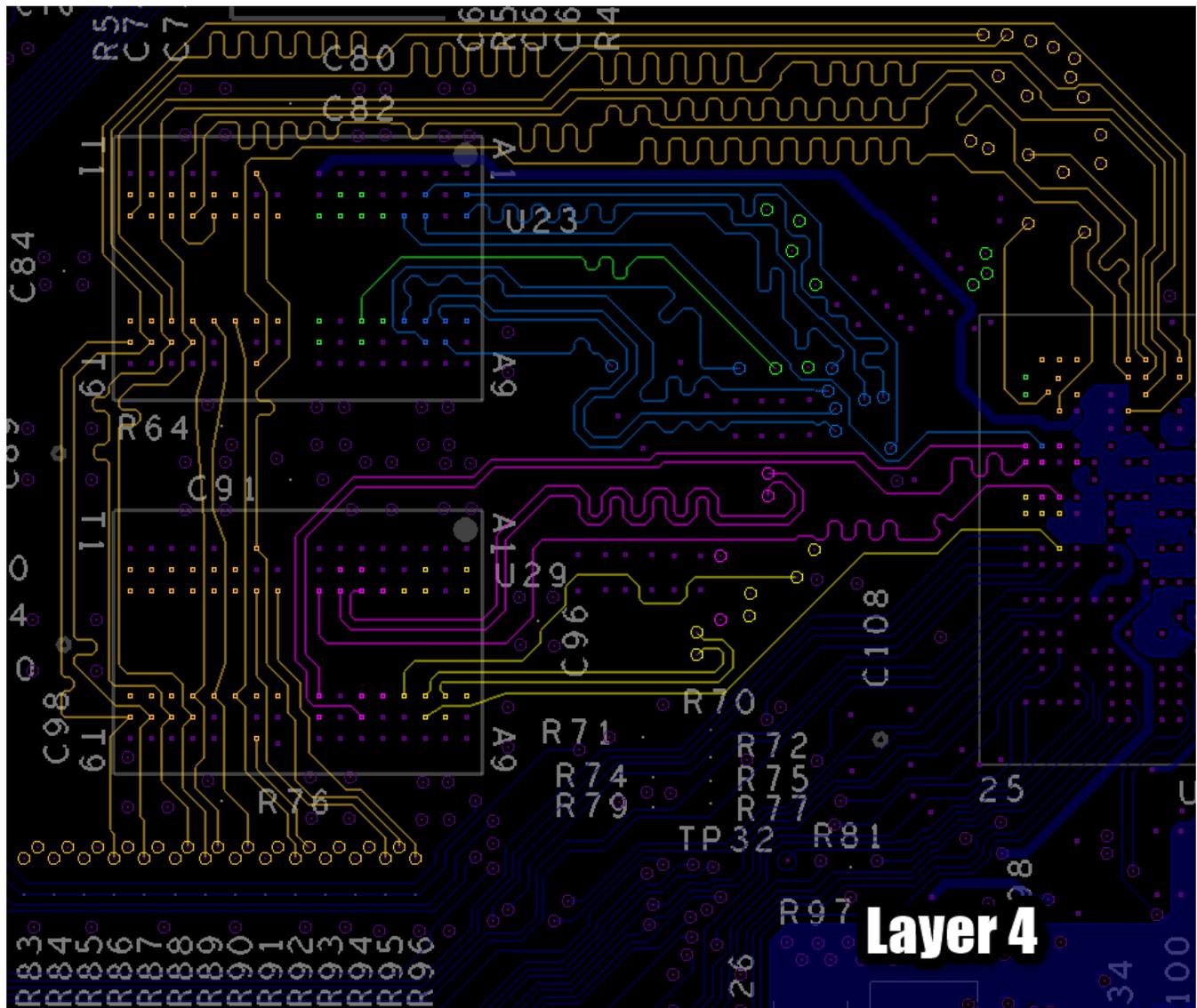


Figure 13. DDR Routing Layer 4

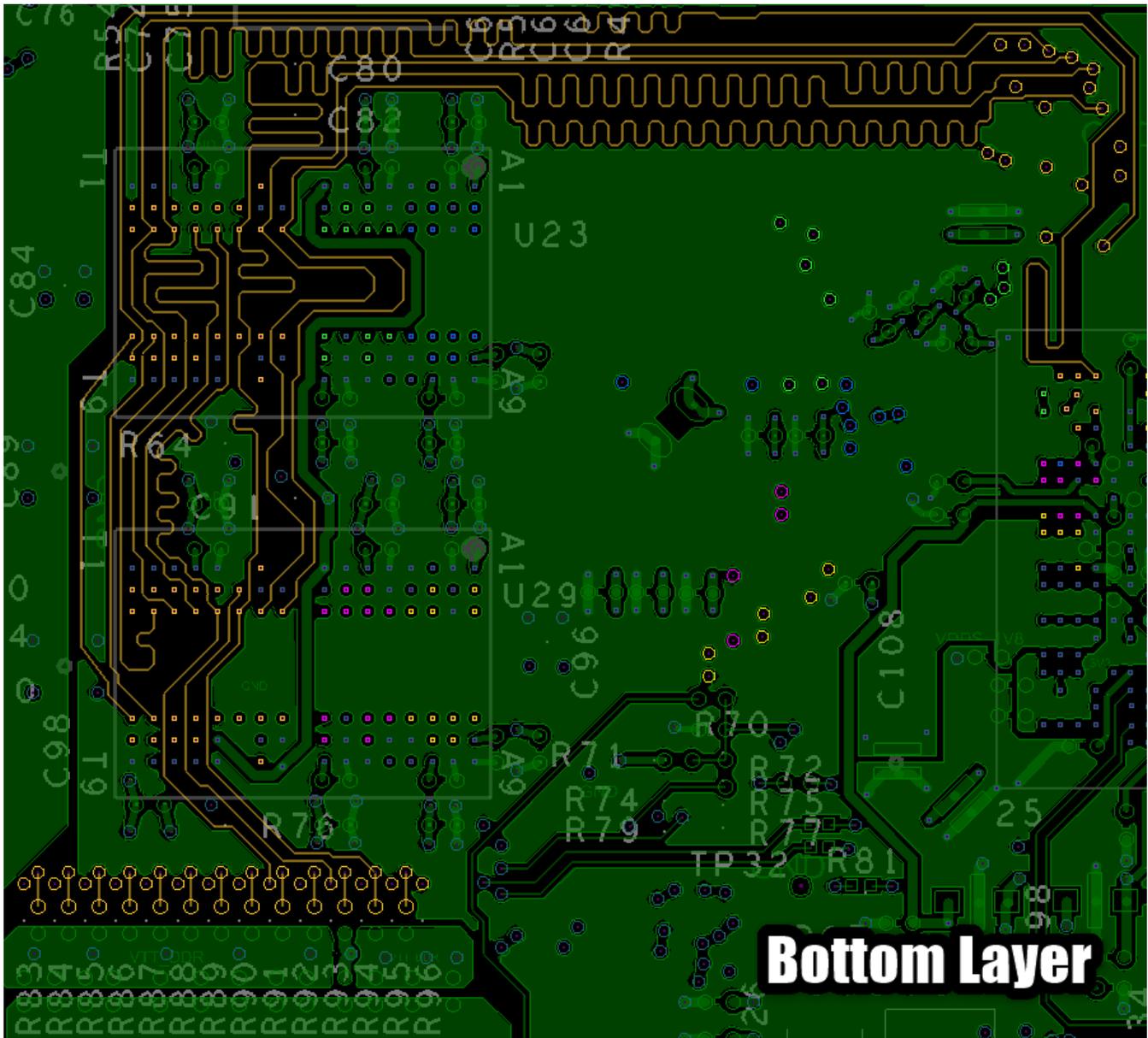


Figure 14. DDR Routing Bottom Layer

## 7 Power Planes and Decoupling

The higher priority synchronous and source synchronous interfaces and PDN connectivity should be routed after the SERDES and DDR interfaces. TI strongly recommends completing all SERDES and DDR routing before routing other interfaces. The PDN portion of the PCB design, including supply decoupling, must be completed before PCB simulations can be executed for the SERDES and DDR routes. The highest speed source-synchronous interfaces, such as RGMII and other high speed interfaces like QSPI and eMMC, may also require simulation. Power supply planes and ground planes must be in place for these simulations as well.

### 7.1 Decoupling under the Device

The power and ground pads in the center of the device form a solid array of pads. Ideally, each pad should have a dedicated via, but with a 0.65-mm pad spacing this is not possible. To create some space on the back side of the PCB to place decoupling capacitors under the BGA device, pads must share a via. [Figure 15](#) shows the routing of the VDD\_CORE\_AVS and the GND power planes on the top layer. You can see that a pattern with a via adjacent to two pads is repeated to create open areas on the bottom of the PCB, to make room for a capacitor. These triangular patterns are also connected with a trace, and the vias are connecting to an internal plane.



Figure 15. Via Sharing on the Top Layer

This approach provides enough room for several decoupling capacitors, which are necessary due to the lack of space for vias around AM570x due to the density of traces on the top layer.

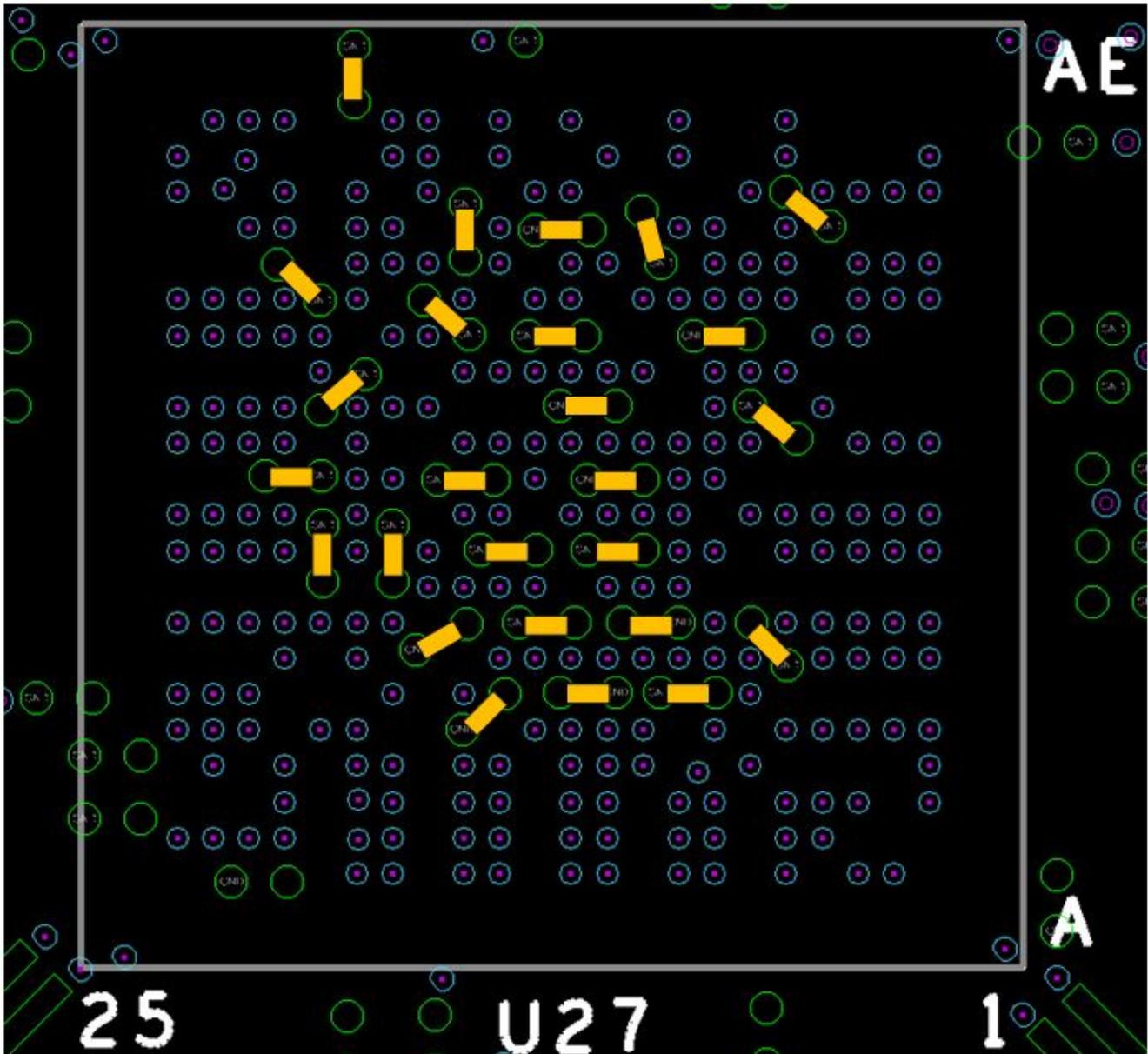


Figure 16. Bottom Layer Capacitors

## 7.2 Decoupling around the Device

Additional bypass capacitors can be placed near AM570x when there is enough room to place vias associated with these capacitors. Placing these capacitors on the back of the PCB minimizes the impact to the top layer routing. In the reference example, these additional capacitors use reverse geometry footprints and a pair of vias for each pad to reduce inductance.

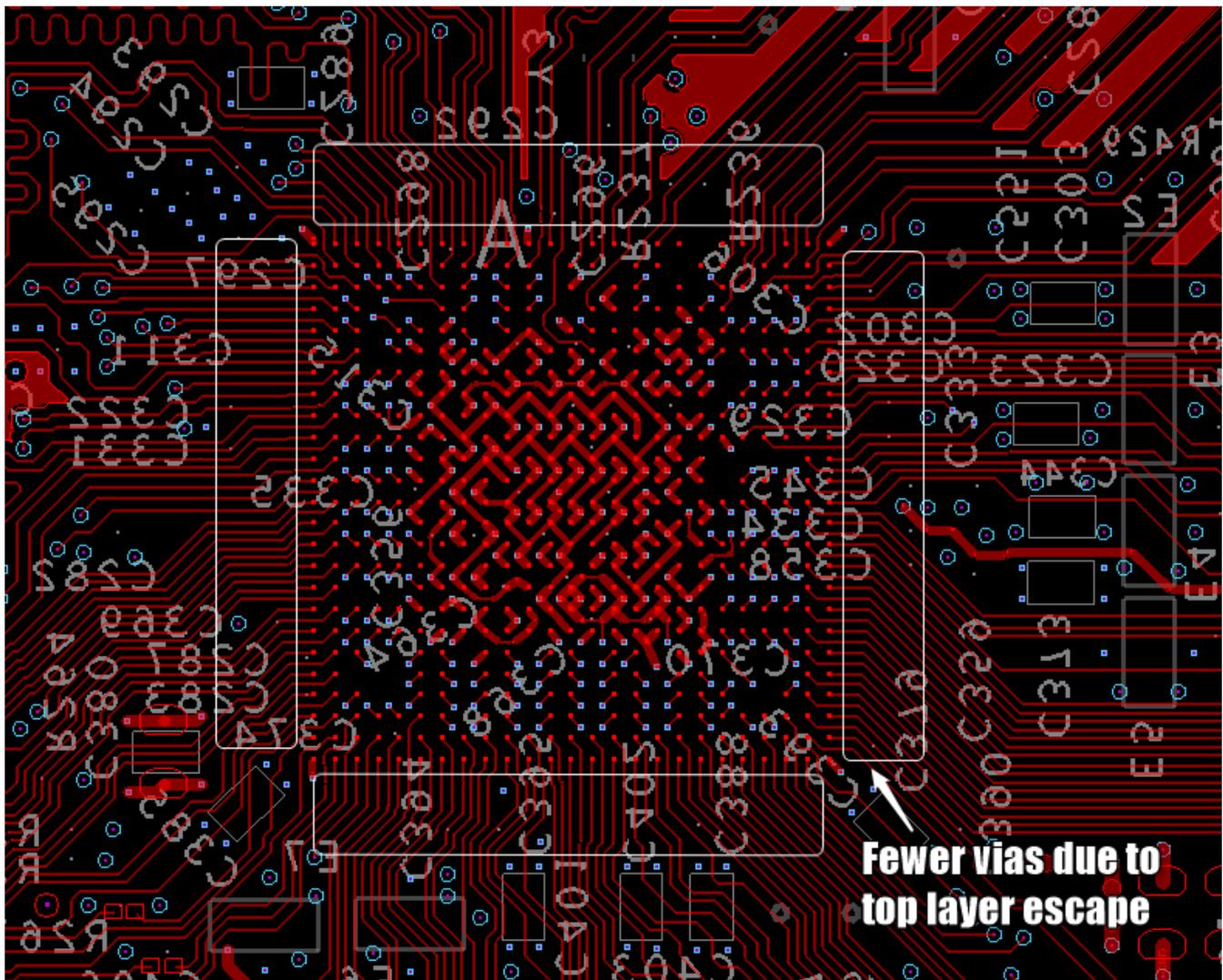


Figure 17. Limited Via Area Around AM570x

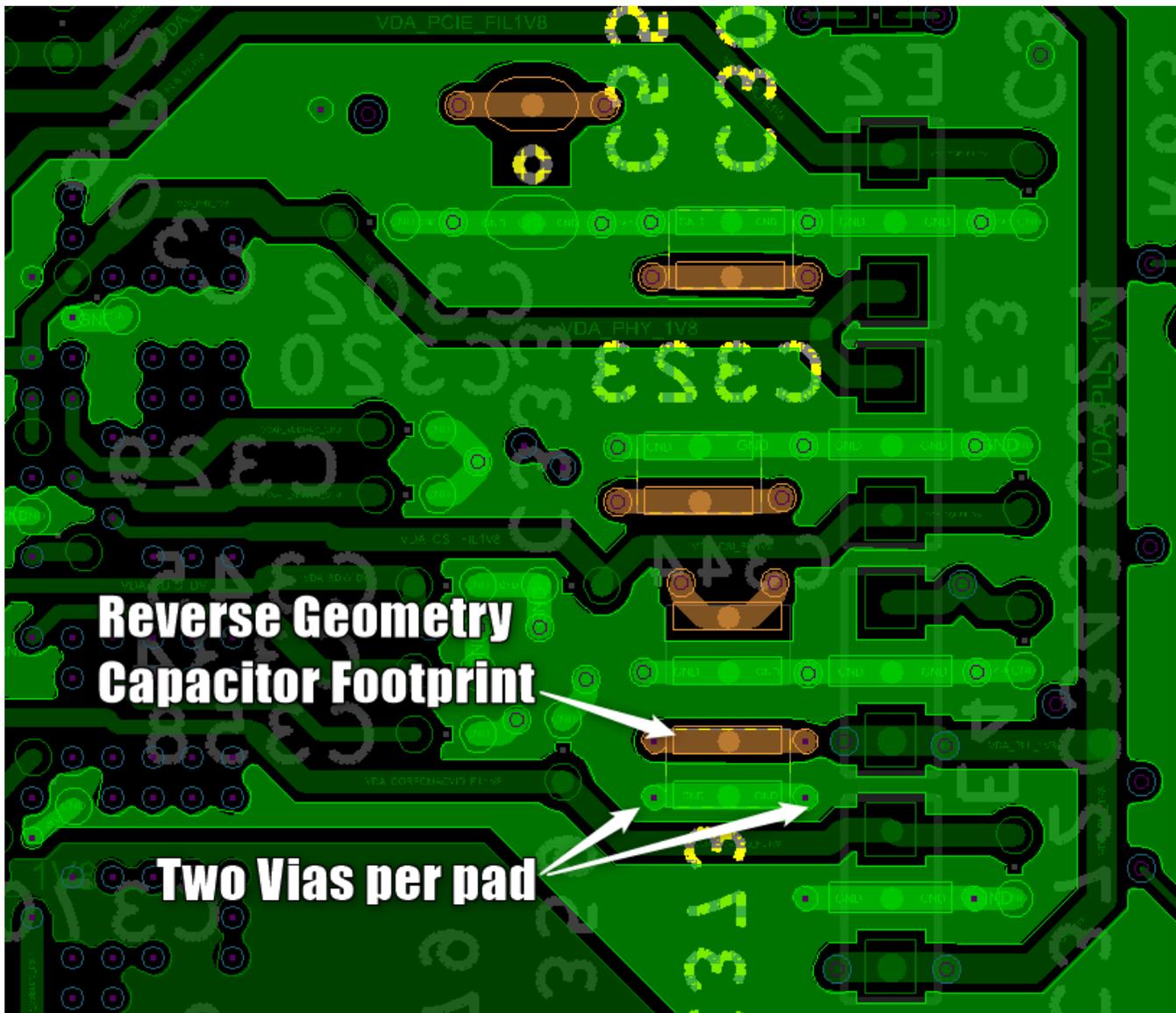


Figure 18. Reverse Geometry Capacitors

Placement, routing, and capacitor values should be checked by performing a PDN analysis on each power supply route. A lack of space on the board is not a sufficient reason for a poor PDN result. If additional capacitors are needed, add layers or increase the size of the board to create the necessary space for capacitors.

### 7.3 Power Planes for the Device

The reference design for AM570x is routed on six layers with four layers defined as signal layers, one power layer and one ground layer. Although the power layer is segmented into many power planes, it is not sufficient for all power planes required by this PCB design. Looking at the internal routing layers 3 and 4, there are several small power planes on those layers, especially under the AM570x. Power pads should not be connected to power supplies with traces. Sufficient power planes under the device should be included for each AM570x power supply rail. This may limit the space available on the inner layers for routing signals away from the device. If six layers are not sufficient to create the necessary power planes in your design, additional layers may be necessary.

## **8 Route Lowest Priority Interfaces Last**

When the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, the layout can continue with the medium and then the lower priority interfaces.

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