66AK2Gxx BGA Escape Routing

User's Guide

Literature Number: SPRUI95A
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1.1 Stackup

The PCB Layout designer needs to balance many different requirements when starting a PCB layout. The first is the board stackup. The 66AK2Gxx device has a 21 mm × 21 mm package which has a 0.80mm pitch ball array of 25 × 25. To minimize cost, this ball grid is nearly a solid array. Due to the number of rows of signal balls around the periphery, designs will need to have 2 routing layers not counting the top and bottom layers which can also contain some signal routes. Also, due to the number of power supply rails, there will need to be 2 layers dedicated for power planes. Ground planes will need to be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. Therefore, designs that route out all of the signal balls will need a 10-layer stackup similar to the following:

Table 1-1. TBD

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads and signal routing
Layer 2	Ground
Layer 3	Signal routing(1)
Layer 4	Ground
Layer 5	Power
Layer 6	Power
Layer 7	Ground
Layer 8	Signal routing(1)
Layer 9	Ground
Layer 10	Component pads (including most decoupling) and signal routing

(1) Bracketing the signal routing between two ground planes eliminates broadside coupling to prevent crosstalk problems.

A 10-layer stack-up like the one discussed above will be needed for relatively dense PCBs. Alternately, the layer count can be reduced assuming one or more of the following exist:

- The PCB is not crowded around the 66AK2Gxx device. This allows for more routing away from the device on the top and bottom layers which can reduce layer congestion.
- Many of the signal balls are unused. Many designs will not use all of the interfaces resulting in unused signal balls. This also reduces routing congestion.
- The PCB layout team has time to carefully place the routes. Note that this can be very time consuming.

It is not acceptable to violate routing rules simply to save money on reduced PCB layers or due to limited routing time. All requirements must still be met. Also, creative routing will increase design validation time - both in simulation and bench testing. This can be minimized if the layout is similar to one of the 66AK2Gxx EVM design.

The 66AK2Gxx EVM is implemented in a 10-layer stack-up similar to the one described above. This design has nearly every signal ball routed to circuitry or a connector. This drives the requirement for the full number of layers. Additionally, this board is designed for optimum signal integrity on the high speed interfaces while limiting the board size. The 66AK2G02 EVM is implemented without an HDI (High Density Interconnect) board using micro vias on both the top 2 and bottom 2 layers. All vias on the 66AK2Gxx EVM pass completely through the board. This complicates the escape from the BGA.

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1.2 Floorplan Component Placement

Optimum trace routing will have routes as short as possible with a minimum of cross-over. This requires careful placement of the components around the 66AK2Gxx device. The figure below shows the default arrangement of the signal balls as well as the power and ground balls. (It is understood that some of the interfaces can move to other locations due to pin multiplex choices and that there are other interfaces not listed that are exposed through pin multiplex choices.) The PCB layout team will need to analyze the locations of the interfaces used and the associated components and connectors.

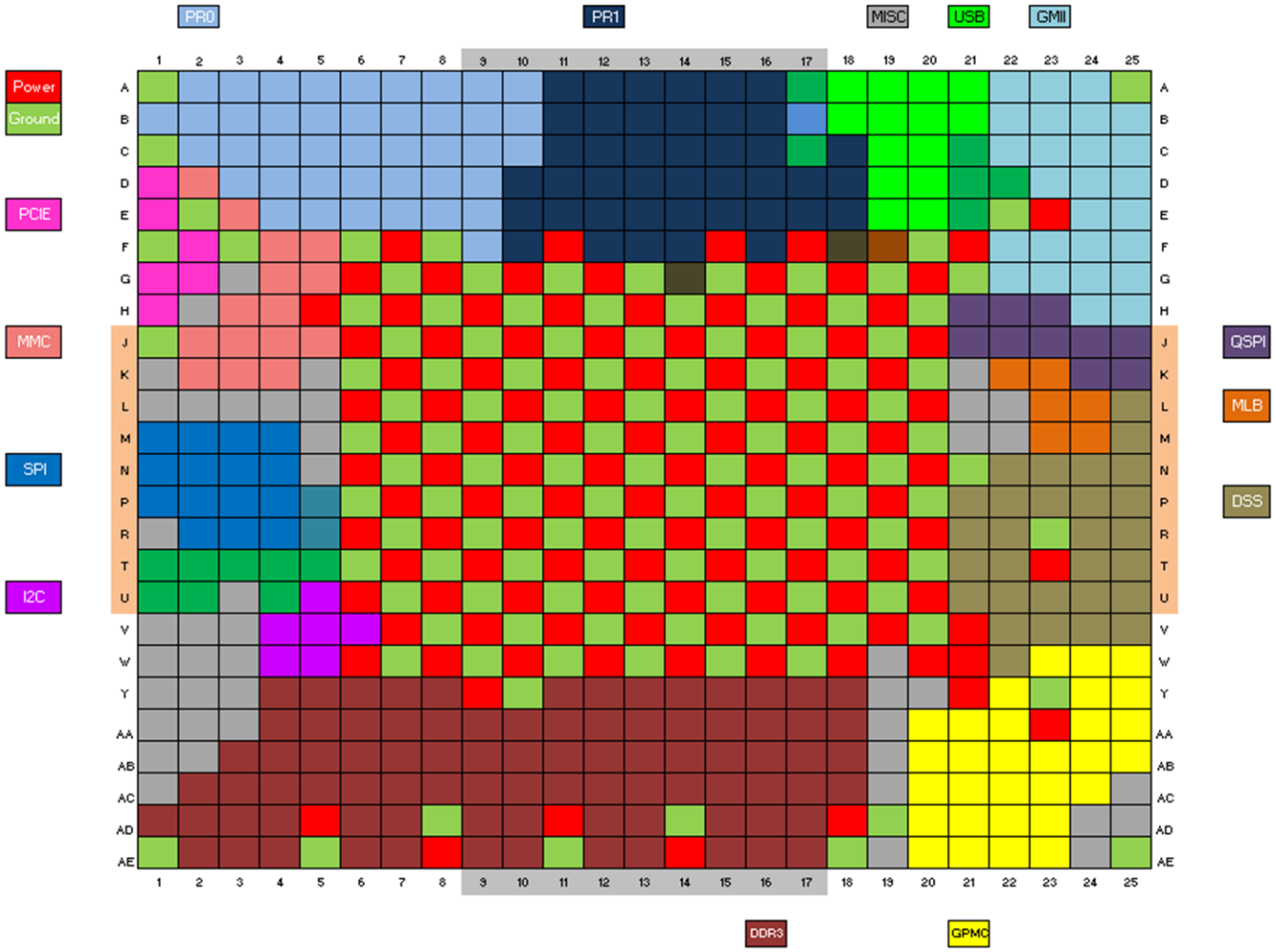

Figure 1-1. Interface Positions

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1.3 Critical Interfaces Impact Placement

Placement of the 66AK2Gxx device and some of the component and connectors will also be dictated by some of the highest performance interfaces. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

1.4 Route Critical Interfaces First

As indicated above, critical interfaces will affect component placement options. Then when routing begins, these critical interfaces must be routed first. The design team needs to establish a priority for the different interfaces. Those with higher priority must be completed before implementing those of lower priority. PCB layout teams often waste considerable effort ripping up and re-routing traces for lower priority interfaces when deficiencies are found in the routing of more critical interfaces. Always complete routing for the critical interfaces first.

The table below lists a recommended priority order for interfaces contained on the 66AK2Gxx family of devices. Individual design requirements may cause this list to change somewhat but this provides a good baseline.

Table 1-2. Routing Priority

Interface	Routing Priority
PCIe	10 (Highest Priority)
DDR3	9
USB2	8
Power distribution	7
RGMII	6
QSPI	6
Parallel Video	5
eMMC	5
Clocks	5
MII / RMII	4
SPI	4
Motor control	4
Analog audio	3
GPMC	2
GPIO	1
UART	1
I2C	1 (Lowest Priority)

The placement of most of these should appear obvious. The multi-gigabit SERDES interfaces are the most critical due to their data rate and loss concerns. PCIe is at the top since it is very sensitive to PCB losses. The limited length for these routes might affect the PCB placement of the PCIe connector and the 66AK2Gxx device. PCIe signals are found on the outside layer of the BGA footprint allowing the traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. It is often left to last. This then results in poor decoupling performance and current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling needs to be allocated before routing the middle and low priority interfaces.**

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1.5 Route SERDES Interfaces First

The previous section highlighted priorities for the PCB routing. The BGA ball map is also arranged to support routing the highest priority interfaces first. You will notice that most of the PCIe SERDES interface is located on the outer row to allow these to route away from the device without requiring vias. See below for the routing of the PCIe Lane 0 signals on the 66AK2Gxx EVM on the top layer.

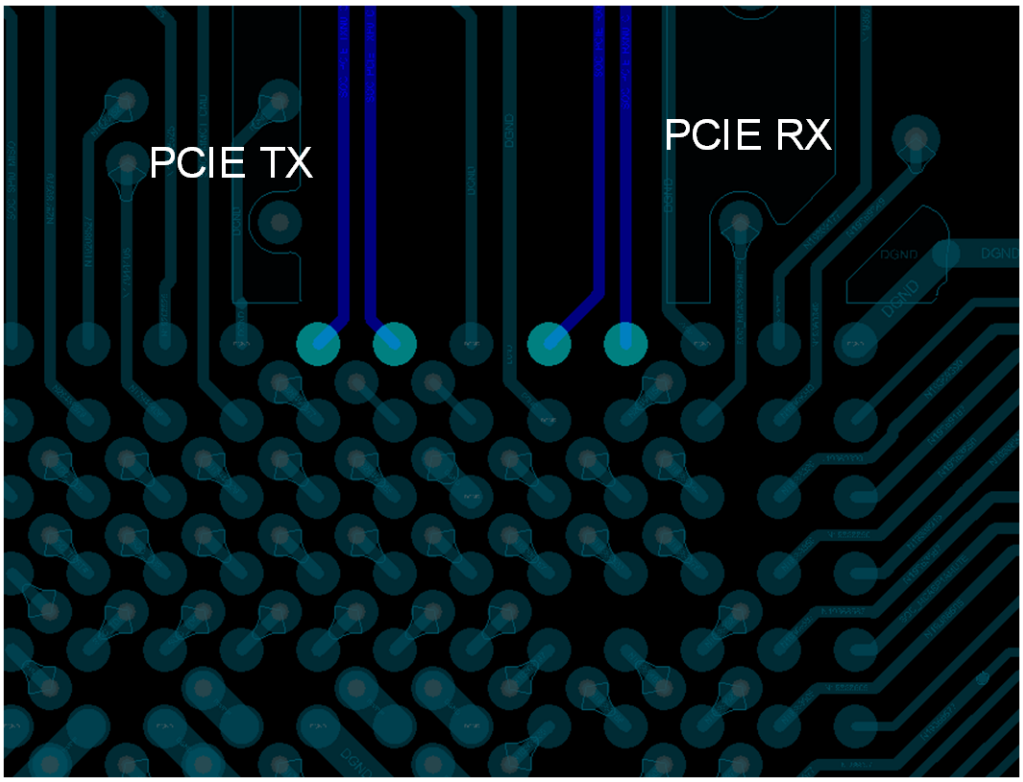

Figure 1-2. SERDES Signal Escape Routing

1.6 Route DDR3 Signals Next

The DDR3 signals need to be routed next. See the 66AK2Gxx data sheets for detailed recommendations for DDR3 routing. The images below show the BGA breakout for the DDR3 on the 66AK2Gxx GP EVM.

The DDR3 SDRAM memory devices should be arranged so that the data group balls are closest to the 66AK2Gxx device. This will allow the data group nets to have the shortest possible routing. The Address, Command and Control signals operate at half the bandwidth of the data so they are expected to be longer.

1.6.1 Data Group Routes

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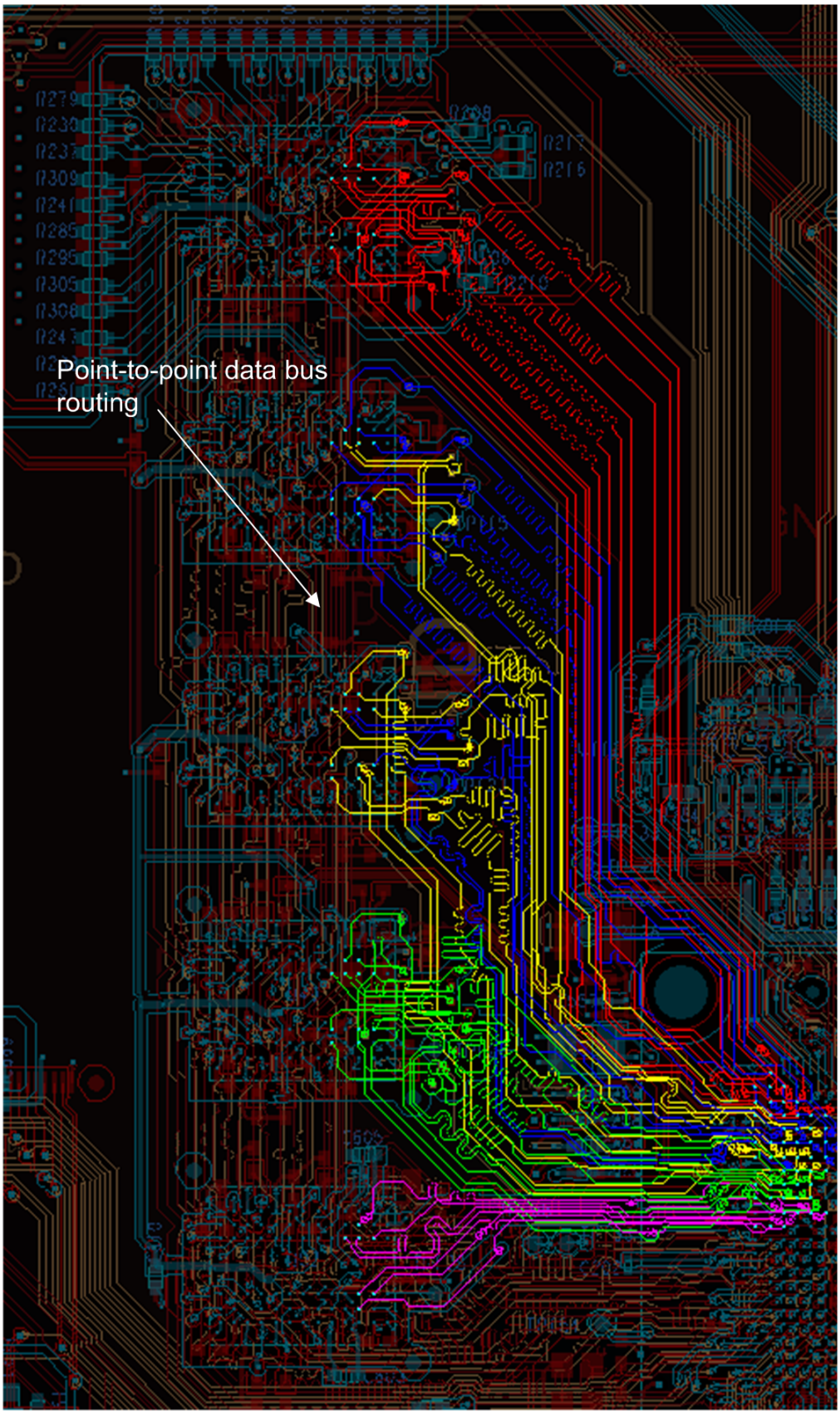

Figure 1-3. DDR3 Data Group Routing

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The following image shows escape of the signals on the top layer of the board. Note that most of the routing is not on the top layer. Signals will travel through traces routed on the top and bottom layer will travel at different speed then traces routed on internal layers. This difference must be included in the length matching calculations. Ideally, all DDR3 signals should be routed on internal layers.

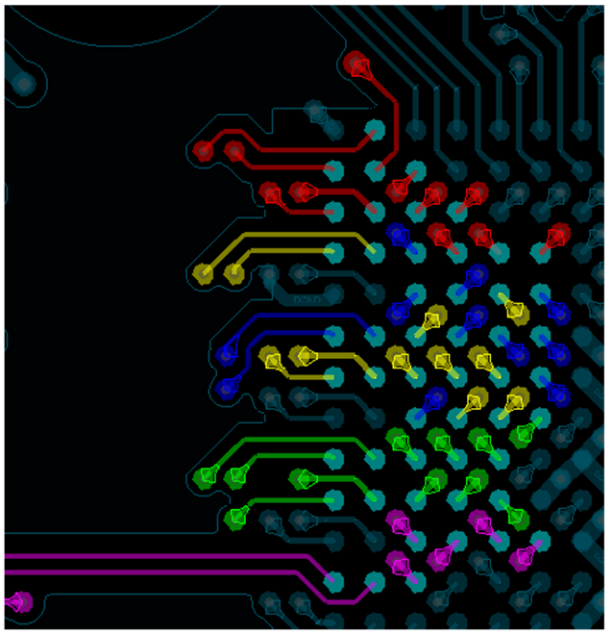

Figure 1-4. DDR3 Data Group Top Layer Escape

The following image shows the routing under the BGA on layer 3. Ideally the odd lanes should be routed on the same layer. The area between the vias for the even lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 3 to escape most of byte lane 1 and all of byte lane 3. Some of the signals from byte lane 2 are also present on this layer.

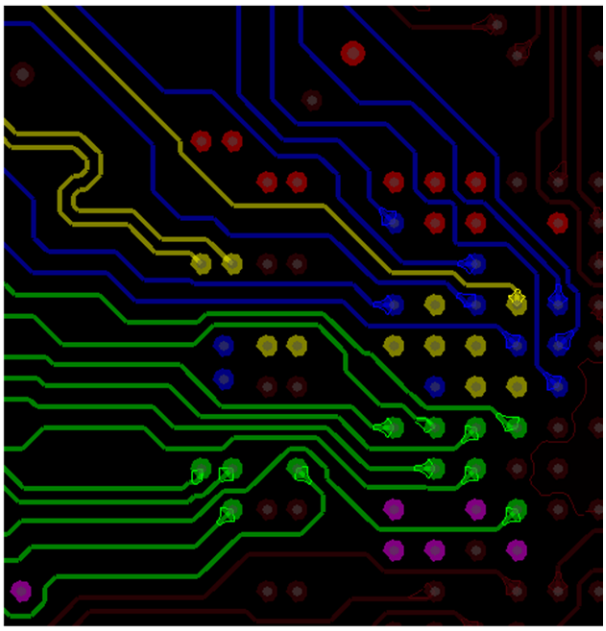

Figure 1-5. DDR3 Data Group Layer 3 Escape

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The following image shows the routing under the BGA on layer 8. Ideally the even lanes should be routed on the same layer. The area between the vias for the odd lanes can be used to escape signals that are in rows closer to the center. The EVM used layer 8 to escape most of byte lane 2and all of byte lane 0 as well as the check byte signals. Some of the signals from byte lane 1 are also present on this layer.

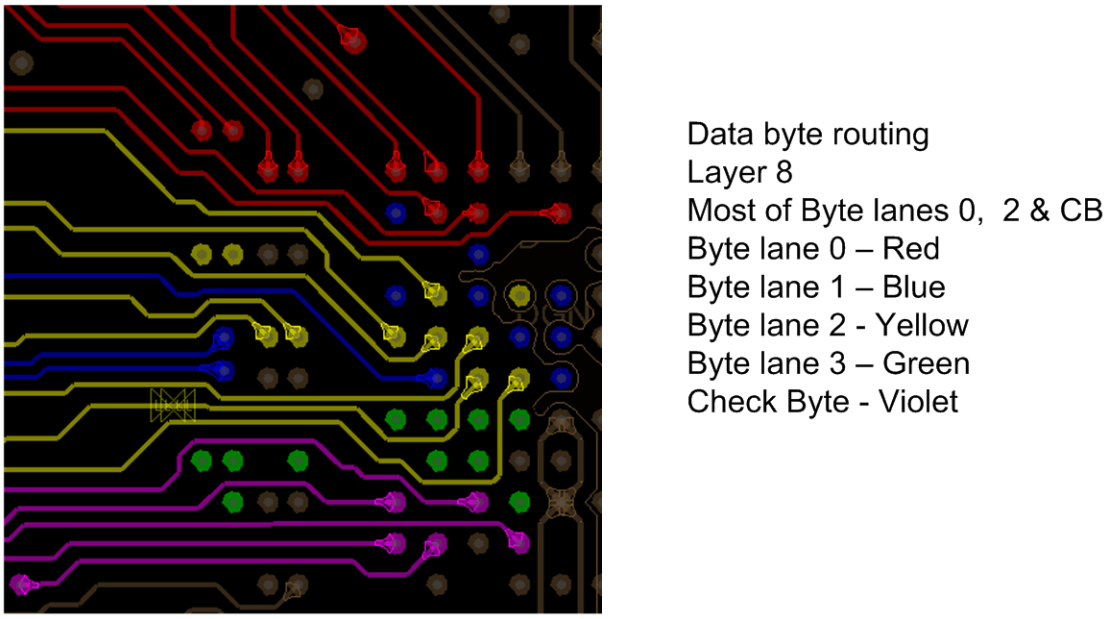

Figure 1-6. DDR3 Data Group Layer 8 Escape

1.6.2 Address, Command, Control and Clock Group Routes

The address, command and clock signals are routed in flyby starting with the check byte memory and moving up to byte lane 0. The VTT termination resistors are placed at the end of the trace past the byte 0 memory device.

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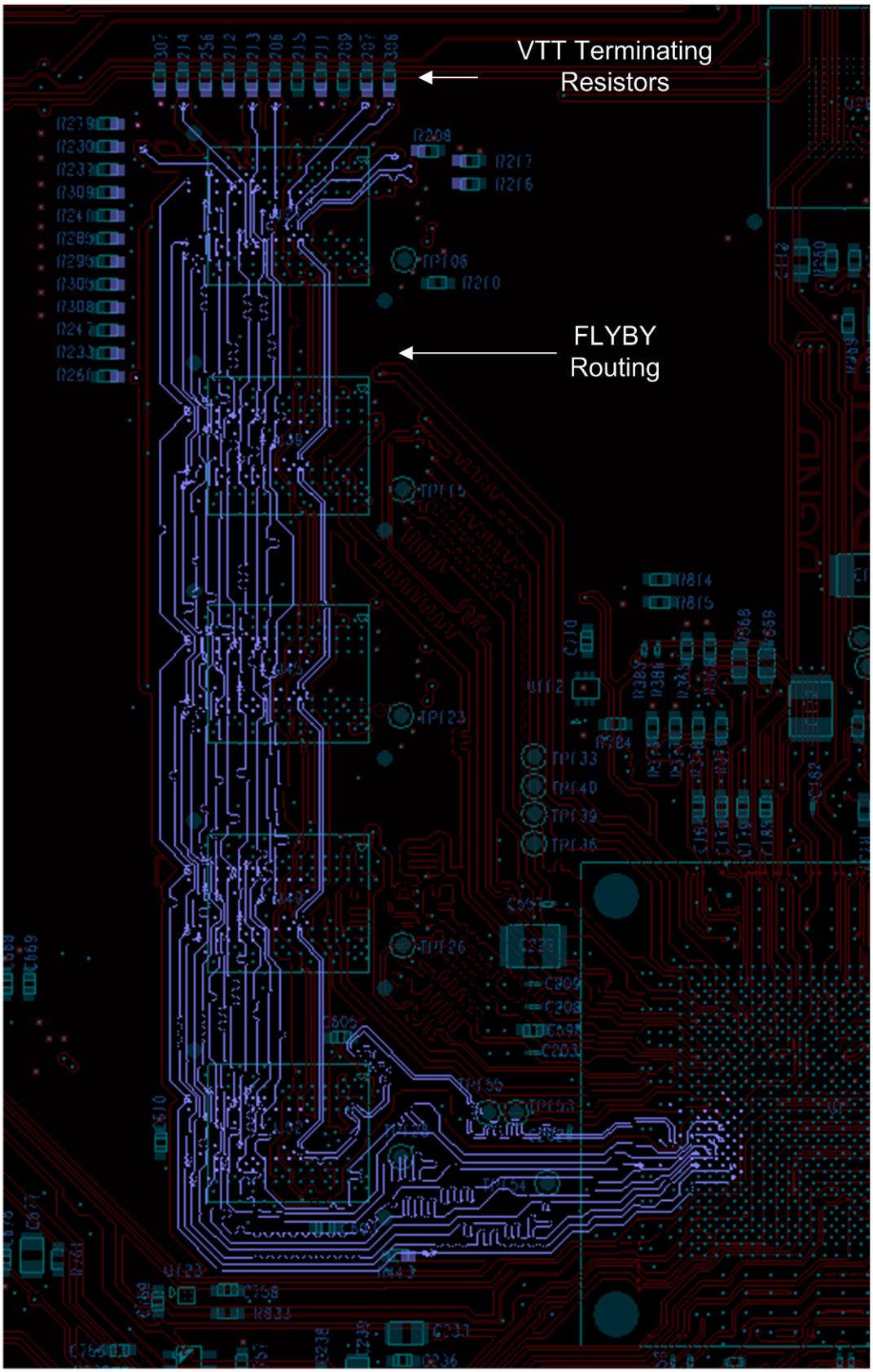

Figure 1-7. DDR3 Address/Command Group Flyby Routing

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The layers 3, 8 and 10 are used to escape and route the address and command signals. The signals must be length matched to ensure that the signals arrive at each memory at the same time. Length matching must be from the SoC to each memory individually including the stub to the memory pad. Simply matching the length of each trace from beginning to end is not sufficient. The speed difference between the signals routed on the bottom layer and the internal layers must also be taken into account.

The escapes of the address and command signals for these three layers are shown below.

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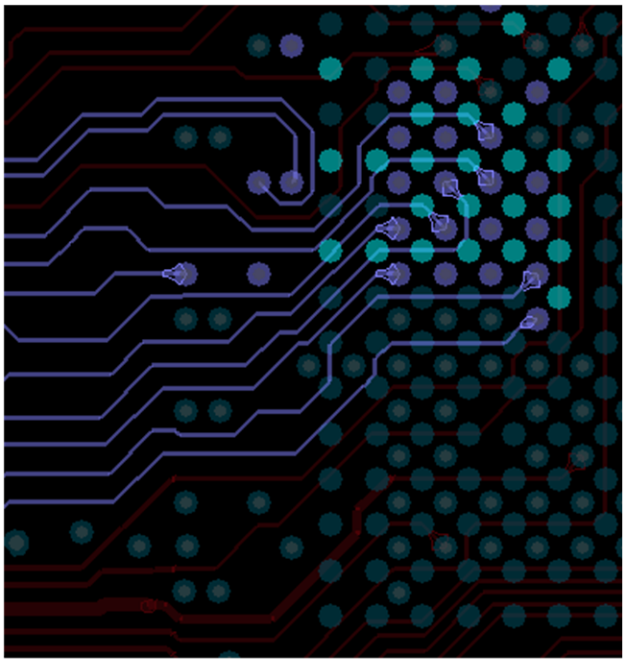
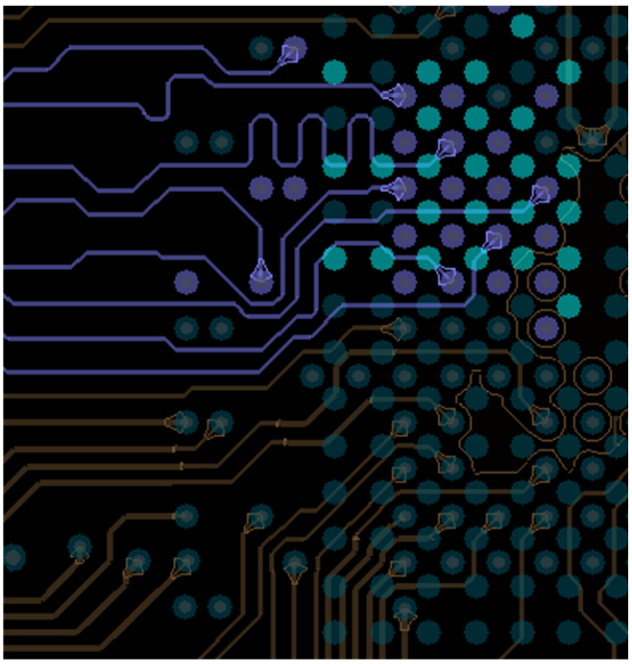
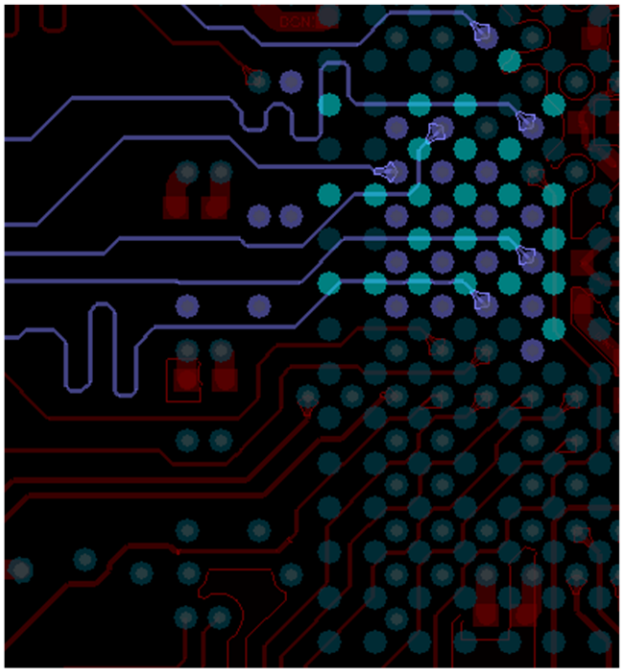


Address/Command signals
Top & Layer 3

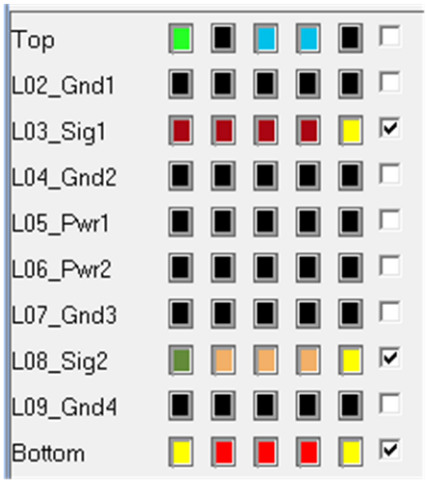


Address/Command signals
Top & Layer 8



Address/Command signals
Top & Bottom (Layer 10)

Highlighted Address/CMD signals
Teal – SOC pads
Violet – Vias and traces



Board Stack-up
Address/Command routed
on layer 1, 2, 8 & 10

Figure 1-8. DDR3 Address/Command Group Escape

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1.6.3 Complete Power Decoupling Next

The middle priority interfaces and the power distribution planes and pours would be routed next after the SERDES and DDR3 interfaces. It is strongly encouraged to complete all SERDES and DDR3 routing before continuing with other interfaces. Note that the power distribution planes and pours and all of the decoupling will need to be placed before PCB simulations are executed for the SERDES and DDR3 routes. The highest speed source-synchronous interfaces like RGMII and QSPI may also require simulation so these may need to be completed at this time as well.

1.6.4 Route Lowest Priority Interfaces Last

Once the length matching and simulations have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision	Page
• Changed 66AK2G02 to 66AK2Gxx.	2

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