TMS320DM36x
Digital Media System-on-Chip (DMSoC)
Timer/Watchdog Timer

User's Guide

Literature Number: SPRUFH0
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Read This First

This document describes the operation of the software-programmable 64-bit timer in the TMS320DM36x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, Timer 3 and Timer 4 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode.

Timer 3 supports additional features over the other timers:

- external clock/event input
- period reload
- output event tied to Real Time Out (RTO) module
- external event capture
- timer counter register read reset

Timer 2 is used only as a watchdog timer.

The GP timer modes can be used to generate periodic interrupts, enhanced direct access (EDMA) synchronization events, and RTO output events (Timer 3 only).

The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation from Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com

SPRUFG5 — ***TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controllerface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

SPRUFJ0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

Trademarks

64-Bit Timer/Watchdog Timer

1 Introduction

This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This processor contains four software-programmable timers. Timer 0, Timer 1, Timer 3 and Timer 4 (general-purpose timers) can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode. Timer 3 supports additional features over the other timers: external clock/event input, period reload, output event tied to Real Time Out (RTO) module, external event capture, and timer counter register read reset. Timer 2 is used only as a watchdog timer and is tied to the device reset.

1.1 Purpose of the Peripheral

The timers support four basic modes of operation: a 64-bit general-purpose (GP) timer, dual unchained 32-bit GP timers, dual chained 32-bit timers, or a watchdog timer. The GP timer modes can be used to generate periodic ARM interrupts and EDMA synchronization events. Timer 3 supports additional features that are necessary for real-time control applications. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop. The capabilities of each of the timers are summarized in Table 1.

Table 1. Supported Timer Features by Instantiation

Capability	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
64-bit general-purpose timer	√	√	-	√	√
Dual 32-bit general-purpose timer (unchained)	√	√	-	√	√
Dual 32-bit general-purpose timer (chained)	√	√	-	√	√
External clock/event input (GPIO1, 2, 3, 4)	-	-	-	√	-
Period reload	-	-	-	√	-
Output event to RTO module	-	-	-	√	-
External event capture	-	-	-	√	-
Timer counter register read reset	-	-	-	√	-
Watchdog timer	-	-	√	-	-

1.2 Features

The 64-bit timer consists of the following features.

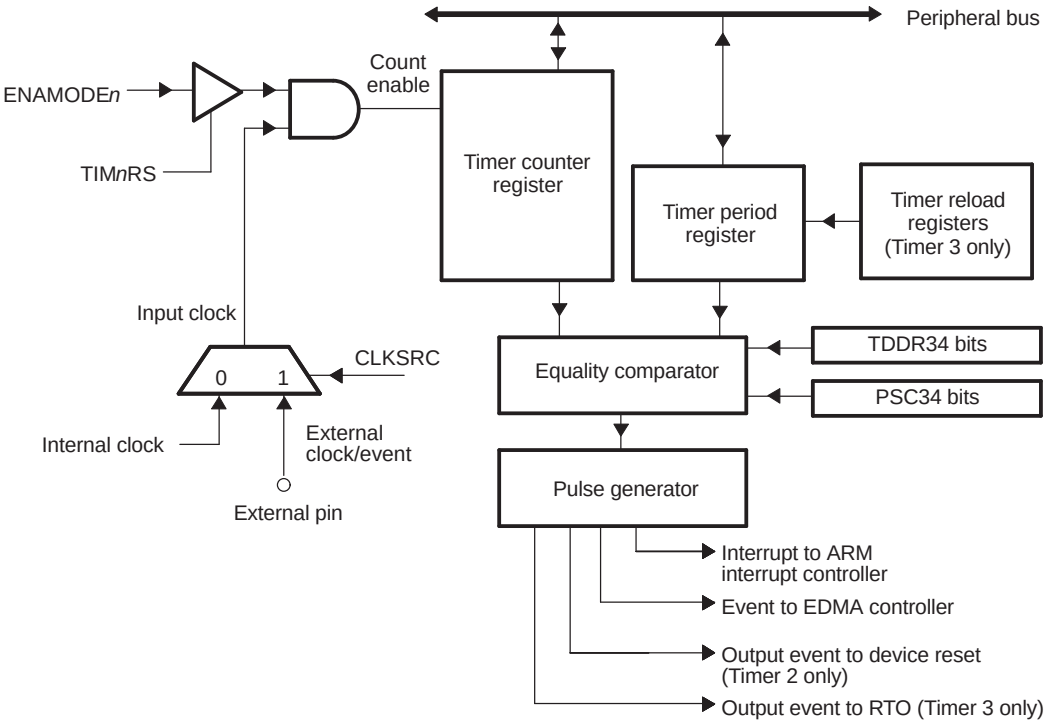
- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
  - Watchdog timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock/event input via timer input pins (Timer 3 only)
- 3 possible operation modes:

  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)
  - Continuous operation with period reload (Timer 3 only)
- Generates interrupts to the ARM CPU
- Generates sync event to EDMA
- Generates output event to device reset (Timer 2 only)
- Generates output event to Real Time Out (RTO) module (Timer 3 only)
- External event capture via timer input pins (Timer 3 only)

1.3 Functional Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the timers is in Section 2 and Section 3.

Figure 1. Timer Block Diagram



1.4 Industry Standard Compatibility Statement

This peripheral is not intended to conform to any specific industry standard.

2 Architecture – General-Purpose Timer Mode

This section describes the timer in the general-purpose (GP) timer mode. Timer 0, Timer 1, Timer 3 and Timer 4 can be used in GP timer mode. Timer 2 can only be used as a watchdog timer. To use timer 2 as a watchdog timer, see Section 3.

2.1 Backward Compatible Mode (Timer 3 Only)

Timer 3 supports the following additional features over the other timers:

- External clock/event input
- Output event to RTO

- Period reload
- External event capture mode
- Timer counter register read reset mode
- Timer counter capture registers
- Interrupt/EDMA/RTO generation control and status

By default, period reload; external event capture mode; timer counter register read reset mode; timer counter capture registers, and interrupt/EDMA/RTO generation control and status are not available and Timer 3 is identical to Timer 0 Timer 1 and Timer 4. To enable these features you must set the backward compatible bit (BW_COMPATIBLE) in the timer global control register (TGCR). These features are described throughout the following sections. External clock/event input and output event to RTO are always available, regardless of the state of the backward compatible bit.

2.2 Clock Control

The timer can use an internal or external clock source for the counter period. The following sections explain how to select the clock source. Table 2 shows which clock sources are supported on each timer.

Table 2. Supported Timer Clock Sources

Clock Source	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
Internal clock source	√	√	√	√	√
External clock/event input (GPIO1, 2, 3, 4 pins)	-	-	-	√	-

As shown in Table 3 and Figure 2, the timer clock source is selected using the clock source (CLKSRC12) and (CLKSRC34) bits in the timer control register (TCR). Two clock sources are available to drive the timer clock:

- internal clock, by setting CLKSRC12 and/or CLKSRC34 = 0.
- external clock on timer 3 input pin (GPIO1, 2, 3, 4), by setting CLKSRC12 and/or CLKSRC34 = 1.

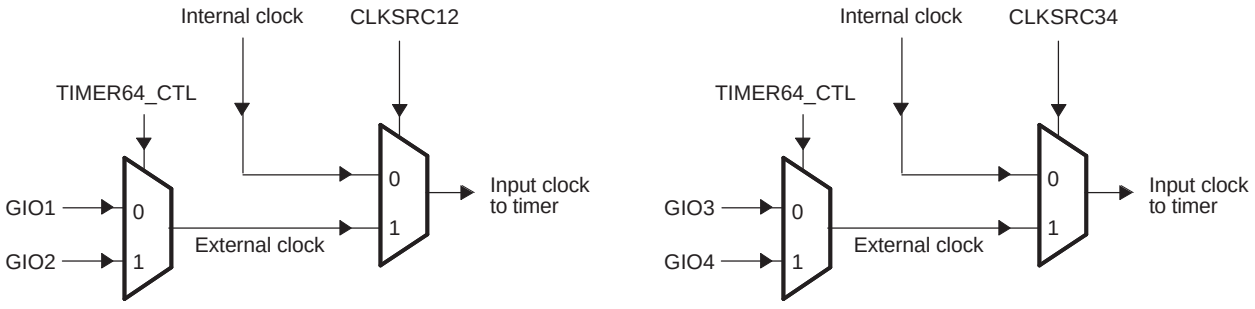
You can select either of two GPIO pins via the register TIMER64_CTL in the System Control module. For information on the System Control module, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections.

Table 3. Timer Clock Source Selection

CLKSRC(12/34)	Input Clock
0	Internal clock (default)
1	External clock on timer input (GPIO1, 2, 3, 4 pins) - Timer 3 only

Figure 2. Timer Clock Source Block Diagram



2.2.1 Using the Internal Clock Source to the Timer

The internal clock source to the timer is driven by the auxiliary clock of the PLL controller. The frequency of the auxiliary clock is equal to the input reference clock of the PLL controller, and therefore is not affected by the multiplier and divider values of the PLL controller. This clock source determines the speed of the timer since the timer counts up in units of source clock cycles. When determining the period and prescaler settings for the timer, choose the desired period in units of source clock cycles. For details on the generation of the on-chip clocks, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

The CLKSRC12 and CLKSRC34 parameters in the timer control register (TCR) control whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer while CLKSRC34 controls the timer 3:4 side of the timer.

To select the internal clock as the clock source for the timer, CLKSRC12 and/or CLKSRC34 in TCR must be cleared to 0. If the timer being used does not support an external clock source, CLKSRC12 and/or CLKSRC34 must always be 0.

2.2.2 Using the External Clock Source to the Timer (Timer 3 only)

An external clock source can be provided to clock the Timer 3 through GPIO pins. The CLKSRC12 and CLKSRC34 parameters in the timer control register (TCR) control whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer while CLKSRC34 controls the timer 3:4 side of the timer.

The external clock source for the timer 1:2 side of the timer can come from either GPIO1 or GPIO2 pin. The external clock source for the timer 3:4 side of the timer can come from either GPIO3 or GPIO4 pin. You can select either of two GPIO pins via the register TIMER64_CTL in the System Control module. For information on the System Control module, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections. To select the external clock as the clock source for the timer, CLKSRC12 and/or CLKSRC34 in TCR must be set to 1. The external clock source frequency must be no greater than the PLL reference clock divided by four (e.g. 24MHz/4).

2.3 Signal Descriptions

As shown in Figure 2, pins GPIO1, 2, 3, and 4 may be used as input to Timer 3. These signals can be used to drive the clock/event count of Timer 3 or used as an external event input for Timer 3 in event capture mode.

2.4 Timer Modes

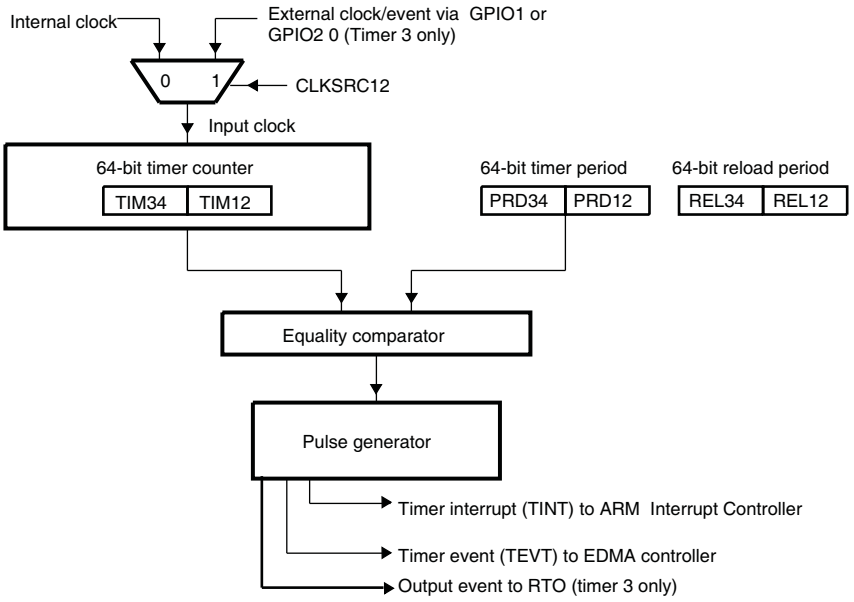
The following section describes the general-purpose (GP) timer modes. To use the timer as a watchdog timer (timer 2 only), see Section 3.

2.4.1 64-Bit Timer Mode (Timer 0, Timer 1, Timer 3 and Timer 4)

The general-purpose timers can each be configured as a 64-bit timer by clearing the TIMMODE bit in the timer global control register (TGCR) to 0. At reset, 0 is the default setting for the TIMMODE bit.

In this mode, the timer operates as a single 64-bit up-counter (Figure 3). The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit timer period register. When the timer is enabled, the timer counter starts incrementing by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT*n*) and a timer EDMA (TEVT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using control bits in TGCR.

Figure 3. 64-Bit Timer Mode Block Diagram



2.4.1.1 Enabling the 64-Bit Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. For the timer to operate in 64-bit timer mode, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, enabled to run continuously, or enabled to run continuously with period reload; the ENAMODE34 bit has no effect in 64-bit timer mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again. When the timer is enabled for continuous operation with period reload (ENAMODE12 = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and PRD34) with the value in the period reload registers (REL12 and REL34), and begins counting again.

Table 4 shows the bit values in TGCR to configure the 64-bit timer.

Table 4. 64-Bit Timer Configurations

64-Bit Timer Configuration	TGCR Bit		TCR Bit
	TIM12RS	TIM34RS	ENAMODE12
To place the 64-bit timer in reset	0	0	0
To disable the 64-bit timer (out of reset)	1h	1h	0
To enable the 64-bit timer for one-time operation	1h	1h	1h
To enable the 64-bit timer for continuous operation	1h	1h	2h
To enable the 64-bit timer for continuous operation with period reload	1h	1h	3h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.4.1.2 Reading the Counter Registers

When reading the timer count in 64-bit timer mode, the CPU must first read TIM12 followed by TIM34. When TIM12 is read, the timer copies TIM34 into a shadow register. When reading TIM34, the hardware logic forces the reads to read from the shadow register. This ensures that the values read from the registers are not affected by the fact that the timer may continue to run as the registers are read. When reading the timers in 32-bit mode, TIM12 and TIM34 may be read in either order.

2.4.1.3 64-Bit Timer Configuration Procedure

To configure the GP timer to operate as a 64-bit timer, follow the steps below:

1. Select 64-bit mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12 and PRD34).
4. Enable the timer (ENAMODE12 in TCR).
5. If ENAMODE12=3h, write the desired timer period for the next timer cycle in the period reload registers (REL12 and REL34). This step can be done at any time before the current timer cycle ends.

2.4.2 Dual 32-Bit Timer Modes (Timer 0, Timer 1, Timer 3 and Timer 4)

Each of the general-purpose timers can be configured as dual 32-bit timers by configuring the TIMMODE bit in the timer global control register (TGCR). In dual 32-bit timer mode, the two 32-bit timers can be operated independently (unchained mode) or in conjunction with each other (chained mode).

2.4.2.1 Chained Mode

The general-purpose timers can each be configured as a dual 32-bit chained timer by setting the TIMMODE bit to 3h in TGCR.

In the chained mode (Figure 4), one 32-bit timer (timer 3:4) is used as a 32-bit prescaler and the other 32-bit timer (timer 1:2) is used as a 32-bit timer. The 32-bit prescaler is used to clock the 32-bit timer. The 32-bit prescaler uses one counter register (TIM34) to form a 32-bit prescale counter register and one period register (PRD34) to form a 32-bit prescale period register.

When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated and the prescale counter register is reset to 0 (see the example in Figure 5).

The other 32-bit timer (timer 1:2) uses one counter register (TIM12) to form a 32-bit timer counter register and one period register (PRD12) to form a 32-bit timer period register. This timer is clocked by the output clock from the prescaler. The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT) and a timer EDMA event (TEVT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS and TIM34RS bits in TGCR. In the chained mode, the upper 16-bits of the timer control register (TCR) are not used.

Figure 4. Dual 32-Bit Timers Chained Mode Block Diagram

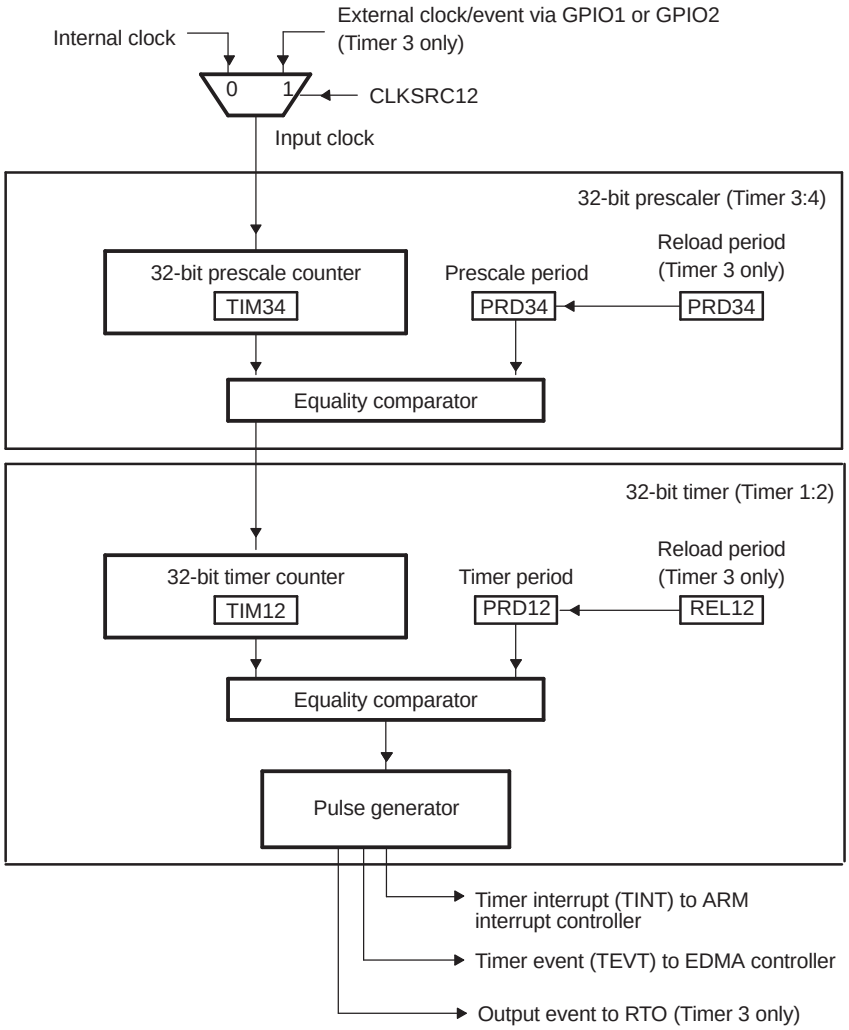
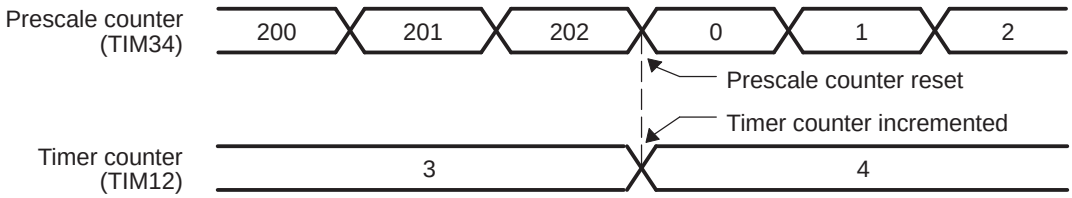


Figure 5. Dual 32-Bit Timers Chained Mode Example

32-bit prescaler settings: count = TIM34 = 200; period = PRD34 = 202
32-bit timer settings: count = TIM12 = 3; period = PRD12= 4



2.4.2.1.1 Enabling the 32-Bit Timer Chained Mode

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bits control the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and TIM34RS bits must be set to 1.

he ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, enabled to run continuously, enabled to run continuously with period reload; the ENAMODE34 bit has no effect in 32-bit timer chained mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again. When the timer is enabled for continuous operation with period reload (ENAMODE12 = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and PRD34) with the value in the period reload registers (REL12 and REL34), and begins counting again.

Table 5 shows the bit values in TGCR to configure the 32-bit timer in chained mode.

Table 5. 32-Bit Timer Chained Mode Configurations

	TGCR Bit		TCR Bit
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 32-bit timer chained mode in reset	0	0	0
To disable the 32-bit timer chained mode (out of reset)	1h	1h	0
To enable the 32-bit timer chained mode for one-time operation	1h	1h	1h
To enable the 32-bit timer chained mode for continuous operation	1h	1h	2h
To enable the 32-bit timer chained mode for continuous operation with period reload (Timer 3 only)	1h	1h	3h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.4.2.1.2 32-Bit Timer Chained Mode Configuration Procedure

To configure the GP timer to operate as a dual 32-bit chained mode timer, follow the steps below:

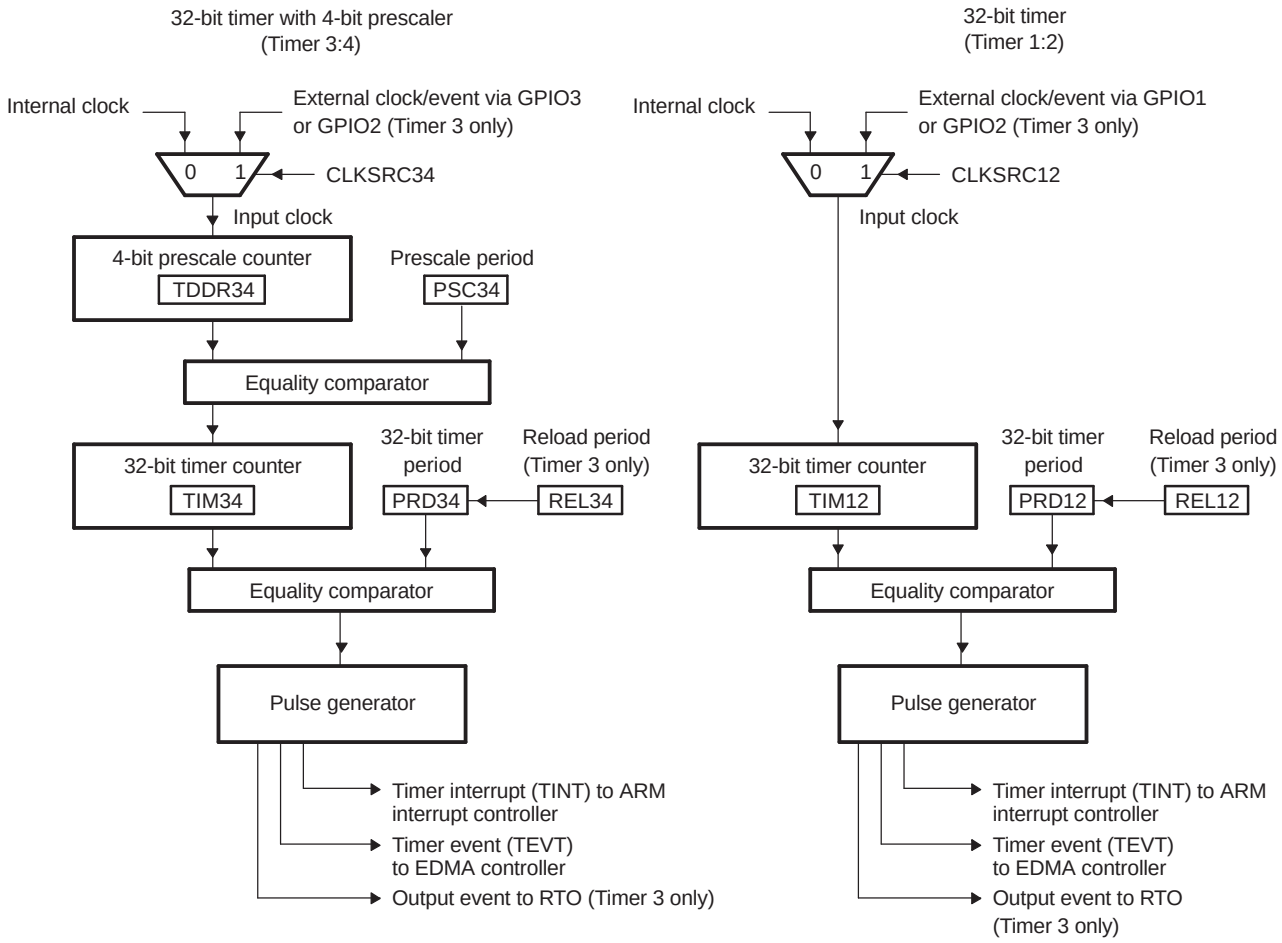
1. Select 32-bit chained mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12).
4. Select the desired timer prescaler value (PRD34).
5. Enable the timer (ENAMODE12 in TCR).
6. If ENAMODE12=3h, write the desired timer period for the next timer cycle in the period reload registers (REL12 and REL34). This step can be done at any time before the current timer cycle ends.

2.4.2.2 Unchained Mode

The general-purpose timers can be configured as a dual 32-bit unchained timers by setting the TIMMODE bit to 1 in TGCR.

In the unchained mode (Figure 6), the timer operates as two independent 32-bit timers. One 32-bit timer (timer 3:4) operates as a 32-bit timer being clocked by a 4-bit prescaler. The other 32-bit timer (timer 1:2) operates as a 32-bit timer with no prescaler.

Figure 6. Dual 32-Bit Timers Unchained Mode Block Diagram

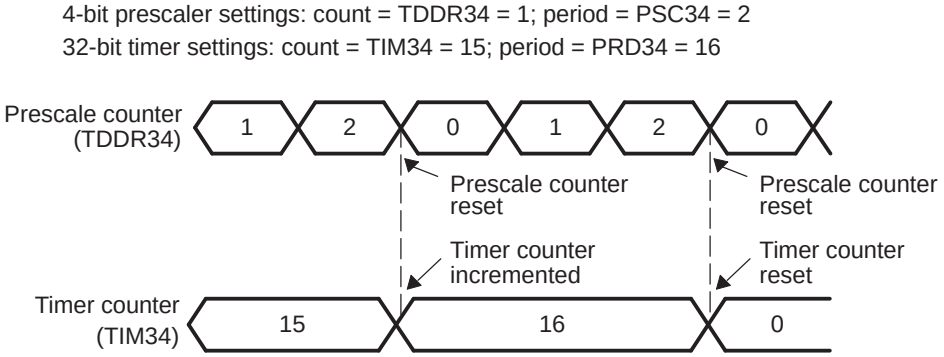


2.4.2.2.1 32-Bit Timer With a 4-Bit Prescaler

In the unchained mode, the 4-bit prescale can be clocked by the internal clock or an external clock source. Use CLKSRC34 to select the clock source. The 4-bit prescaler uses the timer divide-down ratio (TDDR34) bit in TGCR to form a 4-bit prescale counter register and the prescale counter bits (PSC34) to form a 4-bit prescale period register (see Figure 6). When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated for the 32-bit timer.

The 32-bit timer uses TIM34 as a 32-bit timer counter register and PRD34 as a 32-bit timer period register. The 32-bit timer is clocked by the output clock from the 4-bit prescaler (see the example in Figure 7). The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the period, a maskable timer interrupt (TINT*n*), a timer EDMA event (TEVT), and a timer output event to RTO (Timer 3 only) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM34RS bit in TGCR. For timer 3:4, the lower 16 bits of the timer control register (TCR) have no control.

Figure 7. Dual 32-Bit Timers Unchained Mode Example



2.4.2.2.2 32-Bit Timer with No Prescaler

The other 32-bit timer (timer 1:2) uses TIM12 as the 32-bit counter register and PRD12 as a 32-bit timer period register (see Figure 6). When the timer is enabled, the timer counter increments by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT*n*), a timer EDMA event (TEVT), and a timer output event to RTO (Timer 3 only) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS bit in TGCR. For timer 1:2, the upper 16 bit of the timer control register (TCR) have no control.

2.4.2.2.3 Enabling the 32-Bit Unchained Mode Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bit controls the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and/or TIM34RS bits must be set to 1.

The ENAMODE*n* bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously.

- When the timer is disabled (ENAMODE*n* = 0), the timer does not run and maintains its current count value.
- When the timer is enabled for one time operation (ENAMODE*n* = 1), it counts up until the counter value equals the period value and then stops.
- When the timer is enabled for continuous operation (ENAMODE*n* = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.
- When the timer is enabled for continuous operation with period reload (ENAMODE*n* = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and/or PRD34) with the value in the period reload registers (REL12 and/or REL34), and begins counting again.

Table 6 shows the bit values in TGCR to configure the 32-bit timer in unchained mode.

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

Table 6. 32-Bit Timer Unchained Mode Configurations

	TGCR Bit		TCR Bit	
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**	**ENAMODE34**
To place the 32-bit timer unchained mode with 4-bit prescaler in reset	x	0	x	0
To disable the 32-bit timer unchained mode with 4-bit prescaler (out of reset)	x	1h	x	0
To enable the 32-bit timer unchained mode with 4-bit prescaler for one-time operation	x	1h	x	1h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation	x	1h	x	2h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation with period reload	x	1h	x	3h
To place the 32-bit timer unchained mode with no prescaler in reset	0	x	0	x
To disable the 32-bit timer unchained mode with no prescaler (out of reset)	1h	x	0	x
To enable the 32-bit timer unchained mode with no prescaler for one-time operation	1h	x	1h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation	1h	x	2h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation with period reload	1h	x	3h	x

2.4.2.2.4 32-Bit Timer Unchained Mode Configuration Procedure

To configure timer 1:2, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 1:2 from reset (TIM12RS in TGCR).
3. Select the desired timer period for timer 1:2 (PRD12).
4. Select the desired clock source for timer 1:2 (CLKSRC12 in TCR).
5. Enable timer 1:2 (ENAMODE12 in TCR).
6. If ENAMODE12=3h, write the desired timer period for the next timer cycle in the period reload register (REL12). This step can be done at any time before the current timer cycle ends.

To configure timer 3:4, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 3:4 from reset (TIM34RS in TGCR).
3. Select the desired timer period for timer 3:4 (PRD34).
4. Select the desired prescaler value for timer 3:4 (PSC34 in TGCR).
5. Enable timer 3:4 (ENAMODE34 in TCR).
6. If ENAMODE34=3h, write the desired timer period for the next timer cycle in the period reload register (REL34). This step can be done at any time before the current timer cycle ends.

2.4.2.2.5 Event Capture Mode (Timer 3 only)

When the backward compatible bit (BW_COMPATIBLE) in the timer global control register (TGCR) is set, Event Capture Mode is available for Timer 3. Event Capture Mode is available for Timer 3 only and only when Timer 3 is configured in 32-bit unchained mode. When Event Capture Mode is enabled, the timer cycle is restarted when an external input event occurs. In particular, when an external input event occurs, the timer stops counting, generates output events (ARM interrupt, EDMA event, and RTO event), copies values from the timer counter registers (TIM12 and/or TIM34) to the timer capture registers (CAP12 and/or CAP34), reloads the timer period registers (PRD12 and/or PRD34) if in continuous mode with period reload (ENAMODE=3h), and then restarts counting in continuous mode. Event Capture Mode is available only when the timer clock source is the internal timer (CLKSRC=0) and the timer is in continuous mode (ENAMODE=10 or 11).

The external input event for the timer 1:2 side of the timer can come from either GPIO1 or GPIO2 pin. The external input event for the timer 3:4 side of the timer can come from either GPIO3 or GPIO4 pin. You can select either GPIO pin via the register TIMER64_CTL in the System Control module. For information on the System Control module, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

Capture mode is enabled using the Capture mode enable bit (CAPMODE12 and/or CAPMODE34) in the timer control register (TCR). The type of input event is selected by the capture event mode bit (CAPEVTMODE12 and/or CAPEVTMODE34) in the timer control register (TCR). All of the following input event types are available:

- Rising edge of input signal (Use rising edge for RTO output event in device)
- Falling edge of input signal
- Rising or falling edge of input signal

2.4.2.2.6 Timer Counter Register Read Reset Mode (Timer 3 only)

When the backward compatible bit (BW_COMPATIBLE) in the timer global control register (TGCR) is set, Read Reset Mode is available for Timer 3. Read Reset Mode is available for Timer 3 only and only when Timer 3 is configured in 32-bit unchained mode. When Read Reset Mode is enabled, the timer cycle is restarted when the timer counter registers are read (TIM12 and/or TIM34). In particular, when the timer registers are read, the timer stops counting, copies values from the timer counter registers (TIM12 and/or TIM34) to the timer capture registers (CAP12 and/or CAP34), reloads the timer period registers (PRD12 and/or PRD34) if in continuous mode with period reload (ENAMODE=3h), and then restarts counting in continuous mode. Timer output events (ARM interrupt, EDMA event, and RTO event) are not generated during this process. Read Reset Mode is enabled using the read reset mode enable bit (READRSTMODE) in the timer control register (TCR).

2.4.3 Timer Capture Registers (Timer 3 only)

The timer counter capture registers (CAP12 and CAP34) are supported for Timer 3 only.

When the timer has a timeout due to a normal expiration of timer, external input event in Event Capture Mode, read of timer counter registers in Read Reset Mode, the value in the timer counter registers (TIM12 and TIM34) are copied onto the timer counter capture registers. Note that the value in TDDR is not captured when a read of TIM34 happens

2.4.4 Counter and Period Registers Used in GP Timer Modes

Table 7 summarizes how the counter registers (TIM*n*) and period registers (PRD*n*) are used in each GP timer mode.

Table 7. Counter and Period Registers Used in GP Timer Modes

Timer Mode	Counter Registers	Period Registers
64-bit general-purpose	TIM34:TIM12	PRD34:PRD12
Dual 32-bit chained		
Prescaler (Timer 3:4)	TIM34	PRD34
Timer (Timer 1:2)	TIM12	PRD12
Dual 32-bit unchained		
Timer (Timer 1:2)	TIM12	PRD12
Timer with prescaler (Timer 3:4)	TDDR34 bits and TIM34	PSC34 bits and PRD34

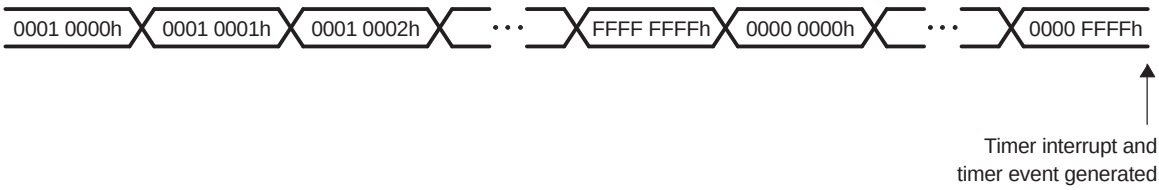
2.5 Timer Operation Boundary Conditions

The following boundary conditions affect the timer operation.

2.5.1 Timer Counter Overflow

Timer counter overflow can happen when the timer counter register is set to a value greater than the value in the timer period register. The counter reaches its maximum value (FFFF FFFFh or FFFF FFFF FFFF FFFFh), rolls over to 0, and continues counting until it reaches the timer period. An example is in Figure 8.

Figure 8. 32-Bit Timer Counter Overflow Example



2.5.2 Writing to Registers of an Active Timer

Writes to most timer registers are not allowed when the timer is active, except for except for setting the timer period reload registers (REL12 and REL34) and stopping and resetting the timers. In the 64-bit and dual 32-bit timer modes, registers that are protected by hardware are:

- TIM12
- TIM34
- PRD12
- PRD34
- TCR (except the ENAMODE bit)
- TGCR (except the TIM12RS and TIM34RS bits)

2.6 General-Purpose Timer Power Management

The timer can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5). The timer can be placed in an idle mode to conserve power when it is not being used.

3 Architecture – Watchdog Timer Mode

This section describes the use of timer 2 as a watchdog timer. Timers 0 and 1 can only be used as general-purpose timers. To use Timer 0, Timer 1, Timer 3 or Timer 4 as general-purpose timers, see Section 2.

3.1 Watchdog Timer

Timer 2 can be configured only as a 64-bit watchdog timer. As a watchdog timer, it can be used to prevent system lockup when the software becomes trapped in loops with no controlled exit.

After a hardware reset, the watchdog timer is disabled. The timer then can be configured as a watchdog timer using the timer mode (TIMMODE) bit in the timer global control register (TGCR) and the watchdog timer enable (WDEN) bit in the watchdog timer control register (WDTCR). In the watchdog timer mode, the timer requires a special service sequence to be executed periodically. Without this periodic servicing, the timer counter increments until it matches the timer period and causes a watchdog timeout event.

When the timeout event occurs, the watchdog timer resets the entire processor.

3.2 Watchdog Timer Mode Restrictions

The watchdog timer mode has the following restrictions:

- No external clock source
- No one-time enabling

3.3 Watchdog Timer Mode Operation

The watchdog timer mode is selected and enabled when:

- TIMMODE = 2h in TGCR
- WDEN = 1 in WDTCR

Figure 9 shows the timer when it is used in the watchdog timer mode. The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit period register. When the timer counter matches the timer period, the timer generates a watchdog timeout event which resets the entire processor.

To activate the watchdog timer, a certain sequence of events must be followed, as shown in the state diagram of Figure 10.

Once the watchdog timer is activated, it can be disabled only by a watchdog timeout event or by a hardware reset. A special key sequence is required to prevent the watchdog timer from being accidentally serviced while the software is trapped in a loop or by some other software failure.

Figure 9. Watchdog Timer Mode Block Diagram

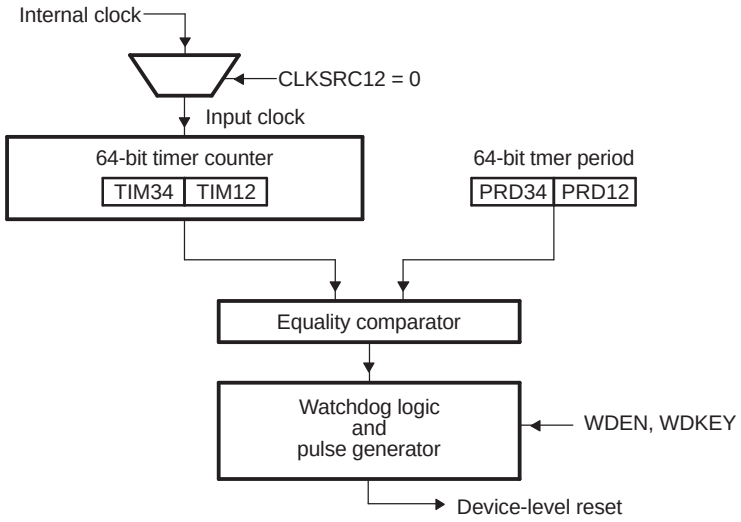
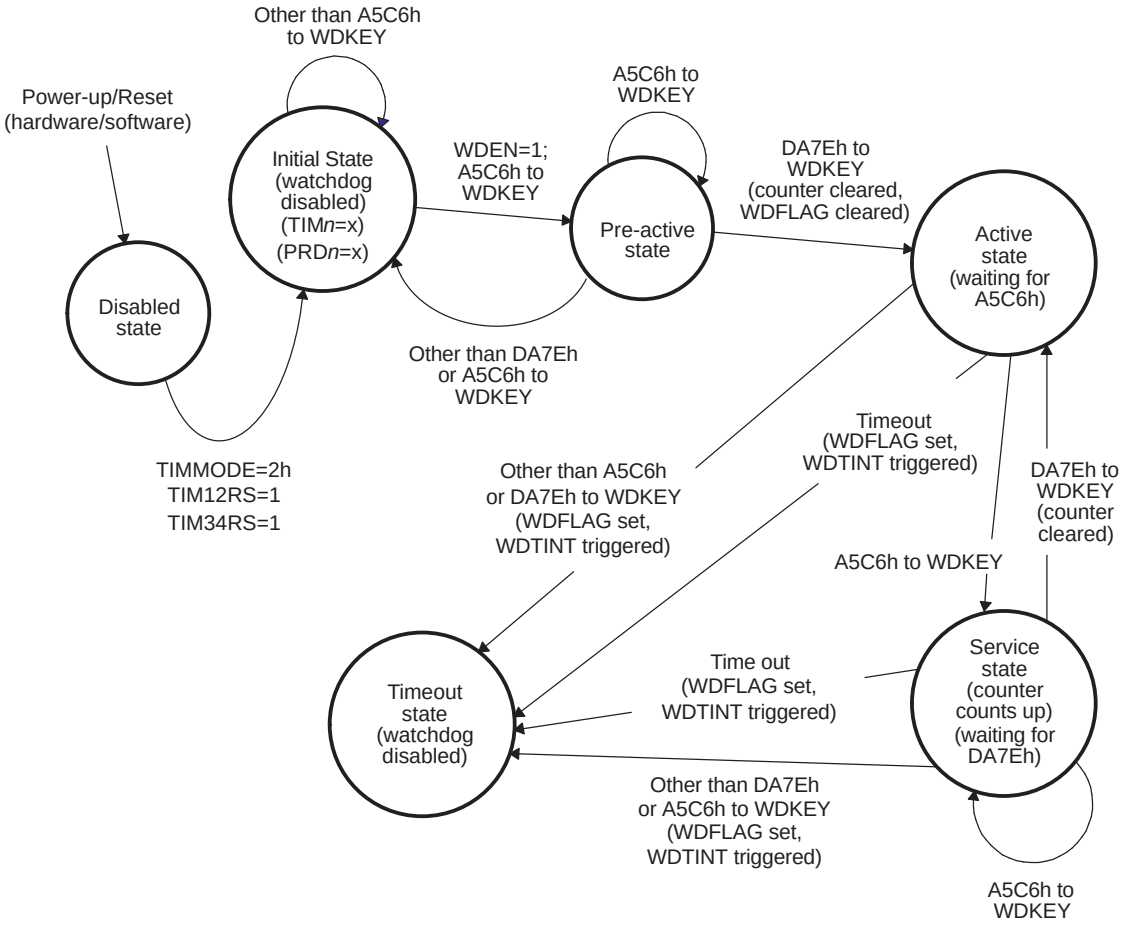


Figure 10. Watchdog Timer Operation State Diagram



To prevent a watchdog timeout event, the timer has to be serviced periodically by writing A5C6h followed by DA7Eh to the watchdog timer service key (WDKEY) bits in WDTCR before the timer finishes counting up. Both A5C6h and DA7Eh are allowed to be written to the WDKEY bits, but only the correct sequence of A5C6h followed by DA7Eh to the WDKEY bits services the watchdog timer. Any other writes to the WDKEY bits triggers the watchdog timeout event immediately.

When the watchdog timer is in the Timeout state, the watchdog timer is disabled, the WDEN bit is cleared to 0, and the timer is reset. After entering the Timeout state, the watchdog timer cannot be enabled again until a hardware reset occurs.

After a hardware reset, the watchdog timer is disabled; however, reads or writes to the watchdog timer registers are allowed. Once the WDEN bit is set (enabling the watchdog timer) and A5C6h is written to the WDKEY bits, the watchdog timer enters the Pre-active state. In the Pre-active state:

- A write to WDTCR is allowed only when the write comes with the correct key (A5C6h or DA7Eh) to the WDKEY bits.
- A write of DA7Eh to the WDKEY bits when the WDEN bit is set to 1 resets the counters and activates the watchdog timer.

The watchdog timer must be configured before the watchdog timer enters the Active state. The WDEN bit must be set to 1 before writing DA7Eh to the WDKEY bits in the Pre-active state. Every time the watchdog timer is serviced by the correct WDKEY sequence, the watchdog timer counter is automatically reset.

3.4 Watchdog Timer Register Write Protection

Once the watchdog timer enters the Pre-active state (see Figure 10), writes to TIM12, TIM34, PRD12, PRD34, and WDTCR are write protected (except for the WDKEY field). While the watchdog timer is in the Timeout state, writing to the WDEN bit has no effect.

Once the watchdog timer enters its Initial state (see Figure 10), do not write to TGCR.

3.5 Watchdog Timer Power Management

The watchdog timer cannot be placed in power-down mode.

4 Reset Considerations

The timer has two reset sources: hardware reset and the timer reset (TIM12RS and TIM34RS) bits in the timer global control register (TGCR).

4.1 Software Reset Considerations

When the TIM12RS bit in the timer global control register (TGCR) is cleared to 0, the TIM12 register is held with the current value.

When the TIM34RS bit in the timer global control register (TGCR) is cleared to 0, the TIM34 register is held with the current value.

Emulator software reset: In the event of an emulator software reset initiated from the ARM side, the timer register values are reset to their default values.

4.2 Hardware Reset Considerations

When a hardware reset is asserted, all timer registers are set to their default values.

5 Interrupt Support

Each of the timers can send either one of two separate interrupt events (TINT*n*) to the ARM and/or the CPU, depending on the operating mode of the timer. The timer interrupts are generated when the count value in the counter register reaches the value specified in the period register.

Table 8 shows the interrupts generated in each mode on each instance of the timer. When the backward compatible bit (BW_COMPATIBLE) is set, Timer 3 supports additional features for control, status, and generation of interrupts. See Section 8 for more information.

Table 8. Timer Interrupts Generated

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
Timer Mode	**ARM**	**ARM**	**ARM**	**ARM**	**ARM**
64-bit mode	TINT0	TINT2	-	TINT6	TINT8
32-bit chained mode	TINT0	TINT2	-	TINT6	TINT8
32-bit unchained mode without prescaler (timer 1:2)	TINT0	TINT2	-	TINT6	TINT8
32-bit unchained mode with prescaler (timer 3:4)	TINT1	TINT3	-	TINT7	TINT9
Watchdog mode	-	-	-	-	-

6 EDMA Event Support

Each of the timers can send either one of two separate timer events (TEVT*n*) to the EDMA, depending on the operating mode the timer. The timer events are generated when the count value in the counters register reaches the value specified in the period register.

Table 9 shows the EDMA events generated in each mode on each instance of the timer. When the backward compatible bit (BW_COMPATIBLE) is set, Timer 3 supports additional features for control, status, and generation of edma events. See Section 8 for more information.

Table 9. Timer EDMA Events Generated

	Timer 0	Timer 1	Timer 2	Timer 3	Timer 4
Timer Mode	**ARM**	**ARM**	**ARM**	**ARM**	**ARM**
64-bit mode	TEVT0	TEVT2	-	TEVT6	TEVT8
32-bit chained mode	TEVT0	TEVT2	-	TEVT6	TEVT8
32-bit unchained mode without prescaler (timer 1:2)	TEVT0	TEVT2	-	TEVT6	TEVT8
32-bit unchained mode with prescaler (timer 3:4)	TEVT1	TEVT3	-	TEVT7	TEVT9
Watchdog mode	-	-	-	-	-

7 RTO Event Support (Timer 3 only)

Timer 3 can send either one of two separate RTO events to the RTO module. The timer 1:2 side of timer 3 is connected to RTO input 0, while the timer 3:4 side of timer 3 is connected to RTO input 1.

RTO events are generated at the same time as interrupt and EDMA events. That is when the count value in the counters register reaches the value specified in the period register or when an external event occurs wile in event capture mode. Also RTO events are only generated when enabled in the interrupt control and status register (INTCTL_STAT), which is described in Section 8.

See the *TMS320DM36x DMSoC Real Time Out (RTO) User's Guide* (literature number, SPRUFH7) for additional information.

8 Interrupt/EDMA/RTO Event Generation Control and Status (Timer 3 only)

When the backward compatible bit (BW_COMPATIBLE) is set, Timer 3 supports additional features for control and status of interrupt, EDMA, and RTO event generation. Timer 3 interrupt/EDMA/RTO events are generated when the count value in the counter registers reaches the value specified in the period registers and they are also generated when Event Capture Mode is enabled and an external event occurs. To generate events in the case when the value specified in the period registers equals the value specified in the period registers, set the compare interrupt enable bit (CMP_INT_EN) in the interrupt control and status register (INTCTL_STAT). The event status for this case is reflected in the compare interrupt status bit (CMP_INT_STST), which is also in the interrupt control and status register (INTCTL_STAT). Similarly, to generate events in Event Capture Mode, set the event interrupt enable bit (EVT_IT_EN) in the interrupt control and status register (INTCTL_STAT). The event status for this case is reflected in the external interrupt status bit (EVT_INT_STAT).

Also, you can force the generation of the event (Interrupt/EDMA/RTO) by writing the event evaluation bit (EVAL) to the event set bit (SET) in the interrupt control and status register (INTCTL_STAT). See Section 11 for additional details.

9 Power Management

The general purpose timers can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

10 Emulation Considerations

Each timer has an emulation management register (EMUMGT_CLKSPD). As shown in Table 10, the FREE and SOFT bits of EMUMGT_CLKSPD determine how the timer responds to an emulation suspend event. An emulation suspend event corresponds to any type of emulator access to the ARM, such as a hardware or software breakpoint or a probe point.

Table 10. Timer Emulation Modes Selection

FREE	SOFT	Emulation Mode
0	0	The timer stops immediately.
0	1	The timer stops when the timer counter value increments and reaches the value in the timer period register.
1	x	The timer runs free regardless of SOFT bit status.

Note that during emulation, the timer count values will increment once every timer peripheral clock (not CPU clock). So when single-steeping though code, the timer values will not update on every CPU clock cycle.

The timer can respond to emulation events from the ARM CPU based on the configuration of the emulation suspend source register (SUSPSRC). See the data manual for detailed information on SUSPSRC and how it is configured.

11 Registers

Table 11 lists the memory-mapped registers for the 64-bit timer. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. TMR Global Registers

Offset	Acronym	Register Description	Section
00h	PID12	Peripheral Identification Register 12	Section 11.1
04h	EMUMGT	Emulation Management Register	Section 11.2
10h	TIM12	Timer Counter Register 12	Section 11.3
14h	TIM34	Timer Counter Register 34	Section 11.3
18h	PRD12	Timer Period Register 12	Section 11.4
1Ch	PRD34	Timer Period Register 34	Section 11.4
20h	TCR	Timer Control Register	Section 11.5
24h	TGCR	Timer Global Control Register	Section 11.6
28h	WDTCR	Watchdog Timer Control Register	Section 11.7
34h	REL12	Timer Reload Register 12	Section 11.8
38h	REL34	Timer Reload Register 34	Section 11.9
3Ch	CAP12	Timer Capture Register 12	Section 11.10
40h	CAP34	Timer Capture Register 34	Section 11.11
44h	INTCTL_STAT	Timer Interrupt Control and Status Register	Section 11.12

11.1 Peripheral Identification Register 12 (PID12)

For Timer 0, Timer 1, Timer2 and Timer 4, the peripheral ID register 12 (PID12) contains identification data (type, class, and revision) for the peripheral. The PID12 is shown in Figure 11 and described in Table 12. For Timer 3 only, the peripheral ID register 12 (PID12) is shown in Figure 12 and described in Table 13.

Figure 11. Timer 0, Timer 1, Timer 2 and Timer 4 Peripheral Identification Register 12 (PID12)

31	23	22	16
Reserved		TYPE	
R-0		R-01h	

15	8	7	0
CLASS		REVISION	
R-07h		R-01h	

LEGEND: R = Read only; -*n* = value after reset

Table 12. Timer 0, Timer 1, Timer 2 and Timer 4 Peripheral Identification Register 12 (PID12) Field Descriptions

Bit	Field	Value	Description
31-23	Reserved	0	Reserved
22-16	TYPE		Identifies type of peripheral
		01h	Timer
15-8	CLASS		Identifies class of peripheral
		07h	Timer
7-0	REVISION		Identifies revision of the timer. This value should be 0x01 and will be incremented each time the design is revised

Figure 12. Timer 3 Peripheral Identification Register 12 (PID12)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R-1		R-0		R - 0x472											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-0x1					R-0x2			R-0x0		R-0xB					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Timer 3 Peripheral Identification Register 12 (PID12) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	0-3h	Scheme value
29-28	Reserved	0	Reserved
27-16	FUNC	0-FFFh	Function
15-11	RTL	0-1Fh	RTL revision
10-8	MAJOR	0-7h	Major number
7-6	CUSTOM	0-3h	Custom
5-0	MINOR	0--3Fh	Minor Number

11.2 Emulation Management Register (EMUMGT)

The emulation management register (EMUMGT) is shown in Figure 13 and described in Table 14.

Figure 13. Emulation Management Register (EMUMGT)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		SOFT	FREE
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Emulation Management Register (EMUMGT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	SOFT		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The timer stops immediately.
		1	The timer stops when the counter increments and reaches the value in the timer period register (PRD*n*).
0	FREE		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The SOFT bit selects the timer mode.
		1	The timer runs free regardless of the SOFT bit.

11.3 Timer Counter Registers (TIM12 and TIM34)

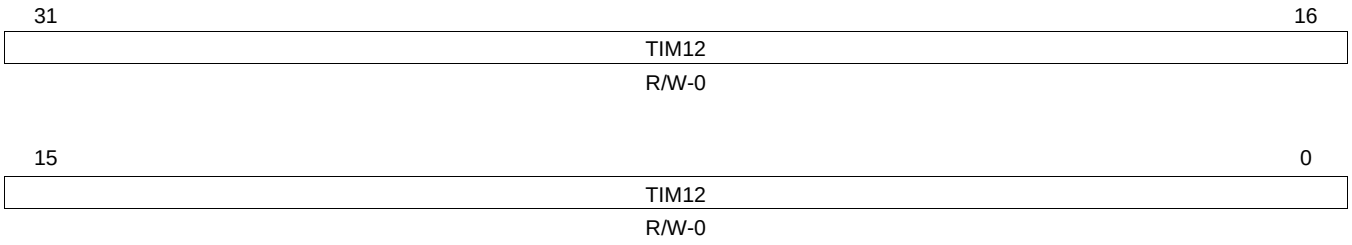
The timer counter register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, TIM12 and TIM34.

In the dual 32-bit timer mode, the 64-bit register is divided with TIM12 acting as one 32-bit counter and TIM34 acting as another. These two registers can be configured as chained or unchained.

11.3.1 Timer Counter Register 12 (TIM12)

The timer counter register 12 (TIM12) is shown in Figure 14 and described in Table 15

Figure 14. Timer Counter Register 12 (TIM12)



LEGEND: R/W = Read/Write; *-n* = value after reset

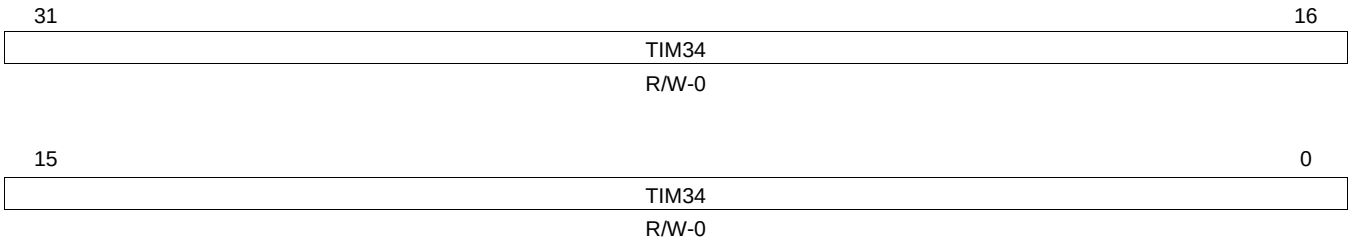
Table 15. Timer Counter Register 12 (TIM12) Field Descriptions

Bit	Field	Value	Description
31-0	TIM12	0-FFFF FFFFh	TIM12 count bits. This 32-bit value is the current count of the main counter.

11.3.2 Timer Counter Register 34 (TIM34)

The timer counter register 34 (TIM34) is shown in Figure 15 and described in Table 16.

Figure 15. Timer Counter Register 34 (TIM34)



LEGEND: R/W = Read/Write; *-n* = value after reset

Table 16. Timer Counter Register 34 (TIM34) Field Descriptions

Bit	Field	Value	Description
31-0	TIM34	0-FFFF FFFFh	TIM34 count bits. This 32-bit value is the current count of the main counter.

11.4 Timer Period Registers (PRD12 and PRD34)

The timer period register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, PRD12 and PRD34.

Similar to TIM*n* in the dual 32-bit timer mode, PRD*n* can be divided into 2 registers: for timer 1:2, PRD12 and for timer 3:4, PRD34. These two registers can be used in conjunction with the two timer counter registers TIM12 and TIM34.

11.4.1 Timer Period Register (PRD12)

The timer period register 12 (PRD12) is shown in Figure 16 and described in Table 17.

Figure 16. Timer Period Register 12 (PRD12)

31	16
PRD12	
R/W-0	

15	0
PRD12	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 17. Timer Period Register (PRD12) Field Descriptions

Bit	Field	Value	Description
31-0	PRD12	0-FFFF FFFFh	PRD12 period bits. This 32-bit value is the number of timer input clock cycles to count.

11.4.2 Timer Period Register 34 (PRD34)

The timer period register 34 (PRD34) is shown in Figure 17 and described in Table 18.

Figure 17. Timer Period Register 34 (PRD34)

31	16
PRD34	
R/W-0	

15	0
PRD34	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 18. Timer Period Register (PRD34) Field Descriptions

Bit	Field	Value	Description
31-0	PRD34	0-FFFF FFFFh	PRD34 period bits. This 16-bit value is the number of timer input clock cycles to count.

11.5 Timer Control Register (TCR)

The timer control register (TCR) is shown in Figure 18 and described in Table 19.

Figure 18. Timer Control Register (TCR)

31	30	29	28	27	26	25	24
Reserved		CAPEVTMODE34		CAPMODE34	READRST MODE34	Reserved	CLKSRC34

23	22	21	20	19	18	17	16
ENAMODE34		Reserved					

15	14	13	12	11	10	9	8
Reserved		CAPVTMODE12		CAPMODE12	READRST MODE12	Reserved	CLKSRC12

7	6	5	4	3	2	1	0
ENAMODE12		Reserved					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Timer Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Reserved
29-28	CAPEVTMODE34		Capture event mode. Uses these bits to specify the type of event for Capture mode.
		0	RISING_EDGE - Event occurs on timer input rising edge
		1h	FALLING_EDGE - Event occurs on time input falling edge
		2h	BOTH_EDGE - Event occurs on both rising and falling edges
		3h	Reserved
27	CAPMODE34		Capture mode enable bit. Determines if external event can reset timer. Capture mode is only available in dual 32-bit unchained mode and when CLKSRC = 0 and ENAMODE = 10 or 11. Output events (interrupt/EDMA/other) are generated when capture mode event occurs.
		0	DISABLE - Timer is not in capture mode
		1	ENABLE - Timer is in capture mode. External event can reset timer.
26	READRSTMODE 34		Read reset mode enable bit. Determines the effect of a timer counter read on TIM*n*. Read reset mode is only available in dual 32-bit unchained. Output events (interrupt/EDMA/other) are not generated when read reset occurs.
		0	DISABLE - There is no effect when timer counter registers (TIM*n*) are read
		1	ENABLE - Timer counter is reset when timer counter registers (TIM*n*) are read
25	Reserved		Reserved
24	CLKSRC34		CLKSRC determines the selected clock source for the timer.
		0	INTERNAL - Internal clock
		1	EXTERNAL - External clock
23-22	ENAMODE34		Enabling mode: determines the enabling modes fo the timer.
		0	DISABLED - The timer is disabled (not counting) and maintains current value.
		1h	ONCE - The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	CONTINUOUS - The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	CONTINUOUS_RELOAD - The timer is enabled continuously with period reload, TIMn increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching, reloads the period register with the values in the reload registers (RELn), and continues counting.

Table 19. Timer Control Register (TCR) Field Descriptions (continued)

Bit	Field	Value	Description
21-14	Reserved	0	Reserved
13-12	CAPVTMODE12		Capture event mode. Uses these bits to specify the type of event for Capture mode.
		0	RISING_EDGE - Event occurs on timer input rising edge
		1h	FALLING_EDGE - Event occurs on time input falling edge
		2h	BOTH_EDGE - Event occurs on both rising and falling edges
		3h	Reserved
11	CAPMODE12		Capture mode enable bit. Determines if external event can reset timer. Capture mode is only available in dual 32-bit unchained mode and when CLKSRC = 0 and ENAMODE = 10 or 11. Output events (interrupt/EDMA/other) are generated when capture mode event occurs.
		0	DISABLE - Timer is not in capture mode
		1	ENABLE - Timer is in capture mode. External event can reset timer.
10	READRSTMODE 12		Read reset mode enable bit. Determines the effect of a timer counter read on TIM*n.* Read reset mode is only available in dual 32-bit unchained. Output events (interrupt/EDMA/other) are not generated when read reset occurs.
		0	DISABLE - There is no effect when timer counter registers (TIM*n*) are read
		1	ENABLE - Timer counter is reset when timer counter registers (TIM*n*) are read
9	Reserved	0	Reserved
8	CLKSRC12		CLKSRC12 determines the selected clock source for the timer.
		0	INTERNAL - Internal clock
		1	INPUT_PIN - Timer input pin
7-6	ENAMODE12		Enabling mode: determines the enabling modes fo the timer.
		0	DISABLED - The timer is disabled (not counting) and maintains current value.
		1h	ONCE - The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	CONTINUOUS - The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	CONTINUOUS_RELOAD - The timer is enabled continuously with period reload, TIMn increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching, reloads the period register with the values in the reload registers (RELn), and continues counting.
5-0	Reserved	0	Reserved

11.6 Timer Global Control Register (TGCR)

The timer global control register (TGCR) is shown in Figure 19 and described in Table 20.

Figure 19. Timer Global Control Register (TGCR)

31	16
Reserved	
R-0	

15	12	11	8
TDDR34		PSC34	
R/W-0		R/W-0	

7	5	4	3	2	1	0
Reserved		BW_ COMPATIBLE	TIMMODE		TIM34RS	TIM12RS
R-0		R/W-0	R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Timer Global Control Register (TGCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	TDDR34	0-Fh	Timer linear divide-down ratio specifies the timer divide-down ratio for timer 3:4. When the timer is enabled, TDDR34 increments every timer clock. The TIM34 counter increments on the cycle after TDDR34 matches PSC34. TDDR34 resets to 0 and continues. When TIM34 matches PRD34, timer 3:4 stops, if timer 3:4 is enabled one time; TIM34 resets to 0 on the cycle after matching PRD34 and timer 3:4 continues, if timer 3:4 is enabled continuously.
11-8	PSC34	0-Fh	TIM34 pre-scalar counter specifies the count for timer 3:4.
7-5	Reserved	0	Reserved
4	BW_ COMPATIBLE		Timer backward compatible bit. To enable new timer features, set this bit to one.
		0	DISABLE - Do not enable new timer features
		1	ENABLE - Enable new timer features
3-2	TIMMODE	0-3h	TIMMODE determines the timer mode.
		0	The timer is in 64-bit GP timer mode.
		1h	The timer is in dual 32-bit timer unchained mode.
		2h	The timer is in 64-bit watchdog timer mode.
		3h	The timer is in dual 32-bit timer, chained mode.
1	TIM34RS		Timer 3:4 reset.(1)
		0	Timer 3:4 is in reset.
		1	Timer 3:4 is not in reset. Timer 3:4 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.
0	TIM12RS		Timer 1:2 reset.(1)
		0	Timer 1:2 is in reset.
		1	Timer 1:2 is not in reset. Timer 1:2 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.

(1) For the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Also, changing this bit does not affect the timer, if the timer is in watchdog active state.

11.7 Watchdog Timer Control Register (WDTCR)

The watchdog timer control register (WDTCR) is shown in Figure 20 and described in Table 21.

Figure 20. Watchdog Timer Control Register (WDTCR)

31	16
WDKEY	
R/W-0	

15	14	13	12	11	0
WDFLAG	WDEN	Reserved		Reserved	
R/W-0	R/W-0	R/W-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. Watchdog Timer Control Register (WDTCR) Field Descriptions

Bit	Field	Value	Description
31-16	WDKEY	0-FFFFh	16-bit watchdog timer service key. Only the sequence of an A5C6h followed by a DA7Eh services the watchdog. Not applicable in regular timer mode.
15	WDFLAG		Watchdog flag bit. WDFLAG can be cleared by enabling the watchdog timer, by device reset, or being written with 1. It is set by a watchdog time-out.
		0	No watchdog time-out occurred.
		1	Watchdog time-out occurred.
14	WDEN		Watchdog timer enable bit.
		0	DISABLE - Disable watchdog timer
		1	ENABLE - Enable watchdog timer
13-12	Reserved	0	Reserved. This bit field must be written as 00b.
11-0	Reserved	0	Reserved

11.8 Timer Reload Register 12 Register (REL12)

The timer period reload register 12 (REL12) is shown in Figure 21 and described in Table 22.

Figure 21. Timer Reload Register 12 (REL12) Register

31	0
REL12	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

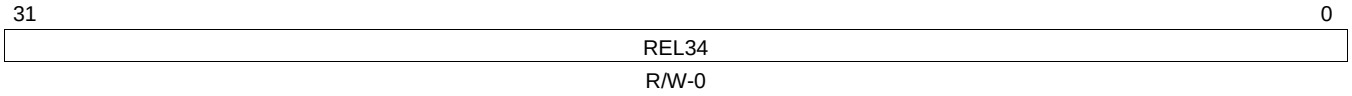
Table 22. Timer Reload Register 12 (REL12) Field Descriptions

Bit	Field	Value	Description
31- 0	REL12		Period reload bits

11.9 Timer Reload Register 34 Register (REL34)

The timer period reload register 34 (REL34) is shown in Figure 22 and described in Table 23.

Figure 22. Timer Reload Register 34 Register (REL34)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

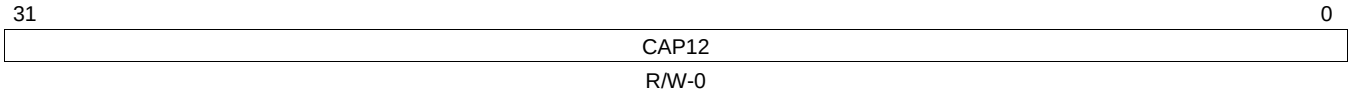
Table 23. Timer Reload Register 34 (REL34) Field Descriptions

Bit	Field	Value	Description
31- 0	REL34		Period reload bits

11.10 Timer Capture Register 12 Register (CAP12)

The timer capture register 12 (CAP12) is shown in Figure 23 and described in Table 24.

Figure 23. Timer Capture Register 12 Register (CAP12)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

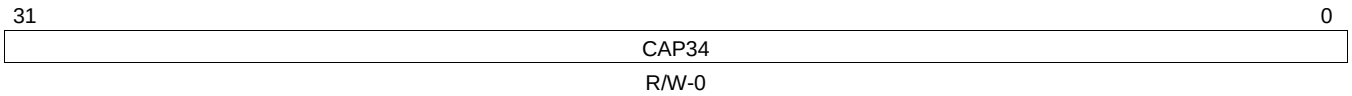
Table 24. Timer Capture Register 12 (CAP12) Field Descriptions

Bit	Field	Value	Description
31- 0	CAP12		Captured timer counter bits

11.11 Timer Capture Register 34 Register (CAP34)

The timer capture register 34 (CAP34) is shown in Figure 24 and described in Table 25.

Figure 24. Timer Capture Register 34 Register (CAP34)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

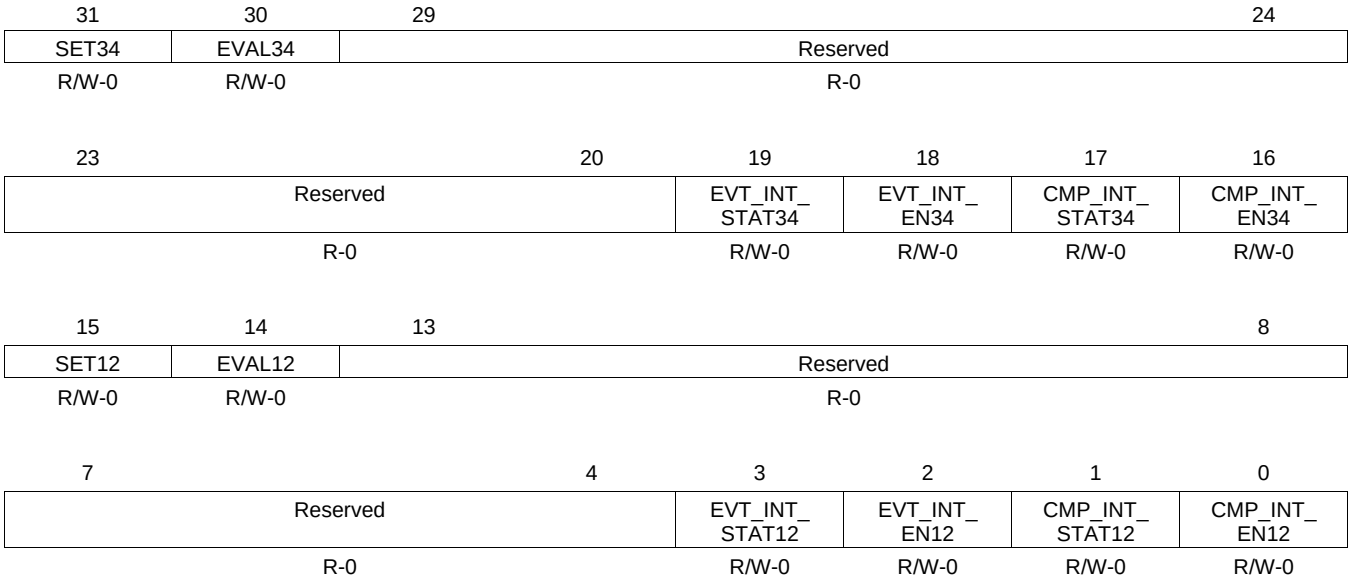
Table 25. Timer Capture Register 34 (CAP34) Field Descriptions

Bit	Field	Value	Description
31- 0	CAP34		Captured timer counter bits

11.12 Timer Interrupt Control and Status Register (INTCTL_STAT)

The timer interrupt control and status register (INTCTL_STAT) is shown in Figure 25 and described in Table 26.

Figure 25. Timer Interrupt Control and Status Register (INTCTL_STAT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 26. Timer Interrupt Control and Status Register (INTCTL_STAT) Field Descriptions

Bit	Field	Value	Description
31	SET34		Setting this bit will pulse the interrupt even if status is not set and interrupt sources are disabled
30	EVAL34		Interrupt eval bit will make the interrupt pulse when there is an interrupt status set.
29 - 20	Reserved	0	Reserved
19	EVT_INT_STAT34		Interrupt status which reflects the condition that an external event caused a timeout when timer is in capture mode.
		0	DISABLE - Interrupt has not occurred
		1	ENABLE - Interrupt has occurred
18	EVT_INT_EN34		Enables the interrupt generation when timer is in capture mode.
		0	DISABLE - Disable interrupt when in event capture mode
		1	ENABLE - Enable interrupt when in event capture mode
17	CMP_INT_STAT34		Interrupt status which reflects the condition that timer counter matched the period register when timer is enabled.
		0	DISABLE - Interrupt has not occurred
		1	ENABLE - Interrupt has occurred
16	CMP_INT_EN34		Enable interrupt generation when timer is enabled in 64-bit/32-bit chained/unchained/watchdog modes.
		0	DISABLE - Disable interrupt
		1	ENABLE - Enable interrupt
15	SET12		Setting this bit will pulse the interrupt even if status is not set and interrupt sources are disabled
14	EVAL12		Interrupt eval bit will make the interrupt pulse when there is an interrupt status set.
13 - 4	Reserved	0	Reserved
3	EVT_INT_STAT34		Interrupt status which reflects the condition that an external event caused a timeout when timer is in capture mode.
		0	DISABLE - Interrupt has not occurred
		1	ENABLE - Interrupt has occurred

Table 26. Timer Interrupt Control and Status Register (INTCTL_STAT) Field Descriptions (continued)

Bit	Field	Value	Description
2	EVT_INT_EN12		Enables the interrupt generation when timer is in capture mode.
		0	DISABLE - Disable interrupt when in event capture mode
		1	ENABLE - Enable interrupt when in event capture mode
1	CMP_INT_STAT12		Interrupt status which reflects the condition that timer counter matched the period register when timer is enabled.
		0	DISABLE - Interrupt has not occurred
		1	ENABLE - Interrupt has occurred
0	CMP_INT_EN12		Enable interrupt generation when timer is enabled in 64-bit/32-bit chained/unchained/watchdog modes.
		0	DISABLE - Disable interrupt
		1	ENABLE - Enable interrupt

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