TMS320DM646x DMSoC
Video Data Conversion Engine (VDCE)

User's Guide

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About This Manual

Describes the operation of the video data conversion engine (VDCE) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUEP8 — ***TMS320DM646x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRUEP9 — ***TMS320DM646x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

SPRUEQ0 — ***TMS320DM646x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRAA84 — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Video Data Conversion Engine (VDCE)

1 Introduction

This document describes the operation of the video data conversion engine (VDCE) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

1.1 Purpose of the Peripheral

The video data conversion engine (VDCE) is used for video data processing in the DM646x DMSoC. The VDCE has several capabilities of not only pure video data processing but also functions that are required from a video codec module.

1.2 Features

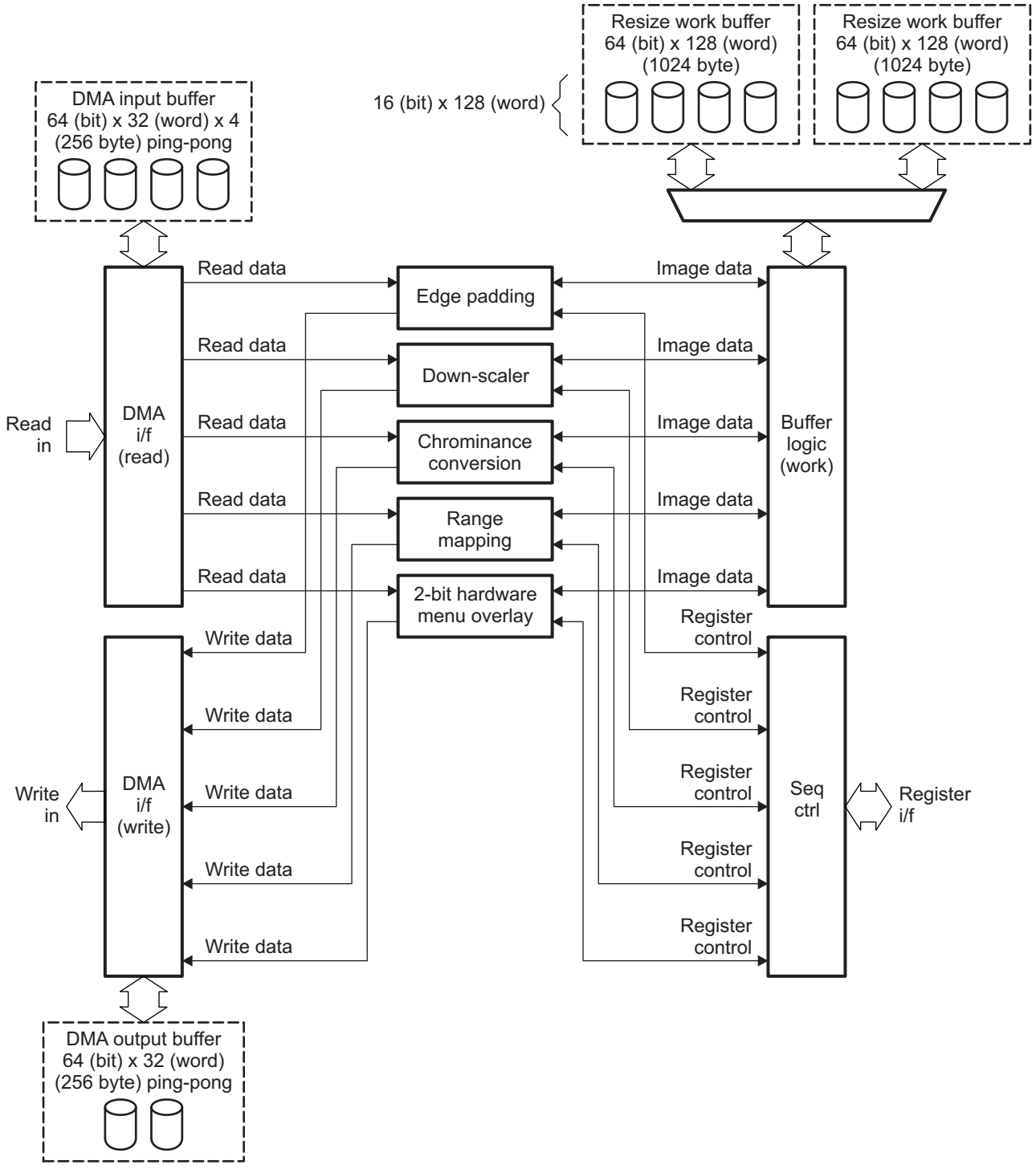
The video data conversion engine (VDCE) supports the following functions:

- Down-scaler function on horizontal (HRSZ) and vertical (VRSZ) with ratio defined by 256/N (N is natural number that ranges from 256 to 2048) with 4 taps interpolation. Magnification ratio of horizontal down-scaler and vertical down-scaler can be configured separately (different value can be configured).
- Anti-alias filter (combination of two kinds of low-pass filter) with horizontal 7 taps, and vertical direction (if this filter is activated for vertical direction, no interpolation on the vertical direction will be the result of the function).
- Chrominance signal format conversion (CCV) on both directions, one is from 4:2:2 to 4:2:0 and one is from 4:2:0 to 4:2:2. This function also uses 4 taps interpolation. MPEG-1 specific format (half-pixel phased from even pixel position of luminance) is also supported.
- Edge padding for preparation of MC with unrestricted motion vector (required by MPEG-4, H.264, VC-1). All modes (progressive, interlace frame, and interlace field) are supported (macro-block level control that is required in H.264 is not supported).
- VC-1 range mapping in advanced profile (in case of displaying decoded reference image or trans-coding from VC-1 to any other format of video codec).
- 2-bit hardware menu overlay function used for multiplexing video image data and sub-title data that has to be supported in digital TV broadcasting in Japan.

1.3 Functional Block Diagram

Functional block diagram with cache and control logic for buffer and processing sequence is shown in Figure 1.

Figure 1. Video Data Conversion Engine (VDCE) Block Diagram

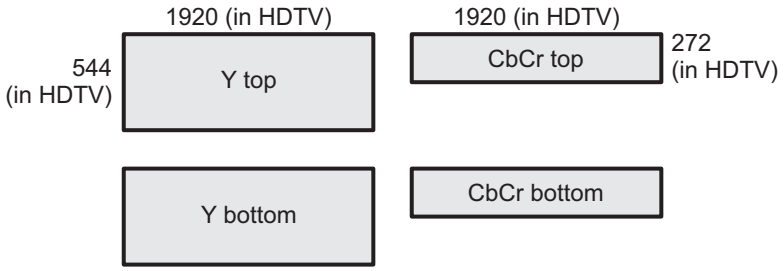


Both of input data and output data are received from/transmitted to SDRAM with the master interface (with 64-bit DMA bus) and the VDCE can be configured from CPU via the slave interface (with 32-bit configuration bus). Processing unit is frame level such as go→done process with register configuration from CPU. After the VDCE finishes processing of the frame, an interrupt pulse is asserted to CPU. After detecting this interrupt, CPU can configure the VDCE to process next frame with next data. So, if you would like to process motion picture with frame rate, you have to configure and initiate the VDCE in the defined frame rate.

As common rule, any picture data processed in this Video Data Conversion Engine can be both of field and frame store format. Field store format means that image data is divided into top and bottom field data independently (irrespective to format, interlace or progressive). Frame store format means that top and bottom field data is interleaved in both of interlace and progressive format. You can select either one mode for each of source and result data. So, you can choose the following configuration; source = field and result = frame. Configuration of this field/frame mode register is common in both of luminance and chrominance field/frame data.

A simple image of data storage using field storage format is shown in Figure 2.

Figure 2. Example of Data Storage Format (field type) in Video Data Conversion Engine (VDCE) (HDTV case)



1.4 Supported Use Case Statement

The video data conversion engine (VDCE) has several performance modes that focus on the usage of result data. The modes are:

- Source is video input data, and output is prepared reference frame of video codec (called pre-codec mode).
- Source is reference frame of video codec, and output is prepared for video output data (called post-codec mode).
- Both source and output are reference frame data of video codec (called trans-code mode).

2 Architecture

This section describes the architecture details of the video data conversion engine (VDCE).

2.1 Clock Control

The input clock for the VDCE is the SYSCLK2 chip-level clock. SYSCLK2 represents PLL1 divided by 2. Typically, SYSCLK2 is 300 MHZ.

2.2 Pre-Codec Mode

NOTE: If you configure the VDCE_MODE bit in the control register (CTRL) to be 2h (pre-codec mode), vertical chrominance conversion is automatically activated. On/Off control of vertical chrominance conversion is not related to the VDCE_CCV_EN bit in CTRL.

This mode is prepared for processing video input data. Processed video input data is to be used in the video codec module, as original (or reference) frame data for the encoder. The following functions inside the VDCE should be activated when in pre-codec mode.

- Horizontal and vertical down-scaler.
- Chrominance format conversion (4:2:2 to 4:2:0).

Processing flow and activated functions are shown in Figure 3 and Figure 4. The number listed beside the function block indicates the processing order used in this mode.

The edge padding function does not have to be activated in pre-codec mode because edge padding is prepared for in-loop processing on the decoder. Additionally, the 2-bit hardware menu overlay function and the range mapping functions are not activated because pre-codec mode is prepared for input from outside of the device and assumed source data of these two functions (2-bit hardware menu overlay and range mapping) are initially prepared in SDRAM (which means that some other peripheral has already stored the data before processing).

2.3 Post-Codec Mode

NOTE: If you would like to enable both the down-scaler and blender, you have to enable the VDCE twice; first enable the VDCE for the down-scaler, and then enable the VDCE for the blender. Simultaneous performance of the down-scaler and blender is restricted in the VDCE.

If you configure the VDCE_MODE bit in the control register (CTRL) to be 3h (post-codec mode), vertical chrominance conversion is automatically activated. On/Off control of vertical chrominance conversion is not related to the VDCE_CCV_EN bit in CTRL.

This mode is prepared for processing reference output data of the video codec (decoder). Processed image data is to be used in the video port interface (VPIF) as output image data to be displayed. The following functions inside the VDCE should be activated when in post-codec mode.

- Horizontal and vertical down-scaler.
- Range mapping (VC-1 advanced profile).
- Chrominance conversion from 4:2:0 to 4:2:2.
- 2-bit hardware menu overlay of video image and artificial bitmap sub-title (ARIB in Japan).

Processing flow and activated functions are shown in Figure 5 and Figure 6. The edge padding function is not activated because output data of the VDCE is not used in video codec in this mode. The number listed beside each function block indicates the processing order in this mode.

Figure 3. Processing Flow of Pre-Codec Mode for Luminance Data

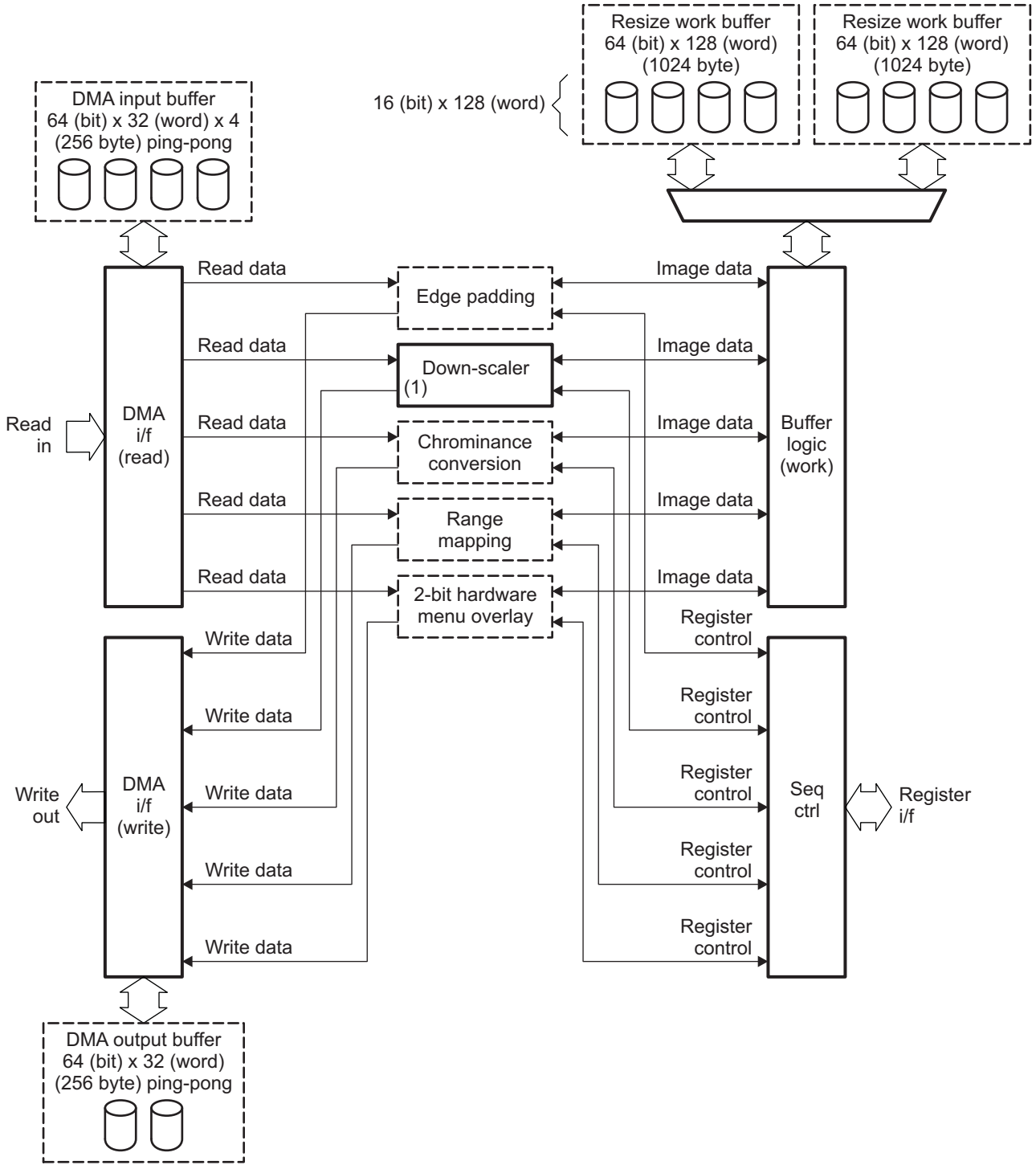


Figure 4. Processing Flow of Pre-Codec Mode for Chrominance Data

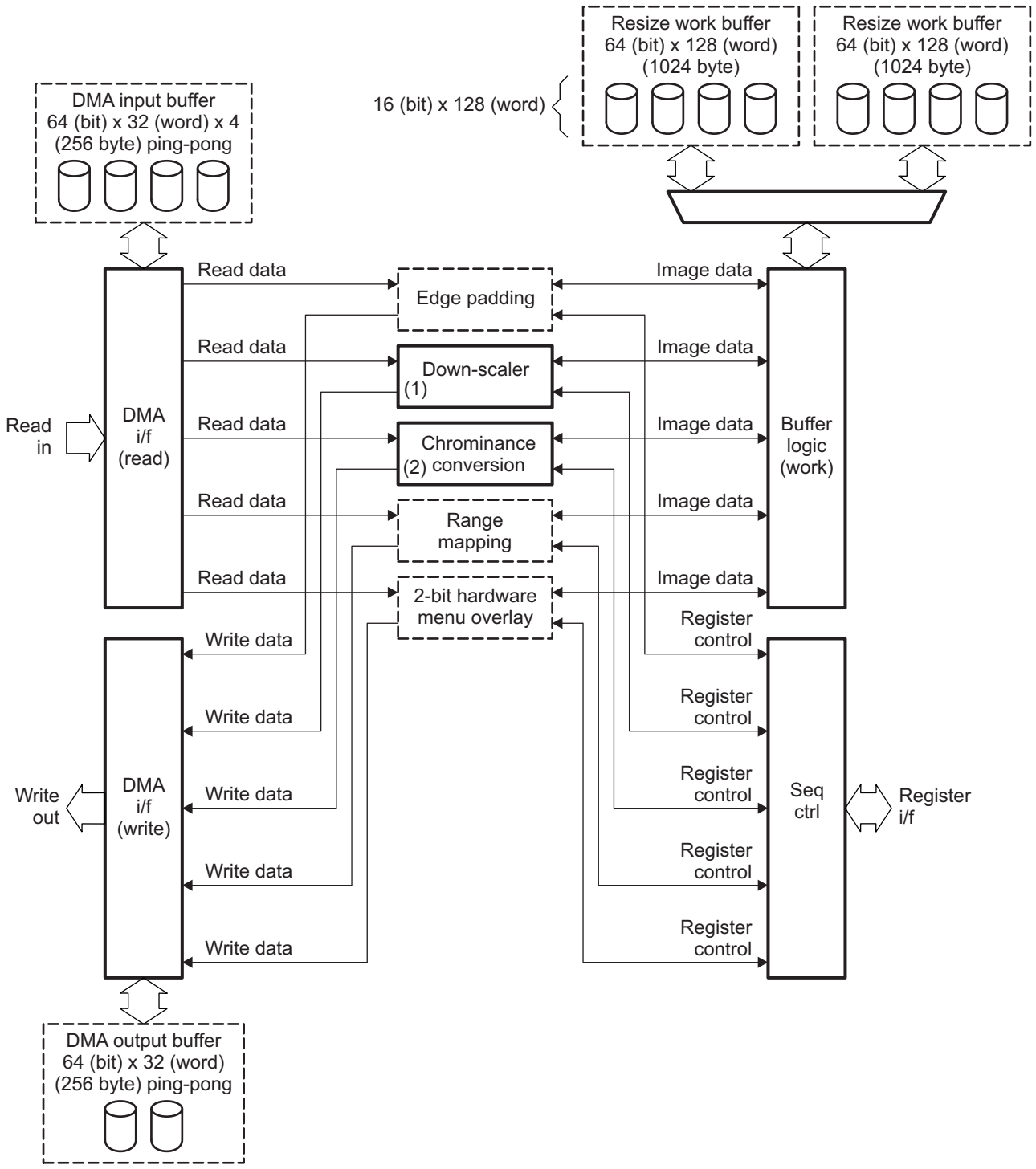


Figure 5. Processing Flow of Post-Codec Mode for Luminance Data

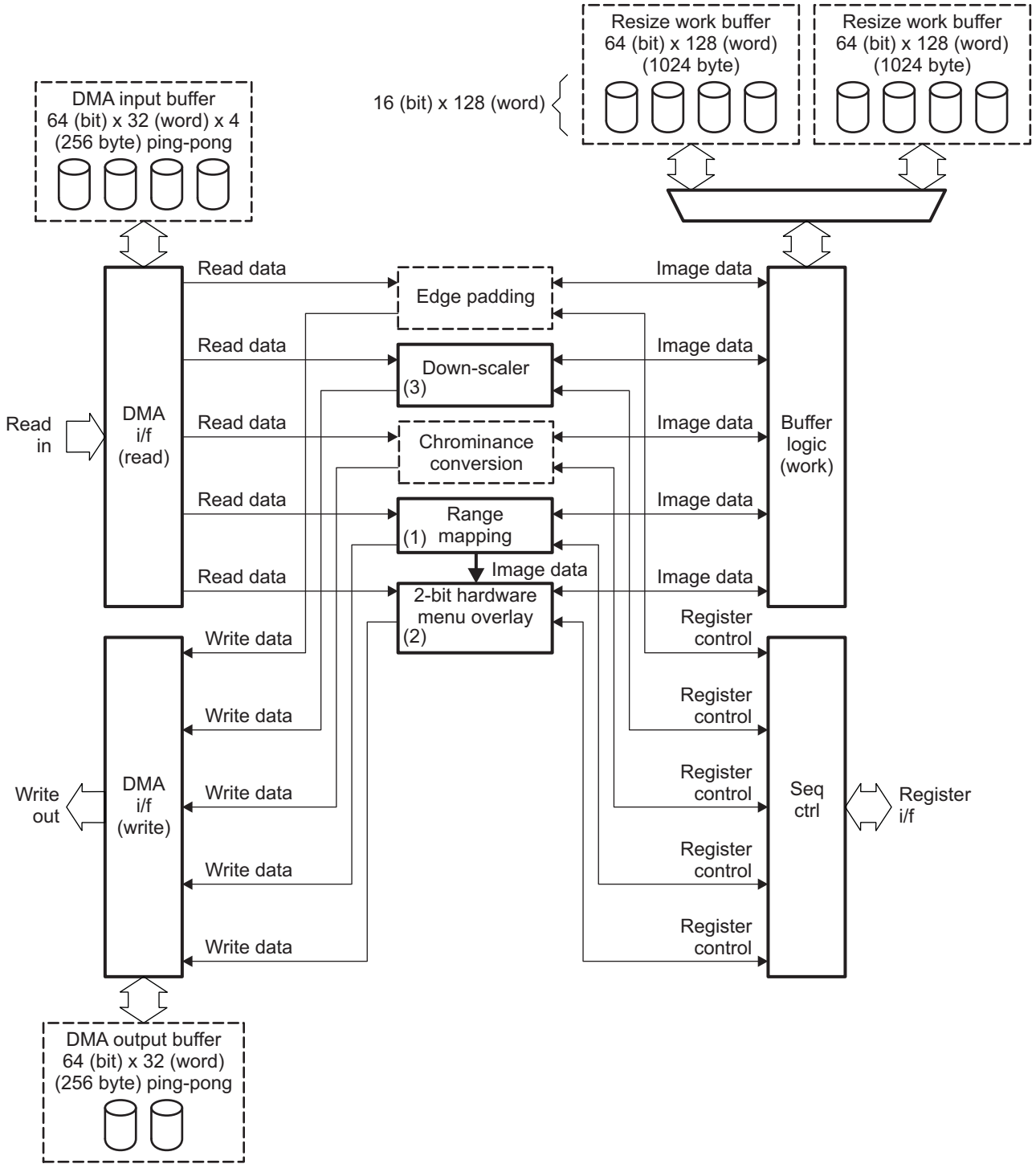
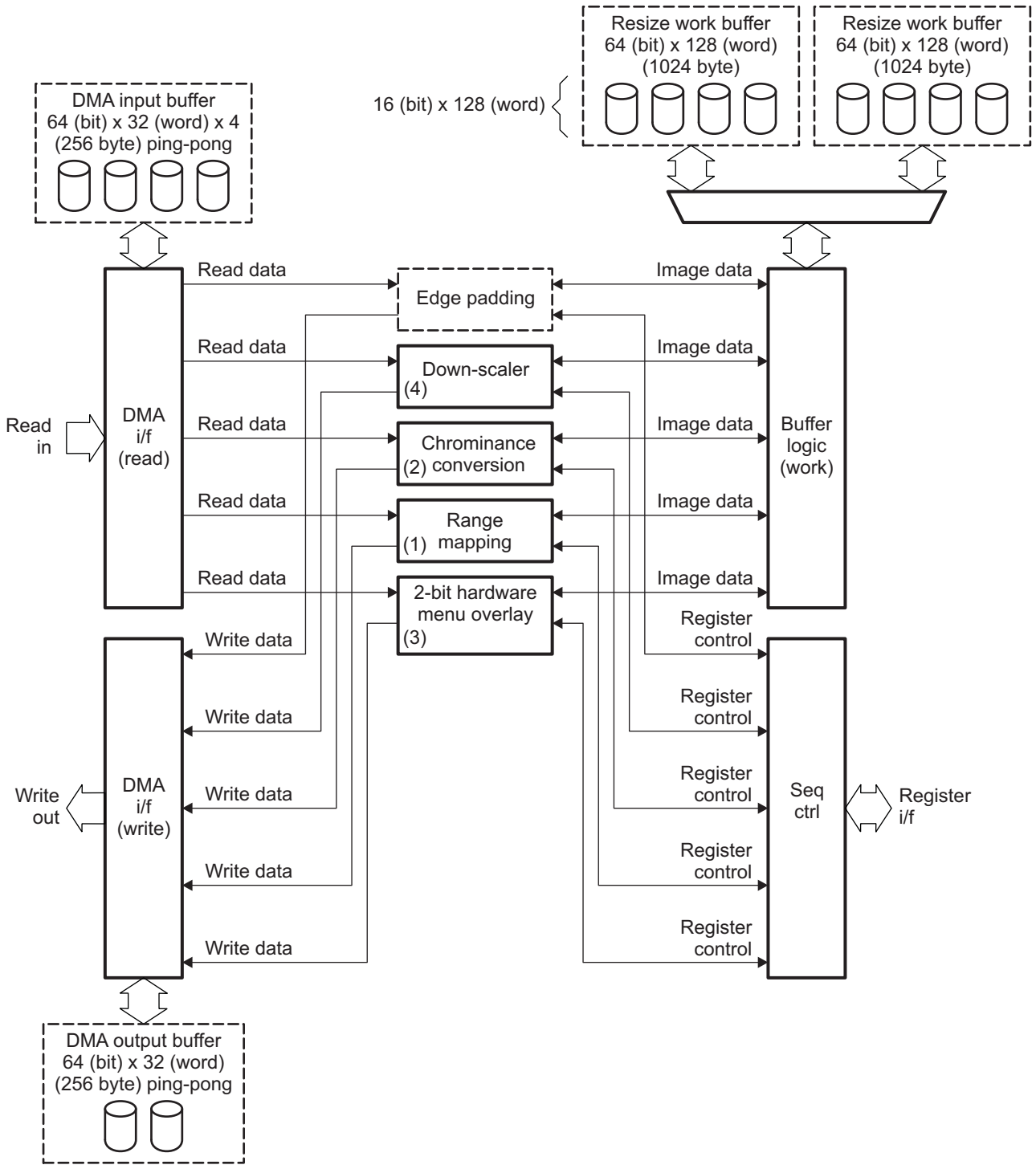


Figure 6. Processing Flow of Post-Codec Mode for Chrominance Data



2.4 Trans-Code Mode

NOTE: If you would like to enable both the down-scaler and blender, you have to enable the VDCE twice; first enable the VDCE for the down-scaler, and then enable the VDCE for the blender. Simultaneous performance of the down-scaler and blender is restricted in the VDCE.

This mode is prepared for processing reference output data of the video codec (decoder), and put back the processed image data to the video codec (encoder) as reference frame data. The following functions inside the VDCE should be activated when in trans-code mode.

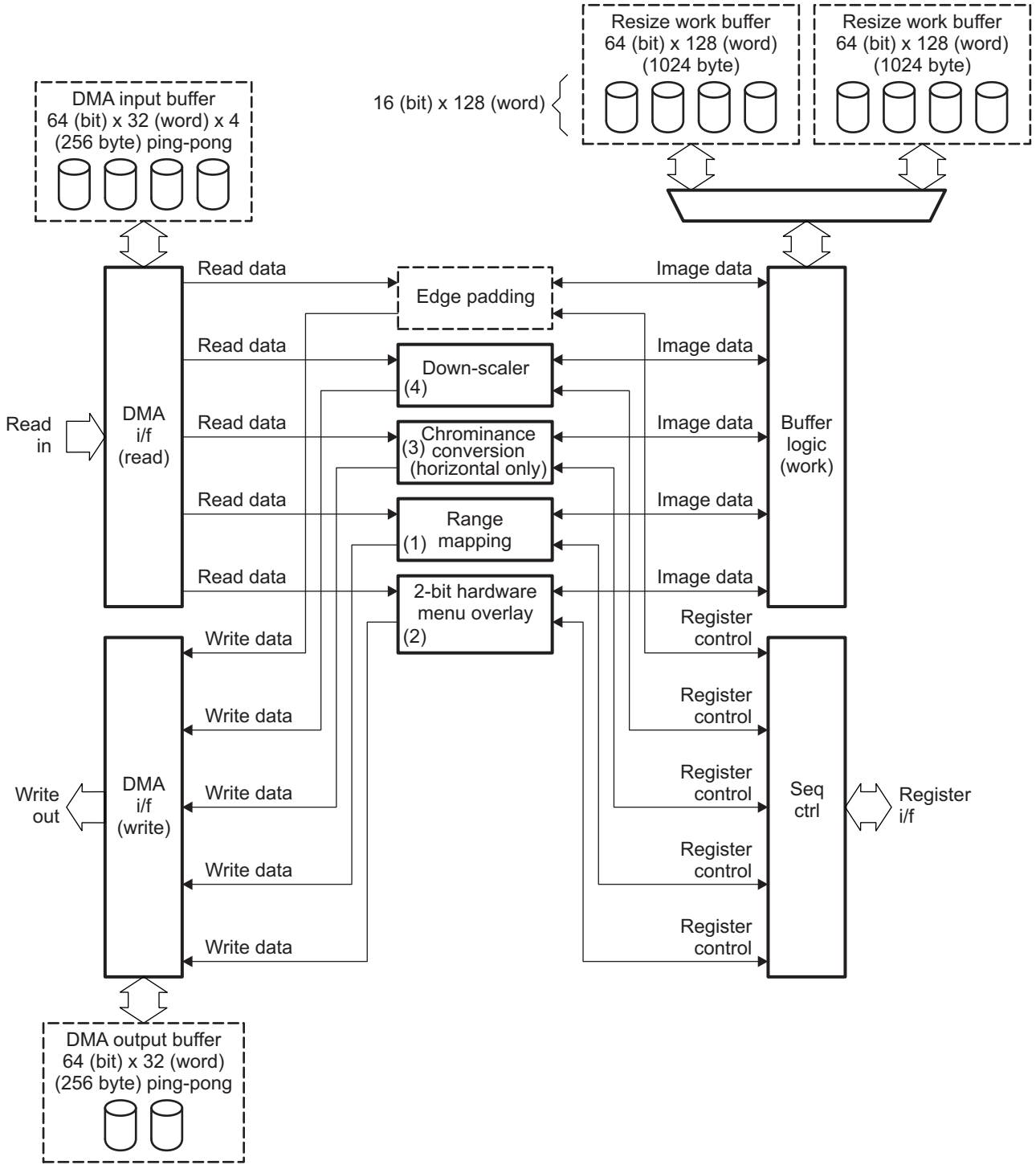
- Horizontal and vertical down-scaler.
- Edge Padding (H.264, VC-1 and MPEG-4).
- 2-bit hardware menu overlay of video image and artificial bitmap sub-title (with 2 bits/pixel bitmap).
- VC-1 range mapping (necessary when trans-coding from VC-1 to any other format of video codec).

Processing flow and activated functions are shown in Figure 7. The vertical chrominance conversion function is not activated in this mode because the reference frame needs to be compliant to 4:2:0 chrominance format, but you can activate the horizontal chrominance conversion function. The number listed beside each function block indicates the processing order in this mode.

The 2-bit hardware menu overlay function is used for blending of pixel data between video image data and artificial bitmap data. This function is mainly used for sub-title data defined in ARIB standard that is DTV broadcasting (Digital TV broadcasting) standard in Japan. Most broadcasted sub-title data has equal to or less than 4 colors. So, we prepare 2 bits/pixel bitmap window with blending step of 256 steps.

The edge padding function can not process with the other 4 functions. If you need to do the edge padding function, you have to prepare the image before you process the edge padding function. This means you have to initiate the VDCE separately, process the function that you want except for edge padding, and then do the edge padding function.

Figure 7. Processing Flow of Trans-Code Mode



2.5 Function of Sub-Module

The function of each core sub-module is described in this section. As discussed in previous sections, the VDCE has several core modules for image data processing. This section explains the concept of image processing carried out inside each sub-module.

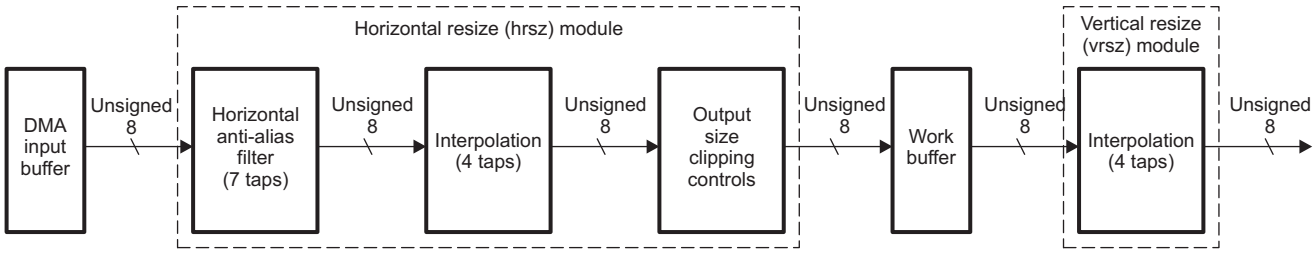
2.5.1 Horizontal and Vertical Down-Scaler

In this section, detailed specification and processing flow of the down-scaler function is described. Both horizontal and vertical down-scaler functions for pixel interpolation (4 taps linear and cubic convolution) are the same.

The down-scaler function can be divided into horizontal down-scaler and vertical down-scaler at the work buffer. Interpolation (4 taps) is same part for both horizontal and vertical down-scaler. This block diagram (and processing flow) is in common for both luminance and chrominance pixel data. Detailed functionality of each block is discussed in a latter description.

The data processing flow is shown in Figure 8.

Figure 8. Processing Flow of Horizontal and Vertical Down-Scaler



2.5.1.1 Horizontal Down-Scaler Module

As shown in Figure 8, horizontal down-scaler module has following functions:

- Anti-alias filter (7 taps) for luminance data.
- Pixel interpolation (4 taps) for common use of luminance and chrominance data.
- Size clipping to configured size on module register.

Block diagram of the anti-alias filter is in Figure 9.

Figure 9. Anti-Alias Filter Block Diagram

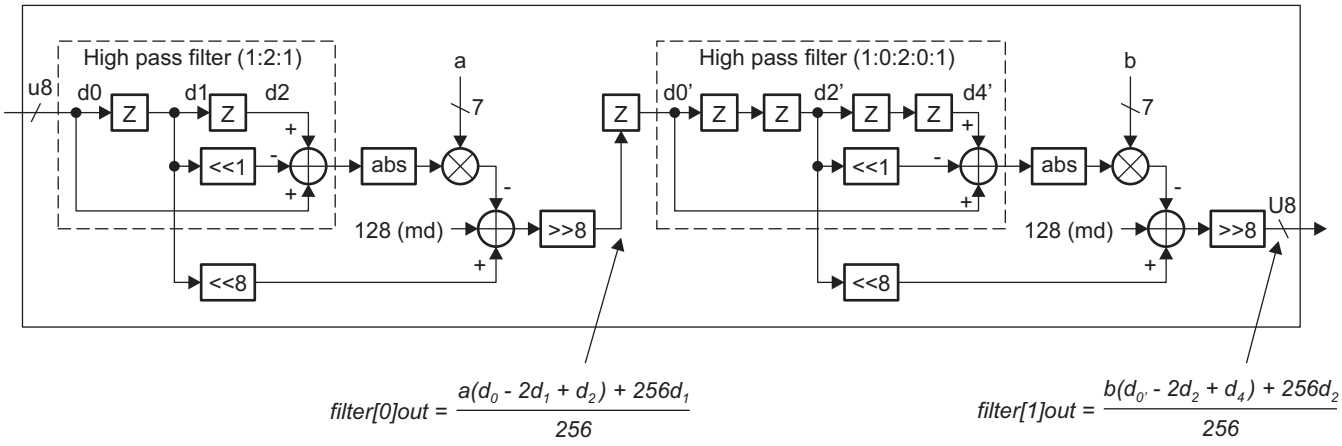


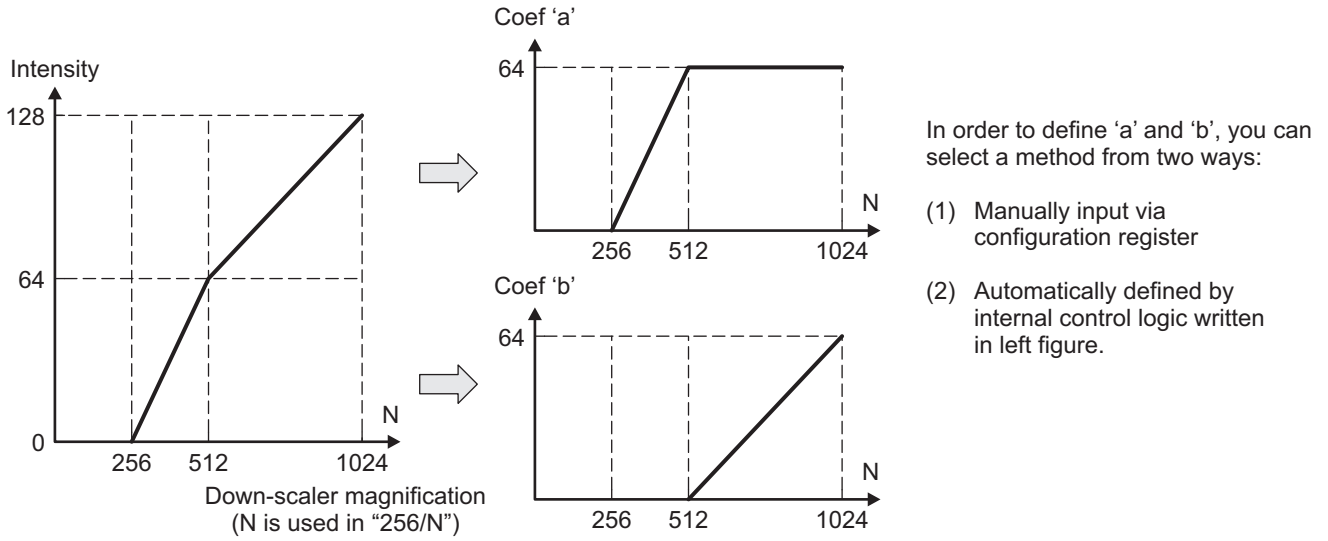
Figure 9 shows an internal diagram of the anti-alias filter that is prepared for the pre-down-scaler filter of luminance data. As you can see, this filter module has two high pass filters; a 3 taps filter and a 5 taps filter and both filters are connected in cascade.

With each high-pass filter, weight coefficients a and b for high-frequency component exists. To remove the high-frequency component (which means activating the filter as a low-pass filter), these coefficients have to be configured to non-zero value; the more low-pass filter you need, the higher the value that coefficients a and b are configured.

There are two methods used to define coefficients a and b. One method is fully manual input from the configuration register. The other method is the automatic method in which internal logic defines these weight coefficients related to the down-scaler magnification ratio.

Concept of the method to define the two coefficients a and b is shown in Figure 10. You can see that these coefficients contribute to the intensity of this anti-alias filter.

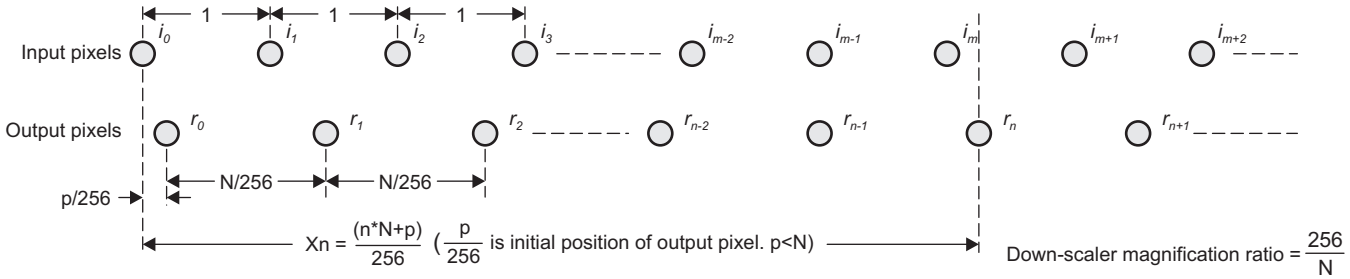
Figure 10. Anti-Alias Filter Coefficients a and b



After treatment of this anti-alias filter, pixel interpolation with 4 taps filter is carried out to generate down-scaled pixel data. Make sure of the placement of each down-scaled pixel data. In other words, make clear the relationship between the down-scaler magnification ratio and placement of the down-scaled pixel data.

As shown in Figure 11, p is the initial position of the output down-scaled pixel. In the register configuration, you should write a value of N to the module register. Inside the module, N/256 is regarded as the distance of each output pixel data, and p/256 is regarded as the initial output pixel position in the down-scaled image.

Figure 11. Image of Down-Scaled Pixel Position with Down-Scaler Magnification Ratio



In order to derive output pixel data, calculate it from nearest 4 pixels with 4 taps filter. The interpolation method is shown in Figure 12.

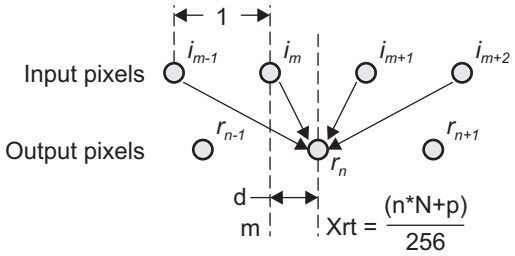
We can select the characteristics of interpolation from two methods, linear interpolation and cubic convolution. Either mode can be selected by configuration of the module register (detailed method will be described later).

This interpolation method is used for not only for horizontal direction but also for vertical direction. In vertical mode, Z is equal to delay per line. (See Figure 12.) So, the internal architecture will be a little bit different from the horizontal down-scaler.

Note that parameter N for the down-scaler magnification ratio should be 256 or more than 256 (it means that only down-scaling is available) due to the issue of SDRAM BW. Because SDRAM BW is full of data traffic, we cannot make source image data to be larger than present except processing for chrominance data format conversion.

Figure 12. Pixel Interpolation Method on Down-Scaler Module

Interpolation method



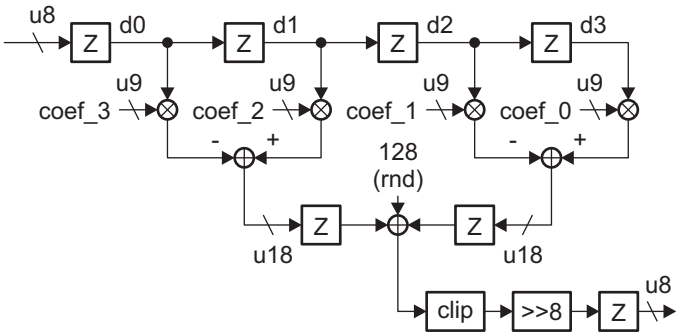
This output pixel r[n] is determined using the nearest 4 input pixels in the following manner:

$$r_n = h(1+d)i_{m-1} + h(d)i_m + h(1-d)i_{m+1} + h(2-d)i_{m+2}$$

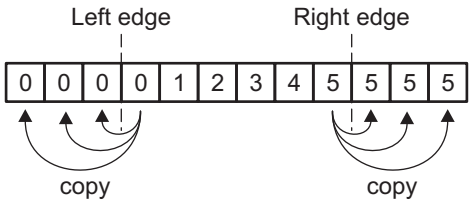
$$m = floor\left(\frac{nN+p}{256}\right),\ d = \frac{nN+p}{256} - m$$

h(n) is interpolation function (coefficient) which can be selected from linear interpolation and cubic convolution

Block diagram of interpolation (in common for vertical resize)



Pixel treatment for "out-frame" pixels



2.5.1.2 Vertical Down-Scaler Module

As shown in Figure 8, the vertical down-scaler process consists of interpolation logic whose concept is the same as the horizontal down-scaler module. See Figure 11 and Figure 12 for pixel interpolation method of down-scaled output pixel data.

The method of vertical down-scaler varies from picture format, interlace, or progressive. In interlace format, the vertical down-scaler function performs for each field independently. All source pixels of interpolation are derived from the same field.

In progressive format, the vertical down-scaler function performs for frame. All source pixels of interpolation are derived from both fields.

In the vertical down-scaler module, you can select output data from non-interpolated data and interpolated data.

2.5.2 Chrominance Conversion

Chrominance conversion module is used for format conversion of chrominance signal between 4:2:2 and 4:2:0 formats. The 4:2:0 format is mainly used for video codec and the 4:2:2 format is used for input or output video signals such as BT.656 or BT.1120.

The 4:2:0 format has two patterns; one is used in MPEG-1 and the other one is used in various types of video codec except for MPEG-1 (namely, MPEG-2/MPEG-4/H.264/VC-1 uses different method for chrominance conversion from MPEG-1). Detailed difference is explained in following descriptions.

Functional performance of chrominance conversion varies from type of video codec. In case of MPEG-2, MPEG-4, H.264, and VC-1, chrominance signal position in horizontal direction is same as even pixel position of luminance signal. But in MPEG-1, chrominance signal places half pixel phased from even pixel position of luminance signal.

Chrominance conversion uses the same algorithm as the down-scaler function; both of 422 → 420 and 420 → 422 conversions can be regarded as the vertical down-scaler of chrominance field/frame data, and phase change in MPEG-1 can be regarded as the horizontal down-scaler of chrominance field/frame data (rescale to same size with initial phase change). So, you can select interpolation algorithm from two methods (4-taps cubic convolution and 4-taps linear interpolation), same as the vertical down-scaler of the picture level.

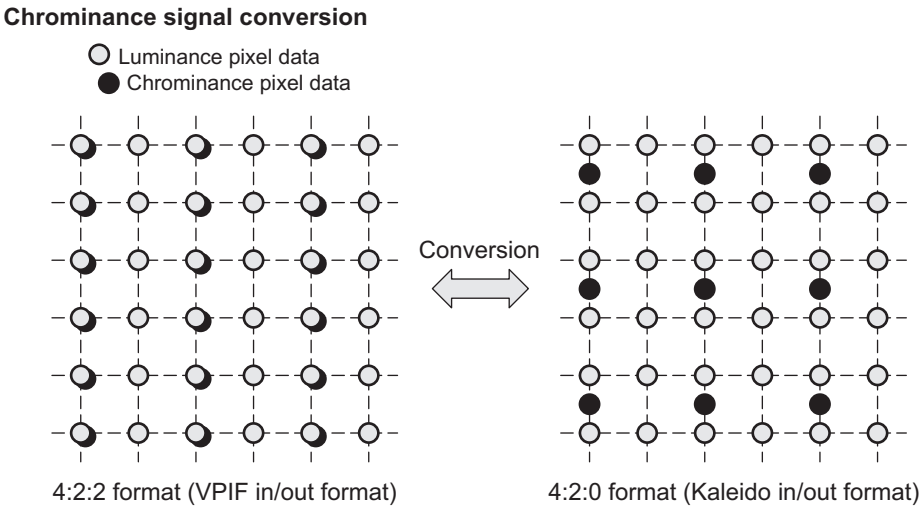
SDRAM storage format is shown in Figure 29 (same as down-scaler).

NOTE: If you configure the VDCE_MODE bit in the control register (CTRL) to 2h (pre-codec mode) or 3h (post-codec mode), vertical chrominance conversion is automatically activated for each proper direction (in pre-case, 422 → 420. in post-case, 420 → 422). On/Off control of vertical chrominance conversion is not related to the VDCE_CCV_EN bit in CTRL.

2.5.2.1 Chrominance Conversion on MPEG-2/MPEG-4/H.264/VC-1

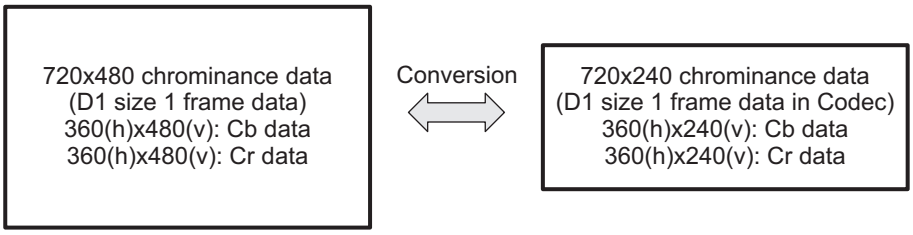
Image of chrominance format conversion is shown in Figure 13. In these types of video codec, the horizontal position of chrominance signal is correspondent to even pixel position of luminance data.

Figure 13. Chrominance Conversion of 4:2:2 and 4:2:0 on MPEG-2/MPEG-4/H.264/VC-1



As shown in Figure 13, both Cb and Cr exist at each chrominance point. The difference between the two formats is the sample number for vertical direction; 4:2:2 format needs twice more samples than 4:2:0 format. So, taking this fact into consideration, this function can be regarded as the vertical down-scaler on chrominance data. If we fix the down-scaler magnification ratio and phase of first pixel data for each usage of conversion, we can accomplish chrominance conversion using the same logic as the vertical down-scaler. This concept is shown in Figure 14.

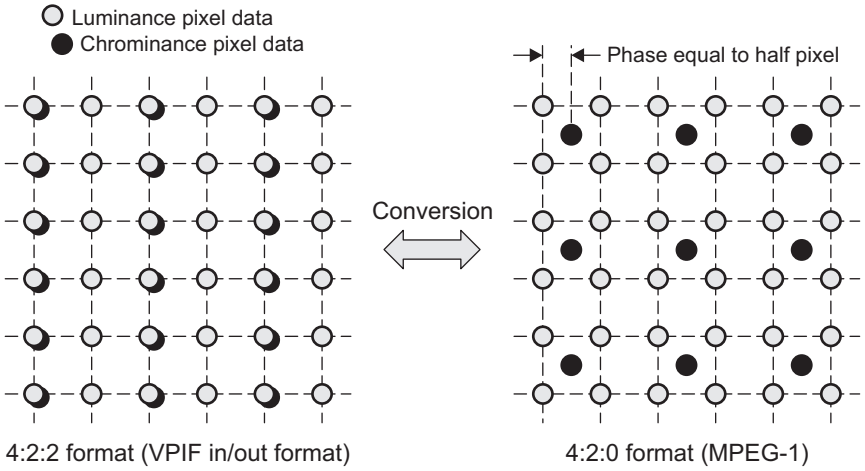
Figure 14. Concept for Method of Chrominance Conversion on Figure 13



2.5.2.2 *Chrominance Conversion on MPEG-1*

An image of chrominance format conversion is shown in Figure 15. In MPEG-1, horizontal position of chrominance signal in 4:2:0 format is half pixel phased from even pixel position of luminance data (sampling number is same as any other codec).

Figure 15. Chrominance Conversion of 4:2:2 and 4:2:0 on MPEG-1



Both Cb and Cr exist at each chrominance point. See Section 2.5.2.1. 4:2:0 sampled chrominance position is horizontally phased from even pixel position of luminance data for half pixel (see Figure 15) that differs from Section 2.5.2.1.

Format conversion for vertical direction can be carried out in the same concept as shown in Figure 14. However, processing for horizontal direction should be carried out prior to format conversion for vertical direction. Processing for horizontal direction can be executed by using the down-scaler module configuration listed below:

- Initial phase = 128 (1/2 pixel phased).
- Down-scaler magnification ratio N = 256 (means no re-scaling; same size as source).

Method for detail data calculation is referred to Figure 11 and Figure 12.

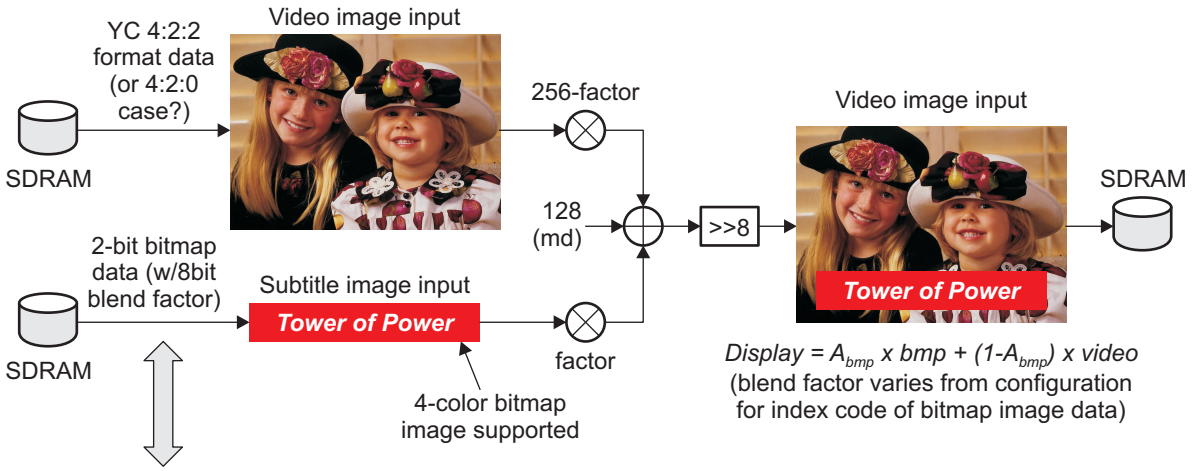
2.5.3 2-Bit Hardware Menu Overlay

The VDCE has a 2-bit hardware menu overlay function that can blend video image (output of decoder module) and artificial bitmap data (2 bits/pixel), like a light OSD function. This function is used for the requirement from the ARIB standard (Digital TV broadcasting in Japan) to process artificial bitmap data that is used for sub-title in most cases. Performance image of this function is shown in Figure 16.

The 2-bit hardware menu overlay function reads two kinds of data (video and bitmap) from SDRAM, and overlays them to one display output data with blending (based on configured value written in each look up table index value).

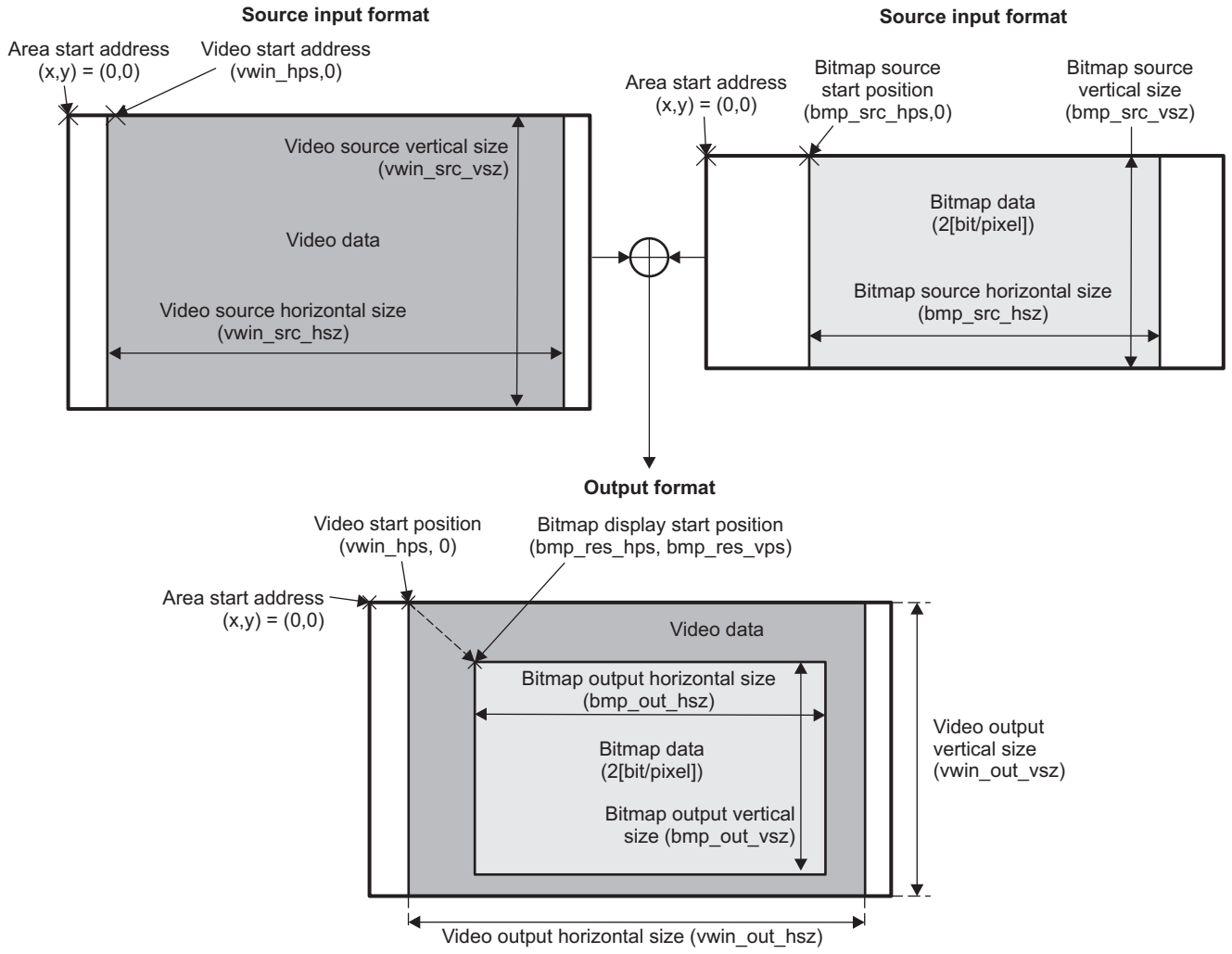
SDRAM data allocation method with displaying image allocation is written in following Figure 17. Bitmap data has 2-bit length and each table value (color code for Y, Cb, Cr, and blend factor with 8-bit length) can be configured from the CPU via the module register. You have to configure the start position of each window in both SDRAM and display. This function starts to work based on the register configuration.

Figure 16. 2-Bit Hardware Menu Overlay Diagram



Code / Index	Color data (given in YC format)	Blend factor (alpha-blend)
0	Color code for index 0	Blend factor for index 0
1	Color code for index 1	Blend factor for index 1
2	Color code for index 2	Blend factor for index 2
3	Color code for index 3	Blend factor for index 3

Figure 17. SDRAM Data (source and result) Allocating Method of 2-Bit Hardware Menu Overlay Function



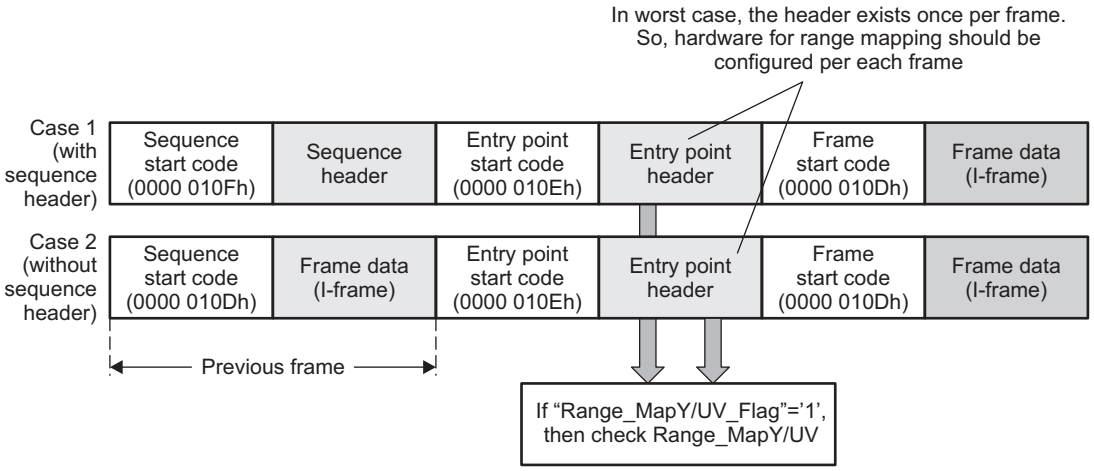
2.5.4 Range Mapping

Range mapping is defined in standard of VC-1. To display reference image data (decoder output) or recover range of decoded pixel data for re-encoding on another video codec format (in case of trans-coding from VC-1 to any other video codec format), you have to do this treatment (in pre-codec mode, this function shall not be activated).

In VC-1 encoding and decoding, reference image data for each pixel should be intentionally ranged down (VC-1 specification defines it). To display (or recover pixel data of) VC-1 decoded image, configure the range mapping module based on parsed result of stream data; activation flag of this range mapping is inserted in the entry point header (Range_MapY_Flag for luminance, and Range_MAPUV_Flag for chrominance). The entry point header exists before every I-frame (or I-field), being the same as the GOP header in specification of MPEG.

Inserted image of the control flags in stream data is shown in Figure 18.

Figure 18. Image of Parsing Control Flag for Range Mapping of VC-1

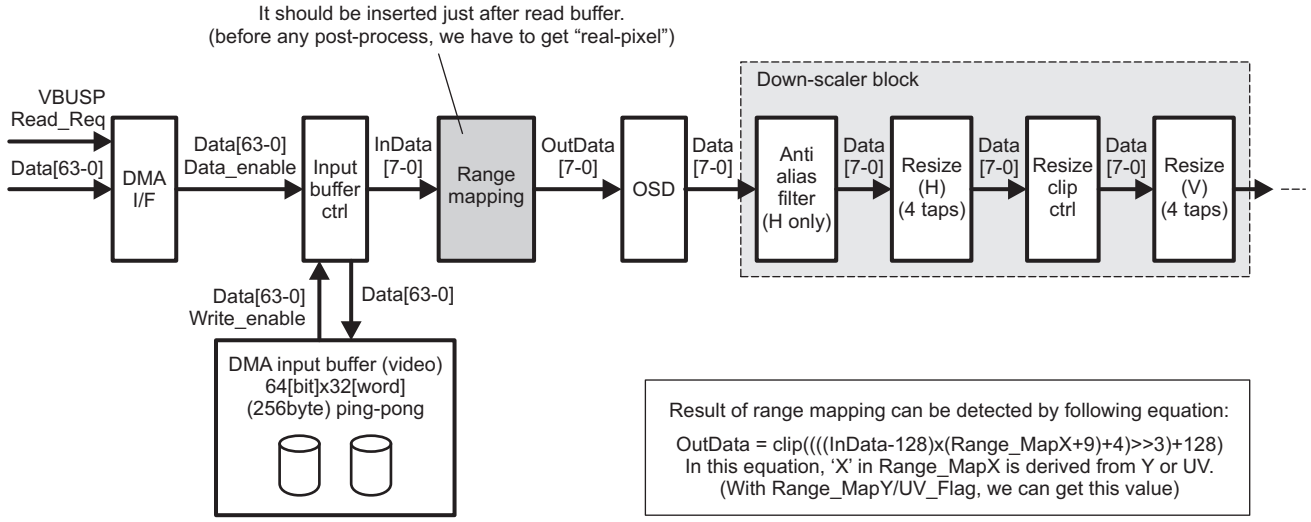


From the result of parsing, the VC-1 range mapping function is configured. If configured to be activated, this should be the first function that the VDCE processes in order to derive range-recovered image data.

Range mapping is carried out with the following equations for luminance and chrominance sample data. Processing flow of this range-mapping with other sub-modules is shown in Figure 19. In following equations, Range_MapY and Range_MapUV are coefficients for multipliers that have 3 bit length and both of Y[n] and C[n] are pixel data to be processed with valid flags.

$$Y[n] = clip((((Y[n]-128)*(Range\_MapY+9)+4)>>3)+128$$
$$C[n] = clip((((C[n]-128)*(Range\_MapUV+9)+4)>>3)+128$$

Figure 19. Processing Flow in VDCE with VC-1 Range Mapping



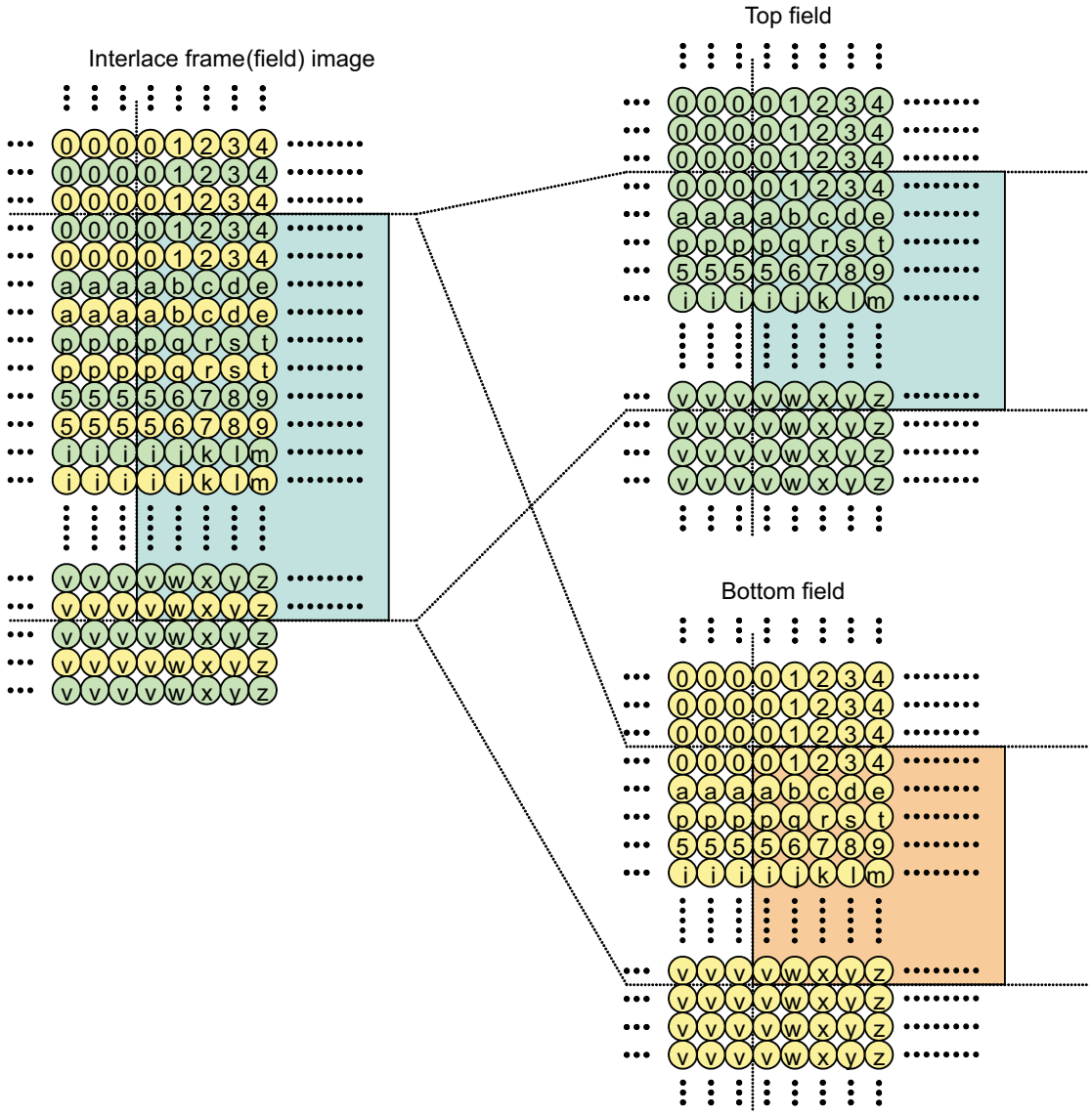
2.5.5 Edge Padding

Edge padding is prepared for enhancement of reference image data to be used in MC (motion compensation) function with unrestricted motion vector that is defined in specification of H.264, VC-1, and MPEG-4. This module copies all edge pixels to the external side of the reference data with configured width for both horizontal and vertical directions (both upper and lower, both left and right of the image data).

This module has to finish working before the decoding function for next frame is started. This module has a very limited working time period in which to process the decoding sequence; from the time when decoding frame [–1] is finished, to the time when decoding frame [n] is started. Taking usage of this function into consideration, it is possible that this function may be independently configured from the CPU via module register.

The method of edge padding varies in two ways, one is progressive format and the other is interlaced format. Padding image of interlace format is shown in Figure 20 and progressive format is shown in Figure 21.

Figure 20. Functional Image of Edge Padding on Interlaced Format

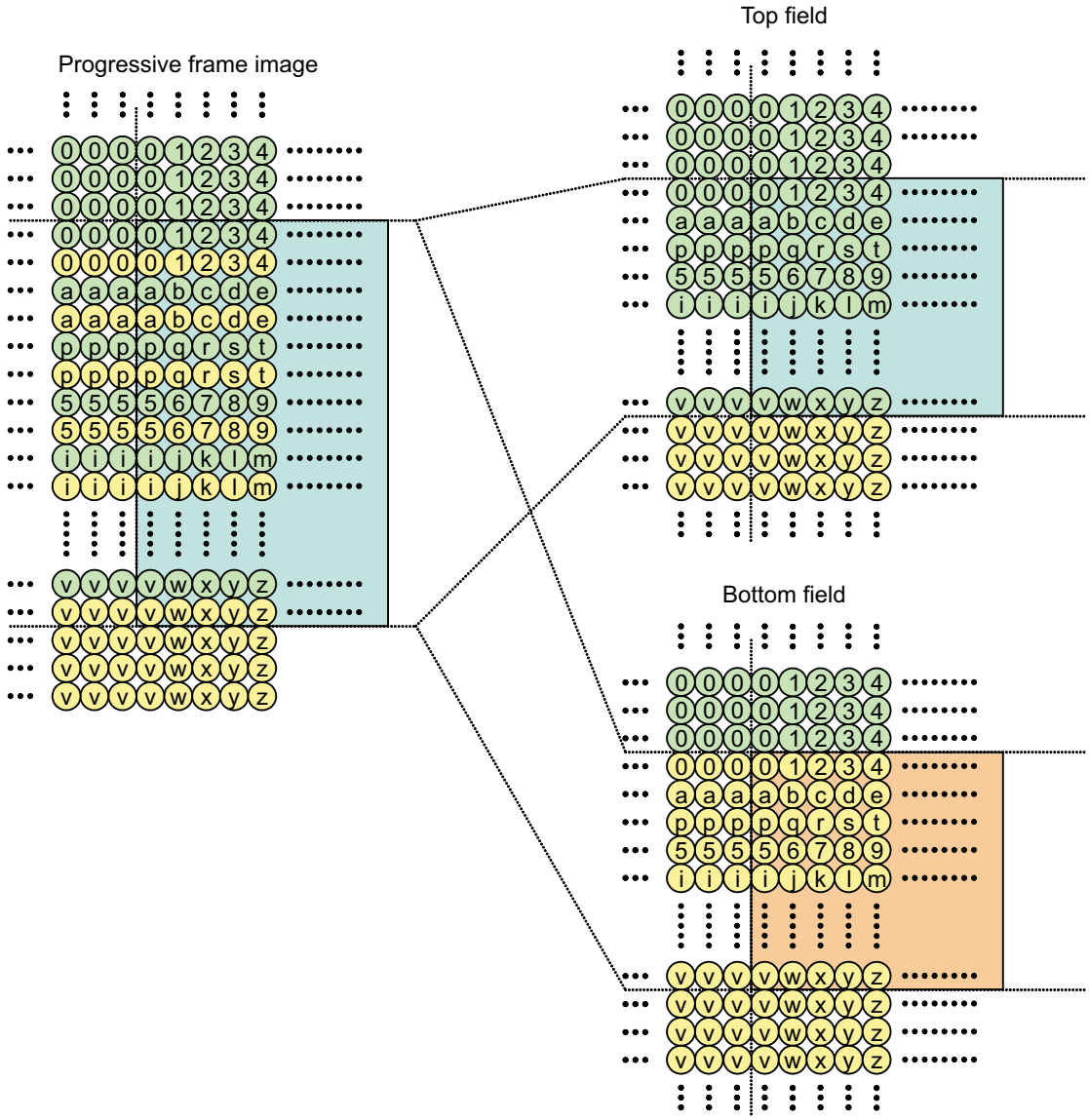


In interlaced format, edge padding for vertical direction should be worked on field based format. It means that the odd line in the padding area should be padded by an odd field, and the even line in the padding area should be padded by an even field. This performance mode is called interlace mode (mode-A) in register map. Functional performance of padding is the same for both the upper side of targeted picture as well as the lower side of targeted picture.

For the left horizontal direction, edge pixels on the left side of targeted picture are copied. See Figure 20. For the right horizontal direction, edge pixels on the right side of targeted picture are copied. Edge padding in horizontal direction needs the same performance for each field.

Contrary to MPEG-1/MPEG-2/MPEG-4/VC-1, MC mode control of H.264 is switched for each macroblock (in the other 4 codecs, this control is switched for each picture level). So, in H.264 decoding case, you should use this field mode. When using this mode for MC function, you should derive the reference picture data from SDRAM (with padded result) based on calculation result of the access address.

Figure 21. Functional Image of Edge Padding on Progressive Format



In progressive image, edge padding for the vertical direction should be worked on a frame based format. It means that the first line of the frame should be copied to upper line of the frame, and the last line of the frame should be copied to lower line of the frame. For module performance, the upper area of each field should be padded by the first line of the top field, and lower area of each field should be padded by the last line of the bottom field. The described performance is shown in Figure 21. This performance is called progressive mode (mode-B) in register map.

Performance on the horizontal direction is the same as that of interlace mode; padding for left horizontal direction is carried out by copying left edge pixels and padding for right direction is carried out by copying right edge pixels. This performance can be also seen in Figure 21.

The relationship around picture type (interlace or progressive), storage format (frame or field), and edge padding parameters are shown in Figure 22 and Figure 23.

Address configuration and source/result start position/size are very important aspects of the control method of edge padding. Parameters including the address value are shown in Figure 24.

Figure 22. Edge Padding Explanation for Frame Storage Mode

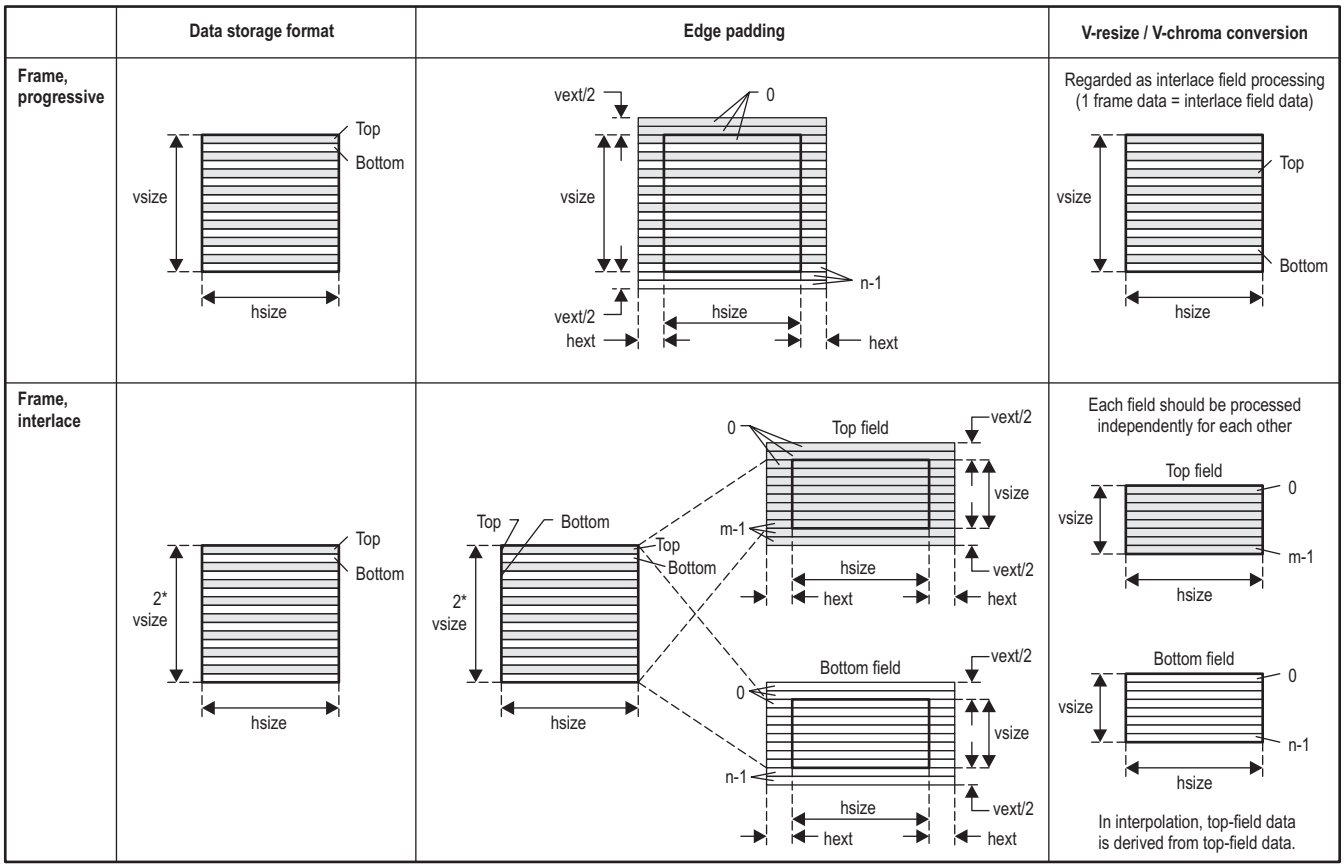


Figure 23. Edge Padding Explanation for Field Storage Mode

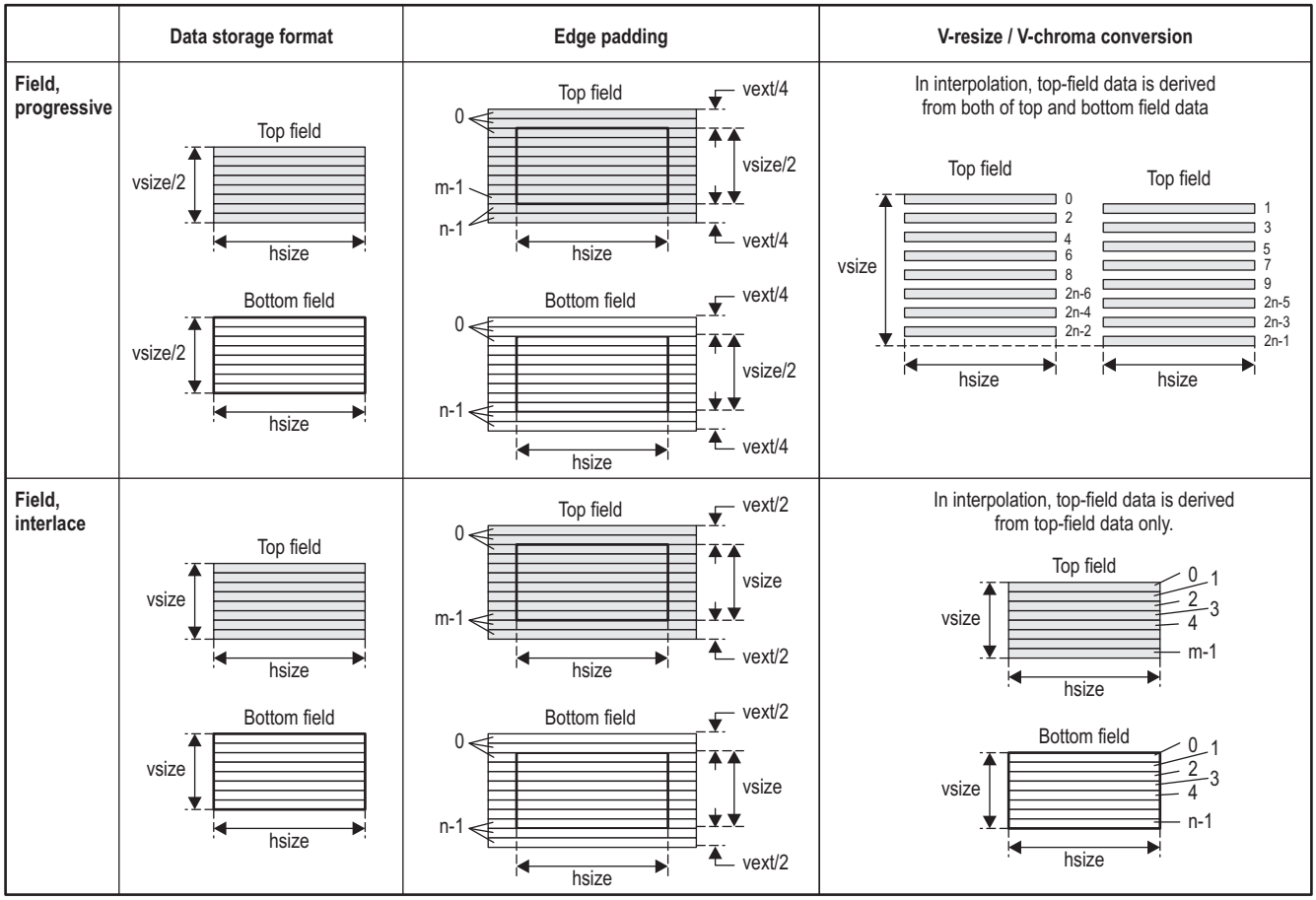
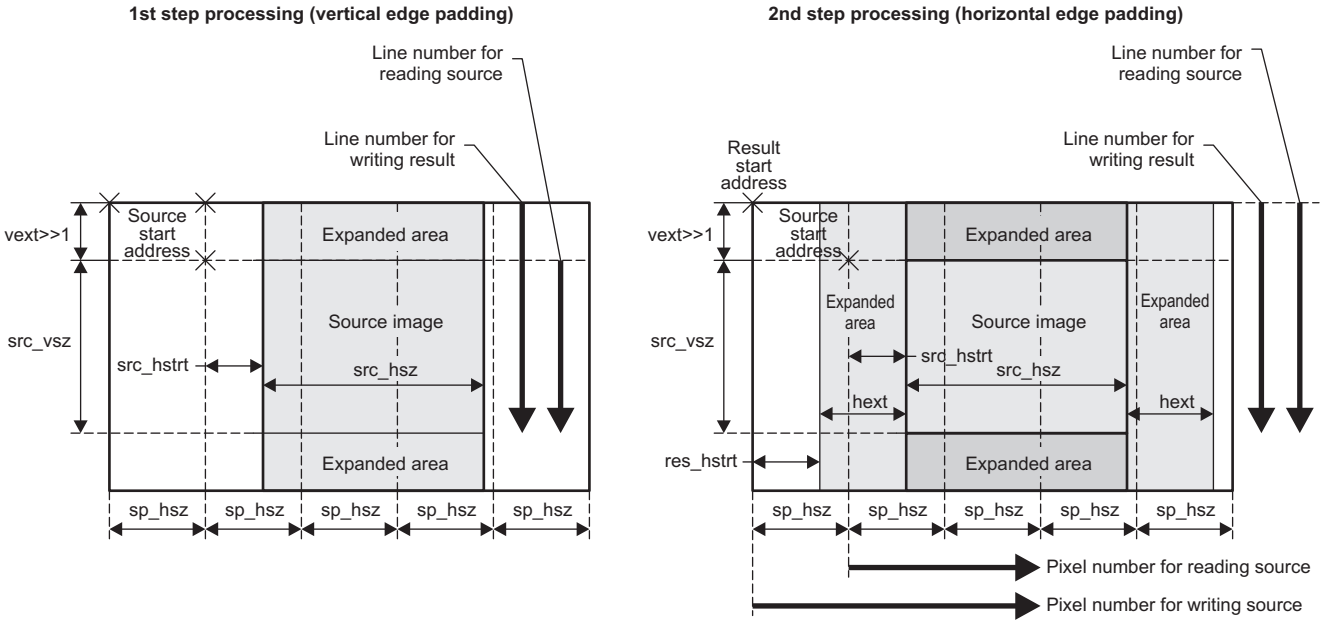
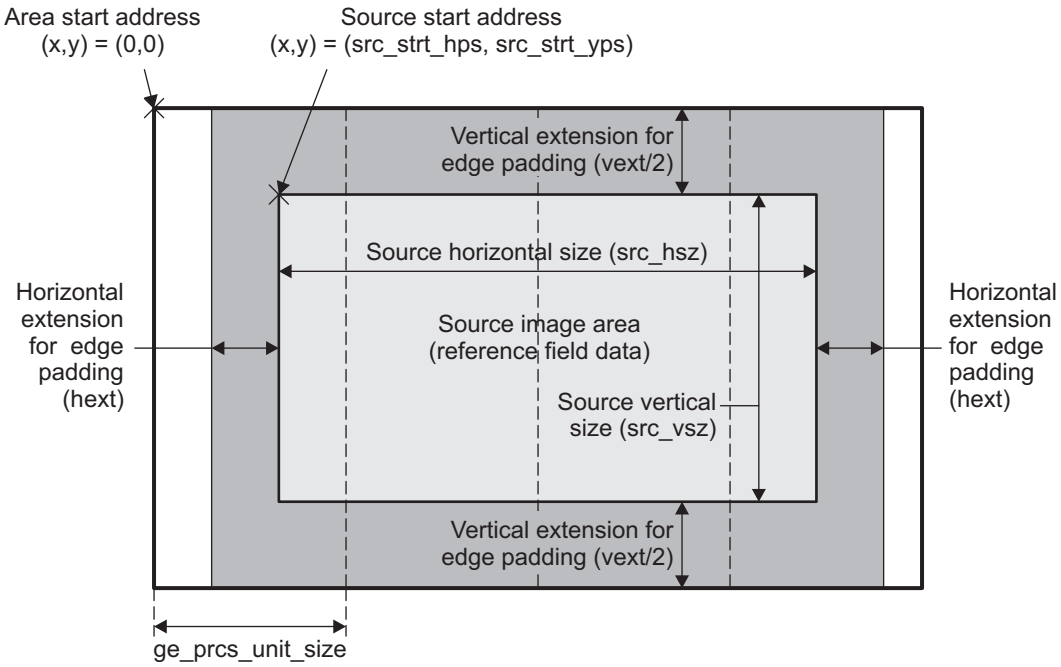


Figure 24. Edge Padding Address Control Method



Configuration registers for edge padding module (prepared for unrestricted motion vector on H.264, VC-1 and MPEG-4) are described in Section 3.64 and Section 3.65. The edge padding function is related to SDRAM data storage format and also type of picture to be decoded (progressive or interlace). Detail functional image is shown in Figure 25.

Figure 25. Parameter Relationship between Address and Position on Edge Padding



2.6 Reset Considerations

The VDCE does not have a software reset future.

2.7 Initialization

You must configure all register bits prior to setting the VDCE_GO bit in the VDCE control register (CTRL), including the following:

- REQ_SIZE register
- PROC_SIZE register
- Either the VDCE_CROMA_EN bit or the VDCE_LUMA_EN bit must be configured to 1.
- Either the VDCE_TOP_FIELD_EN bit or the VDCE_BTM_FIELD_EN bit must be configured to 1, in the case of processing interlace image (VDCE_SRC_NIP = 1).
- Use care of emulation related registers such as EMU_CTRL and SUSPSRC in the System Module (see Section 2.10.2 for more detail). The defaults value of these register are configured to ARM is main processor.

If these registers do not set, you can set the VDCE_GO bit in CTRL, but the VDCE does not work and never comes back in a ready state. If the VDCE is in this wrong state, LPSC can not change VDCE state. Hardware reset is only way to resetting VDCE module.

2.8 Interrupt Events and Requests

The VDCE can send interrupt events to the ARM and/or the DSP. The VDCE interrupt is generated when the configured processing is finished.

The VDCE has a single interrupt source (Table 1) mapped to the ARM interrupt controller. For more information on the ARM interrupt controller (AINTC), see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

Table 1. VDCE Interrupt

ARM Event	Acronym	Source
12	VDCEINT	VDCE

2.9 Power Management

The VDCE can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processors Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

LPSC can control the VDCE state when the VDCE is in ready state. If the VDCE is in GO state, then the LPSC can not change the VDCE state.

2.10 Emulation Considerations

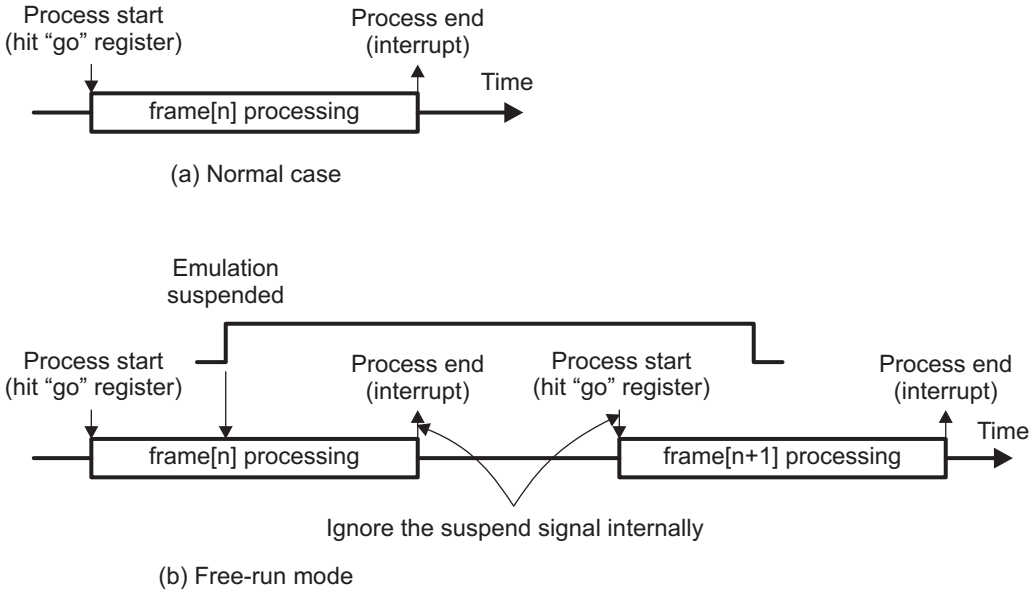
Control register of this interface function is written in the emulation control register (EMU_CTRL). With this register, you can select the following four modes on interfacing logic of the VDCE.

2.10.1 Normal (Free) Mode

Free mode means that each module performs free from polarity of the emulation suspend signal. Each module ignores the emulation suspend signal in this mode. A comparison between normal processing and free mode is shown in Figure 26.

Regardless of the state of emulation suspend, the module configuration register can be accessed by the CPU.

Figure 26. Functional Image of Free-run Mode on Emulation Suspend

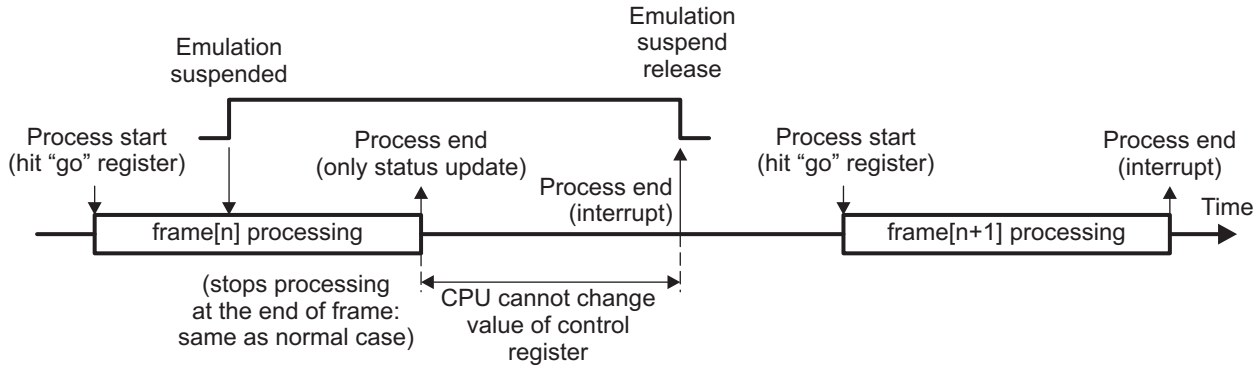


2.10.2 Soft Stop Mode

Soft stop mode means that each module stops processing after the present unit is finished with its on-going process. In addition, the module cannot stop until after the present unit of processing is complete even if the emulation suspend signal is asserted by the CPU during present processing.

A comparison between normal processing and soft stop mode is shown in Figure 27.

Figure 27. Functional Image of Soft Stop Mode on Emulation Suspend



Regardless of the state of emulation suspend, the module configuration register can be accessed by the CPU. Note that when VDCE_GO bit in the control register (CTRL) is on address 1 it cannot accept any write access from the CPU during its period of emulation suspend. This module can start further frame processing when the VDCE_GO bit is activated after the emulation suspend is cleared by the CPU.

The interrupt signal from the VDCE provides the following cases:

1. If in emulation suspend, when processing is finished, an interrupt pulse indicating the end of processing is asserted from the VDCE to the CPU (shown in Figure 27(a)).
2. If in emulation suspend, when processing is finished, the VDCE_STATUS bit is only updated and an interrupt pulse is asserted after the emulation suspend signal becomes low (shown in Figure 27(b)). The VDCE_GO bit is also updated after the emulation suspend signal is de-asserted.

NOTE: You need proper setting of the SUSPSRC register in the in System Module. The default setting of the emulation control register (EMU_CTRL) is Soft Stop mode. The default setting of SUSPSRC for the VDCE is the ARM. In this situation, the ARM has emulation control for the VDCE. If the ARM is halted, the DSP can not start the VDCE. Because the VDCE_GO bit in the control register (CTRL) cannot accept any write access from the DSP during the period when in emulation suspend. In this case, emulation suspend is controlled by the ARM and not the DSP.

2.10.3 Hard Stop Mode

Hard stop mode is prohibited due to specification for handling emulation suspend.

2.11 SDRAM Interface

The SDRAM interface registers are prepared for SDRAM address configuration in which source and result data to be processed (or finished to be processed) by the VDCE is stored. Each register image in actual functionality is shown in Figure 28. The relationship between each address parameter and position parameter is shown in Figure 29.

In the area related to chrominance field configuration on the horizontal direction (start address, line offset, frame (field) start position, and size), the LSB bit of these registers should be configured to be 0; which means that all configurations related to the horizontal location of the chrominance field should be an even number.

Figure 28. Parameter Distribution for SDRAM Storage Method

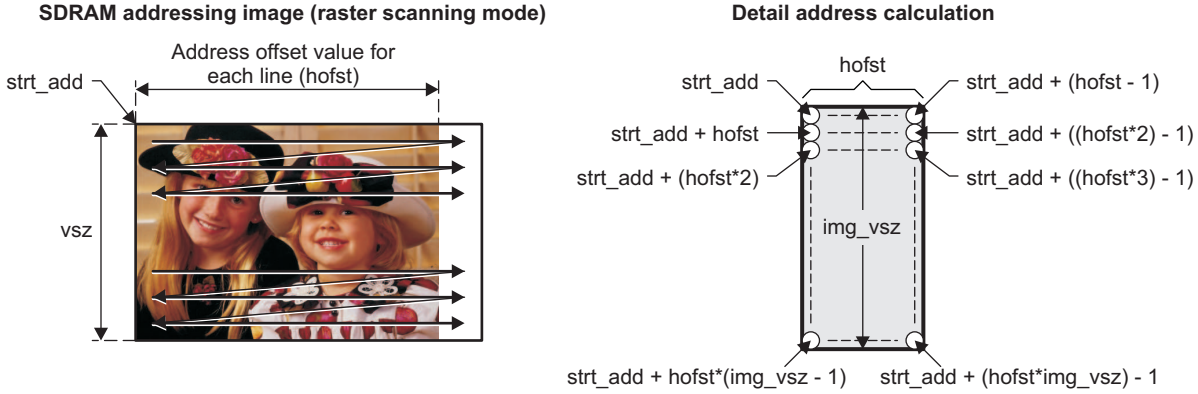
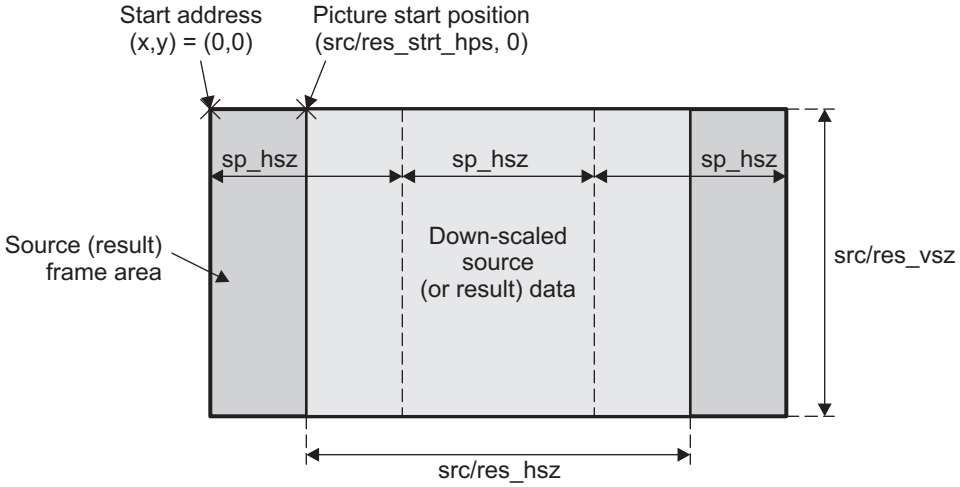


Figure 29. Parameter Relationship between Address and Position Parameters



The address value that is defined in the registers indicates the value of an area start address shown in Figure 29.

Each common scale is to be used for both source and result data storage format.

All register configurations related to Figure 29 should be prepared for both luminance and chrominance independently, because chrominance data is based on 4:2:0 type format in a mode of reference to which is prepared for trans-coder applications with picture size conversion.

3 Registers

Table 2 lists the memory-mapped registers for the video data conversion engine (VDCE). See the device-specific data manual for the memory address of these registers.

Table 2. Video Data Conversion Engine (VDCE) Registers

Offset	Acronym	Register Description	Section
0h	PID	VDCE Peripheral Identification Register	Section 3.2
4h	CTRL	VDCE Control Register	Section 3.3
8h	INTEN	Interrupt Enable Register	Section 3.4
Ch	INTEN_SET	Interrupt Set Register	Section 3.5
10h	INTEN_CLR	Interrupt Clear Register	Section 3.6
14h	INTSTAT	Interrupt Status Register	Section 3.7
18h	INTSTAT_CLR	Interrupt Status Clear Register	Section 3.8
1Ch	EMU_CTRL	Emulation Control Register	Section 3.9
20h	SRD_FRMT	Source/Result Data Store Format Register	Section 3.10
24h	REQ_SIZE	Request Unit Size Register	Section 3.11
28h	PROC_SIZE	Processing Unit Size Register	Section 3.12
40h	TY_SRCADDR	Luminance Top Field Source Start Address Register	Section 3.13
44h	TY_SRCSPSIZE	Luminance Top Field Source Sub-Picture Size Register	Section 3.14
48h	TY_SRCOFFSET	Luminance Top Field Line Source Address Offset Register	Section 3.15
4Ch	BY_SRCADDR	Luminance Bottom Field Source Start Address Register	Section 3.16
50h	BY_SRCSPSIZE	Luminance Bottom Field Source Sub-Picture Size Register	Section 3.17
54h	BY_SRCOFFSET	Luminance Bottom Field Line Source Address Offset Register	Section 3.18
58h	TC_SRCADDR	Chrominance Top Field Source Start Address Register	Section 3.19
5Ch	TC_SRCSPSIZE	Chrominance Top Field Source Sub-Picture Size Register	Section 3.20
60h	TC_SRCOFFSET	Chrominance Top Field Line Source Address Offset Register	Section 3.21
64h	BC_SRCADDR	Chrominance Bottom Field Source Start Address Register	Section 3.22
68h	BC_SRCSPSIZE	Chrominance Bottom Field Source Sub-Picture Size Register	Section 3.23
6Ch	BC_SRCOFFSET	Chrominance Bottom Field Line Source Address Offset Register	Section 3.24
70h	TBMP_SRCADDR	Bitmap Top Field Source Start Address Register	Section 3.25
74h	TBMP_SRCOFFSET	Bitmap Top Field Line Source Address Offset Register	Section 3.26
78h	BBMP_SRCADDR	Bitmap Bottom Field Source Start Address Register	Section 3.27
7Ch	BBMP_SRCOFFSET	Bitmap Bottom Field Line Source Address Offset Register	Section 3.28
80h	TY_RESADDR	Luminance Top Field Result Start Address Register	Section 3.29
84h	TY_RESSPSIZE	Luminance Top Field Result Sub-Picture Size Register	Section 3.30
88h	TY_RESOFFSET	Luminance Top Field Line Result Address Offset Register	Section 3.31
8Ch	BY_RESADDR	Luminance Bottom Field Result Start Address Register	Section 3.32
90h	BY_RESSPSIZE	Luminance Bottom Field Result Sub-Picture Size Register	Section 3.33
94h	BY_RESOFFSET	Luminance Bottom Field Line Result Address Offset Register	Section 3.34
98h	TC_RESADDR	Chrominance Top Field Result Start Address Register	Section 3.35
9Ch	TC_RESSPSIZE	Chrominance Top Field Result Sub-Picture Size Register	Section 3.36
A0h	TC_RESOFFSET	Chrominance Top Field Line Result Address Offset Register	Section 3.37
A4h	BC_RESADDR	Chrominance Bottom Field Result Start Address Register	Section 3.38
A8h	BC_RESSPSIZE	Chrominance Bottom Field Result Sub-Picture Size Register	Section 3.39
ACh	BC_RESOFFSET	Chrominance Bottom Field Line Result Address Offset Register	Section 3.40
C0h	IMG_Y_SRCSTRTPOS	Luminance Source Image Start Position Register	Section 3.41
C4h	IMG_Y_SRCSIZE	Luminance Source Image Size Register	Section 3.42
C8h	IMG_C_SRCSTRTPOS	Chrominance Source Image Start Position Register	Section 3.43
CCh	IMG_C_SRCSIZE	Chrominance Source Image Size Register	Section 3.44

Table 2. Video Data Conversion Engine (VDCE) Registers (continued)

Offset	Acronym	Register Description	Section
D0h	IMG_BMP_SRCSTRTPOS	Bitmap Source Image Start Position Register	Section 3.45
D4h	IMG_BMP_SRCSIZE	Bitmap Source Image Size Register	Section 3.46
E0h	IMG_Y_RESSTRTPOS	Luminance Result Image Start Position Register	Section 3.47
E4h	IMG_Y_RESSIZE	Luminance Result Image Size Register	Section 3.48
E8h	IMG_C_RESSTRTPOS	Chrominance Result Image Start Position Register	Section 3.49
ECh	IMG_C_RESSIZE	Chrominance Result Image Size Register	Section 3.50
F0h	IMG_BMP_RESSTRTPOS	Bitmap Result Image Start Position Register	Section 3.51
100h	RSZ_MODE	Resize Mode Definition Register	Section 3.52
104h	RSZ_HMAG	Horizontal Resize Magnification Ratio Control Register	Section 3.53
108h	RSZ_VMAG	Vertical Resize Magnification Ratio Control Register	Section 3.54
10Ch	RSZ_HPHASE	Phase of Initial Pixel on Horizontal Resize Register	Section 3.55
110h	RSZ_VPHASE	Phase of Initial Pixel on Vertical Resize Register	Section 3.56
114h	RSZ_AFILTER	Horizontal Anti-Aliasing Filter Control Register	Section 3.57
120h	CCV_MODE	Chrominance Conversion Mode Control Register	Section 3.58
140h	BLD_LUT_00	Look-Up Table for Index 00 Register	Section 3.59
144h	BLD_LUT_01	Look-Up Table for Index 01 Register	Section 3.60
148h	BLD_LUT_02	Look-Up Table for Index 02 Register	Section 3.61
14Ch	BLD_LUT_03	Look-Up Table for Index 03 Register	Section 3.62
160h	RGMP_CTRL	Range Mapping Control Register	Section 3.63
184h	EPD_LUMA_WIDTH	Edge Padding Width for Luminance Register	Section 3.64
188h	EPD_CHROMA_WIDTH	Edge Padding Width for Chrominance Register	Section 3.65

3.1 Restrictions for VDCE Registers

Restrictions for configuration of each VDCE register is described in Table 3. Correct performance of the VDCE cannot be assured, if these restrictions are not met.

Table 3. Restrictions for VDCE Registers

Offset	Acronym	Description
2804h	CTRL	VDCE_GO bit should be activated after any other configurations for each register is finished. Either the VDCE_TOP_FIELD_EN bit or VDCE_BTM_FIELD_EN bit and either the VDCE_CROMA_EN bit or VDCE_LUMA_EN bit should be 1, if you enable the VDCE module.
2820h	SRD_FRMT	Both the VDCE_RES_SDR_FMT_TST bit and VDCE_SRC_SDR_FMT_TST bit should be 0 (only raster scanning format is supported).
2824h	REQ_SIZE	This register value must be non-zero.
2844h	TY_SRCSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
2850h	BY_SRCSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
285Ch	TC_SRCSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
2868h	BC_SRCSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
2884h	TY_RESSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
2890h	BY_RESSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
289Ch	TC_RESSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
28A8h	BC_RESSPSIZE	Sub-picture mode is removed. This register value has no effect on functional performance of the module.
290Ch	RSZ_HPHASE	The initial phase value should be 0 (no support for non-zero value).
2910h	RSZ_VPHASE	The initial phase value should be 0 (no support for non-zero value).

3.2 VDCE Peripheral Identification Register (PID)

The VDCE peripheral identification register (PID) is shown in Figure 30 and described in Table 4.

Figure 30. VDCE Peripheral Identification Register (PID)

31	30	29	28	27	16
SCHEME		Reserved		FUNC	
R-1		R-0		R-C09h	

15	11	10	8	7	6	5	0
RTL		MAJOR		CUSTOM		MINOR	
R-0		R-0		R-0		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 4. VDCE Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	0-3h	Used to distinguish between old scheme and current. Fixed to 01b.
29-28	Reserved	0	Reserved
27-16	FUNC	0-FFFh	Function indicates a software-compatible module family. If there is not level of software-compatibility, a new FUNC number (and hence PID) should be assigned
15-11	RTL	0-1Fh	Indicates RTL version, and must be easily ECO-able or controlled during fabrication. Ideally through a top level metal mask or e-fuse. This number is maintained/owned by IP design owner. Fixed to 0.
10-8	MAJOR	0-7h	Major revision number. This number should be updated for each major design change (such as bug fix, and memory size change etc…). Fixed to 0.
7-6	CUSTOM	0-3h	Indicates a special version for a particular device. Consequence of use may avoid use of standard chip support library (CSL). Fixed to 0.
5-0	MINOR	0-3Fh	Minor revision number. This number should be updated for each small design change. Fixed to 0.

3.3 VDCE Control Register (CTRL)

The VDCE control register (CTRL) is shown in Figure 31 and described in Table 5.

Figure 31. VDCE Control Register (CTRL)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
VDCE_BMP_SRC_NFLD_FRM	VDCE_IMG_SRC_NFLD_FRM	VDCE_RES_NFLD_FRM	VDCE_SRC_NIP	VDCE_BLD_EN	VDCE_CCV_EN	VDCE_RGMP_EN	VDCE_RSZ_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
VDCE_TOP_FIELD_EN	VDCE_BTM_FIELD_EN	VDCE_MODE		Reserved	VDCE_CROMA_EN	VDCE_LUMA_EN	VDCE_GO
R/W-0	R/W-0	R/W-0		R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 5. VDCE Control Register (CTRL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	VDCE_BMP_SRC_NFLD_FRM		Defines storage format of source artificial bitmap image data in SDRAM. Field mode means that each of top and bottom field data is prepared in SDRAM independently to each other without being interleaved. Frame mode means that source data in both top and bottom field data is stored in SDRAM with being interleaved. Vertical image size is automatically calculated inside the VDCE. Note that bitmap source data should be “progressive” format.
		0	Field storage format
		1	Frame storage format
14	VDCE_IMG_SRC_NFLD_FRM		Defines storage format of image source (video) data in SDRAM. Field mode means that each of top and bottom field data is prepared in SDRAM independently to each other without interleave. Frame mode means that image data in both top and bottom field data is stored in SDRAM. Vertical image size is automatically calculated inside the module.
		0	Field storage format
		1	Frame storage format
13	VDCE_RES_NFLD_FRM		Defines storage format of result data in SDRAM. Field mode means that each of top and bottom field data is prepared in SDRAM independently to each other without being interleaved. Frame mode means that image data in both top and bottom field data is stored in SDRAM. Vertical image size is automatically calculated inside the module.
		0	Field storage format
		1	Frame storage format
12	VDCE_SRC_NIP		Defines processing method of each picture data in interlace format or progressive format. If source data is in interlaced format, image processing on vertical direction should be performed for each field (without interleave of top and bottom field data). If source data is in progressive format, image processing on vertical direction should be performed on frame format (with interleave of top and bottom field data). Being related to configuration of this bit, the vertical size assignment should be defined as:
		0	Interlaced format (vertical image size should be configured as field size (not frame size)).
		1	Progressive format (vertical image size should be configured as frame size (LSB should be 0)).

Table 5. VDCE Control Register (CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
11	VDCE_BLD_EN		Controls whether the 2-bit hardware menu overlay function (BLD) is activated in the mode defined by the VDCE_MODE bit. If the VDCE_MODE bit is not 1h or 3h , this bit is ignored. This bit should be activated only in the case when the VDCE_RSZ_EN bit is 0. This is a restriction and is described in Section 2.3 and Section 2.4.
		0	2-bit hardware menu overlay function is not activated.
		1	2-bit hardware menu overlay function is activated.
10	VDCE_CCV_EN		Controls whether chrominance format conversion (CCV) for horizontal direction is activated in the mode defined by the VDCE_MODE bit. If the VDCE_MODE bit is 0, this bit is ignored. This bit is the control bit for the horizontal chrominance conversion. The vertical chrominance conversion is automatically controlled by the VDCE_MODE bit.
		0	CCV is not activated.
		1	CCV is activated.
9	VDCE_RGMP_EN		Controls whether range mapping function (RGMP for VC-1 advanced profile) is activated in the mode defined by the VDCE_MODE bit. If the VDCE_MODE bit is not 1h or 3h, this bit is ignored.
		0	RGMP is not activated.
		1	RGMP is activated.
8	VDCE_RSZ_EN		Controls whether resize function (RSZ for horizontal and vertical direction) is activated in the mode defined by the VDCE_MODE bit. If the VDCE_MODE bit is 0, this bit is ignored. This bit should be activated only in the case when the VDCE_BLD_EN bit is 0. This is a restriction and is described in Section 2.3 and Section 2.4.
		0	RSZ is not activated.
		1	RSZ is activated.
7	VDCE_TOP_FIELD_EN		Enables image processing for top field on VDCE. In the case of processing the interlace top field image, you should set this bit to 1. This bit is effective only when processing an interlace image (VDCE_SRC_NIP = 0); otherwise, this bit is ignored. Either the VDCE_TOP_FIELD_EN bit or the VDCE_BTM_FIELD_EN bit must be configured to 1, if VDCE is activated.
		0	Top field processing is disabled.
		1	Top field processing is enabled.
6	VDCE_BTM_FIELD_EN		Enables image processing for bottom field on VDCE . In case of processing the interlace bottom field image, you should set this bit to 1. This bit is effective only when processing an interlace image (VDCE_SRC_NIP = 0); otherwise, this bit is ignored. Either the VDCE_TOP_FIELD_EN bit or the VDCE_BTM_FIELD_EN bit must be configured to 1, if VDCE is activated.
		0	Bottom field processing is disabled.
		1	Bottom field processing is enabled.
5-4	VDCE_MODE	0-3h	Defines performance mode (data flow mode) in the VDCE module.
		0	Edge Padding
		1h	Trans-code mode
		2h	Pre-Codec mode
		3h	Post-Codec mode
3	Reserved	0	Reserved
2	VDCE_CROMA_EN		Indicates that the VDCE processes chrominance data of the targeted frame. With rising edge of VDCE_GO, this bit is detected. If this bit is inactivated with VDCE_GO rising edge, no image processing for chrominance data in the targeted frame will be carried out. Either the VDCE_CROMA_EN bit or the VDCE_LUMA_EN bit must be configured to 1, if VDCE is activated.
		0	Chrominance processing is disabled.
		1	Chrominance processing is enabled.

Table 5. VDCE Control Register (CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
1	VDCE_LUMA_EN		Indicates that the VDCE processes luminance data of the targeted frame. With rising edge of VDCE_GO, this bit is detected. If this bit is inactivated with VDCE_GO rising edge, no image processing for luminance data in the targeted frame will be carried out. Either the VDCE_CROMA_EN bit or the VDCE_LUMA_EN bit must be configured to 1, if VDCE is activated.
		0	Luminance processing is disabled.
		1	Luminance processing is enabled.
0	VDCE_GO		Activating this bit makes the VDCE start 1-frame processing based on register configuration. When this bit is 1, the VDCE is working (means the VDCE is busy). So, the CPU cannot change the bit value during a busy phase. Only when this bit is 0, the CPU can change it to 1 in order to start the VDCE.
		0	VDCE is in idle.
		1	VDCE is busy.

3.4 Interrupt Enable Register (INTEN)

The interrupt enable register (INTEN) is shown in Figure 32 and described in Table 6.

Figure 32. Interrupt Enable Register (INTEN)

31	16
Reserved	
R-0	

15	1	0
Reserved		VDCE_INTEN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. Interrupt Enable Register (INTEN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	VDCE_INTEN		Controls the interrupt from the VDCE to the ARM processor. To activate asserting the interrupt to the ARM, configure this bit to 1 and then configure the VDCE_INTEN_SET bit in the interrupt set register (INTEN_SET) to 1.
		0	Interrupt is disabled.
		1	Interrupt is enabled.

3.5 Interrupt Set Register (INTEN_SET)

The interrupt set register (INTEN_SET) is shown in Figure 33 and described in Table 7.

Figure 33. Interrupt Set Register (INTEN_SET)

31	16
Reserved	
R-0	

15	1	0
Reserved		VDCE_INTEN_SET
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. Interrupt Set Register (INTEN_SET) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	VDCE_INTEN_SET		To activate the interrupt function to the ARM, configure this bit to 1 and set the VDCE_INTEN bit in the interrupt enable register (INTEN) to 1. While activated, this bit remains set to 1. This bit is effective only when the VDCE_INTEN bit is activated; otherwise, this bit is ignored and this bit value stays at 0. You can only write 1 and cannot write 0 to this bit. If you write 1 to the VDCE_INTEN_CLR bit in the interrupt clear register (INTEN_CLR) during this bit being activated, this bit is internally cleared to 0. If activated, an interrupt pulse is asserted when configured processing is finished (1 interrupt per 1 frame).
		0	Interrupt is inactivated.
		1	Interrupt is activated.

3.6 Interrupt Clear Register (INTEN_CLR)

The interrupt clear register (INTEN_CLR) is shown in Figure 34 and described in Table 8.

Figure 34. Interrupt Clear Register (INTEN_CLR)

31	16
Reserved	
R-0	

15	1	0
Reserved		VDCE_INTEN_CLR
R-0		W-0

LEGEND: R = Read only; W = Write only; -*n* = value after reset

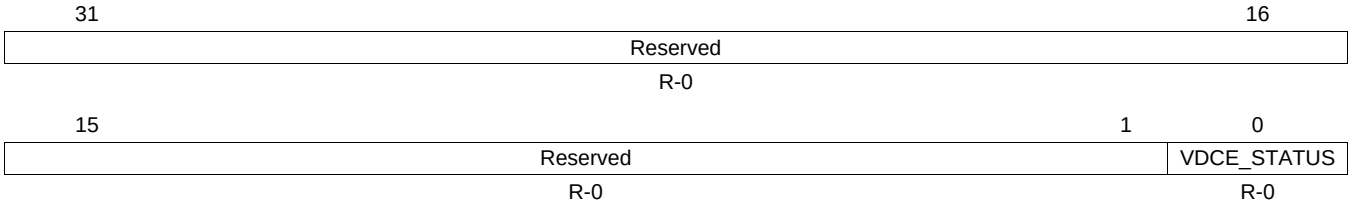
Table 8. Interrupt Clear Register (INTEN_CLR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	VDCE_INTEN_CLR		To inactivate the interrupt function to the ARM, configure this bit to 1 while the VDCE_INTEN bit in the interrupt enable register (INTEN) and the VDCE_INTEN_SET bit in the interrupt set register (INTEN_SET) are set to 1. This bit is effective only when the VDCE_INTEN bit and the VDCE_INTEN_SET bit are activated; otherwise, this bit is ignored. This bit is a write-only bit and you can only write 1 to this bit (you cannot write 0).
		0	No change.
		1	Interrupt is inactivated.

3.7 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 35 and described in Table 9.

Figure 35. Interrupt Status Register (INTSTAT)



LEGEND: R = Read only; -*n* = value after reset

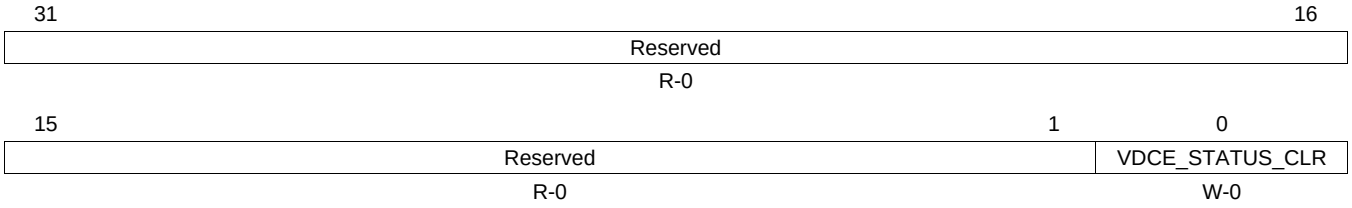
Table 9. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	VDCE_STATUS		Interrupt status. Note that this bit is a read-only bit. To clear this bit, set the VDCE_STATUS_CLR bit in the interrupt status clear register (INTSTAT_CLR) to 1. This status value is internally cleared if the VDCE_STATUS_CLR bit is configured to 1.
		0	Configured one frame processing is under way.
		1	Configured one frame processing is finished, and not checked yet.

3.8 Interrupt Status Clear Register (INTSTAT_CLR)

The interrupt status clear register (INTSTAT_CLR) is shown in Figure 36 and described in Table 10.

Figure 36. Interrupt Status Clear Register (INTSTAT_CLR)



LEGEND: R = Read only; W = Write only; -*n* = value after reset

Table 10. Interrupt Status Clear Register (INTSTAT_CLR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	VDCE_STATUS_CLR		Interrupt status clear register bit. To clear the interrupt status register (INTSTAT), set this bit to 1. This bit is a write-only bit and a written value cannot be read by the ARM.
		0	No change.
		1	Clears the interrupt status register (INTSTAT)

3.9 Emulation Control Register (EMU_CTRL)

The emulation control register (EMU_CTRL) is shown in Figure 37 and described in Table 11.

Figure 37. Emulation Control Register (EMU_CTRL)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		VDCE_EMULSUSP_SOFT	VDCE_EMULSUSP_FREE
R-0		R-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 11. Emulation Control Register (EMU_CTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	VDCE_EMULSUSP_SOFT		Controls whether a soft or hard stop is initiated whenever emulation suspend is asserted. Note that this bit is fixed to 1, due to specification for handling emulation suspend signal.
		0	Hard stop (the VDCE immediately stops processing, after current data transaction is finished; stops at middle of the frame).
		1	soft stop (the VDCE stops processing after current frame process is finished; same as normal process).
0	VDCE_EMULSUSP_FREE		Controls whether the peripheral responds to the emulation suspend signal that it has been programmed to monitor.
		0	functions based on configuration of the VDCE_EMULSUSP_SOFT bit
		1	ignores any emulation suspend signal (non-stop).

3.10 Source/Result Data Store Format Register (SRD_FRMT_TST)

The source/result data store format register (SRD_FRMT_TST) is shown in Figure 38 and described in Table 12.

Figure 38. Source/Result Data Store Format Register (SRD_FRMT_TST)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		VDCE_RES_SDR_FMT_TST	VDCE_SRC_SDR_FMT_TST
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. Source/Result Data Store Format Register (SRD_FRMT_TST)

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	VDCE_RES_SDR_FMT_TST		Test bit for definition of SDRAM data storage format for result of the VDCE. In normal use-case, this bit should be configured to 0 (raster scanning format).
		0	Raster scanning format.
		1	Sub-picture format.
0	VDCE_SRC_SDR_FMT_TST		Test bit for definition of SDRAM data storage format for source of the VDCE. In normal use-case, this bit should be configured to 0 (raster scanning format).
		0	Raster scanning format.
		1	Sub-picture format.

3.11 Request Unit Size Register (REQ_SIZE)

The request unit size register (REQ_SIZE) is shown in Figure 39 and described in Table 13.

Figure 39. Request Unit Size Register (REQ_SIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_REQ_SIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Request Unit Size Register (REQ_SIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_REQ_SIZE	0-1FFh	Defines request unit size for DMA data transfer from/to SDRAM. The VDCE has 64 bit × 64 word ping-pong buffer for each read and write buffer interface, and the VDCE asserts DMA data request to SDRAM in the following case: Mass of stored bytes in the ping-pong buffer reaches configured value. Mass of transmitted bytes from the ping-pong buffer reaches configured value. These data size are either luminance or chrominance. Note that the maximum request unit size is clipped to the internal request size, if the internal request size is less than the configured data size in this bit.
		0-1Fh	Reserved
		20h	32 byte unit size
		21h-3Fh	Reserved
		40h	64 byte unit size
		41h-7Fh	Reserved
		80h	128 byte unit size
		81h-FFh	Reserved
		100h	256 byte unit size
		101h-1FFh	Reserved

3.12 Processing Unit Size Register (PROC_SIZE)

The processing unit size register (PROC_SIZE) is shown in Figure 40 and described in Table 14.

Figure 40. Processing Unit Size Register (PROC_SIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_PRCS_UNIT_SIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Processing Unit Size Register (PROC_SIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_PRCS_UNIT_SIZE	0-1FFh	Defines unit size to be generated in horizontal direction. Because the internal work buffer has a 256-byte width for horizontal direction, the result size is limited by this value especially for resize. This means that you have to configure this bit with a reading size less than 256 bytes. Note that you have to configure this bit to be non-zero before activating the VDCE; otherwise, the VDCE does not start working. Following relationship should be kept: {(Register value) × (N/256) + 9} <= 256. (N is parameter for horizontal resize magnification ratio) For example, if you activate horizontal resize with magnification ratio of 200, this value should be 64 byte from calculation result with buffer size.
		0-Fh	Reserved
		10h	16 byte unit size
		11h-1Fh	Reserved
		20h	32 byte unit size
		21h-3Fh	Reserved
		40h	64 byte unit size
		41h-7Fh	Reserved
		80h	128 byte unit size
		81h-FFh	Reserved
		100h	256 byte unit size
		101h-1FFh	Reserved

3.13 Luminance Top Field Source Start Address Register (TY_SRCADDR)

The luminance top field source start address register (TY_SRCADDR) contains the start address of the source picture area that is prepared for luminance data in the top field on SDRAM. The TY_SRCADDR is shown in Figure 41 and described in Table 15.

Figure 41. Luminance Top Field Source Start Address Register (TY_SRCADDR)

31	0
VDCE_SRC_STRT_ADD_YTOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 15. Luminance Top Field Source Start Address Register (TY_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_YTOP	0-FFFF FFFFh	Start address of source picture area for luminance data in top field on SDRAM.

3.14 Luminance Top Field Source Sub-Picture Size Register (TY_SRCSPSIZE)

The luminance top field source sub-picture size register (TY_SRCSPSIZE) configures the horizontal sub-picture size for top-field luminance data that is stored in SDRAM as source data. The TY_SRCSPSIZE is shown in Figure 42 and described in Table 16.

Figure 42. Luminance Top Field Source Sub-Picture Size Register (TY_SRCSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_SRC_SP_HSZ_YTOP_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. Luminance Top Field Source Sub-Picture Size Register (TY_SRCSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_SRC_SP_HSZ_YTOP_TST	0-1FFh	Defines horizontal sub-picture size for top field luminance data that is stored in SDRAM as source data of the VDCE. This bit is for sub-picture mode test. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.15 Luminance Top Field Line Source Address Offset Register (TY_SRCOFFSET)

The luminance top field line source address offset register (TY_SRCOFFSET) configures the address offset value of each line for top-field luminance data on raster store format. The TY_SRCOFFSET is shown in Figure 43 and described in Table 17.

Figure 43. Luminance Top Field Line Source Address Offset Register (TY_SRCOFFSET)

31	0
VDCE_SRC_ADD_OFST_YTOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 17. Luminance Top Field Line Source Address Offset Register (TY_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_YTOP	0-FFFF FFFFh	Configures the address offset value of each line for top field luminance data on raster store format. The stored luminance data is prepared for source image data to be processed by the VDCE. This value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x] This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored.

3.16 Luminance Bottom Field Source Start Address Register (BY_SRCADDR)

The luminance bottom field source start address register (BY_SRCADDR) contains the start address of source picture area that is prepared for luminance data in bottom field on SDRAM. The BY_SRCADDR is shown in Figure 44 and described in Table 18.

Figure 44. Luminance Bottom Field Source Start Address Register (BY_SRCADDR)

31	0
VDCE_SRC_STRT_ADD_YBTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 18. Luminance Bottom Field Source Start Address Register (BY_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_YBTM	0-FFFF FFFFh	Start address of source picture area for luminance data in bottom field on SDRAM.

3.17 Luminance Bottom Field Sub-Picture Size Register (BY_SRCSPSIZE)

The luminance bottom field sub-picture size register (BY_SRCSPSIZE) configures the horizontal sub-picture size for bottom-field luminance data that is stored in SDRAM as source data. The BY_SRCSPSIZE is shown in Figure 45 and described in Table 19.

Figure 45. Luminance Bottom Field Sub-Picture Size Register (BY_SRCSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_SRC_SP_HSZ_YBTM_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

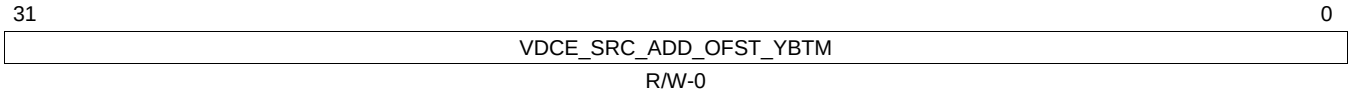
Table 19. Luminance Bottom Field Sub-Picture Size Register (BY_SRCSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_SRC_SP_HSZ_YBTM_TST	0-1FFh	Defines horizontal sub-picture size for bottom-field luminance data that is stored in SDRAM as source data of the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.18 Luminance Bottom Field Line Offset Register (BY_SRCOFFSET)

The luminance bottom field line source address offset register (BY_SRCOFFSET) configures the address offset value of each line for bottom field luminance data on raster store format. The BY_SRCOFFSET is shown in Figure 46 and described in Table 20.

Figure 46. Luminance Bottom Field Line Source Address Offset Register (BY_SRCOFFSET)



LEGEND: R/W = Read/Write; -*n* = value after reset

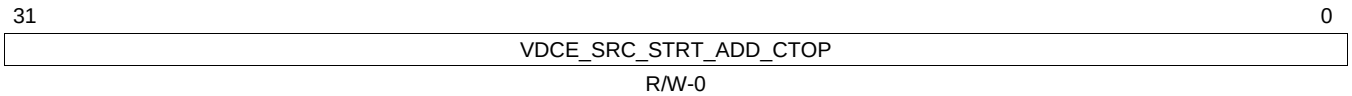
Table 20. Luminance Bottom Field Line Source Address Offset Register (BY_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_YBTM	0-FFFF FFFFh	Configures the address offset value of each line for bottom field luminance data on raster store format. The stored luminance data is for source image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x] This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored.

3.19 Chrominance Top Field Source Start Address Register (TC_SRCADDR)

The chrominance top field source start address register (TC_SRCADDR) contains the start address of source picture area that is prepared for chrominance data in top field on SDRAM. The TC_SRCADDR is shown in Figure 47 and described in Table 21.

Figure 47. Chrominance Top Field Source Start Address Register (TC_SRCADDR)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 21. Chrominance Top Field Source Start Address Register (TC_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_CTOP	0-FFFF FFFFh	Start address of source picture area for chrominance data in top field on SDRAM. Configure this bit to be an even value.

3.20 Chrominance Top Field Source Sub-Picture Size Register (TC_SRCSPSIZE)

The chrominance top field source sub-picture size register (TC_SRCSPSIZE) configures the horizontal sub-picture size for top-field chrominance data that is stored in SDRAM as source data. The TC_SRCSPSIZE is shown in Figure 48 and described in Table 22.

Figure 48. Chrominance Top Field Source Sub-Picture Size Register (TC_SRCSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_SRC_SP_HSZ_CTOP_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. Chrominance Top Field Source Sub-Picture Size Register (TC_SRCSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_SRC_SP_HSZ_CTOP_TST	0-1FFh	Defines horizontal sub-picture size for top-field chrominance data that is stored in SDRAM as source data of the VDCE. This bit is for test of sub-picture mode. In normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.21 Chrominance Top Field Line Source Address Offset Register (TC_SRCOFFSET)

The chrominance top field line source address offset register (TC_SRCOFFSET) configures the address offset value of each line for top field chrominance data on raster store format. The TC_SRCOFFSET is shown in Figure 49 and described in Table 23.

Figure 49. Chrominance Top Field Line Source Address Offset Register (TC_SRCOFFSET)

31	0
VDCE_SRC_ADD_OFST_CTOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 23. Chrominance Top Field Line Source Address Offset Register (TC_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_CTOP	0-FFFF FFFFh	Configures the address offset value of each line for top field chrominance data on raster store format. The stored chrominance data is for source image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x] This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored. Also, configure this bit to be an even value.

3.22 Chrominance Bottom Field Source Start Address Register (BC_SRCADDR)

The chrominance bottom field source start address register (BC_SRCADDR) contains the start address of the source picture area that is prepared for chrominance data in bottom field on SDRAM. The BC_SRCADDR is shown in Figure 50 and described in Table 24.

Figure 50. Chrominance Bottom Field Source Start Address Register (BC_SRCADDR)

31	0
VDCE_SRC_STRT_ADD_CBTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 24. Chrominance Bottom Field Source Start Address Register (BC_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_CBTM	0-FFFF FFFFh	Start address of source picture area for chrominance data in bottom field on SDRAM. Configure this bit to be an even value.

3.23 Chrominance Bottom Field Source Sub-Picture Size Register (BC_SRCSPSIZE)

The chrominance bottom field source sub-picture size register (BC_SRCSPSIZE) configures the horizontal sub-picture size for bottom-field chrominance data that is stored in SDRAM as source data. The BC_SRCSPSIZE is shown in Figure 51 and described in Table 25.

Figure 51. Chrominance Bottom Field Source Sub-Picture Size Register (BC_SRCSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_SRC_SP_HSZ_CBTM_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 25. Chrominance Bottom Field Source Sub-Picture Size Register (BC_SRCSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_SRC_SP_HSZ_CBTM_TST	0-1FFh	Defines horizontal sub-picture size for bottom field chrominance data that is stored in SDRAM as source data of the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.24 Chrominance Bottom Field Line Source Address Offset Register (BC_SRCOFFSET)

The chrominance bottom field line source address offset register (BC_SRCOFFSET) configures the address offset value of each line for bottom field chrominance data on raster store format. The BC_SRCOFFSET is shown in Figure 52 and described in Table 26.

Figure 52. Chrominance Bottom Field Line Source Address Offset Register (BC_SRCOFFSET)

31	0
VDCE_SRC_ADD_OFST_CBTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 26. Chrominance Bottom Field Line Source Address Offset Register (BC_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_CBTM	0-FFFF FFFFh	Configures the address offset value of each line for bottom field chrominance data on raster store format. The stored chrominance data is for source image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x] This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored. Also, configure this bit to be an even value.

3.25 Bitmap Top Field Source Start Address Register (TBMP_SRCADDR)

The bitmap top field source start address register (TBMP_SRCADDR) configures the start address of the source picture area that is prepared for bitmap data in top field on SDRAM. The TBMP_SRCADDR is shown in Figure 53 and described in Table 27.

Figure 53. Bitmap Top Field Source Start Address Register (TBMP_SRCADDR)

31	0
VDCE_SRC_STRT_ADD_BMP_TOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 27. Bitmap Top Field Source Start Address Register (TBMP_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_BMP_TOP	0-FFFF FFFFh	Start address of source picture area for bitmap data in top field on SDRAM.

3.26 Bitmap Top Field Line Source Address Offset Register (TBMP_SRCOFFSET)

The bitmap top field line source address offset register (TBMP_SRCOFFSET) configures the address offset value of each line for top field bitmap data on raster store format. The TBMP_SRCOFFSET is shown in Figure 54 and described in Table 28.

Figure 54. Bitmap Top Field Line Source Address Offset Register (TBMP_SRCOFFSET)

31	0
VDCE_SRC_ADD_OFST_BMP_TOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 28. Bitmap Top Field Line Source Address Offset Register (TBMP_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_BMP_TOP	0-FFFF FFFFh	Configures the address offset value of each line for top field bitmap data on raster store format. The stored bitmap data is for source image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x]. Note that the VDCE does not support sub-picture format for bitmap data; only raster scanning format is supported for bitmap data.

3.27 Bitmap Bottom Field Source Start Address Register (BBMP_SRCADDR)

The bitmap bottom field source start address register (BBMP_SRCADDR) configures the start address of the source picture area that is prepared for bitmap data in the bottom field on SDRAM. The BBMP_SRCADDR is shown in Figure 55 and described in Table 29.

Figure 55. Bitmap Bottom Field Source Start Address Register (BBMP_SRCADDR)

31	0
VDCE_SRC_STRT_ADD_BMP_BTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 29. Bitmap Bottom Field Source Start Address Register (BBMP_SRCADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_STRT_ADD_BMP_BTM	0-FFFF FFFFh	Start address of source picture area for bitmap data in bottom field on SDRAM.

3.28 Bitmap Bottom Field Line Source Address Offset Register (BBMP_SRCOFFSET)

The bitmap bottom field line source address offset register (BBMP_SRCOFFSET) configures the address offset value of each line for bottom field bitmap data on raster store format. The BBMP_SRCOFFSET is shown in Figure 56 and described in Table 30.

Figure 56. Bitmap Bottom Field Line Source Address Offset Register (BBMP_SRCOFFSET)

31	0
VDCE_SRC_ADD_OFST_BMP_BTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 30. Bitmap Bottom Field Line Source Address Offset Register (BBMP_SRCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_SRC_ADD_OFST_BMP_BTM	0-FFFF FFFFh	Configures the address offset value of each line for bottom field bitmap data on raster store format. The stored bitmap data is for source image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = SRC_STRT_ADD + SRC_ADD_OFST × line [x] Note that the VDCE does not support sub-picture format for bitmap data; only raster scanning format is supported for bitmap data.

3.29 Luminance Top Field Result Start Address Register (TY_RESADDR)

The luminance top field result start address register (TY_RESADDR) configures the start address of the result picture area that is prepared for luminance data in top field on SDRAM. The TY_RESADDR is shown in Figure 57 and described in Table 31.

Figure 57. Luminance Top Field Result Start Address Register (TY_RESADDR)

31	0
VDCE_RES_STRT_ADD_YTOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 31. Luminance Top Field Result Start Address Register (TY_RESADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_STRT_ADD_YTOP	0-FFFF FFFFh	Start address of result picture area for luminance data in top field on SDRAM.

3.30 Luminance Top Field Result Sub-Picture Size Register (TY_RESSPSIZE)

The luminance top field result sub-picture size register (TY_RESSPSIZE) configures the horizontal sub-picture size for top-field luminance data that is stored in SDRAM as result data. The TY_RESSPSIZE is shown in Figure 58 and described in Table 32.

Figure 58. Luminance Top Field Result Sub-Picture Size Register (TY_RESSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_RES_SP_HSZ_YTOP_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

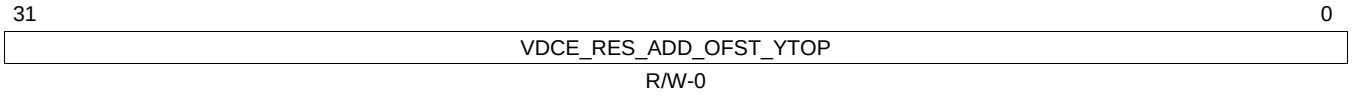
Table 32. Luminance Top Field Result Sub-Picture Size Register (TY_RESSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_RES_SP_HSZ_YTOP_TST	0-1FFh	Defines horizontal sub-picture size for top field luminance data that is stored in SDRAM as result data from the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.31 Luminance Top Field Line Result Address Offset Register (TY_RESOFFSET)

The luminance top field line result address offset register (TY_RESOFFSET) configures the address offset value of each line for top field luminance data on raster store format. The TY_RESOFFSET is shown in Figure 59 and described in Table 33.

Figure 59. Luminance Top Field Line Result Address Offset Register (TY_RESOFFSET)



LEGEND: R/W = Read/Write; -*n* = value after reset

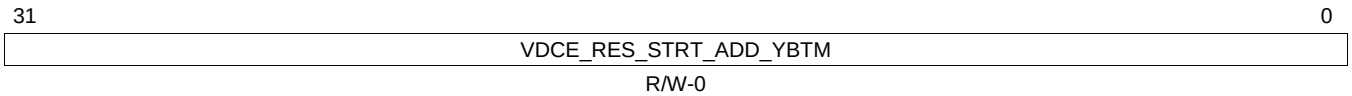
Table 33. Luminance Top Field Line Result Address Offset Register (TY_RESOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_ADD_OFST_YTOP	0-FFFF FFFFh	Configures the address offset value of each line for top field luminance data on raster store format. The stored luminance data is for result image data processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = RES_STRT_ADD + RES_ADD_OFST × line [x]. This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored.

3.32 Luminance Bottom Field Result Start Address Register (BY_RESADDR)

The luminance bottom field result start address register (BY_RESADDR) configures the start address of the result picture area that is prepared for luminance data in bottom field on SDRAM. The BY_RESADDR is shown in Figure 60 and described in Table 34.

Figure 60. Luminance Bottom Field Result Start Address Register (BY_RESADDR)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 34. Luminance Bottom Field Result Start Address Register (BY_RESADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_STRT_ADD_YBTM	0-FFFF FFFFh	Start address of result picture area for luminance data in bottom field on SDRAM.

3.33 Luminance Bottom Field Result Sub-Picture Size Register (BY_RESSPSIZE)

The luminance bottom field result sub-picture size register (BY_RESSPSIZE) configures the horizontal sub-picture size for bottom-field luminance data that is stored in SDRAM as result data. The BY_RESSPSIZE is shown in Figure 61 and described in Table 35.

Figure 61. Luminance Bottom Field Result Sub-Picture Size Register (BY_RESSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_RES_SP_HSZ_YBTM_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

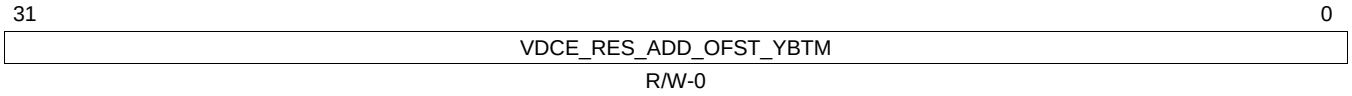
Table 35. Luminance Bottom Field Result Sub-Picture Size Register (BY_RESSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_RES_SP_HSZ_YBTM_TST	0-1FFh	Defines horizontal sub-picture size for bottom field luminance data that is stored in SDRAM as result data from the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.34 Luminance Bottom Field Line Result Address Offset Register (BY_RESOFFSET)

The luminance bottom field line result address offset register (BY_RESOFFSET) configures the address offset value of each line for bottom field luminance data on raster store format. The BY_RESOFFSET is shown in Figure 62 and described in Table 36.

Figure 62. Luminance Bottom Field Line Result Address Offset Register (BY_RESOFFSET)



LEGEND: R/W = Read/Write; -*n* = value after reset

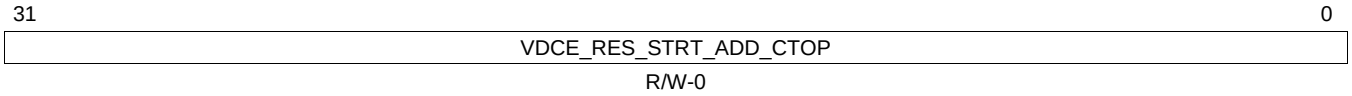
Table 36. Luminance Bottom Field Line Result Address Offset Register (BY_RESOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_ADD_OFST_YBTM	0-FFFF FFFFh	Configures the address offset value of each line for bottom field luminance data on raster store format. The stored luminance data is for result image data to be processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = RES_STRT_ADD + RES_ADD_OFST × line [x]. This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored.

3.35 Chrominance Top Field Result Start Address Register (TC_RESADDR)

The chrominance top field result start address register (TC_RESADDR) configures the start address of the result picture area that is prepared for chrominance data in top field on SDRAM. The TC_RESADDR is shown in Figure 63 and described in Table 37.

Figure 63. Chrominance Top Field Result Start Address Register (TC_RESADDR)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 37. Chrominance Top Field Result Start Address Register (TC_RESADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_STRT_ADD_CTOP	0-FFFF FFFFh	Start address of result picture area for chrominance data in top field on SDRAM. Configure this bit to be an even value.

3.36 Chrominance Top Field Result Sub-Picture Size Register (TC_RESSPSIZE)

The chrominance top field result sub-picture size register (TC_RESSPSIZE) configures the horizontal sub-picture size for top-field chrominance data that is stored in SDRAM as result data. The TC_RESSPSIZE) is shown in Figure 64 and described in Table 38.

Figure 64. Chrominance Top Field Result Sub-Picture Size Register (TC_RESSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_RES_SP_HSZ_CTOP_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 38. Chrominance Top Field Result Sub-Picture Size Register (TC_RESSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_RES_SP_HSZ_CTOP_TST	0-1FFh	Defines horizontal sub-picture size for top field chrominance data that is stored in SDRAM as result data from the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.37 Chrominance Top Field Line Result Address Offset Register (TC_RESOFFSET)

The chrominance top field line result address offset register (TC_RESOFFSET) configures the address offset value of each line for top field chrominance data on raster store format. The TC_RESOFFSET is shown in Figure 65 and described in Table 39.

Figure 65. Chrominance Top Field Line Result Address Offset Register (TC_RESOFFSET)

31	0
VDCE_RES_ADD_OFST_CTOP	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 39. Chrominance Top Field Line Result Address Offset Register (TC_RESOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_ADD_OFST_CTOP	0-FFFF FFFFh	Configures the address offset value of each line for top field chrominance data on raster store format. The stored chrominance data is for result image data processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = RES_STRT_ADD + RES_ADD_OFST × line [x]. This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored. Also, configure this bit to be an even value.

3.38 Chrominance Bottom Field Result Start Address Register (BC_RESADDR)

The chrominance bottom field result start address register (BC_RESADDR) configures the start address of the result picture area that is prepared for chrominance data in the bottom field on SDRAM. The BC_RESADDR is shown in Figure 66 and described in Table 40.

Figure 66. Chrominance Bottom Field Result Start Address Register (BC_RESADDR)

31	0
VDCE_RES_STRT_ADD_CBTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 40. Chrominance Bottom Field Result Start Address Register (BC_RESADDR) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_STRT_ADD_CBTM	0-FFFF FFFFh	Start address of result picture area for chrominance data in bottom field on SDRAM. Configure this bit to be an even value.

3.39 Chrominance Bottom Field Result Sub-Picture Size Register (BC_RESSPSIZE)

The chrominance bottom field result sub-picture size register (BC_RESSPSIZE) configures the horizontal sub-picture size for bottom-field chrominance data that is stored in SDRAM as result data. The BC_RESSPSIZE is shown in Figure 67 and described in Table 41.

Figure 67. Chrominance Bottom Field Result Sub-Picture Size Register (BC_RESSPSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		VDCE_RES_SP_HSZ_CBTM_TST	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 41. Chrominance Bottom Field Result Sub-Picture Size Register (BC_RESSPSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	VDCE_RES_SP_HSZ_CBTM_TST	0-1FFh	Defines horizontal sub-picture size for bottom field chrominance data that is stored in SDRAM as result data from the VDCE. This bit is for test of sub-picture mode. So, in normal use-case, this bit value should be configured to the same value as the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).
		0-Fh	Reserved
		10h	16 pixel
		11h-1Fh	Reserved
		20h	32 pixel
		21h-3Fh	Reserved
		40h	64 pixel
		41h-7Fh	Reserved
		80h	128 pixel
		81h-FFh	Reserved
		100h	256 pixel
		101h-1FFh	Reserved

3.40 Chrominance Bottom Field Line Result Address Offset Register (BC_RESOFFSET)

The chrominance bottom field line result address offset register (BC_RESOFFSET) configures the address offset value of each line for bottom field chrominance data on raster store format. The BC_RESOFFSET is shown in Figure 68 and described in Table 42.

Figure 68. Chrominance Bottom Field Line Result Address Offset Register (BC_RESOFFSET)

31	0
VDCE_RES_ADD_OFST_CBTM	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 42. Chrominance Bottom Field Line Result Address Offset Register (BC_RESOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	VDCE_RES_ADD_OFST_CBTM	0-FFFF FFFFh	Configures the address offset value of each line for bottom field chrominance data on raster store format. The stored chrominance data is for result image data processed by the VDCE. This bit value is given in bytes. Address calculation method on line [x] is written in the following equation: Address = RES_STRT_ADD + RES_ADD_OFST × line [x]. This bit is valid only if SDRAM storage mode is in raster scanning format; in sub-picture mode, this bit is ignored. Also, configure this bit to be an even value.

3.41 Luminance Source Image Start Position Register (IMG_Y_SRCSTRTPOS)

The luminance source image start position register (IMG_Y_SRCSTRTPOS) configures the horizontal start position of the source luminance image data. The IMG_Y_SRCSTRTPOS is shown in Figure 69 and described in Table 43.

Figure 69. Luminance Source Image Start Position Register (IMG_Y_SRCSTRTPOS)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		SRC_Y_STRT_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 43. Luminance Source Image Start Position Register (IMG_Y_SRCSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	SRC_Y_STRT_HPS	0-FFh	Defines horizontal start position of luminance source image data. The start position is the relative displacement from area start address. Note that LSB value has to be 0. This bit value should be less than the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).

3.42 Luminance Source Image Size Register (IMG_Y_SRCSIZE)

The luminance source image size register (IMG_Y_SRCSIZE) is shown in Figure 70 and described in Table 44.

Figure 70. Luminance Source Image Size Register (IMG_Y_SRCSIZE)

31	27	26	16
Reserved		SRC_Y_VSZ	
R-0		R/W-0	

15	12	11	0
Reserved		SRC_Y_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 44. Luminance Source Image Size Register (IMG_Y_SRCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	SRC_Y_VSZ	0-FFFh	Defines vertical size of source luminance image data. In interlace mode, this vertical size is equal to each field size. In progressive mode, this vertical size is equal to frame size.
15-12	Reserved	0	Reserved
11-0	SRC_Y_HSZ	0-FFFh	Defines horizontal size of source luminance image data. Note that LSB value has to be 0.

3.43 Chrominance Source Image Start Position Register (IMG_C_SRCSTRTPOS)

The chrominance source image start position register (IMG_C_SRCSTRTPOS) is shown in Figure 71 and described in Table 45.

Figure 71. Chrominance Source Image Start Position Register (IMG_C_SRCSTRTPOS)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		SRC_C_STRT_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 45. Chrominance Source Image Start Position Register (IMG_C_SRCSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	SRC_C_STRT_HPS	0-FFh	Defines horizontal start position of source chrominance image data. The start position is the relative displacement from area start address. Note that LSB value has to be 0. This bit value should be less than the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).

3.44 Chrominance Source Image Size Register (IMG_C_SRCSIZE)

The chrominance source image size register (IMG_C_SRCSIZE) is shown in Figure 72 and described in Table 46.

Figure 72. Chrominance Source Image Size Register (IMG_C_SRCSIZE)

31	27	26	16
Reserved		SRC_C_VSZ	
R-0		R/W-0	

15	12	11	0
Reserved		SRC_C_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 46. Chrominance Source Image Size Register (IMG_C_SRCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	SRC_C_VSZ	0-FFFh	Defines vertical size of source chrominance image data. In interlace mode, this vertical size is equal to each field size. In progressive mode, this vertical size is equal to frame size. Note that LSB value should be configured to 0 in pre-codec mode.
15-12	Reserved	0	Reserved
11-0	SRC_C_HSZ	0-FFFh	Defines horizontal size of source chrominance image data. Note that LSB value has to be 0.

3.45 Bitmap Source Image Start Position Register (IMG_BMP_SRCSTRTPOS)

The bitmap source image start position register (IMG_BMP_SRCSTRTPOS) is shown in Figure 73 and described in Table 47.

Figure 73. Bitmap Source Image Start Position Register (IMG_BMP_SRCSTRTPOS)

31	16
Reserved	
R-0	

15	5	4	0
Reserved		SRC_BMP_STRT_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 47. Bitmap Source Image Start Position Register (IMG_BMP_SRCSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4-0	SRC_BMP_STRT_HPS	0-1Fh	Defines offset value from SDRAM word boundary for bitmap data used in BLD function. Because each bitmap data has 2 bits/pixel data width, this bit defines only the offset value inside the SDRAM word, and the location of the SDRAM word should be configured by the address register. This bit value should be less than the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).

3.46 Bitmap Source Image Size Register (IMG_BMP_SRCSIZE)

The bitmap source image size register (IMG_BMP_SRCSIZE) is shown in Figure 74 and described in Table 48.

Figure 74. Bitmap Source Image Size Register (IMG_BMP_SRCSIZE)

31	27	26	16
Reserved		SRC_BMP_VSZ	
R-0		R/W-0	

15	12	11	0
Reserved		SRC_BMP_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

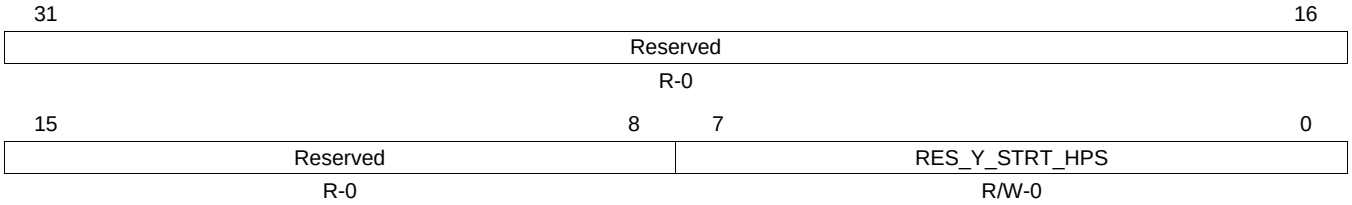
Table 48. Bitmap Source Image Size Register (IMG_BMP_SRCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	SRC_BMP_VSZ	0-FFFh	Defines vertical size of BLD source image data for bitmap window. In interlace mode, this vertical size is equal to each field size. In progressive mode, this vertical size is equal to frame size.
15-12	Reserved	0	Reserved
11-0	SRC_BMP_HSZ	0-FFFh	Defines horizontal size of BLD source image data for bitmap window. Note that LSB value has to be 0.

3.47 Luminance Result Image Start Position Register (IMG_Y_RESSTRTPOS)

The luminance result image start position register (IMG_Y_RESSTRTPOS) is shown in Figure 75 and described in Table 49.

Figure 75. Luminance Result Image Start Position Register (IMG_Y_RESSTRTPOS)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

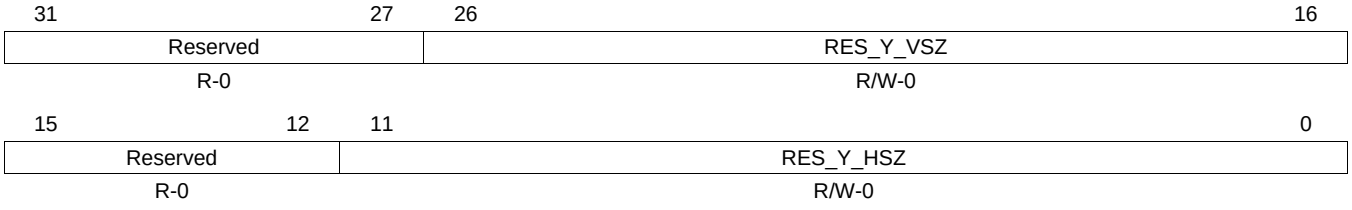
Table 49. Luminance Result Image Start Position Register (IMG_Y_RESSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	RES_Y_STRT_HPS	0-FFh	Defines horizontal start position of result luminance image data. The start position is the relative displacement from area start address. Note that LSB value has to be 0. This bit value should be less than the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).

3.48 Luminance Result Image Size Register (IMG_Y_RESSIZE)

The luminance result image size register (IMG_Y_RESSIZE) is shown in Figure 76 and described in Table 50.

Figure 76. Luminance Result Image Size Register (IMG_Y_RESSIZE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 50. Luminance Result Image Size Register (IMG_Y_RESSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	RES_Y_VSZ	0-FFFh	Defines vertical size of result luminance image data. In interlace mode, this vertical size is equal to each field size. In progressive mode, this vertical size is equal to frame size.
15-12	Reserved	0	Reserved
11-0	RES_Y_HSZ	0-FFFh	Defines horizontal size of result luminance image data. Note that LSB value has to be 0.

3.49 Chrominance Result Image Start Position Register (IMG_C_RESSTRTPOS)

The chrominance result image start position register (IMG_C_RESSTRTPOS) is shown in Figure 77 and described in Table 51.

Figure 77. Chrominance Result Image Start Position Register (IMG_C_RESSTRTPOS)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		RES_C_STRT_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 51. Chrominance Result Image Start Position Register (IMG_C_RESSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	RES_C_STRT_HPS	0-FFh	Defines horizontal start position of result chrominance image data. The start position is the relative displacement from area start address. Note that LSB value has to be 0. This bit value should be less than the VDCE_PRCS_UNIT_SIZE bit in the processing unit size register (PROC_SIZE).

3.50 Chrominance Result Image Size Register (IMG_C_RESSIZE)

The chrominance result image size register (IMG_C_RESSIZE) is shown in Figure 78 and described in Table 52.

Figure 78. Chrominance Result Image Size Register (IMG_C_RESSIZE)

31	27	26	16
Reserved		RES_C_VSZ	
R-0		R/W-0	

15	12	11	0
Reserved		RES_C_HSZ	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 52. Chrominance Result Image Size Register (IMG_C_RESSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	RES_C_VSZ	0-FFFh	Defines vertical size of resize result chrominance image data. In interlace mode, this vertical size is equal to each field size. In progressive mode, this vertical size is equal to frame size. Note that LSB value should be configured to 0 in post-codec mode.
15-12	Reserved	0	Reserved
11-0	RES_C_HSZ	0-FFFh	Defines horizontal size of resize result chrominance image data. Note that LSB value has to be 0.

3.51 Bitmap Result Image Start Position Register (IMG_BMP_RESSTRTPOS)

The bitmap result image start position register (IMG_BMP_RESSTRTPOS) configures the start position of the bitmap window to be blended to image data. The IMG_BMP_RESSTRTPOS is shown in Figure 79 and described in Table 53.

Figure 79. Bitmap Result Image Start Position Register (IMG_BMP_RESSTRTPOS)

31	27	26	16
Reserved		RES_BMP_STRT_VPS	
R-0		R/W-0	

15	12	11	0
Reserved		RES_BMP_STRT_HPS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 53. Bitmap Result Image Start Position Register (IMG_BMP_RESSTRTPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	RES_BMP_STRT_VPS	0-FFFh	Defines vertical start position of bitmap window to be blended to image data. The start position is the relative displacement from start position of video image data. Actual effect of this bit is shown in Figure 17. Note that LSB value has to be 0.
15-12	Reserved	0	Reserved
11-0	RES_BMP_STRT_HPS	0-FFFh	Defines horizontal start position of bitmap window to be blended to image data. The start position is the relative displacement from start position of video image data. Actual effect of this bit is shown in Figure 17. Note that LSB value has to be 0.

3.52 Resize Mode Definition Register (RSZ_MODE)

The resize mode definition register (RSZ_MODE) is shown in Figure 80 and described in Table 54.

Figure 80. Resize Mode Definition Register (RSZ_MODE)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved			RSZ_V_ALF_EN	Reserved		RSZ_H_ALF_MODE	RSZ_H_ALF_EN
R-0			R/W-0	R-0		R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved		RSZ_V_TYPE	RSZ_V_EN	Reserved		RSZ_H_TYPE	RSZ_H_EN
R-0		R/W-0	R/W-0	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 54. Resize Mode Definition Register (RSZ_MODE) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12	RSZ_V_ALF_EN		Vertical anti-alias filter control bit. If this bit is activated, output data of vertical resize shall be throughout data from result of horizontal resize (no vertical interpolation can be done in vertical resize; just down-sampling will be done when this bit is 1).
		0	Vertical anti-alias filter is inactive (vertical interpolation active).
		1	Vertical anti-alias filter is active (vertical interpolation inactive).
11-10	Reserved	0	Reserved
9	RSZ_H_ALF_MODE		Anti-alias filter mode control bit. The anti-alias filter has weight coefficient defined as a and b on Figure 9 and Figure 10. This bit selects a method to define these coefficients on manual or automatic. If manual is selected, both coefficients a and b have to be defined.
			Note that this bit is effective only when the RSZ_H_ALF_EN bit is set to 1; otherwise, this bit is ignored.
		0	Automatic calculated value for weight coefficient.
		1	Manual input for weight coefficient.
8	RSZ_H_ALF_EN		Horizontal anti-alias filter control bit. Filter characteristics can be seen in Section 2.5.1.
		0	Anti-alias filter is inactive.
		1	Anti-alias filter is active.
7-6	Reserved	0	Reserved
5	RSZ_V_TYPE		Vertical resize functional type selection bit.
			Note that this bit is effective only when the RSZ_V_EN bit is set to 1; otherwise, this bit is ignored.
		0	4-tap cubic convolution.
		1	4-tap linear interpolation.
4	RSZ_V_EN		Vertical resize function control bit. To re-scale source image for vertical direction, activate this bit and also configure the resize magnification ratio.
		0	Vertical resize is disabled.
		1	Vertical resize is enabled.
3-2	Reserved	0	Reserved
1	RSZ_H_TYPE		Horizontal resize functional type selection bit.
			Note that this bit is effective only when the RSZ_H_EN bit is set to 1; otherwise, this bit is ignored.
		0	4-tap cubic convolution.
		1	4-tap linear interpolation.

Table 54. Resize Mode Definition Register (RSZ_MODE) Field Descriptions (continued)

Bit	Field	Value	Description
0	RSZ_H_EN		Horizontal resize function control bit. To re-scale source image for horizontal direction, activate this bit and also configure the resize magnification ratio.
		0	Horizontal resize is disabled.
		1	Horizontal resize is enabled.

3.53 Horizontal Resize Magnification Ratio Control Register (RSZ_HMAG)

The horizontal resize magnification ratio control register (RSZ_HMAG) is shown in Figure 81 and described in Table 55.

Figure 81. Horizontal Resize Magnification Ratio Control Register (RSZ_HMAG)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		RSZ_H_MAG	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

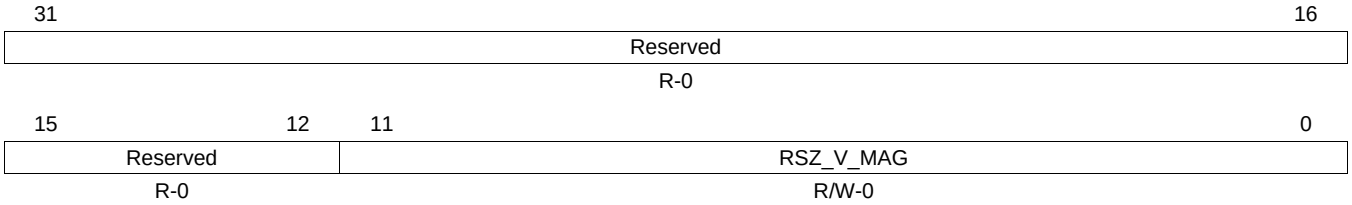
Table 55. Horizontal Resize Magnification Ratio Control Register (RSZ_HMAG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	RSZ_H_MAG	0-FFFh	Defines resize magnification ratio for horizontal direction. Real ratio is derived from following equation: Magnification ratio = 256/(RSZ_H_MAG) Note that the RSZ_H_MAG value can vary from 256 to 2048. Any value less than 256 is not valid.

3.54 Vertical Resize Magnification Ratio Control Register (RSZ_VMAG)

The vertical resize magnification ratio control register (RSZ_VMAG) is shown in Figure 82 and described in Table 56.

Figure 82. Vertical Resize Magnification Ratio Control Register (RSZ_VMAG)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 56. Vertical Resize Magnification Ratio Control Register (RSZ_VMAG) Field Descriptions

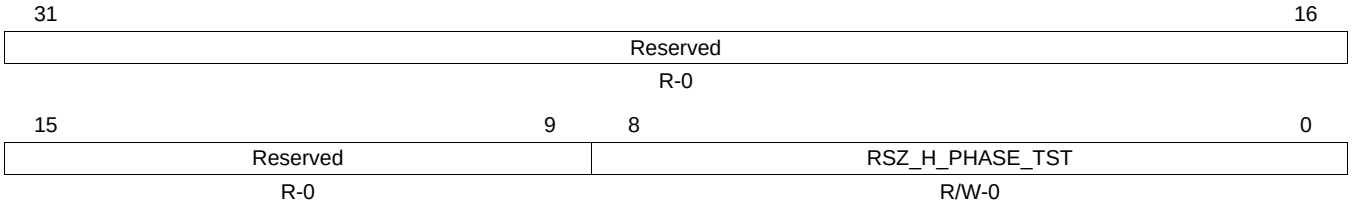
Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	RSZ_V_MAG	0-FFFh	Defines resize magnification ratio for vertical direction. Real ratio is derived from following equation: Magnification ratio = 256/(RSZ_V_MAG) Note that the RSZ_V_MAG value can vary from 256 to 2048. Any value less than 256 is not valid.

3.55 Phase of Initial Pixel on Horizontal Resize Register (RSZ_HPHASE)

This register configures the horizontal phase displacement of the first resized output pixel position from the first pixel in the source image.

The phase of initial pixel on horizontal resize register (RSZ_HPHASE) is shown in Figure 83 and described in Table 57.

Figure 83. Phase of Initial Pixel on Horizontal Resize Register (RSZ_HPHASE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 57. Phase of Initial Pixel on Horizontal Resize Register (RSZ_HPHASE) Field Descriptions

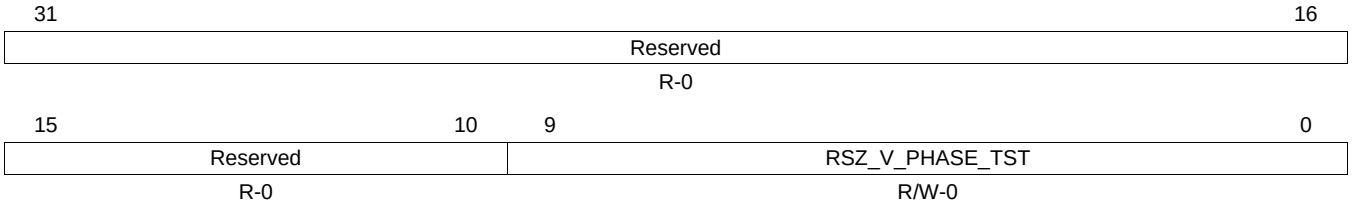
Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	RSZ_H_PHASE_TST	0-1FFh	Defines phase of displacement of first resized output pixel position from first pixel in source image. Real displacement value is derived from following equation: First resized pixel position = (RSZ_H_PHASE_TST)/512 (Detail image in Figure 11) In normal use-case, RSZ_H_PHASE_TST should be configured to 0.

3.56 Phase of Initial Pixel on Vertical Resize Register (RSZ_VPHASE)

This register configures the vertical phase displacement of the first resized output pixel position from the first pixel in the source image.

The phase of initial pixel on vertical resize register (RSZ_VPHASE) is shown in Figure 84 and described in Table 58.

Figure 84. Phase of Initial Pixel on Vertical Resize Register (RSZ_VPHASE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 58. Phase of Initial Pixel on Vertical Resize Register (RSZ_VPHASE) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Reserved
9-0	RSZ_V_PHASE_TST	0-3FFh	Defines phase of displacement of first resized output pixel position from first pixel in source image. Real displacement value is derived from following equation: First resized pixel position = (RSZ_V_PHASE_TST)/1024 (Detail image in Figure 11) In normal use-case, RSZ_V_PHASE_TST should be configured to 0.

3.57 Intensity of Horizontal Anti-Aliasing Filter Register (RSZ_AFILTER)

The intensity of horizontal anti-aliasing filter register (RSZ_AFILTER) is shown in Figure 85 and described in Table 59.

Figure 85. Intensity of Horizontal Anti-Aliasing Filter Register (RSZ_AFILTER)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		RSZ_ALF_INTENSITY	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

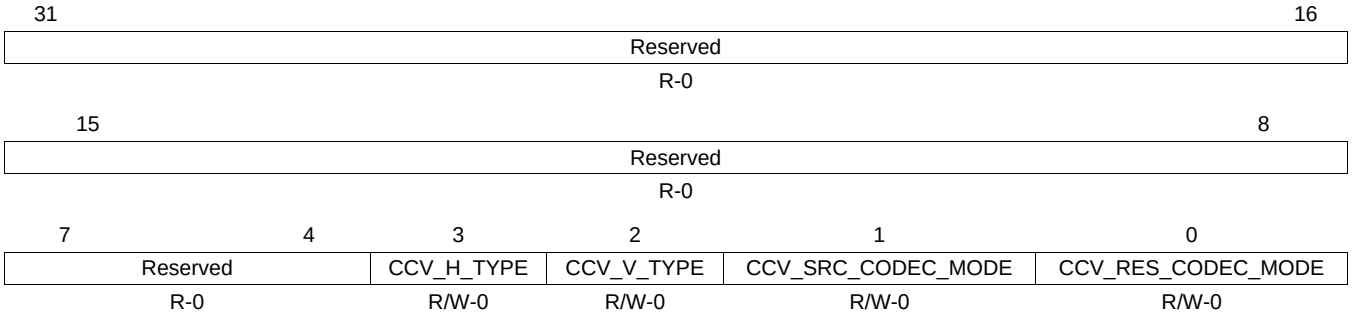
Table 59. Intensity of Horizontal Anti-Aliasing Filter Register (RSZ_AFILTER) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	RSZ_ALF_INTENSITY	0-FFh	Defines intensity of horizontal anti-aliasing filter (see Figure 9 and Figure 10). Note that this value must not be over 128 (if over, the value shall be clipped to 128). This bit is effective only when the RSZ_H_ALF_MODE and RSZ_H_ALF_EN bits in the resize mode definition register (RSZ_MODE) are set to 1; otherwise, the configured value shall be ignored. Weight coefficient on Figure 10 is derived from following equations; Weight coefficient a = clip (RSZ_ALF_INTENSITY, 0, 64) Weight coefficient b = clip (RSZ_ALF_INTENSITY, 64, 128) Note: clip(x, min, max) works as: If (x < min) then clip(x, min, max) = min; else if (max < x) then clip(x, min, max) = max; else clip(x, min, max) = x

3.58 Chrominance Conversion Mode Control Register (CCV_MODE)

The chrominance conversion mode control register (CCV_MODE) is shown inFigure 86 and described in Table 60.

Figure 86. Chrominance Conversion Mode Control Register (CCV_MODE)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 60. Chrominance Conversion Mode Control Register (CCV_MODE) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Reserved
3	CCV_H_TYPE		Chrominance conversion functional type selection bit (for horizontal). Note that this bit has functional effect only when the codec format for either source data or result data is MPEG-1; that is, CCV_MODE bits [1:0] are configured to 1H or 2h; otherwise, this bit is ignored.
		0	4-tap cubic convolution.
		1	4-tap linear interpolation.
2	CCV_V_TYPE		Chrominance conversion functional type selection bit (for vertical).
		0	4-tap cubic convolution.
		1	4-tap linear interpolation.
1	CCV_SRC_CODEC_MODE		This bit contributes to mode control for chrominance conversion source data. As discussed in Section 2.5.2, functional performance of chrominance conversion varies from types of video codec; we can distinguish it between MPEG-1 and others. This bit is effective only when the VDCE_CCV_EN bit in the control register (CTRL) is set to 1; otherwise, this bit is ignored.
		0	Chrominance conversion on MPEG-2/MPEG-4/H.264/VC-1
		1	Chrominance conversion on MPEG-1
0	CCV_RES_CODEC_MODE		This bit contributes to mode control for chrominance conversion result data. As discussed in Section 2.5.2, functional performance of chrominance conversion varies from types of video codec; we can distinguish it between MPEG-1 and others. This bit is effective only when the VDCE_CCV_EN bit in the control register (CTRL) is set to 1; otherwise, this bit is ignored.
		0	Chrominance conversion on MPEG-2/MPEG-4/H.264/VC-1
		1	Chrominance conversion on MPEG-1

3.59 Look-Up Table for Index 00 Register (BLD_LUT_00)

The look-up table for index 00 register (BLD_LUT_00) is shown in Figure 87 and described in Table 61.

Figure 87. Look-Up Table for Index 00 Register (BLD_LUT_00)

31	24	23	16
BLD_LUT_00_FCT		BLD_LUT_00_Y	
R/W-0		R/W-0	

15	8	7	0
BLD_LUT_00_CB		BLD_LUT_00_CR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 61. Look-Up Table for Index 00 Register (BLD_LUT_00) Field Descriptions

Bit	Field	Value	Description
31-24	BLD_LUT_00_FCT	0-FFh	Blend factor for color defined in index value 00b.
23-16	BLD_LUT_00_Y	0-FFh	Luminance data for color defined in index value 00b.
15-8	BLD_LUT_00_CB	0-FFh	Chrominance (Cb) data for color defined in index value 00b.
7-0	BLD_LUT_00_CR	0-FFh	Chrominance (Cr) data for color defined in index value 00b.

3.60 Look-Up Table for Index 01 Register (BLD_LUT_01)

The look-up table for index 01 register (BLD_LUT_01) is shown in Figure 88 and described in Table 62.

Figure 88. Look-Up Table for Index 01 Register (BLD_LUT_01)

31	24	23	16
BLD_LUT_01_FCT		BLD_LUT_01_Y	
R/W-0		R/W-0	

15	8	7	0
BLD_LUT_01_CB		BLD_LUT_01_CR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 62. Look-Up Table for Index 01 Register (BLD_LUT_01) Field Descriptions

Bit	Field	Value	Description
31-24	BLD_LUT_01_FCT	0-FFh	Blend factor for color defined in index value 01b.
23-16	BLD_LUT_01_Y	0-FFh	Luminance data for color defined in index value 01b.
15-8	BLD_LUT_01_CB	0-FFh	Chrominance (Cb) data for color defined in index value 01b.
7-0	BLD_LUT_01_CR	0-FFh	Chrominance (Cr) data for color defined in index value 01b.

3.61 Look-Up Table for Index 02 Register (BLD_LUT_02)

The look-up table for index 02 register (BLD_LUT_02) is shown in Figure 89 and described in Table 63.

Figure 89. Look-Up Table for Index 02 Register (BLD_LUT_02)

31	24	23	16
BLD_LUT_02_FCT		BLD_LUT_02_Y	
R/W-0		R/W-0	

15	8	7	0
BLD_LUT_02_CB		BLD_LUT_02_CR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 63. Look-Up Table for Index 02 Register (BLD_LUT_02) Field Descriptions

Bit	Field	Value	Description
31-24	BLD_LUT_02_FCT	0-FFh	Blend factor for color defined in index value 10b.
23-16	BLD_LUT_02_Y	0-FFh	Luminance data for color defined in index value 10b.
15-8	BLD_LUT_02_CB	0-FFh	Chrominance (Cb) data for color defined in index value 10b.
7-0	BLD_LUT_02_CR	0-FFh	Chrominance (Cr) data for color defined in index value 10b.

3.62 Look-Up Table for Index 03 Register (BLD_LUT_03)

The look-up table for index 03 register (BLD_LUT_03) is shown in Figure 90 and described in Table 64.

Figure 90. Look-Up Table for Index 03 Register (BLD_LUT_03)

31	24	23	16
BLD_LUT_03_FCT		BLD_LUT_03_Y	
R/W-0		R/W-0	

15	8	7	0
BLD_LUT_03_CB		BLD_LUT_03_CR	
R/W-0		R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 64. Look-Up Table for Index 03 Register (BLD_LUT_03) Field Descriptions

Bit	Field	Value	Description
31-24	BLD_LUT_03_FCT	0-FFh	Blend factor for color defined in index value 11b.
23-16	BLD_LUT_03_Y	0-FFh	Luminance data for color defined in index value 11b.
15-8	BLD_LUT_03_CB	0-FFh	Chrominance (Cb) data for color defined in index value 11b.
7-0	BLD_LUT_03_CR	0-FFh	Chrominance (Cr) data for color defined in index value 11b.

3.63 Range Mapping Control Register (RGMP_CTRL)

The range mapping control register (RGMP_CTRL) is shown in Figure 91 and described in Table 65.

Figure 91. Range Mapping Control Register (RGMP_CTRL)

31	16
Reserved	
R-0	

15	12	11	10	8
Reserved		RANGE_MAP_C_EN	RANGE_MAP_C	
R-0		R/W-0	R/W-0	

7	4	3	2	0
Reserved		RANGE_MAP_Y_EN	RANGE_MAP_Y	
R-0		R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

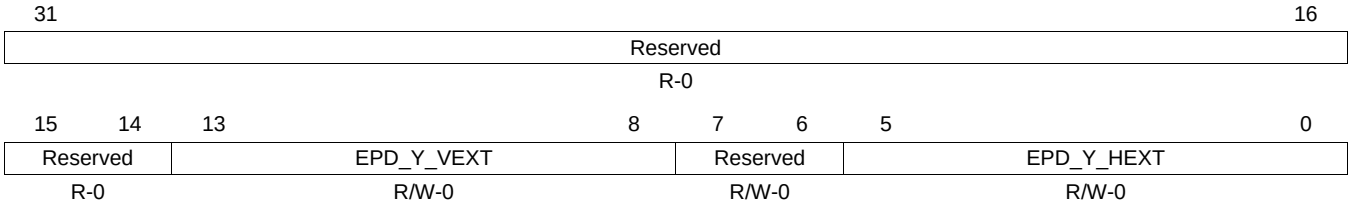
Table 65. Range Mapping Control Register (RGMP_CTRL) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11	RANGE_MAP_C_EN		Control bit for range mapping on chrominance. "Range_MapUV_Flag" value that is inserted in entry point header has to be reflected.
		0	Chrominance range mapping is disabled.
		1	Chrominance range mapping is enabled.
10-8	RANGE_MAP_C	0-7h	Coefficient for multiplier of equation to calculate chrominance pixel value for range mapping. This bit is effective only when the enable flag (Range_MAPUV_Flag) is activated; otherwise, this bit is ignored.
7-4	Reserved	0	Reserved
3	RANGE_MAP_Y_EN		Control bit for range mapping on luminance. "Range_MapY_Flag" value that is inserted in entry point header has to be reflected.
		0	Luminance range mapping is disabled.
		1	Luminance range mapping is enabled.
2-0	RANGE_MAP_Y	0-7h	Coefficient for multiplier of equation to calculate luminance pixel value for range mapping. This bit is effective only when the enable flag (Range_MAPY_Flag) is activated; otherwise, this bit is ignored.

3.64 Edge Padding Width for Luminance Register (EPD_LUMA_WIDTH)

The edge padding width for luminance register (EPD_LUMA_WIDTH) configures the extension width of the edge padding function for luminance field data in SDRAM. The EPD_LUMA_WIDTH is shown in Figure 92 and described in Table 66.

Figure 92. Edge Padding Width for Luminance Register (EPD_LUMA_WIDTH)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 66. Edge Padding Width for Luminance Register (EPD_LUMA_WIDTH) Field Descriptions

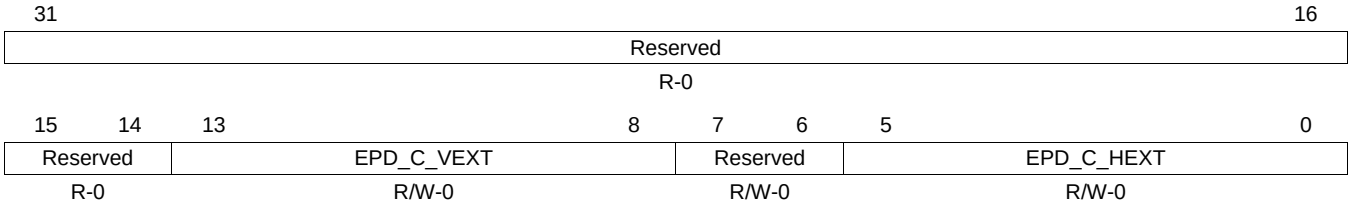
Bit	Field	Value	Description
31-14	Reserved	0	Reserved
13-8	EPD_Y_VEXT	0-3Fh	Defines vertical extension width of edge padding function for luminance field data in SDRAM. Half size of defined number of pixels is added to both upper and lower edge of field (total extension size is equal to this bit value).
7-6	Reserved	0	Reserved
5-0	EPD_Y_HEXT	0-3Fh	Defines horizontal extension width of edge padding function for luminance field data in SDRAM. Defined values of pixels are added to both left and right edge of field.

3.65 Edge Padding Width for Chrominance Register (EPD_CHROMA_WIDTH)

This register configures the extension width of the edge padding function for chrominance field data in SDRAM.

The edge padding width for chrominance register (EPD_CHROMA_WIDTH) is shown in Figure 93 and described in Table 67.

Figure 93. Edge Padding Width for Chrominance Register (EPD_CHROMA_WIDTH)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 67. Edge Padding Width for Chrominance Register (EPD_CHROMA_WIDTH) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Reserved
13-8	EPD_C_VEXT	0-3Fh	Defines vertical extension width of edge padding function for chrominance field data in SDRAM. Half size of defined number of pixels is added to both upper and lower edge of field (total extension size is equal to this value).
7-6	Reserved	0	Reserved
5-0	EPD_C_HEXT	0-3Fh	Defines horizontal extension width of edge padding function for chrominance field data in SDRAM. Defined values of pixels are added to both left and right edge of field. Note that LSB value should be 0 (only even value is acceptable).

Appendix A Revision History

This document has been revised to include the following technical change(s).

Table 68. Document Revision History

Reference	Additions/Modifications/Deletions
Section 2.5.1.2	Deleted last sentence in last paragraph.
Table 54	Changed Description of RSZ_V_ALF_EN bit.