TMS320DM646x DMSoC
Transport Stream Interface (TSIF) Module

User's Guide

Literature Number: SPRUEQ2E
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About This Manual

Describes the operation of the transport stream interface (TSIF) module in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUEP8 — ***TMS320DM646x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRUEP9 — ***TMS320DM646x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

SPRUEQ0 — ***TMS320DM646x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRAA84 — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Transport Stream Interface (TSIF) Module

1 Introduction

This document describes the operation of the transport stream interface (TSIF) module in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

1.1 Purpose of the Peripheral

The purpose of the transport stream interface (TSIF) module is to parser stream including TS (Time Stamp) header, adaptation field, payload and packet ID (PID) table, and to input and output stream with a parallel and serial interface. The DM646x DMSoC includes two independent transport stream interface (TSIF0 and TSIF1) modules with corresponding clock reference generator (CRGEN) modules for system time-clock recovery.

1.2 Features

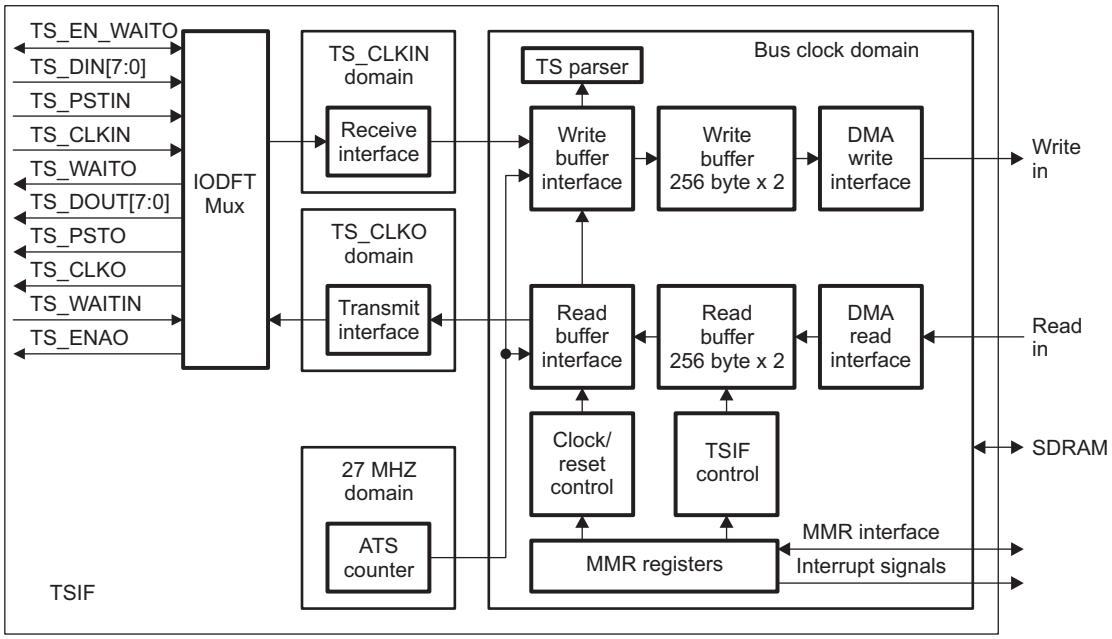
The TSIF consists of the following features.

- Simple I/O section that consists of serial and parallel interface (I/F) with both synchronous and asynchronous modes.
- Stream Parser and PID filter (TS header parser, adaptation field parser, payload parser, and PID table).
- Absolute time stamp (ATS) generator and checker for time management by CPU and video codec.
- Ring buffer controller prepared for SDRAM access.
- Input and output ping-pong buffer (one buffer has 256 byte (64 bit $\times$ 32 word)).
- Serial and parallel I/F with both synchronous and asynchronous modes.
- Data bus width is 1 bit on serial I/F (using MSB of parallel I/F) and 8 bits on parallel I/F.
- Stream input/output (I/O) speed rate is configurable by I/O clock speed.
- Input data is stored into SDRAM in 32-bit little-endian mode only with 192 byte/unit format or 256 byte/unit format.
- ATS detection, correction, and addition mode are implemented.
- Automatically detect program association table (PAT) and program map table (PMT) and reflect to PID table assignment in itself (partial TS only; stream type and PID should be one-to-one mapping).
- PID filter with 7 PID filter tables and stream type assignments.
- Bypass mode is implemented so that not only TS data but also any other data can be received or transmitted by this module.
- Ring buffer control for both write (8 channels) and read (1 channel) control for SDRAM.
- Specific packet support which is prepared for indicating boundary of plural program on TS.
- Full-TS can be supported in one mode (semiautomatic A mode) with communication to the CPU. Mainly, TS-related functions are available only in partial TS (semiautomatic B mode and full automatic mode can support only partial TS whose stream type and PID is one-to-one mapping).

1.3 Functional Block Diagram

The TSIF functional block diagram is shown in Figure 1.

Figure 1. TSIF Block Diagram



1.4 Terminology Used in This Document

The following is a brief explanation of some terms used in this document:

Term	Meaning
ARIB	Association of Radio Industries and Businesses
ATS	absolute time stamp
DIT	discontinuity information table
PAT	program association table
PES	packetized elementary stream
PID	packet ID
PMT	program map table
PS	program stream
STC	system time clock
TS	time stamp
TSIF	transport stream interface

2 Architecture

This section describes the architecture of the transport stream interface (TSIF) module.

2.1 Clock Control

The TSIF module receives and transfers video packet data. In receive mode, the source of the driving clock comes from an external device (host device). In transfer mode, the source of the driving clock is the internal clock of the DM646x DMSoC. See the device-specific data manual for detailed information about clock control.

From the standpoint of controlling the stream clock, the most applicable way to use the TSIF module is:

1. Start providing the stream clock to the TSIF module (but do not start sending data).
2. Activate the TSIF module via the register configuration.
3. Start sending the stream data from the data initiator to the TSIF.
4. After the data is finished sending, inactivate the TSIF module via the register configuration.
5. Stop providing the stream clock to the TSIF module.

2.2 Signal Descriptions

The TSIF provides the I/O signals listed in Table 1.

Table 1. TSIF Signal Descriptions

	Serial				Parallel			
	Synchronous		Asynchronous		Synchronous		Asynchronous	
Port Name	**I/O**	**Function**	**I/O**	**Function**	**I/O**	**Function**	**I/O**	**Function**
TS*n*_CLKO	O	Transmit clock	O	Transmit clock	O	Transmit clock	O	Transmit clock
TS*n*_ENAO	O	Data enable	O	Data enable	O	Data enable	O	Data enable
TS*n*_WAITIN	I	Not used	I	Wait in	I	Not used	I	Wait in
TS*n*_PSTO	O	Packet start out	O	Packet start out	O	Packet start out	O	Packet start out
TS*n*_DOUT7	O	Data out	O	Data out	O	Data[7] out	O	Data[7] out
TS*n*_DOUT[6:0]	O	Not used	O	Not used	O	Data[6:0] out	O	Data[6:0] out
TS*n*_CLKIN	I	Receive clock	I	Receive clock	I	Receive clock	I	Receive clock
TS*n*_EN_WAITO	I	Data enable	O	Wait out	I	Data enable	O	Wait out
TS*n*_WAITO	O	Not used	O	Not used	O	Not used	O	Wait out
TS*n*_PSTIN	I	Packet start in	I	Packet start in	I	Packet start in	I	Packet start in
TS*n*_DIN7	I	Data in	I	Data in	I	Data[7] in	I	Data[7] in
TS*n*_DIN[6:0]	I	Not used	I	Not used	I	Data[6:0] in	I	Data[6:0] in

2.3 Pin Multiplexing

On the DM646x DMSoC, extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the TSIF.

2.4 General Architecture

This section describes the internal architecture of the TSIF module. The DM646x DMSoC has two TSIF modules. The TSIF0 module is able to use the parallel interface and serial interface. The TSIF1 module is able to use only the serial interface.

2.4.1 PID Filter Control

Four types of PID filter methods are supported and are controlled by the PID_FILTER_CTL and PID_FILTER_EN bits in the TSIF control register 1 (CTRL1).

2.4.1.1 Bypass Mode

This mode does not use the PID_FILTER_CTL bit in CTRL1. When the PID_FILTER_EN bit in CTRL1 is cleared to 0, input data is stored directly to ring buffer channel 7.

2.4.1.2 Full Manual Mode

In this mode, the CPU configures all PID of packets to be filtered and stored into SDRAM. The CPU is required to know information such as stream type of each category (video, audio, etc.) and PID of targeted category before stream data comes from the host device. The hardware does not have to detect PAT and PMT data.

Note: The TSIF module does not detect PAT/PMT nor aware of what stream each PID carries in this mode. The TSIF module only PID filters based on the PID filter settings.

2.4.1.3 Semi-automatic Mode-A

In this mode, the TSIF module detects PAT and PMT and stores in SDRAM. Then, the CPU reads PAT and PMT stored in SDRAM, and configures the PID filter assignments with the stream type.

Note: In some cases, the CPU asserts an interrupt to the Host device and the Host device stalls to assert the source stream data, if PAT/PMT (which has updated version number) detect an interrupt asserted by the TSIF module.

2.4.1.4 Semi-automatic Mode-B

Semi-automatic mode-B is prepared for partial TS reception. At first, the CPU is required to configure the PID filter assignments to be filtered. Then any change of PAT and PMT of the incoming TS data is automatically detected and reflected into the PID filter assignment table. In this case, the following restrictions exist so that this mode performs correctly and effectively.

- The TSIF module holds the configuration of the stream type on the PID filter assignment table as first configured by the CPU and the TSIF module automatically changes only the PID value, if PAT and PMT are changed.
- The incoming TS data can include only one program. This means that only one type of program number on the PAT loop part can be detected.
- When a new PMT comes, the TSIF module automatically changes the PID value, whose stream type is the same as the first configured value by the CPU. So, in this mode, each stream type and each PID value should be one-to-one mapping.

2.4.1.5 Full Automatic Mode

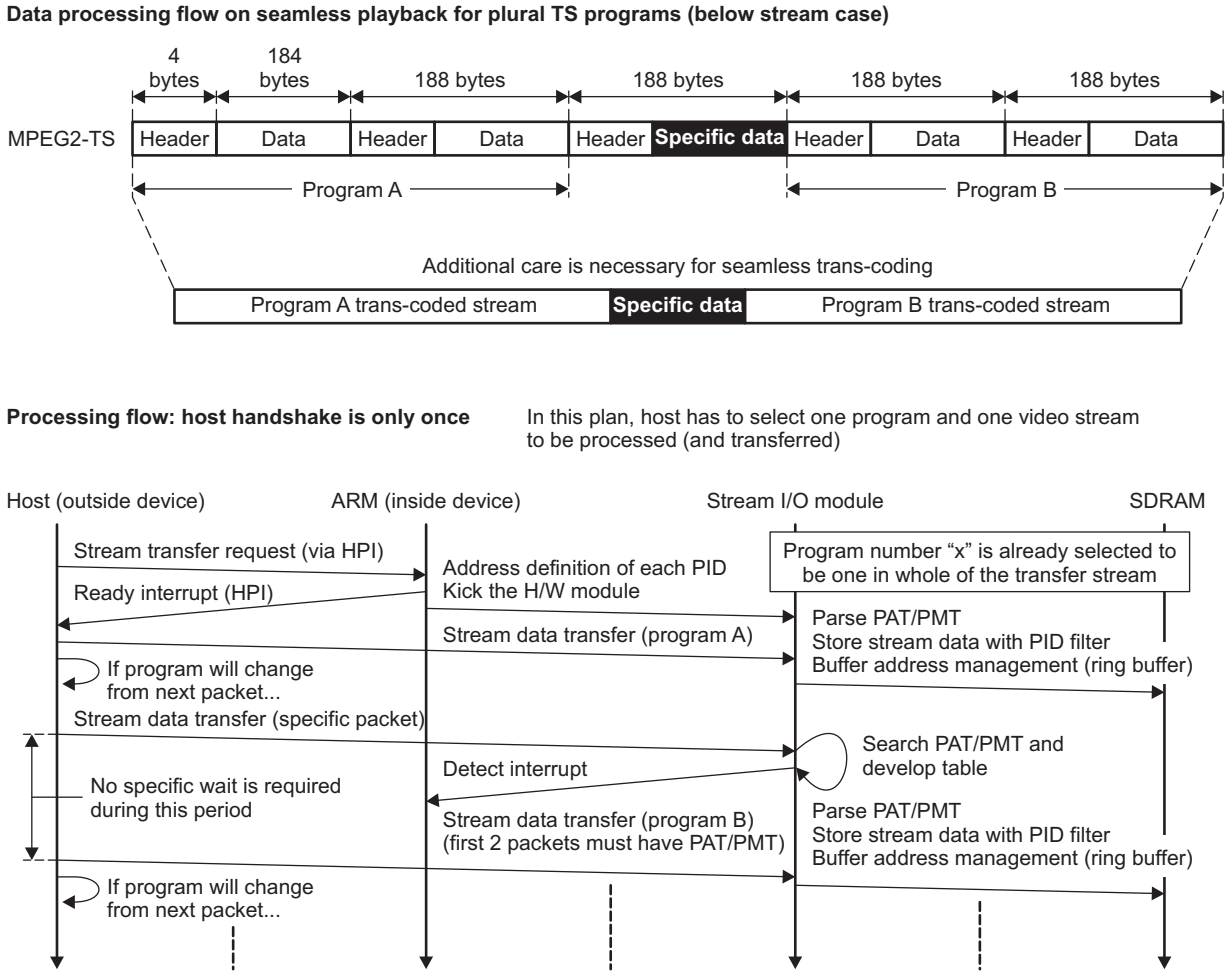
Full automatic mode is prepared for partial TS reception. The CPU enables the TSIF module without any configuration, except the stream type on the PID filter table assignment. After the first configuration, all changes of PAT and PMT are detected and reflected into the PID filter table assignment automatically. In this case, similar restrictions exist as for semi-automatic mode-B (Section 2.4.1.4).

2.4.2 Seamless Trans-Coding on Plural Program

In the case where some plural programs exist consecutively in one TS data, a specific data is inserted at the boundary of two programs (see Figure 2). In ARIB format, DIT is defined as such a boundary indicator. DIT needs the main engine to be reset. In order to change the program configuration without any reset action, this specific code is necessary. This specific code is called a boundary sensing packet.

The functional protocol and format is shown in Figure 2.

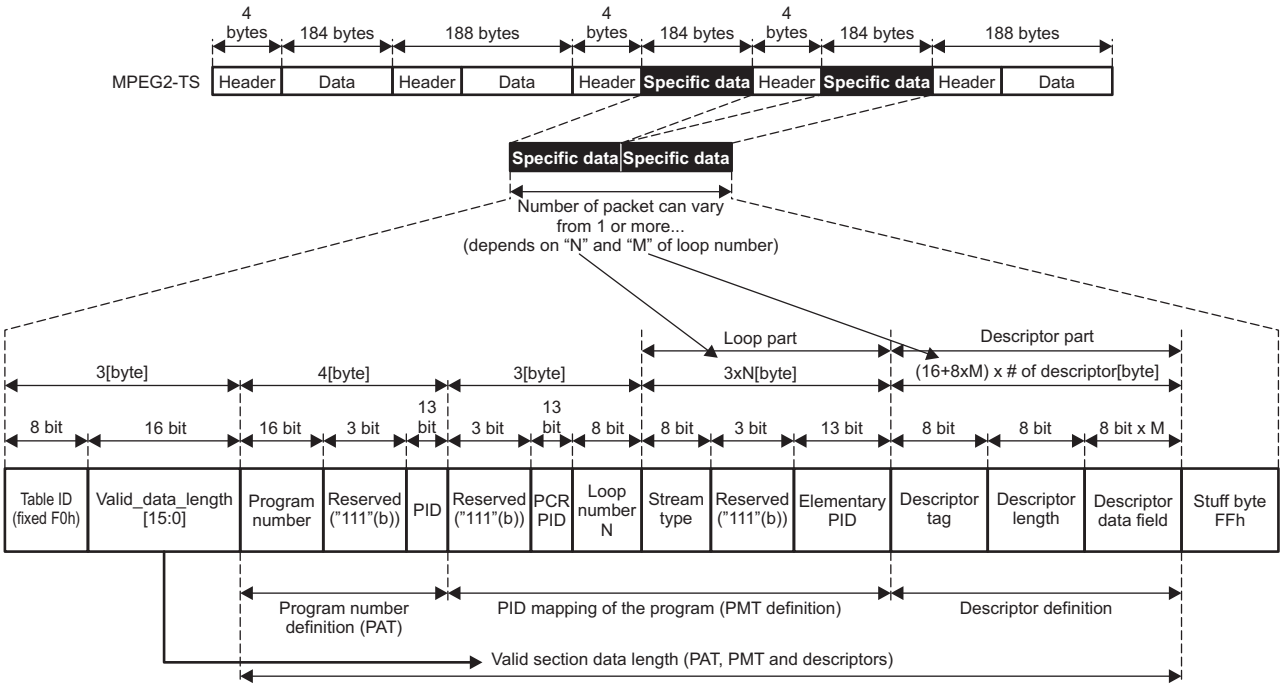
Figure 2. Seamless Trans-Coding on Plural Programs



2.4.2.1 Detecting Boundary Sensing Packet

The boundary sensing packet is based on the private section format. This packet is inserted at the boundary position of plural TS programs. The logical packet format is shown in Figure 3.

Figure 3. Logical Format of Boundary Sensing Packet



The PID of the packet can be configured by the SEAMLESS_BOUNDARY_INPUT_PID bit in the boundary sensing packet input register (BSP_IN). Once the hardware module senses this packet, an interrupt pulse is asserted to the CPU and stores the packet data in SDRAM from the start address defined by the SEAMLESS_BOUNDARY_PKT_STRT_ADD bit in the boundary sensing packet store address register (BSP_STORE_ADDR). When the CPU detects the interrupt from the TSIF module, the CPU accesses the defined address in SDRAM and parses data to process it.

The procedure of processing this packet is:

1. When the TSIF module detects a boundary sensing packet, the TSIF module asserts an interrupt pulse to the CPU. In addition, the TSIF module clears all configurations on the PID filter table.
2. After sending a boundary sensing packet, the host device needs to stall sending the stream data to the TSIF module.
3. The CPU detects the interrupt pulse on step 1, and reads the packet data from SDRAM.
4. The CPU parses the packet data and reflects the results of parsing in the configuration of the PID filter table (including PAT and PMT). The module registers related to the PID filter table are configured.
5. The CPU asserts an interrupt to the host device, and the host device starts to assert stream data to be processed in the TSIF module.

This procedure is common in all 4 modes.

2.4.2.2 Detecting DIT

DIT is defined in ARIB standard format. DIT and boundary sensing is similar, except DIT needs the receiver and transmitter devices to be reset. The procedure of processing this packet is:

1. When the TSIF module detects DIT packets, the TSIF module asserts an interrupt pulse to the CPU. In addition, the TSIF module clears all configurations on the PID filter table including PAT and PMT sensing table.
2. After stage 1, the normal PID filter process is re-started in accordance with the definition of modes for the PID filter method.

This procedure is common in all 4 modes.

2.4.3 Ring Buffer Control

After demultiplexing of the source incoming stream and before assertion of the outgoing stream, the TSIF module accesses SDRAM. Then, the TSIF module is required to know the read or write address to be accessed. The TSIF module has an address management tool known as the ring buffer controller, which helps address management by the CPU to avoid buffer overrun and underrun.

2.4.4 ATS Control

The TSIF module supports ATS. This section describes the ATS control with receive case and transfer case.

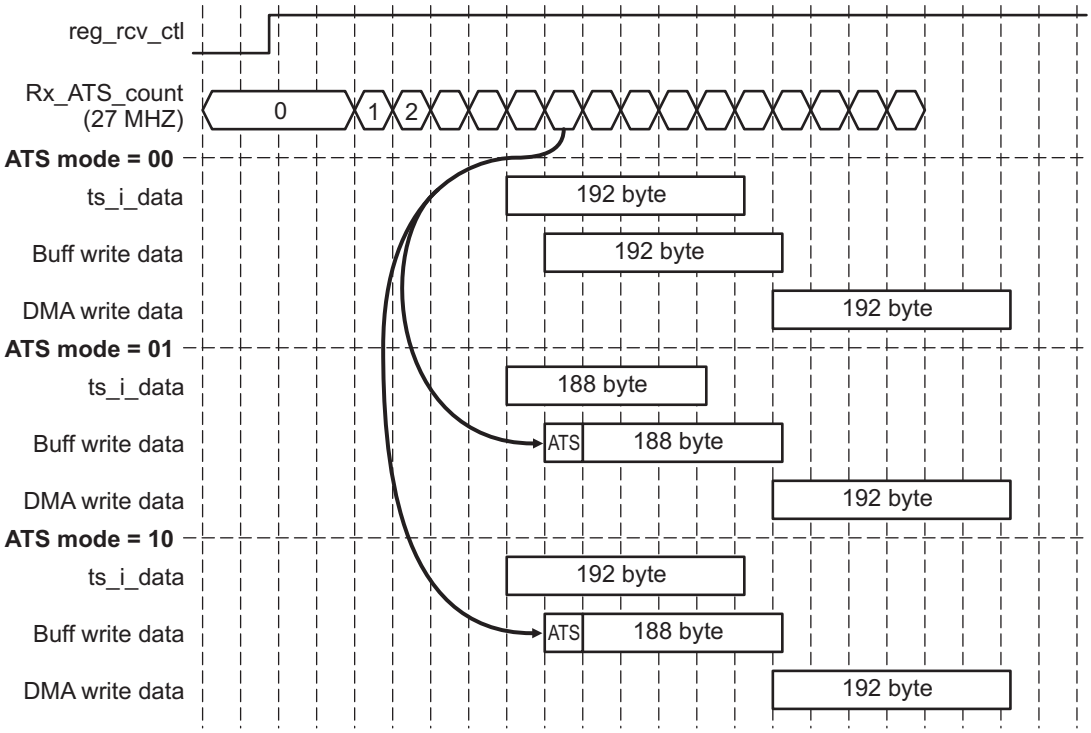
2.4.4.1 ATS Control with Receive Case

ATS control with receive case has 3 modes (Table 2). It is configured by the RCV_ATS_MODE bit in the TSIF control register 0 (CTRL0). The format is shown in Figure 4.

Table 2. ATS Control with Receive Case

RCV_ATS_MODE	Description
0	Do nothing mode. ATS value is stored as 192-byte packet data into SDRAM without any change.
1h	Add ATS mode. ATS value is added to the incoming 188-byte packet data.
2h	Replace ATS mode. ATS value is replaced in the incoming 192-byte packet data.

Figure 4. ATS Control with Receive Case



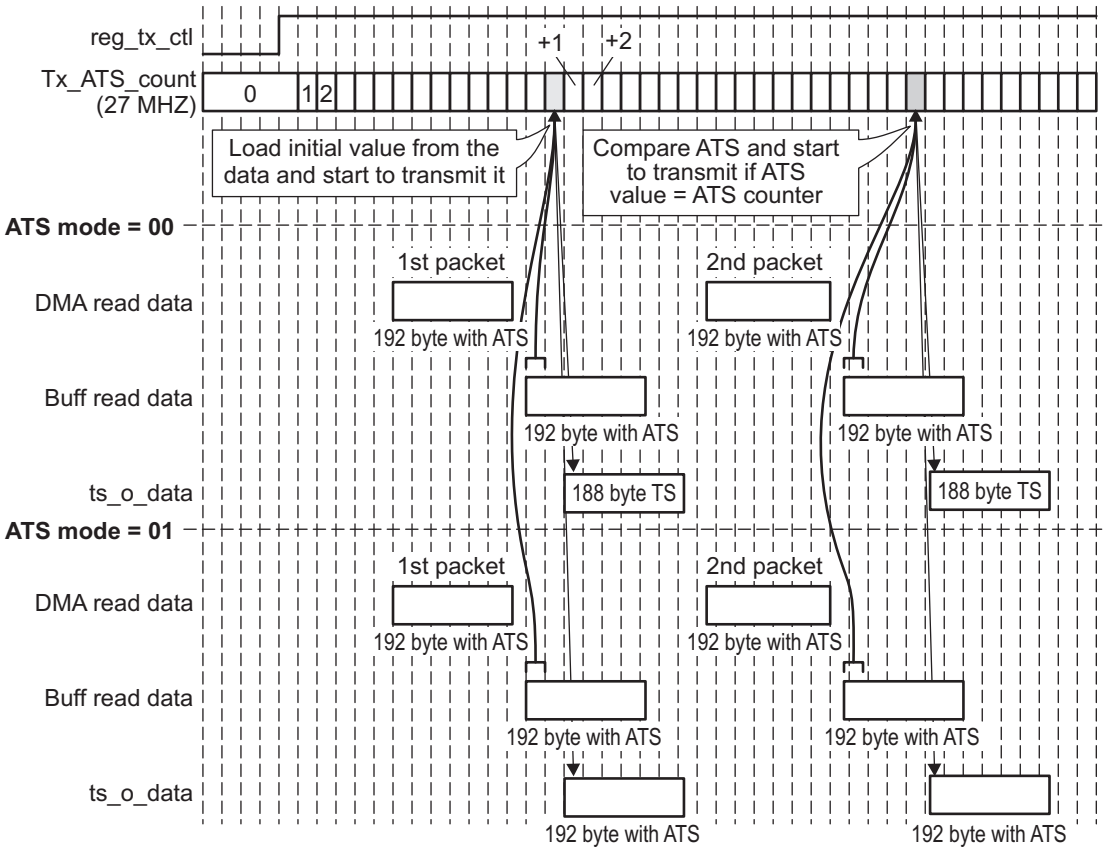
2.4.4.2 ATS Control with Transfer Case

TS transfer with ATS has 2 cases and each case has 2 modes.

2.4.4.2.1 ATS Control with Packet Data Initial Value

In this case, the 1st packet uses the packet data initial value when the 1st packet data is transferred. The TX_ATS_INIT_EN bit in the transmit ATS initialization register (TX_ATS_INIT) is cleared 0. The format is shown in Figure 5.

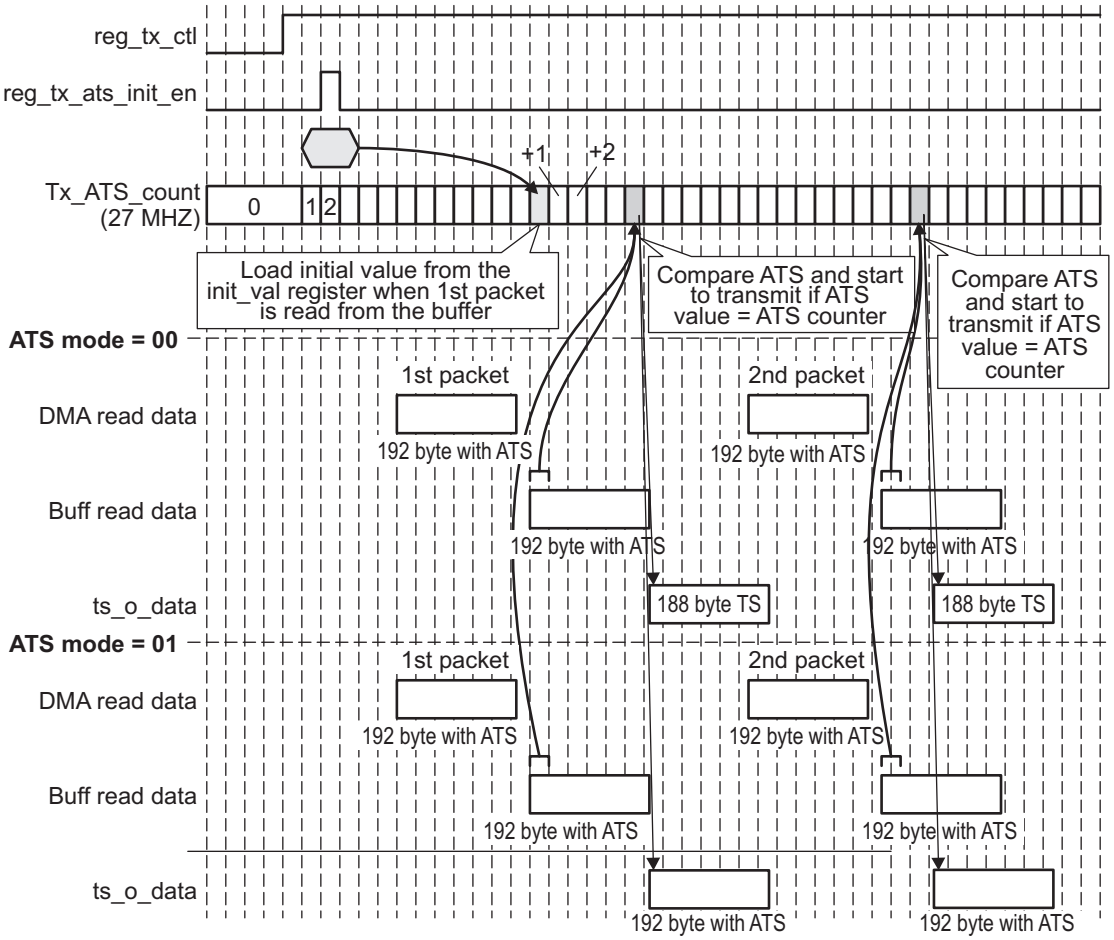
Figure 5. ATS Control with Transfer Case using Packet Data Initial Value



2.4.4.2.2 ATS Control with Module Initial Value

In this case, the 1st packet uses the TX_ATS_INIT bits in the transmit ATS initialization register (TX_ATS_INIT) when the 1st packet data is transferred. The TX_ATS_INIT_EN bit in TX_ATS_INIT is set to 1. The format is shown in Figure 6.

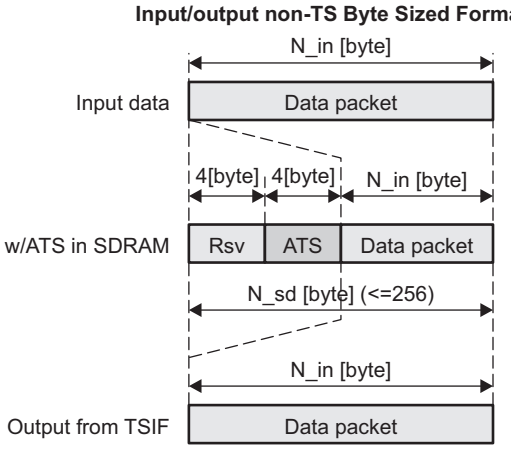
Figure 6. ATS Control with Transfer Case using Module Initial Value



2.4.5 Variable Packet Sizing for non-TS mode

Variable packet sizing is supported for non-TS mode. Supported unit size is 200-256 bytes with 8-byte aligned. Packet size configuration in non-TS mode and data format when ATS timing control is enabled is shown in Figure 7.

Figure 7. Variable Packet Sizing in non-TS Mode



TSIF supports non-TS Byte Size Format

N_in [byte/packet] / Mode of timestamp	200	208	216	224	232	240	248	256
Timestamp enable inside TSIF	○	○	○	○	○	○	○	×
Timestamp disable inside TSIF	○	○	○	○	○	○	○	○

2.4.6 SDRAM Data Storage Format

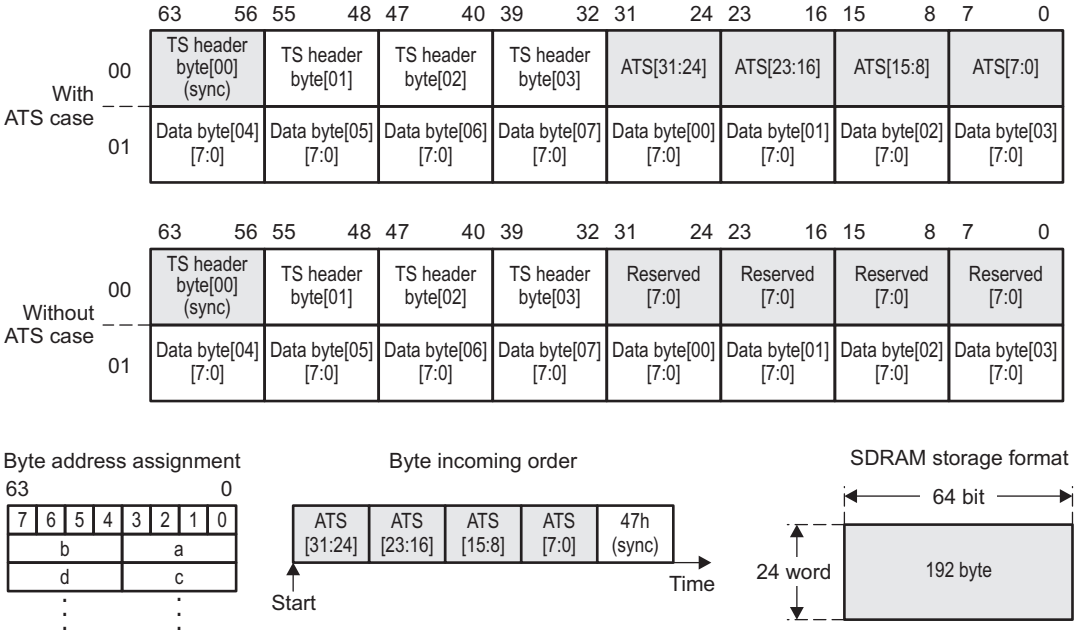
The TSIF module supports two formats for stroing data in SDRAM. The TSIF module can receive and transmit any format of stream data in by-pass mode and can parse MPEG transport stream data. Each data transfer is handled as 192 bytes for one unit access in TS transfer mode and is stored in SDRAM. In non-TS transfer mode, each data transfer is handled as 256 bytes for one unit access (the reason is the unit data size of PS is 2048 bytes/pack). The DMA data bus width is 64 bits (16-bit DDR × 2 with 300 MHZ).

2.4.6.1 32-Bit Little-Endian Mode

The CPU has to process data inside the SDRAM in 32-bit little-endian mode, the TSIF module can store the stream data in 32-bit little-endian format. The format is shown in Figure 8.

As shown in Figure 8, the input data is stored into the MSB side of each 32-bit word as input order. Number *n* of data_byte[*n*] is input and output byte order on MPEG-TS data.

Figure 8. Data Storage Format of 32-Bit Little-Endian Mode on SDRAM



2.4.6.2 64-Bit Big-Endian Mode

The TSIF module can support 64-bit big endian format for SDRAM storage mode. The format is shown in Figure 9.

As shown in Figure 9, the first input data is stored in LSB-sided byte position, and consecutive bytes are stored from LSB-side of the current memory word (1 word = 64 bits). Number *n* of data_byte[*n*] is input and output byte order on MPEG-TS data.

In both 32-bit little-endian mode and 64-bit big-endian mode, bit-level order inside a byte is MSB-first regardless of the storage mode, as shown in Figure 10. In both modes, each byte data is stored in SDRAM in MSB-first order.

Figure 9. Data Storage Format of 64-Bit Big-Endian Mode on SDRAM

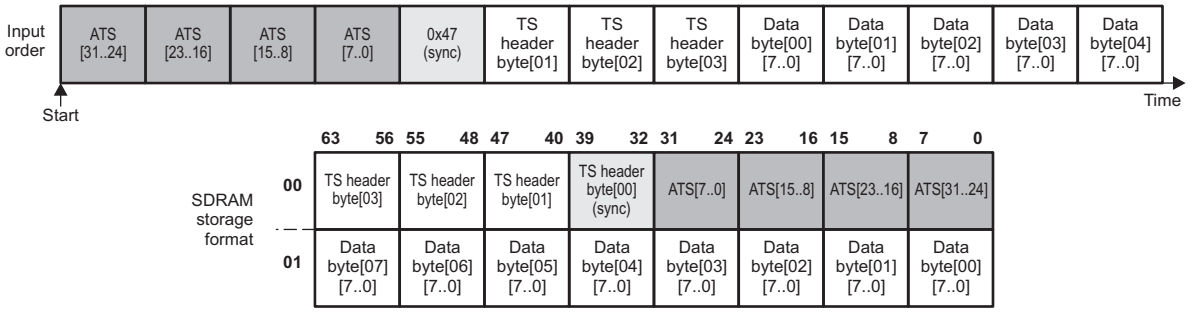
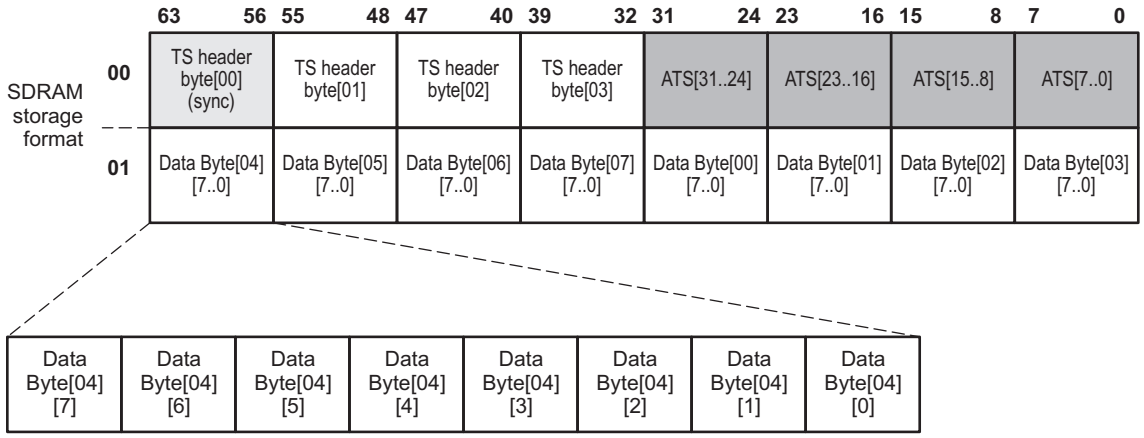


Figure 10. Bit-Level Endian Format in SDRAM Format



2.5 Hardware Reset Considerations

The TSIF hardware reset is controlled by the DM646x DMSoC. See the device-specific data manual for more information.

2.6 Interrupt Support

The TSIF module outputs two interrupts that are routed to the CPU (Table 3). The TSIF interrupt request is generated by the following events:

- Ring Buffer status: SDRAM writing/reading address on Ring Buffer write/read channel has reached to a subtracted pointer address. There are 8 status register bits (RBW*n*_STATUS) for each write Ring Buffer and 1 status register bit (RBR0_FULL_STATUS) for read Ring Buffer.
- STC status: STC counter value has reached the configured value in the STC interrupt entry *n* register (STC_INT*n*). There are 8 status registers for STC interrupts.
- Receive packet error status: Status for receive packet error (RCV_PKT_ERR_STATUS bit).
- PMT detect status: Detection of new PMT data (PMT_DETECT_STATUS bit).
- PAT detect status: Detection of new PAT data (PAT_DETECT_STATUS).
- GOP start status: Detection of GOP start packet (GOP_START_STATUS bit).
- Boundary specific status: Detection of specific word (BOUNDARY_SPECIFIC_STATUS bit) that is implemented at dividing pointer (boundary) of program data in transferred TS data.

See the TSIF interrupt status register (INTSTAT) for interrupt events and the receive packet status register (RX_PKT_STAT) for receive packet status events.

Note: The Ring Buffer Write interrupt is generated when the DMA transfer is completed for the packet that includes the address with subtract value.

The Ring Buffer Read interrupt is generated when the current address reaches the address that is indicated with the subtract address.

Table 3. TSIF Module Interrupts

ARM Event	Acronym	Source
10	TSINT0	TSIF 0
11	TSINT1	TSIF 1

2.7 Emulation Suspend Mode

The TSIF module does support the emulation suspend signal from the CPU. The emulation suspend signal (high indicates that the CPU is suspended) is asserted by the CPU when the CPU is halted with a breakpoint or any other reason during debug.

Note: The emulation suspend signal is multiplexed with CPU signals. When emulation suspend mode is used, it is required to select the ARM or DSP.

3 Use Cases

3.1 Input and Output Interface Structure

The TSIF module has the following three physical and logical interfaces:

- serial interface (data, clock, enable/wait and packet/byte start)
- parallel interface (data, clock, enable/wait, packet/byte start and 8-bit data bus width)
- consequential interface (source and result data of the TSIF shall be stored in SDRAM)

The serial and parallel interfaces are interfaced directly to the host device, and the consequential interface is used to store/read source stream data into/from SDRAM with HPI or PCI modules. In consequential interface, all data paths are driven in same clock (SDRAM clock).

3.1.1 Serial Interface

The serial interface is used to stream directly to/from the external host device with a 1-bit data line and control lines. Two types of interface protocol exist: non-real time (handshake:asynchronous) mode and real time (pushingsynchronous) mode. In the interface protocol, asynchronous means that the transmitted data by the initiator is not always detected by the receiver with zero wait.

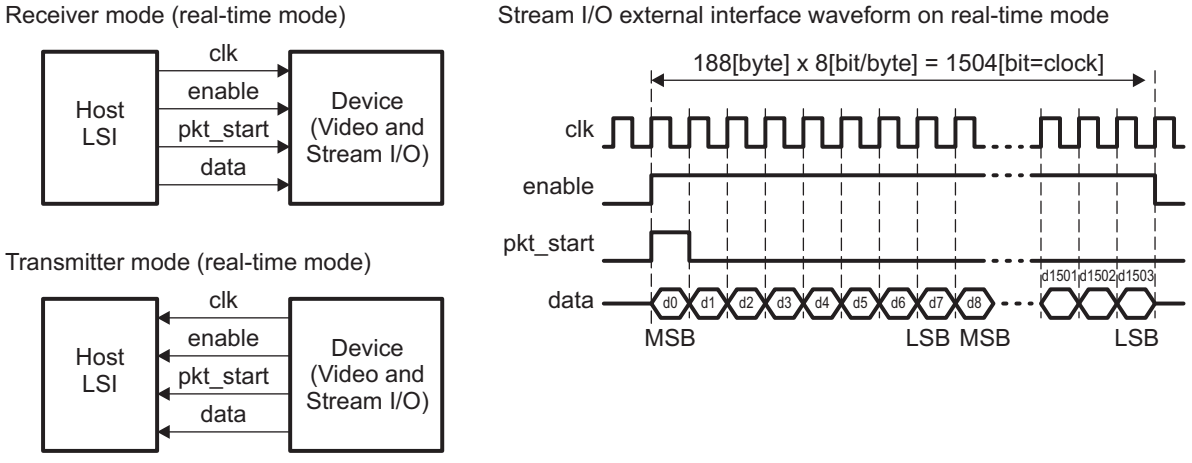
3.1.1.1 Serial Interface Format in Synchronous Mode

In synchronous format, all initiated data is detected by the receiver. Therefore, the host device and the DM646x DMSoC are regarded as synchronous to each other. All signals are generated by a data initiator with a packet start pulse and an enable signal. The enable signal is inactive during data transfer of a packet. In addition, the enable signal sometimes stays active during consecutive packets.

When incoming (outgoing) stream data is not TS data (for example, PES or PS data), then the packet start signal is also asserted similar to the TS case, so that the receiver detects the number of bytes/packets in the received data by counting the start signal pulses and clocks in between.

The physical and logical format of the serial interface in real time (synchronous) mode is shown in Figure 11

Figure 11. Serial Interface Format in Synchronous Mode

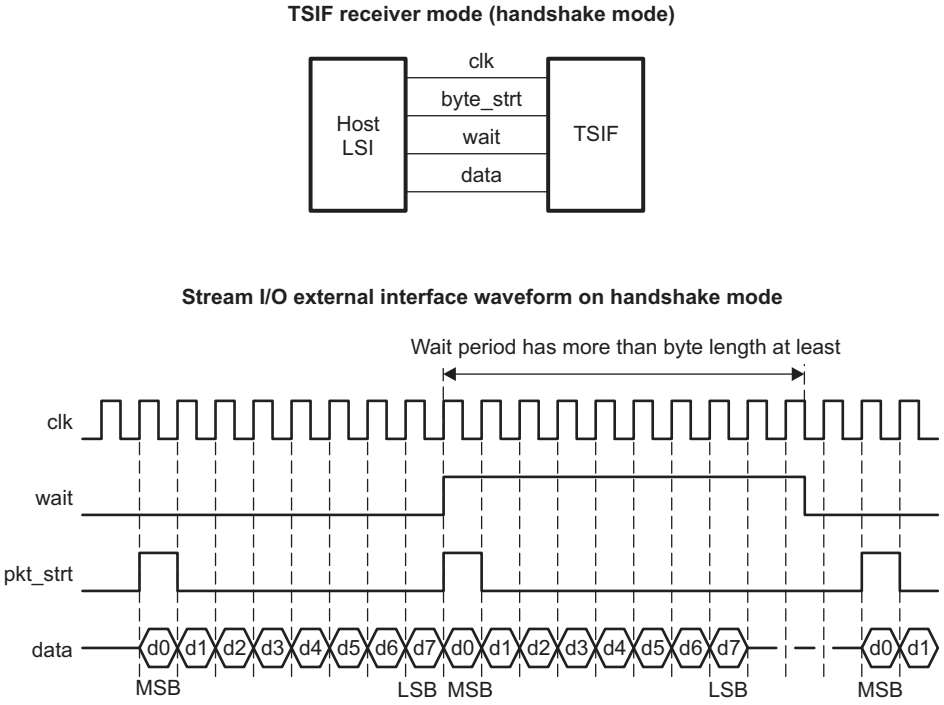


3.1.1.2 Serial Interface Format in Asynchronous Mode

In asynchronous format, the receiver mode and the transmitter mode of the DM646x DMSoC have different formats. In receiver mode, three signals (clock, data, and byte start pulse) are initiated by the external host device while the wait signal is generated by the DM646x DMSoC. Figure 12 shows the logical interface of the receiver mode. When the ring buffer is filled with data, the TSIF module asserts a data write request but is waiting for an acknowledge and when the internal cache is full of data, the wait signal is asserted. The asserted wait signal is detected by the host processor, the host processor stalls data assertion during an activated period of the wait signal.

The physical and logical format of the serial interface input in non-real time (asynchronous) mode is shown in Figure 12.

Figure 12. Serial Interface Input Format in Asynchronous Mode

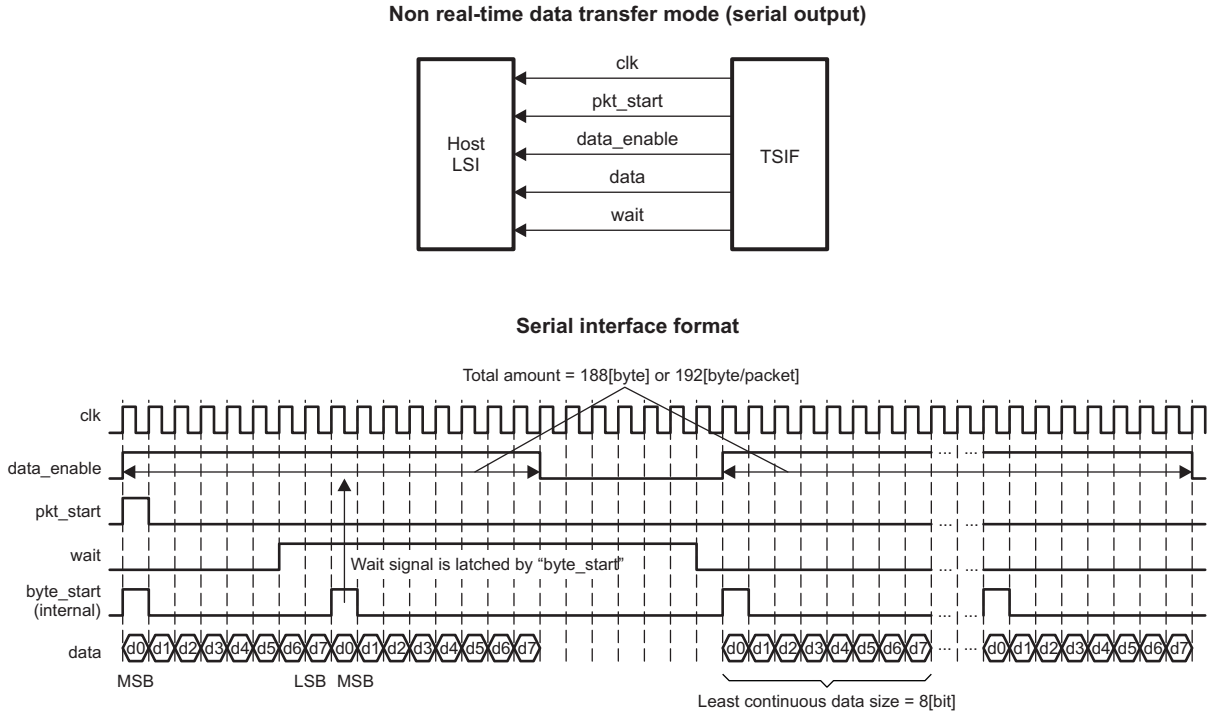


In transmitter mode, the wait signal from the external host device is detected by the TSIF module. The wait signal is latched by the pulse signal that indicates the start of a byte data (byte_start signal for internal use). If the signal is detected by the TSIF module, the module stalls the output after a byte transfer is finished. The minimum unit of data transfer is a byte. All data with a data_enable signal is detected by the external host device.

If you pull down the wait input, the interface format is the same as the synchronous mode. Note that you have to keep the distance between the end of a packet to the start of the next packet as 0/32/64/128 $\times$ 8 clocks.

The physical and logical format of the serial interface output in non-real time (asynchronous) mode is shown in Figure 13.

Figure 13. Serial Interface Output Format in Asynchronous Mode

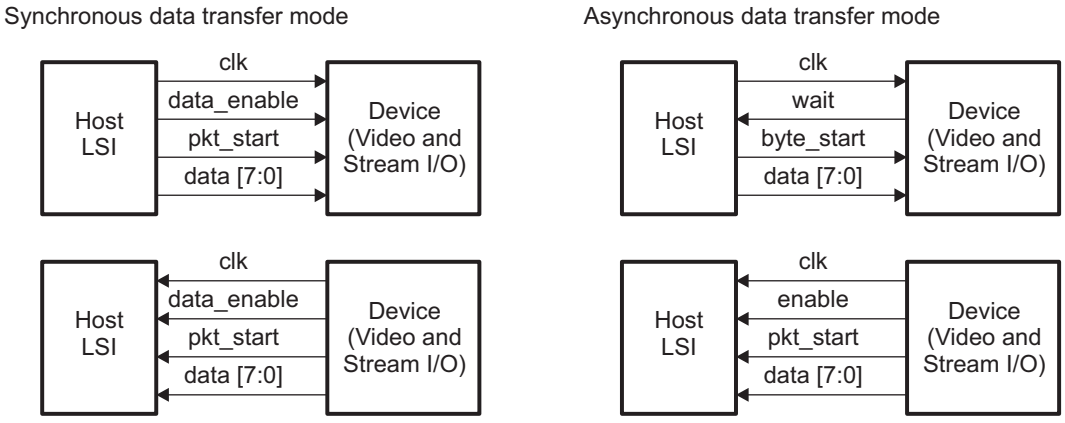


3.1.2 Parallel Interface

The protocol of the parallel interface format is similar to the serial interface. One difference from the serial interface is the data bus width, the serial interface has 1 bit for data but the parallel interface has 8 bits for data.

The physical format of the parallel interface is shown in Figure 14.

Figure 14. Parallel Interface Format



3.2 Packet Data Configuration

Packet data configuration is set in the TSIF control register 0 (CTRL0). Transfer/receiver packet data is required to select the TS mode and ATS mode.

- The TS mode configuration is set by the TX_STREAM_MODE and the RCV_STREAM_MODE bits.
- In TS mode, the packet data ATS mode configuration is set by the TX_ATS_MODE and the RCV_ATS_MODE bits.
- In non-TS mode, the packet data size and ATS mode configuration is required to be set.
  - Packet data size is set by the TX_PKT_SIZE and the RCV_PKT_SIZE bits.
  - ATS mode is set by the TX_ATS_EN and the RCV_ATS_EN bits.

.

Note: When ATS mode is enabled, the non-TS packet size cannot be set to 256 bytes (TX_PKT_SIZE = 7h).

3.3 Transfer/Receiver Interface Configuration

The transfer/receiver interface configuration is set in the TSIF control register 0 (CTRL0).

- Transfer interface and synchronous mode is set by the TX_IF_MODE bit.
- Receiver interface and synchronous mode is set by the RCV_IF_MODE bit.

3.4 PID Control

In order to parse input stream data and divide into data with each PID, the TSIF module can perform PID filter in four modes. Bypass mode is enabled when the PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is cleared to 0. Full manual, semi-automatic mode-A, semi-automatic mode-B, and full automatic mode is enabled when in TS mode and when the PID_FILTER_EN bit is set to 1.

- In manual mode, all PIDs are set with the CPU. PAT/PMTdetection isnotavailable in this mode.
- In semi-automatic mode-A, all PIDs are set with the CPU. PAT/PMTis detected when the program is changed.
- In semi-automatic mode-B, PIDs are set with the CPU andthen all PIDs are updated automatically whenreceiving new PAT/PMT. This mode is supported for partial TS only.
- In full automatic mode,all PIDs are set automatically by detecting PAT/PMT1. This mode is supported for partial TS only.

3.4.1 Bypass Mode

In bypass mode, input data from the host device is stored directory to ring buffer channel 7.

- The PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is cleared to 0.
- Ring buffer write channel 7 registers (RING_BUF_WR_CH7) require configuration.

3.4.2 Full Manual Mode

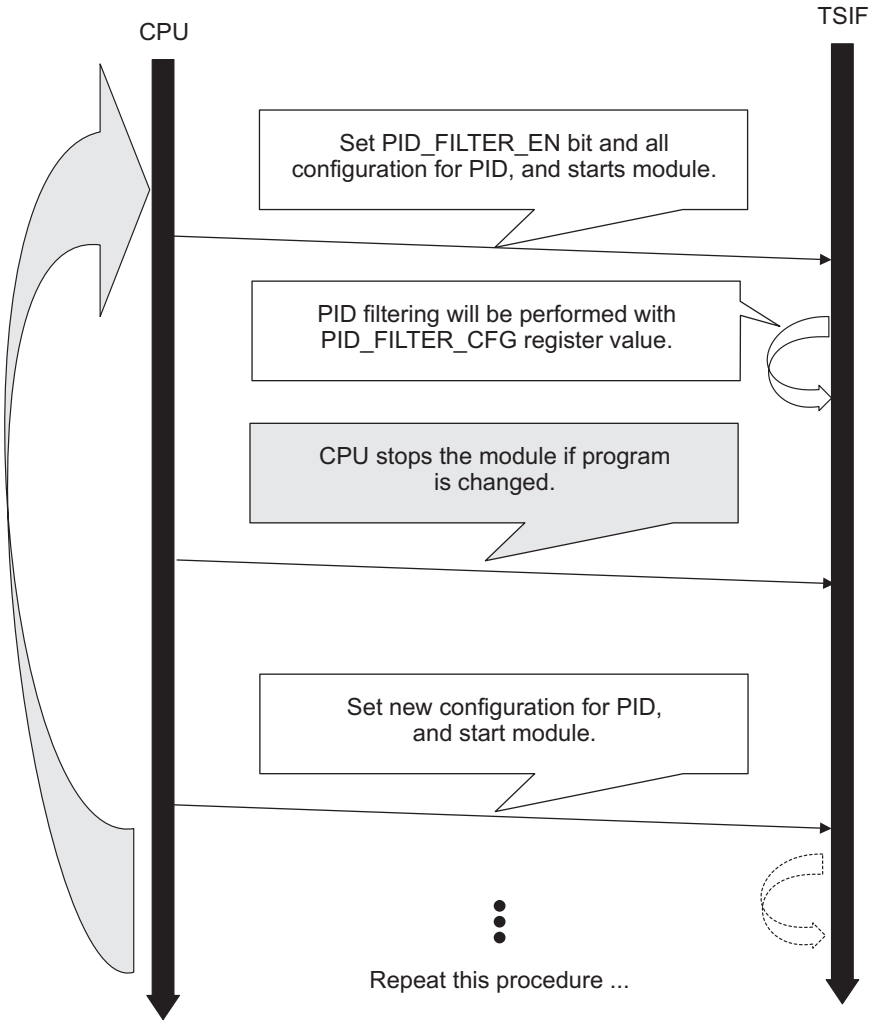
The processing and hardware control flow chart for full manual mode of the PID filter configuration including communication between CPU and TSIF is shown in Figure 15.

The following configurations related to the PID filter are necessary to accomplish full manual mode:

1. PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is set to 1.
2. PID_FILTER_CTL bit in CTRL1 is cleared to 0.
3. PAT_SENSE_EN bit in the PAT sense configuration register (PAT_SEN_CFG) is cleared to 0.
4. PMT_SENSE_EN bit in the PMT sense configuration register (PMT_SEN_CFG) is cleared to 0.
5. PID*n*_FILTER_EN bit in the PID*n* filter configuration register (PID*n*_FILT_CFG) is set to 1.
6. STREAM_TYPE*n* bit in PID*n*_FILT_CFG is set to stream type number.
7. Set ring buffer control.

In this mode, PCR-PID is defined by the register configuration as PMT parsing is done by the CPU. When using the TSIF module in real time mode, this process is mandatory.

Figure 15. Processing on Full Manual Mode of PID Filter



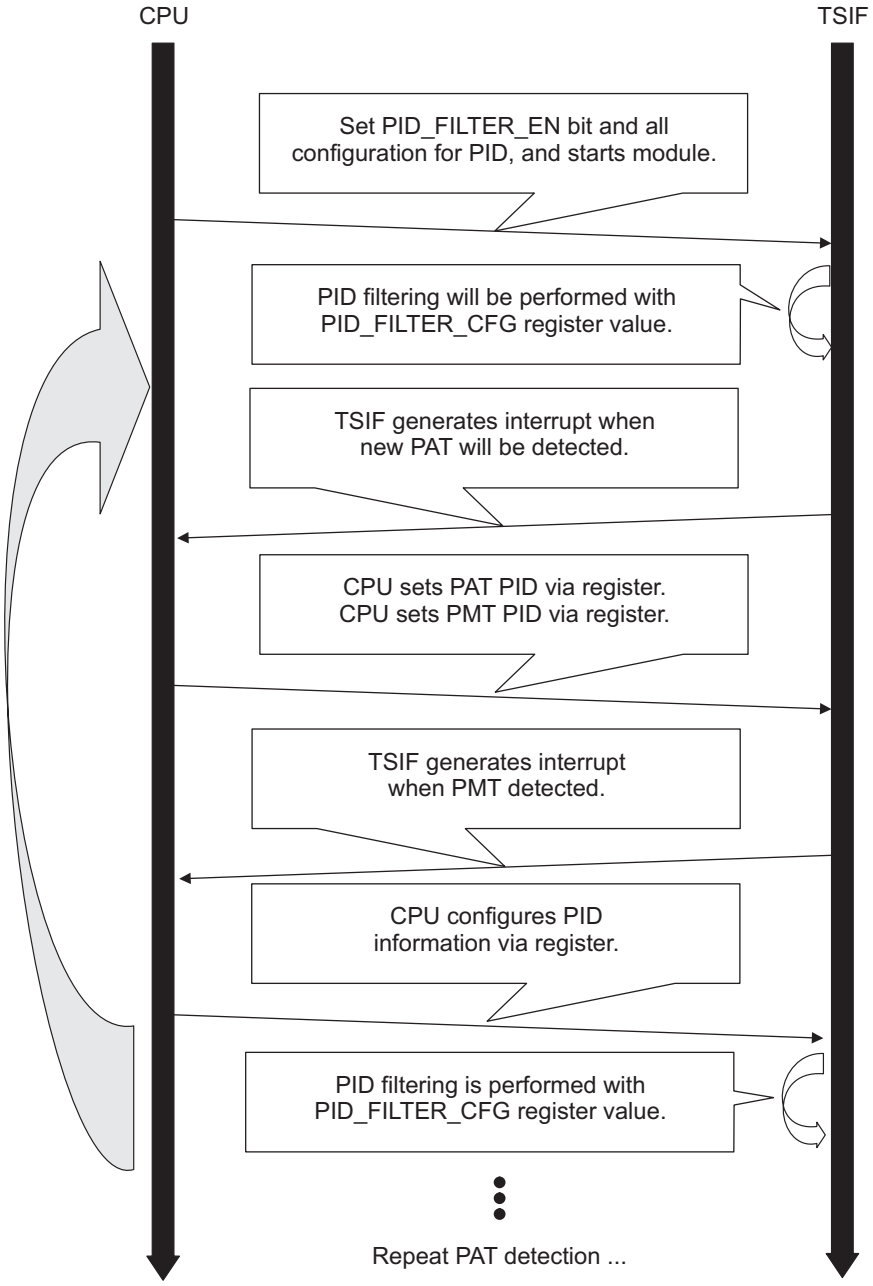
3.4.3 Semi-Automatic Mode-A

The processing and hardware control flow chart for semi-automatic mode-A of the PID filter configuration including communication between CPU and TSIF is shown in Figure 16.

The following configurations related to the PID filter are necessary to accomplish semi-automatic mode-A:

1. PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is set to 1.
2. PID_FILTER_CTL bit in CTRL1 is set to 1.
3. CPU sets PAT_SENSE_EN bit in the PAT sense configuration register (PAT_SEN_CFG) to 1 to detect PAT.
4. PAT_STORE_ADD bit in the PAT store address register (PAT_STR_ADDR) is set to store address for PAT.
5. TSIF module generates an interrupt when PAT is detected.
6. CPU sets PMT_SENSE_EN bit in the PMT sense configuration register (PMT_SEN_CFG) to 1 to detect PMT.
7. PMT_PID bit in PMT_SEN_CFG is configured.
8. PMT_STORE_ADD bit in the PMT store address register (PMT_STR_ADDR) is set to store address for PMT.
9. TSIF module generates an interrupt when PMT is detected.
10. CPU sets all PID*n*_FILTER_EN bits in the PID*n* filter configuration registers (PID*n*_FILT_CFG) to 1.
11. STREAM_TYPE*n* bit in PID*n*_FILT_CFG is set to stream type number.
12. Set ring buffer control.
13. TSIF module continues to monitor PAT. When TSIF module detects new PAT, all of the enables for PMT and other PID are automatically cleared. Then the TSIF module generates an interrupt to the CPU.
14. Procedure repeats from step 6.

Figure 16. Processing on Semi-Automatic Mode-A of PID Filter



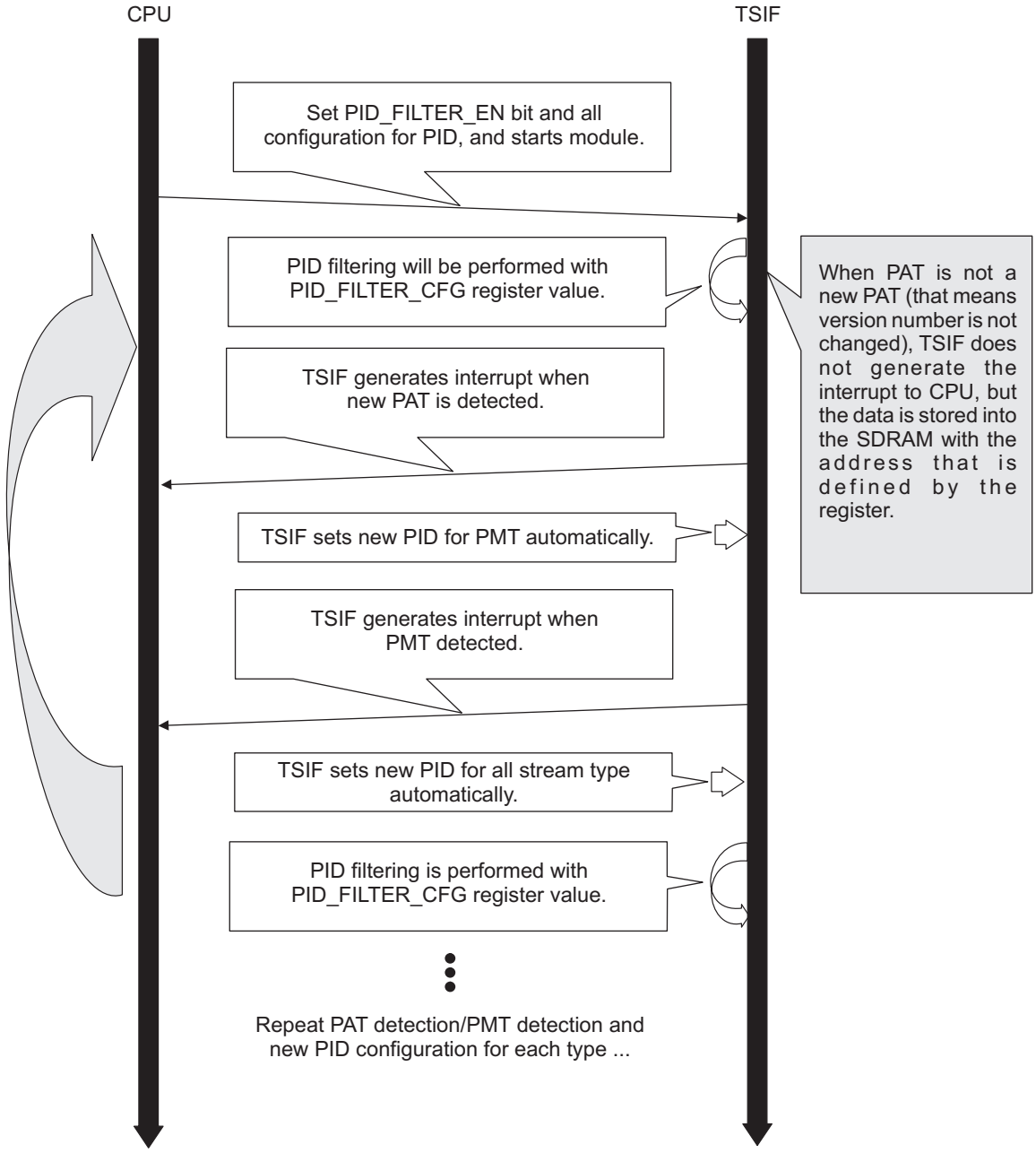
3.4.4 Semi-Automatic Mode-B

The processing and hardware control flow chart for semi-automatic mode-B of the PID filter configuration including communication between CPU and TSIF is shown in Figure 17.

The following configurations related to the PID filter are necessary to accomplish semi-automatic mode-B:

1. PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is set to 1.
2. PID_FILTER_CTL bit in CTRL1 is set to 2h.
3. PID*n*_FILTER_EN bit in the PID*n* filter configuration register (PID*n*_FILT_CFG) is set to 1.
4. STREAM_TYPE*n* bit in PID*n*_FILT_CFG is set to stream type number.
5. PAT_SENSE_EN bit in the PAT sense configuration register (PAT_SEN_CFG) is set to 1.
6. PAT_STORE_ADD bit in the PAT store address register (PAT_STR_ADDR) is set to store address for PAT.
7. PMT_SENSE_EN bit in the PMT sense configuration register (PMT_SEN_CFG) is set to 1.
8. PMT_STORE_ADD bit in the PMT store address register (PMT_STR_ADDR) is set to store address for PMT.
9. TSIF module continues to monitor PAT. When TSIF module detects new PAT:
   a. PMT_PID bit in PMT_SEN_CFG is set to detect PMT.
   b. All of the enables for PMT are automatically cleared.
   c. TSIF module generates an interrupt to the CPU.
10. TSIF module continues to monitor PMT. When TSIF module detects new PMT:
    a. All STREAM_TYPE*n* bits in PID*n*_FILT_CFG are set to stream type number.
    b. All PID*n*_FILTER_EN bits in PID*n*_FILT_CFG are set to 1.
    c. TSIF module generates an interrupt to the CPU.
11. TSIF module continues to monitor PAT. When TSIF module detects new PAT, procedure repeats from step 9.

Figure 17. Processing on Semi-Automatic Mode-B of PID Filter



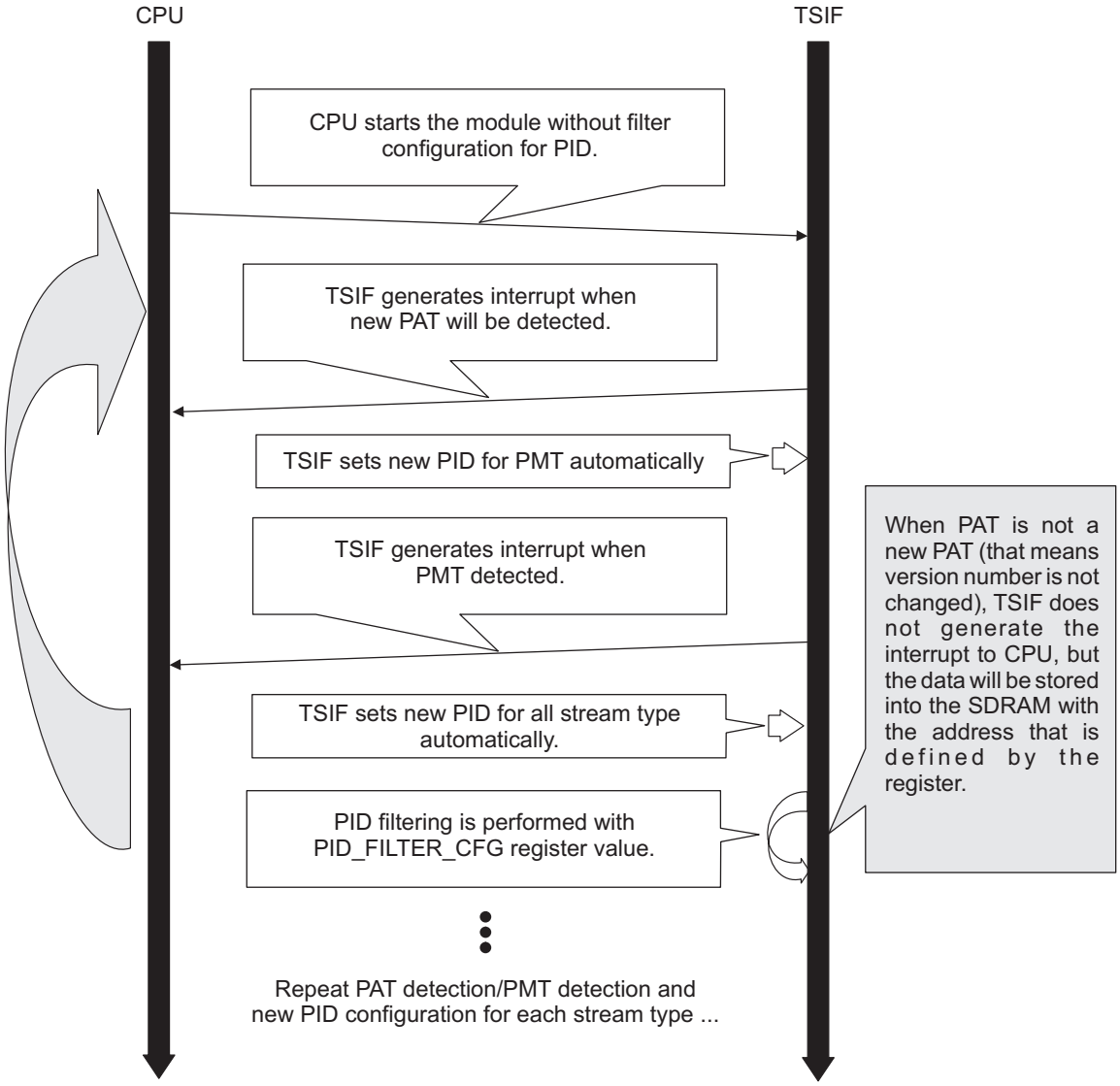
3.4.5 Full Automatic Mode

The processing and hardware control flow chart for full automatic mode of the PID filter configuration including communication between CPU and TSIF is shown in Figure 18.

The following configurations related to the PID filter are necessary to accomplish full automatic mode:

1. PID_FILTER_EN bit in the TSIF control register 1 (CTRL1) is set to 1.
2. PID_FILTER_CTL bit in CTRL1 is set to 3h.
3. CPU sets PAT_SENSE_EN bit in the PAT sense configuration register (PAT_SEN_CFG) to 1 to detect PAT.
4. PAT_STORE_ADD bit in the PAT store address register (PAT_STR_ADDR) is set to store address for PAT.
5. TSIF module continues to monitor PAT. When TSIF module detects new PAT:
   a. PMT_PID bit in the PMT sense configuration register (PMT_SEN_CFG) is set to detect PMT.
   b. All of the enables for PMT are automatically cleared.
   c. TSIF module generates an interrupt to the CPU.
6. TSIF module continues to monitor PMT. When TSIF module detects new PMT:
   a. All STREAM_TYPE*n* bits in PID*n*_FILT_CFG are set to stream type number.
   b. All PID*n*_FILTER_EN bits in PID*n*_FILT_CFG are set to 1.
   c. TSIF module generates an interrupt to the CPU.
7. TSIF module continues to monitor PAT. When TSIF module detects new PAT, procedure repeats from step 5.

Figure 18. Processing on Full Automatic Mode of PID Filter



3.5 Ring Buffer Control

The configuration for the ring buffer controller is shown in Figure 19.

The TSIF module is required to configure the buffer area and the ring buffer interrupt timing for each channel.

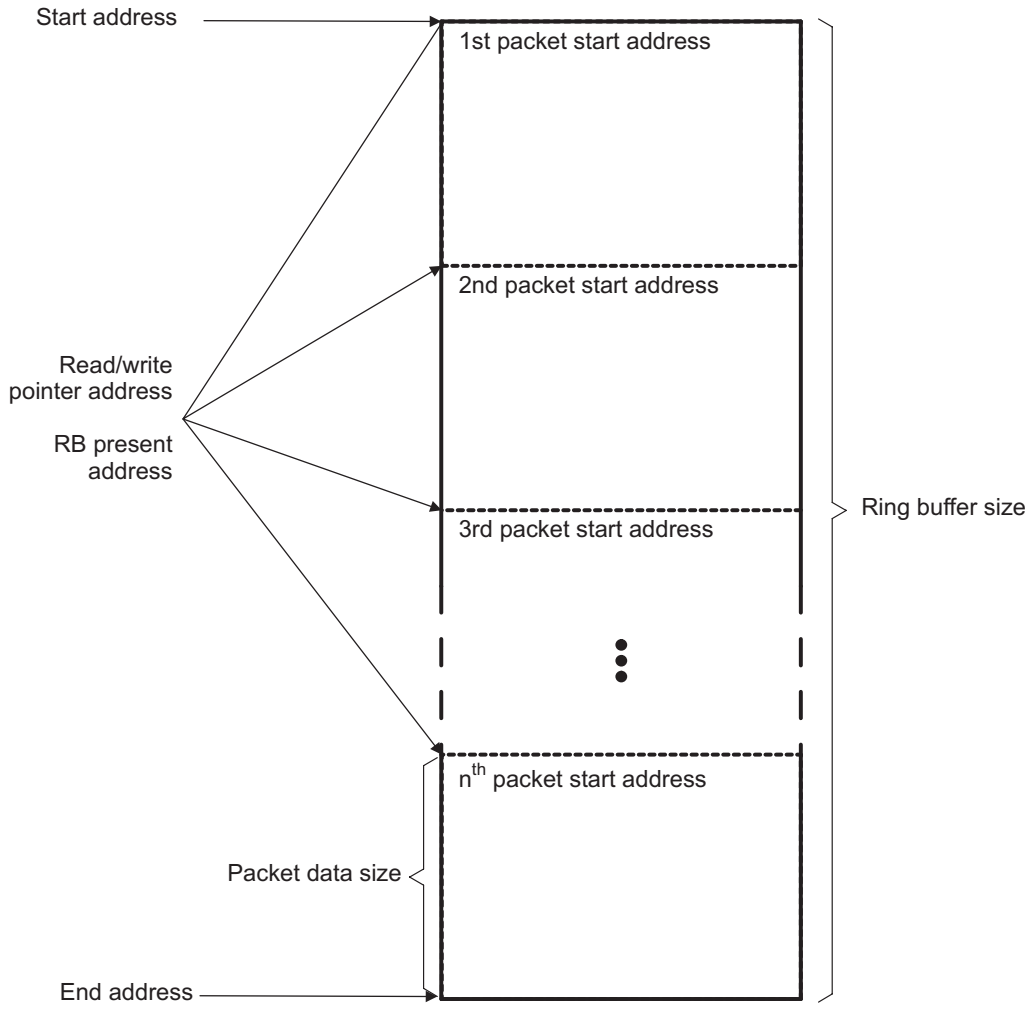
- Buffer area configuration requires setting the buffer start address and end address. Then the buffer size should be set to multiples of the packet size.
  - The start address is set by the RBW*n*_STRT_ADD bit in the write ring buffer channel *n* start address register (RING_BUF_WR_CH*n*_START_ADDR).
  - The end address is set by the RBW*n*_END_ADD bit in the write ring buffer channel *n* end address register (RING_BUF_WR_CH*n*_END_ADDR).
  - When start address and end address are set, the TSIF module is required to stop.

- Ring buffer interrupt timing configuration requires setting the pointer address and subtraction bytes from pointer address.

– The pointer address is set by the RBW*n*_RP_ADD bit in the write ring buffer channel *n* read pointer address register (RING_BUF_WR_CH*n*_RD_POINT_ADDR).
– Subtraction bytes are set by the RBW*n*_SUB_ADD bit in the write ring buffer channel *n* subtraction register (RING_BUF_WR_CH*n*_SUB).
– The subtraction bytes value is required to be less than the total buffer size (end address - start address).

Note: The address registers and subtraction registers should be set for an 8-byte boundary.

Figure 19. Ring Buffer Controller



4 Registers

Table 4 lists the memory-mapped registers for the transport stream interface (TSIF) module. See the device-specific data manual for the memory address of these registers. The module base address is 01C1 3000h for TSIF0 and 01C1 3400h for TSIF1.

Table 4. Transport Stream Interface (TSIF) Module Registers

Offset	Acronym	Register Description	Section
0h	PID	TSIF Peripheral Identification Register	Section 4.1
4h	CTRL0	Control Register 0	Section 4.2
8h	CTRL1	Control Register 1	Section 4.3
Ch	INTEN	Interrupt Enable Register	Section 4.4
10h	INTEN_SET	Interrupt Enable Set Register	Section 4.5
14h	INTEN_CLR	Interrupt Enable Clear Register	Section 4.6
18h	INTSTAT	Interrupt Status Register	Section 4.7
1Ch	INTSTAT_CLR	Interrupt Status Clear Register	Section 4.8
20h	EMU_CTRL	Emulation Control Register	Section 4.9
24h	ASYNC_TX_WAIT	Asynchronous Transmit Wait Time Register	Section 4.10
28h	PAT_SEN_CFG	PAT Sense Configuration Register	Section 4.11
2Ch	PAT_STR_ADDR	PAT Store Address Register	Section 4.12
30h	PMT_SEN_CFG	PMT Sense Configuration Register	Section 4.13
34h	PMT_STR_ADDR	PMT Store Address Register	Section 4.14
38h	BSP_IN	BSP Input Register	Section 4.15
3Ch	BSP_STORE_ADDR	BSP Input Store Address Register	Section 4.16
40h	PCR_SENSE_CFG	PCR Sense Configuration Register	Section 4.17
44h	PID0_FILT_CFG	PID0 Filter Configuration Register	Section 4.18
48h	PID1_FILT_CFG	PID1 Filter Configuration Register	Section 4.18
4Ch	PID2_FILT_CFG	PID2 Filter Configuration Register	Section 4.18
50h	PID3_FILT_CFG	PID3 Filter Configuration Register	Section 4.18
54h	PID4_FILT_CFG	PID4 Filter Configuration Register	Section 4.18
58h	PID5_FILT_CFG	PID5 Filter Configuration Register	Section 4.18
5Ch	PID6_FILT_CFG	PID6 Filter Configuration Register	Section 4.18
60h	BYPASS_CFG	Bypass Mode Configuration Register	Section 4.19
64h	TX_ATS_INIT	Transmit ATS Initialization Register	Section 4.20
68h	TX_ATS_MON	Transmit ATS Monitor Register	Section 4.21
70h	RX_PKT_STAT	Receive Packet Status Register	Section 4.22
80h	STC_INIT_CTRL	STC Initialization Control Register	Section 4.23
84h	STC_INIT_VAL	STC Initialization Value Register	Section 4.24
88h	STC_INT0	STC Interrupt Entry 0 Register	Section 4.25
8Ch	STC_INT1	STC Interrupt Entry 1 Register	Section 4.25
90h	STC_INT2	STC Interrupt Entry 2 Register	Section 4.25
94h	STC_INT3	STC Interrupt Entry 3 Register	Section 4.25
98h	STC_INT4	STC Interrupt Entry 4 Register	Section 4.25
9Ch	STC_INT5	STC Interrupt Entry 5 Register	Section 4.25
A0h	STC_INT6	STC Interrupt Entry 6 Register	Section 4.25
A4h	STC_INT7	STC Interrupt Entry 7 Register	Section 4.25
C0h	WRB_CTRL	Write Ring Buffer Channel Control Register	Section 4.26
C4h	WRB0_STRT_ADDR	Write Ring Buffer Channel 0 Start Address Register	Section 4.27

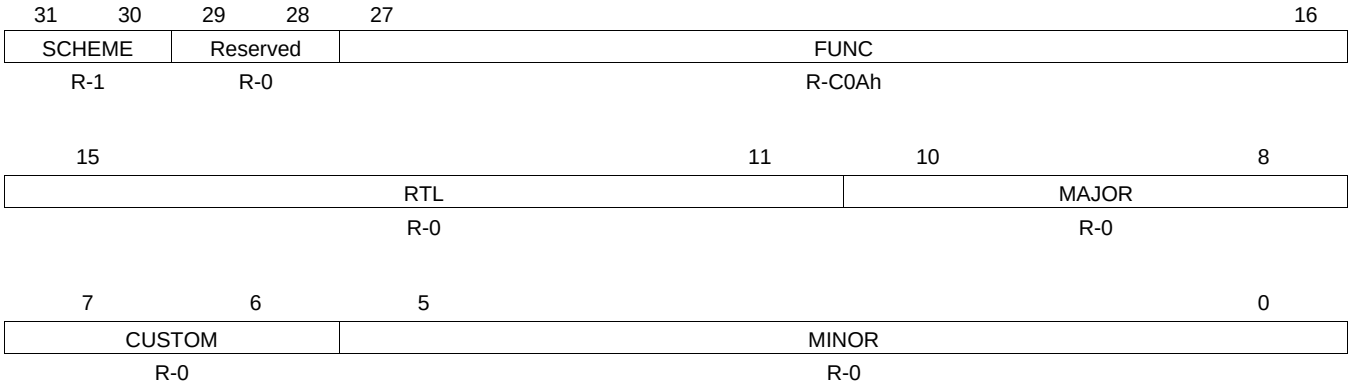
Table 4. Transport Stream Interface (TSIF) Module Registers (continued)

Offset	Acronym	Register Description	Section
C8h	WRB0_END_ADDR	Write Ring Buffer Channel 0 End Address Register	Section 4.28
CCh	WRB0_RDPTR	Write Ring Buffer Channel 0 Read Pointer Register	Section 4.29
D0h	WRB0_SUB	Write Ring Buffer Channel 0 Subtraction Register	Section 4.30
D4h	WRB0_WRPTR	Write Ring Buffer Channel 0 Write Pointer Register	Section 4.31
E0h	WRB1_STRT_ADDR	Write Ring Buffer Channel 1 Start Address Register	Section 4.27
E4h	WRB1_END_ADDR	Write Ring Buffer Channel 1 End Address Register	Section 4.28
E8h	WRB1_RDPTR	Write Ring Buffer Channel 1 Read Pointer Register	Section 4.29
ECh	WRB1_SUB	Write Ring Buffer Channel 1 Subtraction Register	Section 4.30
F0h	WRB1_WRPTR	Write Ring Buffer Channel 1 Write Pointer Register	Section 4.31
100h	WRB2_STRT_ADDR	Write Ring Buffer Channel 2 Start Address Register	Section 4.27
104h	WRB2_END_ADDR	Write Ring Buffer Channel 2 End Address Register	Section 4.28
108h	WRB2_RDPTR	Write Ring Buffer Channel 2 Read Pointer Register	Section 4.29
10Ch	WRB2_SUB	Write Ring Buffer Channel 2 Subtraction Register	Section 4.30
110h	WRB2_WRPTR	Write Ring Buffer Channel 2 Write Pointer Register	Section 4.31
120h	WRB3_STRT_ADDR	Write Ring Buffer Channel 3 Start Address Register	Section 4.27
124h	WRB3_END_ADDR	Write Ring Buffer Channel 3 End Address Register	Section 4.28
128h	WRB3_RDPTR	Write Ring Buffer Channel 3 Read Pointer Register	Section 4.29
12Ch	WRB3_SUB	Write Ring Buffer Channel 3 Subtraction Register	Section 4.30
130h	WRB3_WRPTR	Write Ring Buffer Channel 3 Write Pointer Register	Section 4.31
140h	WRB4_STRT_ADDR	Write Ring Buffer Channel 4 Start Address Register	Section 4.27
144h	WRB4_END_ADDR	Write Ring Buffer Channel 4 End Address Register	Section 4.28
148h	WRB4_RDPTR	Write Ring Buffer Channel 4 Read Pointer Register	Section 4.29
14Ch	WRB4_SUB	Write Ring Buffer Channel 4 Subtraction Register	Section 4.30
150h	WRB4_WRPTR	Write Ring Buffer Channel 4 Write Pointer Register	Section 4.31
160h	WRB5_STRT_ADDR	Write Ring Buffer Channel 5 Start Address Register	Section 4.27
164h	WRB5_END_ADDR	Write Ring Buffer Channel 5 End Address Register	Section 4.28
168h	WRB5_RDPTR	Write Ring Buffer Channel 5 Read Pointer Register	Section 4.29
16Ch	WRB5_SUB	Write Ring Buffer Channel 5 Subtraction Register	Section 4.30
170h	WRB5_WRPTR	Write Ring Buffer Channel 5 Write Pointer Register	Section 4.31
180h	WRB6_STRT_ADDR	Write Ring Buffer Channel 6 Start Address Register	Section 4.27
184h	WRB6_END_ADDR	Write Ring Buffer Channel 6 End Address Register	Section 4.28
188h	WRB6_RDPTR	Write Ring Buffer Channel 6 Read Pointer Register	Section 4.29
18Ch	WRB6_SUB	Write Ring Buffer Channel 6 Subtraction Register	Section 4.30
190h	WRB6_WRPTR	Write Ring Buffer Channel 6 Write Pointer Register	Section 4.31
1A0h	WRB7_STRT_ADDR	Write Ring Buffer Channel 7 Start Address Register	Section 4.27
1A4h	WRB7_END_ADDR	Write Ring Buffer Channel 7 End Address Register	Section 4.28
1A8h	WRB7_RDPTR	Write Ring Buffer Channel 7 Read Pointer Register	Section 4.29
1ACh	WRB7_SUB	Write Ring Buffer Channel 7 Subtraction Register	Section 4.30
1B0h	WRB7_WRPTR	Write Ring Buffer Channel 7 Write Pointer Register	Section 4.31
1C0h	RRB_CTRL	Read Ring Buffer Channel Control Register	Section 4.32
1C4h	RRB_STRT_ADDR	Read Ring Buffer Channel Start Address Register	Section 4.33
1C8h	RRB_END_ADDR	Read Ring Buffer Channel End Address Register	Section 4.34
1CCh	RRB_WRPTR	Read Ring Buffer Channel Write Pointer Register	Section 4.35
1D0h	RRB_SUB	Read Ring Buffer Channel Subtraction Register	Section 4.36
1D4h	RRB_RDPTR	Read Ring Buffer Channel Read Pointer Register	Section 4.37
1D8h	PKT_CNT	Packet Counter Value Register	Section 4.38

4.1 TSIF Peripheral Identification Register (PID)

The TSIF peripheral identification register (PID) is shown in Figure 20 and described in Table 5.

Figure 20. TSIF Peripheral Identification Register (PID)



LEGEND: R = Read only; -*n* = value after reset

Table 5. TSIF Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	1	Used to distinguish between old scheme and current. Fixed to 01.
29-28	Reserved	0	Reserved
27-16	FUNC	0-FFFh	Function indicates a software-compatible module family.
15-11	RTL	0	Indicates RTL version. Fixed to 0.
10-8	MAJOR	0	Major revision number. Fixed to 0.
7-6	CUSTOM	0	Indicates a special version for a particular device. Fixed to 0.
5-0	MINOR	0	Minor revision number. Fixed to 0.

4.2 TSIF Control Register 0 (CTRL0)

The TSIF control register 0 (CTRL0) is shown in Figure 21 and described in Table 6.

Figure 21. TSIF Control Register 0 (CTRL0)

31	30 28	27	26 24
TX_CLK_INV	Reserved	TX_ATS_EN	TX_PKT_SIZE
R/W-0	R-0	R/W-0	R/W-0

23 22	21	20	19 18	17	16
TX_ATS_MODE	TX_STREAM_MODE	TX_PKTSTRT_WIDTH	TX_IF_MODE	TX_DMA_CTL	TX_CTL
R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

15 12	11	10 8
Reserved	RCV_ATS_EN	RCV_PKT_SIZE
R-0	R/W-0	R/W-0

7 6	5	4	3 2	1	0
RCV_ATS_MODE	RCV_STREAM_MODE	RCV_INPUT_PORT	RCV_IF_MODE	RCV_DMA_CTL	RCV_CTL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 6. TSIF Control Register 0 (CTRL0) Field Descriptions

Bit	Field	Value	Description
31	TX_CLK_INV		Controls output timing of transmit clock. This bit should not be changed when transmit function is enabled.
		0	Data outputs at falling edge of transmit clock.
		1	Data outputs at rising edge of transmit clock.
30-28	Reserved	0	Reserved
27	TX_ATS_EN		This bit is effective when TX_STREAM_MODE = 0 (non-TS mode), and enables time stamp controls with ATS in non-TS packet.
		0	Time stamp controls with ATS in non-TS packet is disabled.
		1	Time stamp controls with ATS in non-TS packet is enabled.
26-24	TX_PKT_SIZE	0-7h	This bit is effective when TX_STREAM_MODE = 0 (non-TS mode), and defines unit data size in non-TS mode. If you need to control the output timing by TX_ATS_EN = 1, you can not set this bit to 256 bytes for non-TS packet size.
		0	200 bytes per packet
		1h	208 bytes per packet
		2h	216 bytes per packet
		3h	224 bytes per packet
		4h	232 bytes per packet
		5h	240 bytes per packet
		6h	248 bytes per packet
		7h	256 bytes per packet

Table 6. TSIF Control Register 0 (CTRL0) Field Descriptions (continued)

Bit	Field	Value	Description
23-22	TX_ATS_MODE	0-3h	Defines a method of processing ATS for outgoing TS packet data. This bit is effective when the TX_STREAM_MODE bit is activated for TS mode (bit = 1). Each packet data is generated by ARM processor with ATS at the beginning of the packet.
		0	Outgoing packet has 188 byte. The hardware checks ATS value in order to adjust assertion timing and remove ATS RCV_INPUT_PORT.
		1h	Outgoing packet has 192 byte. The hardware checks ATS value in order to adjust assertion timing.
		2h-3h	Reserved
21	TX_STREAM_MODE		Defines if output stream data is based on TS (MPEG transport stream) format. If you define non-TS format in this bit, no TS-related function (timing alignment with monitoring ATS value in synchronous data transfer mode) is activated in receiver function. Data transfer unit is different from each other; in TS mode, the hardware transfers 192 bytes for a packet (transport unit size; configured by the TX_ATS_MODE bit). But in non-TS mode, the hardware transfers 256 bytes for a transport unit size.
		0	Non-TS mode (Any type of data will come; acts as universal mode. Data size should be defined by the TX_PKT_SIZE bit.)
		1	TS mode (monitoring sync byte: 188 or 192 bytes/unit transport).
20	TX_PKTSTRT_WIDTH		Controls pulse width of Packet start (TSIF_data_strt_o) in serial mode.
		0	1 cycle width of STR_TX_CLK_O
		1	8 cycle width of STR_TX_CLK_O
19-18	TX_IF_MODE	0-3h	Selects interface mode of data transmitter from following three modes. You have to take alignment of performance mode between receiver and transmitter, if you decide to use serial interface on both of receiver and transmitter.
		0	Serial interface with synchronous interface.
		1h	Serial interface with asynchronous interface.
		2h	Parallel (8 bit/clock transfer mode) with synchronous interface.
		3h	Parallel (8 bit/clock transfer mode) with asynchronous interface.
17	TX_DMA_CTL		Controls DMA access used in case of data transfer from the DM646x DMSoC to external host. You should control this bit with the TX_CTL bit if you would like to read data from SDRAM to external host.
		0	Internal DMA read access is disabled.
		1	Internal DMA read access is enabled.
16	TX_CTL		Controls transmitter of the TSIF module. If you write 1 to this bit when the bit is 0, the transmitter module starts to transmit output stream data to external host. If you write 0 to this bit when the bit is 1, the transmitter module starts to stall. SDRAM access is started by another register.
		0	TSIF transmitter to be inactivated.
		1	TSIF transmitter to be activated.
15-12	Reserved	0	Reserved
11	RCV_ATS_EN		This bit is effective when RCV_STREAM_MODE = 0 (non-TS mode), and enables time stamp addition of ATS value in non-TS packet.
		0	Time stamp addition of ATS value in non-TS packet is disabled.
		1	Time stamp addition of ATS value in non-TS packet is enabled.
10-8	RCV_PKT_SIZE	0-7h	This bit is effective when RCV_STREAM_MODE = 0 (non-TS mode), and defines unit data size for receiving non-TS data. If you need to control the output timing by RCV_ATS_EN = 1, you can not set this bit to 256 bytes for non-TS packet size.
		0	200 bytes per packet
		1h	208 bytes per packet
		2h	216 bytes per packet
		3h	224 bytes per packet
		4h	232 bytes per packet
		5h	240 bytes per packet
		6h	248 bytes per packet
		7h	256 bytes per packet

Table 6. TSIF Control Register 0 (CTRL0) Field Descriptions (continued)

Bit	Field	Value	Description
7-6	RCV_ATS_MODE	0-3h	Defines a method of processing ATS for incoming TS packet data. This bit is effective when the RCV_INPUT_PORT bit is activated for TS mode.
		0	Do nothing with incoming data (192 byte)
		1h	Add reserved data to incoming data (188 byte)
		2h	Change ATS of incoming data (192 byte)
		3h	Reserved
5	RCV_STREAM_MODE		Defines if the input stream data is based on TS (MPEG transport stream) format. If you define non-TS format in this bit, no PID filter and no TS-related function is activated in receiver function. Transport unit size varies from selected mode; in non-TS mode, data transport unit is 256 bytes fixed. But in TS-mode, data transport unit size is 188 bytes or 192 bytes, which is configured in the RCV_ATS_MODE bit.
		0	Non-TS mode (any type of data will come; acts as universal mode. Data size should be defined by the RCV_PKT_SIZE bit.)
		1	TS mode (monitoring sync byte: 188 or 192 bytes/unit transport).
4	RCV_INPUT_PORT		Controls where input stream data comes from. If you select stream interface (bit = 0) as input port of source stream, the RCV_IF_MODE bit configures interface mode.
			If you use PCI or HPI module as stream receiver, this bit should be configured to 1.
		0	Stream source data comes from stream interface (defined by RCV_IF_MODE bit).
		1	Stream source data comes from DMA interface (comes from PCI/HPI).
3-2	RCV_IF_MODE	0-3h	Selects interface mode of data receiver from following three modes. You have to take alignment of performance mode between receiver and transmitter, if you decide to use serial interface on both of receiver and transmitter. This bit is effective only if the RCV_INPUT_PORT bit is 0; if the RCV_INPUT_PORT bit is 1, this bit has no meaning.
		0	Serial synchronous interface
		1h	Serial asynchronous interface
		2h	Parallel (8 bit/clock transfer mode) synchronous interface
		3h	Parallel (8 bit/clock transfer mode) asynchronous interface
1	RCV_DMA_CTL		Controls DMA access used in case of data transfer from external host to the DM646x DMSoC. You should control this bit with the RCV_CTL bit if you would like to write all data from external host into SDRAM.
			This bit is effective only if the RCV_INPUT_PORT bit is 0 (stream interfacing mode). If the RCV_INPUT_PORT bit is 1 (HPI/PCI interfacing mode), this value should be ignored.
		0	Internal DMA write access is disabled (no data writing onto SDRAM).
		1	Internal DMA write access is enabled (data writing onto SDRAM).
0	RCV_CTL		Controls receiver of the TSIF module. If you write 1 to this bit when the bit is 0, the receiver module starts to receive input stream data from outside the module. If you write 0 to this bit when the bit is 1, the receiver module shall stall. SDRAM access is started by another register.
			If you would like to start the module with SDRAM access, set RCV_DMA_CTL = 1. Otherwise, no access to SDRAM will be asserted from TSIF module in stream interfacing mode (in PCI/HPI mode, normal access can be started without any effect of the RCV_DMA_CTL bit.
		0	TSIF receiver function is inactivated.
		1	TSIF receiver function is activated.

4.3 TSIF Control Register 1 (CTRL1)

The TSIF control register 1 (CTRL1) is shown in Figure 22 and described in Table 7.

Figure 22. TSIF Control Register 1 (CTRL1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
ARM_INT_EN	ENDIAN_CTL	Reserved	CRC_FLT_EN	Reserved		TPEI_FLT_EN	SBYTE_FLT_EN
R/W-0	R/W-0	R-0	R/W-0	R-0		R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved		GOP_DETECT_EN	STREAM_BNDRY_CTL	PID_FILTER_EN	PID_FILTER_CTL		
R-0		R/W-0	R/W-0	R/W-0	R/W-0		

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 7. TSIF Control Register 1 (CTRL1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15	ARM_INT_EN		Enables interrupt to the ARM due to the interrupt conditions indicated by the bits set in the TSIF interrupt status register (INTSTAT).
		0	Interrupt is disabled.
		1	Interrupt is enabled.
14	ENDIAN_CTL		Selects storage data format into SDRAM. The details on each format are described in Section 2.4.6.
		0	32-bit little-endian mode
		1	64-bit big-endian mode
13	Reserved	0	Reserved
12	CRC_FLT_EN		Enables CRC check for PAT/PMT parsing when PID_FILTER_EN is enabled. The error packet will be ignored.
		0	CRC FLT is disabled.
		1	CRC FLT is enabled.
11-10	Reserved	0	Reserved
9	TPEI_FLT_EN		Enables filtering transport error indicator = 1 in TS header when PID_FILTER_EN is enabled. The error packet will be ignored.
		0	TPEI FLT is disabled.
		1	TPEI FLT is enabled.
8	SBYTE_FLT_EN		Enables filtering sync byte error in TS header when PID_FILTER_EN is enabled. The error packet will be ignored.
		0	SBYTE FLT is disabled.
		1	SBYTE FLT is enabled.
7-6	Reserved	0	Reserved
5	GOP_DETECT_EN		Enables detection of GOP start packet with following conditions. This bit is effective when PID_FILTER_EN is enabled.
		0	Payload_unit_start_indicator = 1
		1	Transport_priority = 1

Table 7. TSIF Control Register 1 (CTRL1) Field Descriptions (continued)

Bit	Field	Value	Description
4	STREAM_BNDRY_CTL		Selects controlling method at stream boundary between consecutive two programs that have different profile for each other. If you select specific word for this control (bit = 1), you have to configure a register to define PID value of the specific packet. This bit is effective when PID_FILTER_EN is enabled.
		0	Use DIT to detect stream boundary.
		1	Use user-specific packet to detect stream boundary.
3	PID_FILTER_EN		Enables PID filter. This bit is effective if the RCV_STREAM_MODE bit in the TSIF control register 0 (CTRL0) is set to 1; if the RCV_STREAM_MODE bit is 0, this bit has no effect.
		0	PID filter is disabled (bypass mode is activated). In this mode, none of the PID filters are used. The hardware holds the register value even while the ARM enables/disables the interrupt.
		1	PID filter is enabled (normal mode with PID filter).
2-0	PID_FILTER_CTL	0-7h	Selects PID filter performance mode. In order to parse input stream data and divide into data with each PID, this module can perform PID filter in four modes:
		0	Full manual mode
			PID filter with PID configuration from external host via ARM (no necessity to decode PAT/PMT; all configurations about PID to be transcoded and necessary information is provided from external host).
		1h	Semi-automatic mode-A
			First, the hardware decodes PAT/PMT and store into SDRAM area specified by ARM. Then: 1. ARM reads the stored PAT data, selects one PMT_PID, and configures the module to filter PMT. The module asserts interrupt, if new PAT comes. 2. After detecting PMT, table data is stored into SDRAM (in this case, the module also asserts interrupt pulse to ARM). ARM reads PMT, and configured PID0~5 filter in this module. ARM has to enable the hardware. 3. Once detecting discontinuity code (or other specific code that indicates boundary of plural program inserted in a TS data), the hardware asserts interrupt pulse to ARM and returns to state in which the module is waiting for coming next PAT.
		2h	Semi-automatic mode-B
			First, the ARM configures PAT/PMT information about starting packet of first program and activates the hardware. Then: 1. Once ARM enables hardware (bits[1-0] are 11b), the hardware module starts to parse input stream data according to configured PID. 2. If hardware detects change of PID by detecting change of PAT/PMT, hardware automatically changes internal PAT/PMT table and also PID filter table. This reflection is carried out with monitoring stream type (if different PID is detected in same stream type, the table value for the PID is replaced).
		3h	Full-automatic mode
			If only one program data that consists of one video, one audio, and other sub-streams exists in transferred TS data, hardware decodes PAT/PMT and stores into internal register. Hardware then performs PID filtering with registered PID data decoded from PAT/PMT. Later method is same as semi-automatic mode-B method.
		4h-7h	Reserved

4.4 TSIF Interrupt Enable Register (INTEN)

The TSIF interrupt enable register (INTEN) is shown in Figure 23 and described in Table 8.

The bits in INTEN enable assertion of the interrupt to the ARM. In order to enable each interrupt condition and assert the interrupt, configure bit[*n*] in INTEN and in the TSIF interrupt enable set register (INTEN_SET) to 1. To stall the interrupt temporarily, configure bit[*n*] in the TSIF interrupt enable clear register (INTEN_CLR) to 1.

Detail interrupt condition is described in the TSIF interrupt status register (INTSTAT).

Figure 23. TSIF Interrupt Enable Register (INTEN)

31							24
Reserved							
R-0							

23	22	21	20	19	18	17	16
STC_07_INTEN	STC_06_INTEN	STC_05_INTEN	STC_04_INTEN	STC_03_INTEN	STC_02_INTEN	STC_01_INTEN	STC_00_INTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
RBW7_INTEN	RBW6_INTEN	RBW5_INTEN	RBW4_INTEN	RBW3_INTEN	RBW2_INTEN	RBW1_INTEN	RBW0_INTEN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved	RCV_PKTERR _INTEN	Reserved	RBR0_INTEN	PMT_DETECT _INTEN	PAT_DETECT _INTEN	GOP_START _INTEN	BOUNDARY _SPECIFIC _INTEN
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. TSIF Interrupt Enable Register (INTEN) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	STC_07_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
22	STC_06_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
21	STC_05_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
20	STC_04_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
19	STC_03_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
18	STC_02_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

Table 8. TSIF Interrupt Enable Register (INTEN) Field Descriptions (continued)

Bit	Field	Value	Description
17	STC_01_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
16	STC_00_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
15	RBW7_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
14	RBW6_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
13	RBW5_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
12	RBW4_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
11	RBW3_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
10	RBW2_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
9	RBW1_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
8	RBW0_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
7	Reserved	0	Reserved
6	RCV_PKT_ERR		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
5	Reserved	0	Reserved
4	RBR0_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
3	PMT_DETECT_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
2	PAT_DETECT_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
1	GOP_START_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

Table 8. TSIF Interrupt Enable Register (INTEN) Field Descriptions (continued)

Bit	Field	Value	Description
0	BOUNDARY_SPECIFIC_INTEN		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

4.5 TSIF Interrupt Enable Set Register (INTEN_SET)

The TSIF interrupt enable set register (INTEN_SET) is shown in Figure 24 and described in Table 9.

The bits in INTEN_SET enable assertion of the interrupt to the ARM when the corresponding interrupt condition occurs. The hardware holds the register value even while the ARM enables/disables the interrupt.

INTEN_SET[*n*] is effective if the corresponding bit[*n*] in the TSIF interrupt enable register (INTEN) is set; otherwise, any configuration should be ignored.

Figure 24. TSIF Interrupt Enable Set Register (INTEN_SET)

31	24
Reserved	
R-0	

23	22	21	20	19	18	17	16
STC_07_INTEN_SET	STC_06_INTEN_SET	STC_05_INTEN_SET	STC_04_INTEN_SET	STC_03_INTEN_SET	STC_02_INTEN_SET	STC_01_INTEN_SET	STC_00_INTEN_SET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
RBW7_INTEN_SET	RBW6_INTEN_SET	RBW5_INTEN_SET	RBW4_INTEN_SET	RBW3_INTEN_SET	RBW2_INTEN_SET	RBW1_INTEN_SET	RBW0_INTEN_SET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
Reserved	RCV_PKTERR_INTEN_SET	Reserved	RBR0_INTEN_SET	PMT_DETECT_INTEN_SET	PAT_DETECT_INTEN_SET	GOP_START_INTEN_SET	BOUNDARY_SPECIFIC_INTEN_SET
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. TSIF Interrupt Enable Set Register (INTEN_SET) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	STC_07_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
22	STC_06_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
21	STC_05_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

Table 9. TSIF Interrupt Enable Set Register (INTEN_SET) Field Descriptions (continued)

Bit	Field	Value	Description
20	STC_04_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
19	STC_03_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
18	STC_02_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
17	STC_01_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	INTERRUPT enable
16	STC_00_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
15	RBW7_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
14	RBW6_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
13	RBW5_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
12	RBW4_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
11	RBW3_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
10	RBW2_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
9	RBW1_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
8	RBW0_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
7	Reserved	0	Reserved
6	RCV_PKTERR_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
5	Reserved	0	Reserved
4	RBR0_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

Table 9. TSIF Interrupt Enable Set Register (INTEN_SET) Field Descriptions (continued)

Bit	Field	Value	Description
3	PMT_DETECT_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
2	PAT_DETECT_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
1	GOP_START_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable
0	BOUNDARY_SPECIFIC_INTEN_SET		Interrupt condition and detection enable.
		0	Interrupt disable
		1	Interrupt enable

4.6 TSIF Interrupt Enable Clear Register (INTEN_CLR)

The TSIF interrupt enable clear register (INTEN_CLR) is shown in Figure 25 and described in Table 10.

The bits in INTEN_CLR disable assertion of the interrupt to the ARM. In order to disable each interrupt condition temporarily (even if bit[*n*] in the TSIF interrupt enable register (INTEN) stays 1), configure INTEN_CLR[*n*] to 1. The registers cannot be read by ARM.

INTEN_CLR[*n*] is effective if the corresponding bit[*n*] in the TSIF interrupt enable register (INTEN) and in the TSIF interrupt enable set register (INTEN_SET) are set; otherwise, any configuration should be ignored.

Figure 25. TSIF Interrupt Enable Clear Register (INTEN_CLR)

31	30	29	28	27	26	25	24
Reserved							
R-0							

23	22	21	20	19	18	17	16
STC_07_INTEN_CLR	STC_06_INTEN_CLR	STC_05_INTEN_CLR	STC_04_INTEN_CLR	STC_03_INTEN_CLR	STC_02_INTEN_CLR	STC_01_INTEN_CLR	STC_00_INTEN_CLR
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

15	14	13	12	11	10	9	8
RBW7_INTEN_CLR	RBW6_INTEN_CLR	RBW5_INTEN_CLR	RBW4_INTEN_CLR	RBW3_INTEN_CLR	RBW2_INTEN_CLR	RBW1_INTEN_CLR	RBW0_INTEN_CLR
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

7	6	5	4	3	2	1	0
Reserved	RCV_PKT_ERR_INTEN _CLR	Reserved	RBR0_INTEN_CLR	PMT_DETECT_INTEN _CLR	PAT_DETECT_INTEN _CLR	GOP_START_INTEN _CLR	BOUNDARY_SPECIFIC_INTEN _CLR
R-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R = Read only; W = Write only; -*n* = value after reset

Table 10. TSIF Interrupt Enable Clear Register (INTEN_CLR) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	STC_07_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
22	STC_06_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
21	STC_05_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
20	STC_04_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
19	STC_03_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
18	STC_02_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
17	STC_01_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
16	STC_00_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
15	RBW7_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
14	RBW6_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
13	RBW5_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
12	RBW4_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
11	RBW3_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
10	RBW2_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
9	RBW1_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated

Table 10. TSIF Interrupt Enable Clear Register (INTEN_CLR) Field Descriptions (continued)

Bit	Field	Value	Description
8	RBW0_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
7	Reserved	0	Reserved
6	RCV_PKT_ERR_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
5	Reserved	0	Reserved
4	RBR0_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
3	PMT_DETECT_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
2	PAT_DETECT_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
1	GOP_START_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated
0	BOUNDARY_SPECIFIC_INTEN_CLR		Interrupt condition and detection enable.
		0	No change
		1	Inactivated

4.7 TSIF Interrupt Status Register (INTSTAT)

The TSIF interrupt status register (INTSTAT) is shown in Figure 26 and described in Table 11.

All status bits work as normal, regardless of the configured value of the INTEN[*n*] bit in the TSIF interrupt enable register (INTEN) or the ARM_INT_EN bit in the TSIF control register 1 (CTRL1).

Figure 26. TSIF Interrupt Status Register (INTSTAT)

31							24
Reserved							
R-0							

23	22	21	20	19	18	17	16
STC_07_STATUS	STC_06_STATUS	STC_05_STATUS	STC_04_STATUS	STC_03_STATUS	STC_02_STATUS	STC_01_STATUS	STC_00_STATUS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

15	14	13	12	11	10	9	8
RBW7_STATUS	RBW6_STATUS	RBW5_STATUS	RBW4_STATUS	RBW3_STATUS	RBW2_STATUS	RBW1_STATUS	RBW0_STATUS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
Reserved	RCV_PKT_ERR _STATUS	Reserved	RBR0_FULL _STATUS	PMT_DETECT _STATUS	PAT_DETECT _STATUS	GOP_START _STATUS	BOUNDARY _SPECIFIC _STATUS
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 11. TSIF Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	STC_07_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT7.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_07_STATUS_CLR bit on INTSTAT_CLR register.
22	STC_06_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT6.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_06_STATUS_CLR bit on INTSTAT_CLR register.
21	STC_05_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT5.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_05_STATUS_CLR bit on INTSTAT_CLR register.
20	STC_04_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT4.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_04_STATUS_CLR bit on INTSTAT_CLR register.

Table 11. TSIF Interrupt Status Register (INTSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
19	STC_03_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT3.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_03_STATUS_CLR bit on INTSTAT_CLR register.
18	STC_02_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT2.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_02_STATUS_CLR bit on INTSTAT_CLR register.
17	STC_01_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT1.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_01_STATUS_CLR bit on INTSTAT_CLR register.
16	STC_00_STATUS		STC counter value has reached configured value of STC interrupt entry counter register on STC_INT0.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the STC_00_STATUS_CLR bit on INTSTAT_CLR register.
15	RBW7_STATUS		SDRAM writing address on write ring buffer channel 7 has reached subtracted pointer address configured by ARM via the write ring buffer channel 7 subtraction register (RING_BUF_WR_CH7_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW7_STATUS_CLR bit on INTSTAT_CLR register.
14	RBW6_STATUS		SDRAM writing address on write ring buffer channel 6 has reached subtracted pointer address configured by ARM via the write ring buffer channel 6 subtraction register (RING_BUF_WR_CH6_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW6_STATUS_CLR bit on INTSTAT_CLR register.
13	RBW5_STATUS		SDRAM writing address on write ring buffer channel 5 has reached subtracted pointer address configured by ARM via the write ring buffer channel 5 subtraction register (RING_BUF_WR_CH5_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW5_STATUS_CLR bit on INTSTAT_CLR register.
12	RBW4_STATUS		SDRAM writing address on write ring buffer channel 4 has reached subtracted pointer address configured by ARM via the write ring buffer channel 4 subtraction register (RING_BUF_WR_CH4_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW4_STATUS_CLR bit on INTSTAT_CLR register.
11	RBW3_STATUS		SDRAM writing address on write ring buffer channel 3 has reached subtracted pointer address configured by ARM via the write ring buffer channel 3 subtraction register (RING_BUF_WR_CH3_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW3_STATUS_CLR bit on INTSTAT_CLR register.
10	RBW2_STATUS		SDRAM writing address on write ring buffer channel 2 has reached subtracted pointer address configured by ARM via the write ring buffer channel 2 subtraction register (RING_BUF_WR_CH2_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW2_STATUS_CLR bit on INTSTAT_CLR register.

Table 11. TSIF Interrupt Status Register (INTSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
9	RBW1_STATUS		SDRAM writing address on write ring buffer channel 1 has reached subtracted pointer address configured by ARM via the write ring buffer channel 1 subtraction register (RING_BUF_WR_CH1_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW1_STATUS_CLR bit on INTSTAT_CLR register.
8	RBW0_STATUS		SDRAM writing address on write ring buffer channel 0 has reached subtracted pointer address configured by ARM via the write ring buffer channel 0 subtraction register (WRB0_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBW0_STATUS_CLR bit on INTSTAT_CLR register.
7	Reserved	0	Reserved
6	RCV_PKT_ERR_STATUS		Receive packet status error.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RCV_PKT_ERR_STATUS_CLR bit on INTSTAT_CLR register.
5	Reserved	0	Reserved
4	RBR0_FULL_STATUS		SDRAM reading address on read ring buffer channel 0 has reached subtracted pointer address configured by ARM via the read ring buffer channel 0 subtraction register (RRB_SUB).
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the RBR0_STATUS_CLR bit on INTSTAT_CLR register.
3	PMT_DETECT_STATUS		Detection of new PMT data.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the PMT_DETECT_STATUS_CLR bit on INTSTAT_CLR register.
2	PAT_DETECT_STATUS		Detection of new PAT data.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the PAT_DETECT_STATUS_CLR bit on INTSTAT_CLR register.
1	GOP_START_STATUS		If the TSIF module detects GOP start packet that has following conditions, this interrupt status flag is activated.
			When the following two conditions are satisfied, this interrupt can be activated:
			payload_unit_start_indicator = 1
			transport_priority = 1
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the GOP_START_STATUS_CLR bit on INTSTAT_CLR register.
0	BOUNDARY_SPECIFIC_STATUS		Host due to detection of specific word that is implemented at dividing point (boundary) of program data in transferred TS data.
		0	No interrupt condition occurs.
		1	Interrupt condition has occurred. You can clear the status by writing 1 to the BOUNDARY_SPECIFIC_STATUS_CLR bit on INTSTAT_CLR register.

4.8 TSIF Interrupt Status Clear Register (INTSTAT_CLR)

The TSIF interrupt status clear register (INTSTAT_CLR) is shown in Figure 27 and described in Table 12.

To clear the status of bit[*n*] on the STATUS register, write a 1 to INTSTAT_CLR[*n*].

All status bits work as normal, regardless of the configured value of the INTEN[*n*] bit in the TSIF interrupt enable register (INTEN) or the ARM_INT_EN bit in the TSIF control register 1 (CTRL1).

Figure 27. TSIF Interrupt Status Clear Register (INTSTAT_CLR)

31	24
Reserved	
R-0	

23	22	21	20	19	18	17	16
STC_07_STATUS_CLR	STC_06_STATUS_CLR	STC_05_STATUS_CLR	STC_04_STATUS_CLR	STC_03_STATUS_CLR	STC_02_STATUS_CLR	STC_01_STATUS_CLR	STC_00_STATUS_CLR
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

15	14	13	12	11	10	9	8
RBW7_STATUS_CLR	RBW6_STATUS_CLR	RBW5_STATUS_CLR	RBW4_STATUS_CLR	RBW3_STATUS_CLR	RBW2_STATUS_CLR	RBW1_STATUS_CLR	RBW0_STATUS_CLR
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

7	6	5	4	3	2	1	0
Reserved	RCV_PKT_ERR_STATUS_CLR	Reserved	RBR0_STATUS_CLR	PMT_DETECT_STATUS_CLR	PAT_DETECT_STATUS_CLR	GOP_START_STATUS_CLR	BOUNDARY_SPECIFIC_STATUS_CLR
R-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: W = Write only; -*n* = value after reset

Table 12. TSIF Interrupt Status Clear Register (INTSTAT_CLR) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23	STC_07_STATUS_CLR		Status clear register for STC_07_STATUS.
		0	No change
		1	Inactivated
22	STC_06_STATUS_CLR		Status clear register for STC_06_STATUS.
		0	No change
		1	Inactivated
21	STC_05_STATUS_CLR		Status clear register for STC_05_STATUS.
		0	No change
		1	Inactivated
20	STC_04_STATUS_CLR		Status clear register for STC_04_STATUS.
		0	No change
		1	Inactivated
19	STC_03_STATUS_CLR		Status clear register for STC_03_STATUS.
		0	No change
		1	Inactivated
18	STC_02_STATUS_CLR		Status clear register for STC_02_STATUS.
		0	No change
		1	Inactivated

Table 12. TSIF Interrupt Status Clear Register (INTSTAT_CLR) Field Descriptions (continued)

Bit	Field	Value	Description
17	STC_01_STATUS_CLR		Status clear register for STC_01_STATUS.
		0	No change
		1	Inactivated
16	STC_00_STATUS_CLR		Status clear register for STC_00_STATUS.
		0	No change
		1	Inactivated
15	RBW7_STATUS_CLR		Status clear register for RBW7_STATUS.
		0	No change
		1	Inactivated
14	RBW6_STATUS_CLR		Status clear register for RBW6_STATUS.
		0	No change
		1	Inactivated
13	RBW5_STATUS_CLR		Status clear register for RBW5_STATUS.
		0	No change
		1	Inactivated
12	RBW4_STATUS_CLR		Status clear register for RBW4_STATUS.
		0	No change
		1	Inactivated
11	RBW3_STATUS_CLR		Status clear register for RBW3_STATUS.
		0	No change
		1	Inactivated
10	RBW2_STATUS_CLR		Status clear register for RBW2_STATUS.
		0	No change
		1	Inactivated
9	RBW1_STATUS_CLR		Status clear register for RBW1_STATUS.
		0	No change
		1	Inactivated
8	RBW0_STATUS_CLR		Status clear register for RBW0_STATUS.
		0	No change
		1	Inactivated
7	Reserved	0	Reserved
6	RCV_PKT_ERR_STATUS_CLR		Status clear register for RCV_PKT_ERR_STATUS.
		0	No change
		1	Inactivated
5	Reserved	0	Reserved
4	RBR0_STATUS_CLR		Status clear register for RBR0_FULL_STATUS.
		0	No change
		1	Inactivated
3	PMT_DETECT_STATUS_CLR		Status clear register for PMT_DETECT_STATUS.
		0	No change
		1	Inactivated
2	PAT_DETECT_STATUS_CLR		Status clear register for PAT_DETECT_STATUS.
		0	No change
		1	Inactivated
1	GOP_START_STATUS_CLR		Status clear register for GOP_START_STATUS.
		0	No change
		1	Inactivated

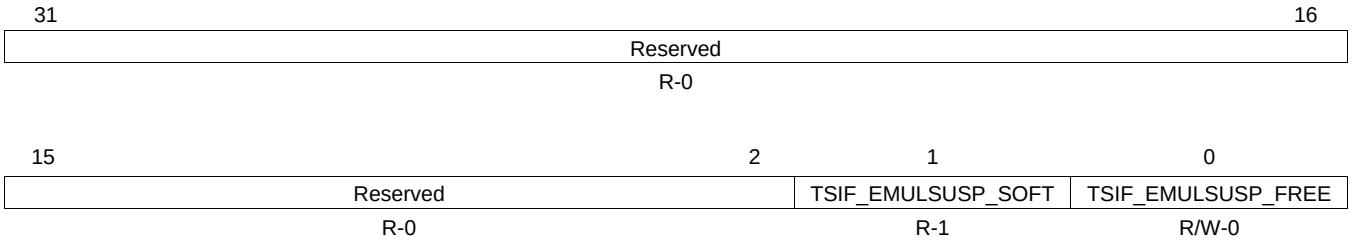
Table 12. TSIF Interrupt Status Clear Register (INTSTAT_CLR) Field Descriptions (continued)

Bit	Field	Value	Description
0	BOUNDARY_SPECIFIC_STATUS_CLR		Status clear register for BOUNDARY_SPECIFIC_STATUS.
		0	No change
		1	Inactivated

4.9 TSIF Emulation Control Register (EMU_CTRL)

The TSIF emulation control register (EMU_CTRL) is shown in Figure 28 and described in Table 13.

Figure 28. TSIF Emulation Control Register (EMU_CTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

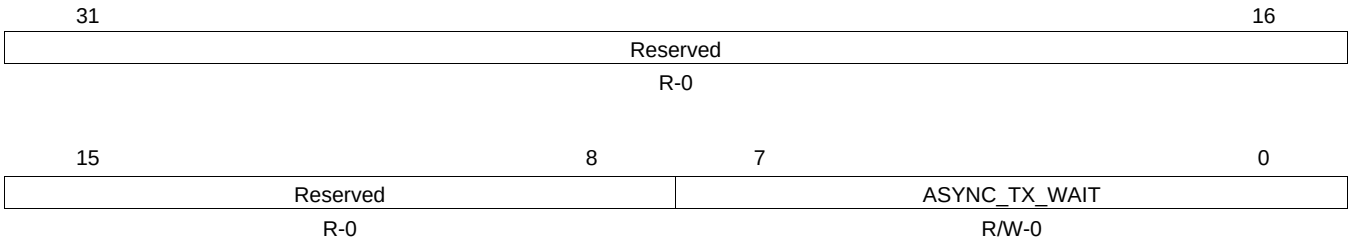
Table 13. TSIF Emulation Control Register (EMU_CTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	TSIF_EMULSUSP_SOFT	1	Defines whether or not a soft or hard stop is initiated whenever the emususp is asserted. This bit is fixed to 1 and read-only for the TSIF module. TSIF module supports only soft stop due to functional restriction related to MPEG-TS (each processing should be executed for each packet as processing unit size).
0	TSIF_EMULSUSP_FREE		Controls whether or not the peripheral responds to the emulation suspend signal that it has been programmed to monitor.
		0	Functions based on configuration of TSIF_EMULSUSP_SOFT.
		1	Ignores any emulation suspend signal (non-stop).

4.10 Asynchronous Transmit Wait Register (ASYNC_TX_WAIT)

The asynchronous transmit wait register (ASYNC_TX_WAIT) is shown in Figure 29 and described in Table 14.

Figure 29. Asynchronous Transmit Wait Register (ASYNC_TX_WAIT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Asynchronous Transmit Wait Register (ASYNC_TX_WAIT) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7-0	ASYNC_TX_WAIT	0-FFh	Controls intentional wait time between consecutive packets. This bit is effective only if the TSIF module transmits stream data to host device in asynchronous mode. Wait time can be calculated with the following equation. Register configuration unit is byte count. (serial mode) wait time = Async_TX_wait byte × 8 clk/byte at stream clk (parallel mode) wait time = Async_TX_wait byte × clk/byte at stream clk

4.11 PAT Sense Configuration Register (PAT_SEN_CFG)

The program association table (PAT) sense configuration register (PAT_SEN_CFG) is shown in Figure 30 and described in Table 15.

Figure 30. PAT Sense Configuration Register (PAT_SEN_CFG)

31	17	16
Reserved		PAT_SENSE_EN
R-0		R/W-0

15	0
PGM_ID	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. PAT Sense Configuration Register (PAT_SEN_CFG) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved
16	PAT_SENSE_EN		Sensing of program association table enable control. If the TSIF module detects new PAT packet that has updated version number with activated “current next flag” and “payload unit start indicator”, interrupt pulse is generated and status is reflected to INT_CTRL[2].
		0	No PAT filter is active
		1	PAT filter is active
15-0	PGM_ID	0-FFFFh	Filtered program number of PAT. Read-only bits and available in semi-automatic B-mode and full automatic mode (in these two modes, parsed program number should be reflected onto this register area for debug).

4.12 PAT Store Address Register (PAT_STR_ADDR)

The program association table (PAT) store address register (PAT_STR_ADDR) is shown in Figure 31 and described in Table 16.

Figure 31. PAT Store Address Register (PAT_STR_ADDR)

31	0
PAT_STORE_ADD	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 16. PAT Store Address Register (PAT_STR_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	PAT_STORE_ADD	0-FFFF FFFFh	Defines start address of SDRAM in which detected PAT is stored. If the TSIF module detects new PAT that has new version number with activated "current next flag" and "payload unit start indicator", the detected PAT is stored into SDRAM whose start address is defined by this register. During inactivated “payload unit start indicator”, SDRAM address to store PMT data is incremented. Only when above conditions (new version number with both of “current next flag” and “payload unit start indicator”) are satisfied, the SDRAM address should be reset to this defined address.

4.13 PMT Sense Configuration Register (PMT_SEN_CFG)

The program map table (PMT) sense configuration register (PMT_SEN_CFG) is shown in Figure 32 and described in Table 17.

Figure 32. PMT Sense Configuration Register (PMT_SEN_CFG)

31	17	16
Reserved		PMT_SENSE_EN
R-0		R/W-0

15	13	12	0
Reserved		PMT_PID	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. PMT Sense Configuration Register (PMT_SEN_CFG) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved
16	PMT_SENSE_EN		Sensing of program map table enable control. If the TSIF module detects new PMT packet that has updated version number with activated “current next flag” and “payload unit start indicator”, interrupt pulse is generated and status is reflected to INT_CTRL[3].
		0	No PMT filter is active
		1	PMT filter is active
15-13	Reserved	0	Reserved
12-0	PMT_PID	0-1FFFh	Filtered PMT_PID. This value is defined by PAT with parsing program number of loop section inside PAT.

4.14 PMT Store Address Register (PMT_STR_ADDR)

The program map table (PMT) store address register (PMT_STR_ADDR) is shown in Figure 33 and described in Table 18.

Figure 33. PMT Store Address Register (PMT_STR_ADDR)

31	0
PMT_STORE_ADD	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 18. PMT Store Address Register (PMT_STR_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	PMT_STORE_ADD	0-FFFF FFFFh	Defines start address of SDRAM in which detected PMT is stored. If the TSIF module detects new PMT that has new version number with activated "current next flag" and "payload unit start indicator", the detected PMT is stored into SDRAM whose start address is defined by this register. During inactivated “payload unit start indicator”, SDRAM address to store PMT data is incremented. Only when above conditions (new version number with both of “current next flag” and “payload unit start indicator”) are satisfied, the SDRAM address should be reset to this defined address.

4.15 BSP Input Register (BSP_IN)

The boundary sensing packet (BSP) input register (BSP_IN) is shown in Figure 34 and described in Table 19.

Figure 34. Boundary Sensing Packet Input Register (BSP_IN)

31	16
Reserved	
R-0	

15	13	12	0
Reserved		SEAMLESS_BOUNDARY_INPUT_PID	
R-0		R/W-1FFFh	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Boundary Sensing Packet Input Register (BSP_IN) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved
12-0	SEAMLESS_BOUNDARY_INPUT_PID	0-1FFFh	Defines PID of specific packet that is inserted at boundary of plural programs inside one TS data. If the STREAM_BNDRY_CTL bit in the TSIF control register 1 (CTRL1) is set, this value is valid. In such case, the interrupt pulse is asserted to the ARM processor if the hardware detects the packet with this PID (status is reflected in the TSIF control register 0 (CTRL0)).

4.16 BSP Input Store Address Register (BSP_STORE_ADDR)

The boundary sensing packet (BSP) input store address register (BSP_STORE_ADDR) is shown in Figure 35 and described in Figure 35.

Figure 35. Boundary Sensing Packet Input Store Address Register (BSP_STORE_ADDR)

31	0
SEAMLESS_BOUNDARY_PKT_STRT_ADD	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 20. Boundary Sensing Packet Input Store Address Register (BSP_STORE_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	SEAMLESS_BOUNDARY_PKT_STRT_ADD	0-FFFF FFFFh	Defines start address of SDRAM in which detected boundary sensing packet is stored. If the TSIF module detects the boundary sensing packet, the packet is stored into SDRAM whose start address is defined by this register.

4.17 PCR Sense Configuration Register (PCR_SENSE_CFG)

The program clock reference (PCR) sense configuration register (PCR_SENSE_CFG) is shown in Figure 36 and described in Figure 36.

Figure 36. PCR Sense Configuration Register (PCR_SENSE_CFG)

31	17	16
Reserved		PCR_SENSE_EN
R-0		R/W-0

15	13	12	0
Reserved		PCR_PID	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. PCR Sense Configuration Register (PCR_SENSE_CFG) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved
16	PCR_SENSE_EN		Sensing of program map table enable control 0:No PCR_PID filter (sensing) is active. This control bit is effective only when the PID_FILTER_CTL bit in the TSIF control register 1 (CTRL1) is 0 (full manual mode) or 1 (semi-automatic mode-A). Otherwise, the value of this bit is ignored (PCR_PID detection is carried out automatically in semi-automatic mode-B and full-automatic mode).
		0	PCR_PID inactivated
		1	PCR_PID activated
15-13	Reserved	0	Reserved
12-0	PCR_PID	0-1FFFh	Filtered PCR_PID. This value is defined by PCR_PID value inserted in PMT

4.18 PIDn Filter Configuration Registers (PID0_FILT_CFG-PID6_FILT_CFG)

The packet identifier *n* (PID*n*) filter configuration register (PID*n*_FILT_CFG) is shown in Figure 37 and described in Figure 37.

If PID value of incoming TS packet is not corresponding to all configured values on PID*n*, the incoming TS packet data is regarded as other data and stored into SDRAM with defined address by write ring buffer channel 7.

Figure 37. PID*n* Filter Configuration Register (PID*n*_FILT_CFG)

31	25	24	23	16
Reserved		PID*n*_FILTER_EN	STREAM_TYPE*n*	
R-0		R/W-0	R/W-0	

15	13	12	0
Reserved		PID*n*	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. PID*n* Filter Configuration Register (PID*n*_FILT_CFG) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Reserved
24	PID*n*_FILTER_EN		Control register of PID filter with configured PID*n*. This bit also enables write ring buffer channel *n*.
		0	Filter is disabled.
		1	Filter is enabled.
23-16	STREAM_TYPE*n*	0-FFh	Stream type to be filtered and stored into SDRAM with configured PID*n* or automatically sensed PID (if in full-automatic mode).
15-13	Reserved	0	Reserved
12-0	PID*n*	0-1FFFh	PID*n* to be filtered and stored into SDRAM with configured address.

4.19 Bypass Mode Configuration Register (BYPASS_CFG)

The bypass mode configuration register (BYPASS_CFG) is shown in Figure 38 and described in Table 23.

Figure 38. Bypass Mode Configuration Register (BYPASS_CFG)

31	25	24	23	16
Reserved		BYPASS_MODE_EN	Reserved	
R-0		R/W-0	R-0	

15	0
Reserved	
R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23. Bypass Mode Configuration Register (BYPASS_CFG) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Reserved
24	BYPASS_MODE_EN		Enables SDRAM write access on bypass mode. When this bit is 0, no input data is written onto SDRAM in bypass mode. So, to write all data in bypass mode onto SDRAM, configure this bit to 1.
		0	Bypass mode is disabled.
		1	Bypass mode is enabled.
23-0	Reserved	0	Reserved

4.20 Transmit ATS Initialization Register (TX_ATS_INIT)

Transmit arrival time stamp (ATS) initialization register (TX_ATS_INIT) is shown in Figure 39 and described in Table 24.

Figure 39. Transmit ATS Initialization Register (TX_ATS_INIT)

31	30	29	16
Rsvd	TX_ATS_INIT_EN	TX_ATS_INIT	
R-0	R/W-0	R/W-0	

15	0
TX_ATS_INIT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

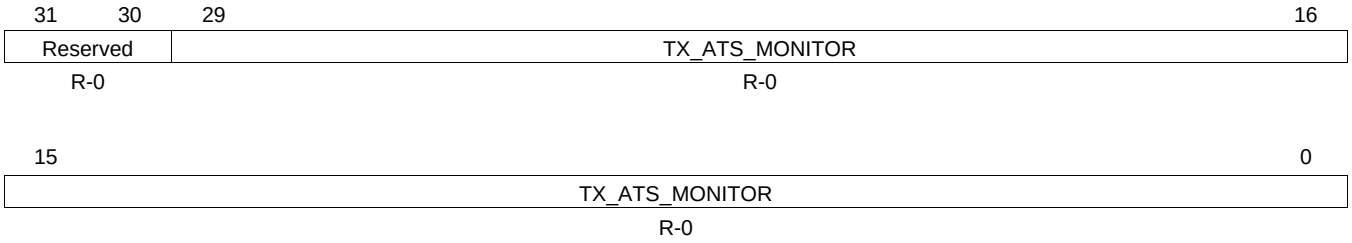
Table 24. Transmit ATS Initialization Register (TX_ATS_INIT) Field Descriptions

Bit	Field	Value	Description
31	Reserved	0	Reserved
30	TX_ATS_INIT_EN		This bit is used as the ATS (arrival time stamp) control counter reset bit. If this bit is set, a loading pulse is asserted into the TSIF module and ATS counter value is initialized to the value defined in TX_ATS_INIT. This register is write-only register (cannot read the bit value). Processing flow is: 1. CPU configures this bit to 1. 1-clock pulse is asserted inside the TSIF module. 2. TX_ATS_INIT value is loaded into ATS counter when next packet data is loaded into TX buffer, and starts to increments the counter value. See Section 2.4.4.2.2. 3. After sequence (2), TSIF module starts to assert data request signal to SDRAM in order to read source data to be transmitted to external host device. 4. If first packet data is arrived and prepared to be transmitted, then ATS counter restarts to increment and the stored data is asserted to the external host device.
		0	ATS initialization is disabled.
		1	ATS initialization is enabled.
29-0	TX_ATS_INIT	0-2FFF FFFFh	Initialization value for the ATS counter. This value is used to initialize the ATS counter whenever a write of 1 is detected on TX_ATS_INIT_EN.

4.21 Transmit ATS Monitor Register (TX_ATS_MON)

The transmit arrival time stamp (ATS) monitor register is shown in Figure 40 and described in Table 25.

Figure 40. Transmit ATS Monitor Register (TX_ATS_MON)



LEGEND: R = Read only; -*n* = value after reset

Table 25. Transmit ATS Monitor Register (TX_ATS_MON) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Reserved
29-0	TX_ATS_MONITOR	0-2FFF FFFFh	Monitoring register with which CPU can read present counter value of ATS counter driven in 27 MHZ.

4.22 Receive Packet Status (RX_PKT_STAT)

The receive packet status register (RX_PKT_STAT) is shown in Figure 41 and described in Table 26.

Figure 41. Receive Packet Status (RX_PKT_STAT)

31	29	28	16
Reserved		DIAG_PID_STATUS	
R-0		R-0	

15	14	8
RBWDMA_ERR	Reserved	
R-0	R-0	

7	6	5	4	3	2	1	0
Reserved	ABORT_VIDEO_PKT	CRC_ERR	Reserved		TPE_ERR	SBYTE_ERR	Reserved
R-0	R-0	R-0	R-0		R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

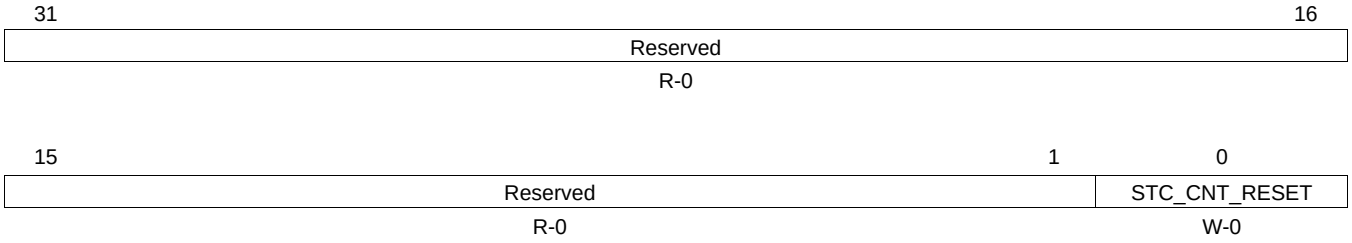
Table 26. Receive Packet Status (RX_PKT_STAT) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Reserved
28-16	DIAG_PID_STATUS	0-1FFFh	Indicates PID status of receive error packet. Used for debug purpose.
15	RBWDMA_ERR	0-1	Ring buffer write DMA error in sync mode. When this bit is 1, received packet is discarded due to count stall or DMA request has not been finished. This bit is effective only in synchronous mode.
14-7	Reserved	0	Reserved
6	ABORT_VIDEO_PKT	0-1	Indicates when video packet is ignored until GOP detection. This bit is effective when GOP detection is enabled GOP_DETECT_EN.
5	CRC_ERR	0-1	Indicates when CRC error occurs in PAT/PMT parsing. This bit is effective when PAT_SEN_CFG/PMT_SEN_CFG is enabled and the CRC_FLT_EN bit in the TSIF control register 1 (CTRL1) is set. The packet is ignored and none of the PID are not updated in semi-automatic mode-B/full-automatic mode.
4-3	Reserved	0	Reserved
2	TPE_ERR	0-1	Indicates when the packet is ignored with transport error. Indicator is set to 1 in TS header. This bit is effective when PID_FILTER_EN and TPEI_FLT_EN bits in the TSIF control register 1 (CTRL1) are set.
1	SBYTE_ERR	0-1	Indicates when the packet is ignored when sync byte is not matched. Indicator is set to 47h in TS header. This bit is effective when PID_FILTER_EN and SBYTE_FLT_EN bits in the TSIF control register 1 (CTRL1) are set.
0	Reserved	0	Reserved

4.23 STC Initialization Control Register (STC_INIT_CTRL)

The system time clock (STC) initialization control register (STC_INIT_CTRL) is shown in Figure 42 and described in Table 27.

Figure 42. STC Initialization Control Register (STC_INIT_CTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

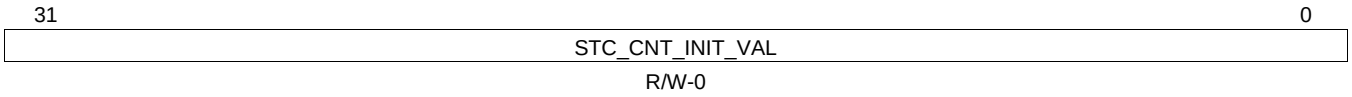
Table 27. STC Initialization Control Register (STC_INIT_CTRL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	STC_CNT_RESET	0-1	When set loads the initialize counter value on STC_INIT_VAL onto STC counter implemented in counter module on the receiver. This bit is write-only and the rising edge of this bit is regarded as loading pulse signal of initialize value for STC counter. The initialize value is written in STC_INIT_VAL.

4.24 STC Initialization Value Register (STC_INIT_VAL)

The system time clock (STC) initialization value register (STC_INIT_VAL) is shown in Figure 43 and described in Table 28.

Figure 43. STC Initialization Value Register (STC_INIT_VAL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

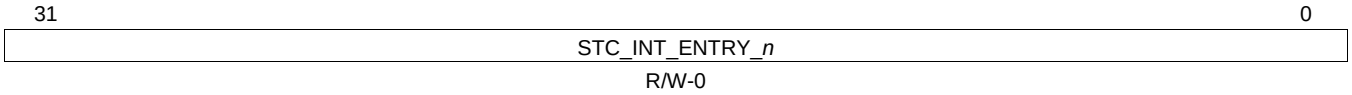
Table 28. STC Initialization Value Register (STC_INIT_VAL) Field Descriptions

Bit	Field	Value	Description
31-0	STC_CNT_INIT_VAL	0-FFFF FFFFh	Defines the STC counter initialize value. The configured value is loaded onto the STC counter with the reset pulse that is generated by STC_INIT_CTRL.

4.25 STC Interrupt Entry *n* Registers (STC_INT0-STC_INT7)

The system time clock (STC) interrupt entry *n* register (STC_INT_ENTRY_*n*) is shown in Figure 44 and described in Table 29.

Figure 44. STC Interrupt Entry *n* Register (STC_INT_ENTRY_*n*)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 29. STC Interrupt Entry *n* Register (STC_INT_ENTRY_*n*) Field Descriptions

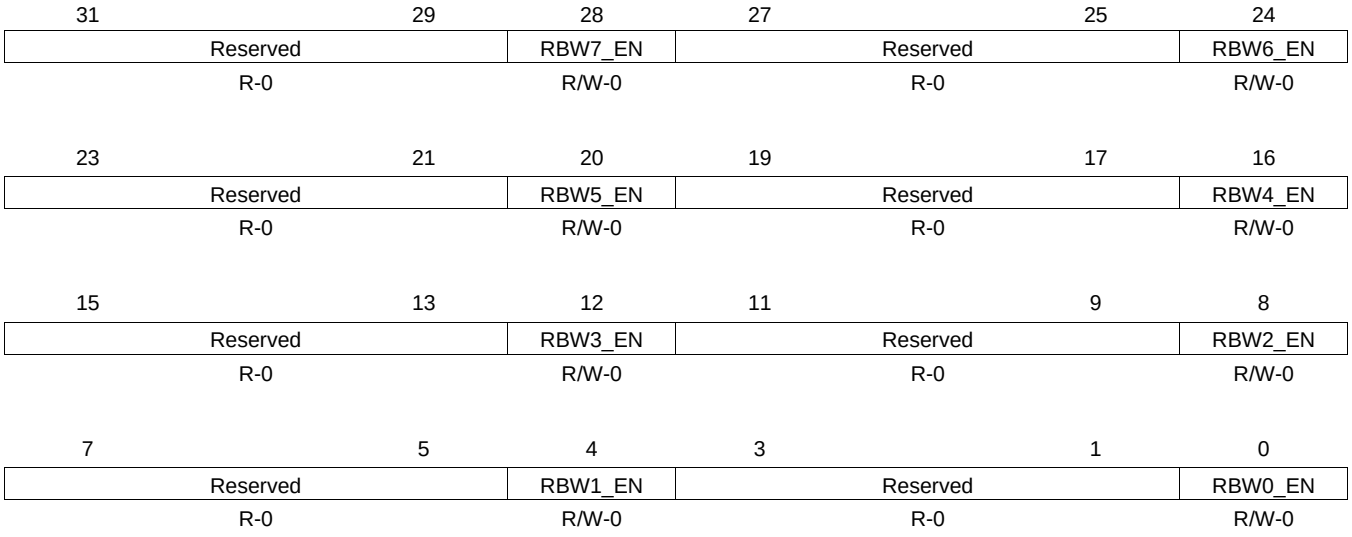
Bit	Field	Value	Description
31-0	STC_INT_ENTRY_*n*	0-FFFF FFFFh	Defines counter value of the STC counter to assert interrupt pulse to the CPU. If the STC counter reaches this register value and the interrupt condition of this register is enabled, the counter asserts an interrupt pulse to the CPU.

4.26 Write Ring Buffer Channel Control Register (WRB_CTRL)

The write ring buffer channel control register (WRB_CTRL) is shown in Figure 45 and described in Table 30.

Each ring buffer has 4 configuration registers; start, end, pointer, and subtraction value from pointer address that indicates redundant bytes from pointer address.

Figure 45. Write Ring Buffer Channel Control Register (WRB_CTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 30. Write Ring Buffer Channel Control Register (WRB_CTRL) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Reserved

Table 30. Write Ring Buffer Channel Control Register (WRB_CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
28	RBW7_EN		RBW7 (Ring buffer write channel 7) enable. RBW7 works for stream data whose PID is not assigned in PID configuration registers from PID0 to PID6. RBW7 can work in bypass mode.
		0	Ring buffer channel 7 is disabled.
		1	Ring buffer channel 7 is enabled.
27-25	Reserved	0	Reserved
24	RBW6_EN		RBW6 (Ring buffer write channel 6) enable. Valid only if PID6_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 6 is disabled.
		1	Ring buffer channel 6 is enabled.
23-21	Reserved	0	Reserved
20	RBW5_EN		RBW5 (Ring buffer write channel 5) enable. Valid only if PID5_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 5 is disabled.
		1	Ring buffer channel 5 is enabled.
19-17	Reserved	0	Reserved
16	RBW4_EN		RBW4 (Ring buffer write channel 4) enable. Valid only if PID4_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 4 is disabled.
		1	Ring buffer channel 4 is enabled.
15-13	Reserved	0	Reserved
12	RBW3_EN		RBW3 (Ring buffer write channel 3) enable. Valid only if PID3_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 3 is disabled.
		1	Ring buffer channel 3 is enabled.
11-9	Reserved	0	Reserved
8	RBW2_EN		RBW2 (Ring buffer write channel 2) enable. Valid only if PID2_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 2 is disabled.
		1	Ring buffer channel 2 is enabled.
7-5	Reserved	0	Reserved
4	RBW1_EN		RBW1 (Ring buffer write channel 1) enable. Valid only if PID1_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 1 is disabled.
		1	Ring buffer channel 1 is enabled.
3-1	Reserved	0	Reserved
0	RBW0_EN		RBW0 (Ring buffer write channel 0) enable. Valid only if PID0_FILTER_EN is set to 1 (enable).
		0	Ring buffer channel 0 is disabled.
		1	Ring buffer channel 0 is enabled.

4.27 Write Ring Buffer Channel *n* Start Address Registers (WRB0_STRT_ADDR-WRB7_STRT_ADDR)

The write ring buffer channel *n* start address register (WRB*n*_STRT_ADDR) is shown in Figure 46 and described in Table 31. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 46. Write Ring Buffer Channel *n* Start Address Register (WRB*n*_STRT_ADDR)

31	3	2	1	0
RBW*n*_STRT_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 31. Write Ring Buffer Channel *n* Start Address Register (WRB*n*_STRT_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	RBW*n*_STRT_ADD	0-FFFF FFFFh	Start address of RBW*n* (write ring buffer channel *n*). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low). This register should not be changed while the channel is enabled.

4.28 Write Ring Buffer Channel *n* End Address Registers (WRB0_END_ADDR-WRB7_END_ADDR)

The write ring buffer channel *n* end address register (WRB*n*_END_ADDR) is shown in Figure 47 and described in Table 32. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 47. Write Ring Buffer Channel *n* End Address Register (WRB*n*_END_ADDR)

31	3	2	1	0
RBW*n*_END_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 32. Write Ring Buffer Channel *n* End Address Register (WRB*n*_END_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	RBW*n*_END_ADD	0-FFFF FFFFh	End address of RBW*n* (write ring buffer channel *n*). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low). This register should not be changed while the channel is enabled.

4.29 Write Ring Buffer Channel *n* Read Pointer Registers (WRB0_RDPTR-WRB7_RDPTR)

The write ring buffer channel *n* read pointer address register (WRB*n*_RDPTR) is shown in Figure 48 and described in Table 33. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 48. Write Ring Buffer Channel *n* Read Pointer Register (WRB*n*_RDPTR)

31	3	2	1	0
RBW*n*_RP_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 33. Write Ring Buffer Channel *n* Read Pointer Register (WRB*n*_RDPTR) Field Descriptions

Bit	Field	Value	Description
31-0	RBW*n*_RP_ADD	0-FFFF FFFFh	Read pointer address for RBW*n* (write ring buffer channel *n*). If write address reaches this address, further write access is stalled until the ring buffer pointer address is updated with reactivation of this channel. The pointer must be placed at multiples of the packet size (unit = byte). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low).

4.30 Write Ring Buffer Channel *n* Subtraction Registers (WRB0_SUB-WRB7_SUB)

Th write ring buffer channel *n* subtraction register (WRB*n*_SUB) is shown in Figure 49 and described in Table 34. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 49. Write Ring Buffer Channel *n* Subtraction Register (WRB*n*_SUB)

31	3	2	1	0
RBW*n*_SUB_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

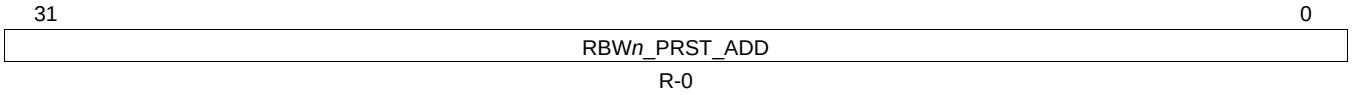
Table 34. Write Ring Buffer Channel *n* Subtraction Register (WRB*n*_SUB) Field Descriptions

Bit	Field	Value	Description
31-0	RBW*n*_SUB_ADD	0-FFFF FFFFh	Defines the distance of the temporal read address pointer from the read pointer address for RBW*n* (write ring buffer channel *n*). If the write pointer address reaches to the address which can be defined by subtracting this register value from the read pointer address, an interrupt pulse is asserted to the ARM processor with status flag (INT_CTRL). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low) and set with a minimum 8-byte offset (for example, Packet Size × n + 8).

4.31 Write Ring Buffer Channel *n* Write Pointer Registers (WRB0_WRPTR-WRB7_WRPTR)

The write ring buffer channel *n* present address register (WRB*n*_WRPTR) is shown in Figure 50 and described in Table 35.

Figure 50. Write Ring Buffer Channel *n* Write Pointer Register (WRB*n*_WRPTR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

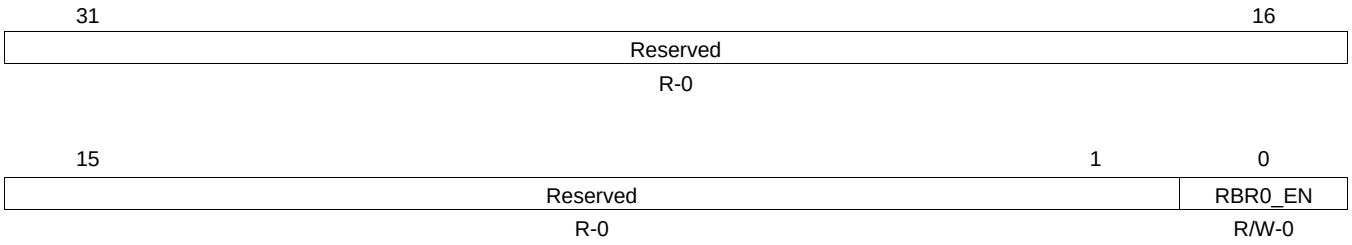
Table 35. Write Ring Buffer Channel *n* Write Pointer Register (WRB*n*_WRPTR) Field Descriptions

Bit	Field	Value	Description
31-0	RBW*n*_PRST_ADD	0-FFFF FFFFh	Present writing address of RBW*n* (write ring buffer channel *n*).

4.32 Read Ring Buffer Channel Control Register (RRB_CTRL)

The read ring buffer channel control register (RRB_CTRL) is shown in Figure 51 and described in Table 36.

Figure 51. Read Ring Buffer Channel Control Register (RRB_CTRL)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 36. Read Ring Buffer Channel Control Register (RRB_CTRL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	RBR0_EN		RBR0 (read ring buffer channel 0) enable. RBR0 controls reading source stream data (multiplexed by ARM processor) from SDRAM.
		0	Read channel 0 is disabled.
		1	Read channel 0 is enabled.

4.33 Read Ring Buffer Channel Start Address Register (RRB_STRT_ADDR)

The read ring buffer channel start address register (RRB_STRT_ADDR) is shown in Figure 52 and described in Table 37. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 52. Read Ring Buffer Channel Start Address Register (RRB_STRT_ADDR)

31	3	2	1	0
RBR0_STRT_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 37. Read Ring Buffer Channel Start Address Register (RRB_STRT_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	RBR0_STRT_ADD	0-FFFF FFFFh	Start address of RBR0 (read ring buffer channel 0). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low). This register should not be changed while the channel is enabled.

4.34 Read Ring Buffer Channel End Address Register (RRB_END_ADDR)

The read ring buffer channel end address register (RRB_END_ADDR) is shown in Figure 53 and described in Table 38. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 53. Read Ring Buffer Channel End Address Register (RRB_END_ADDR)

31	3	2	1	0
RBR0_END_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 38. Read Ring Buffer Channel End Address Register (RRB_END_ADDR) Field Descriptions

Bit	Field	Value	Description
31-0	RBR0_END_ADD	0-FFFF FFFFh	End address of RBR0 (read ring buffer channel 0). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low). This register should not be changed while the channel is enabled.

4.35 Read Ring Buffer Channel Write Pointer Register (RRB_WRPTR)

The read ring buffer channel write pointer register (RRB_WRPTR) is shown in Figure 54 and described in Table 39. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 54. Read Ring Buffer Channel Write Pointer Register (RRB_WRPTR)

31	3	2	1	0
RBR0_WP_ADD		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 39. Read Ring Buffer Channel Write Pointer Register (RRB_WRPTR) Field Descriptions

Bit	Field	Value	Description
31-0	RBR0_WP_ADD	0-FFFF FFFFh	Write pointer address for RBR0 (read ring buffer channel 0). If read address reaches this address, further read access is stalled until the ring buffer pointer address is updated with reactivation of this channel. The pointer must be placed at multiples of the packet size (unit = byte). This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low).

4.36 Read Ring Buffer Channel Subtraction Register (RRB_SUB)

The read ring buffer channel subtraction register (RRB_SUB) is shown in Figure 55 and described in Table 40. Bits 2-0 are permanently tied low, as the address must be aligned on an 8-byte boundary.

Figure 55. Read Ring Buffer Channel Subtraction Register (RRB_SUB)

31	3	2	1	0
RBR0_WP_SUB		0	0	0
R/W-0			R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 40. Read Ring Buffer Channel Subtraction Register (RRB_SUB) Field Descriptions

Bit	Field	Value	Description
31-0	RBR0_WP_SUB	0-FFFF FFFFh	Defines distance of temporal write address pointer from read pointer address for RBR0 (read ring buffer channel 0). If read pointer address reaches to the address that can be defined by subtraction of this register value from the write pointer address, an interrupt pulse is asserted to the ARM processor with status flag. This register should be set for 8-byte boundary address (bits 2-0 are read only and are permanently tied low) and set with a minimum 8-byte offset (for example, Packet Size × n + 8).

4.37 Read Ring Buffer Channel Read Pointer Register (RRB_RDPTR)

The read ring buffer channel read pointer register (RRB_RDPTR) is shown in Figure 56 and described in Table 41.

Figure 56. Read Ring Buffer Channel Read Pointer Register (RRB_RDPTR)

31	0
RBR0_PRST_ADD	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 41. Read Ring Buffer Channel Read Pointer Register (RRB_RDPTR) Field Descriptions

Bit	Field	Value	Description
31-0	RBR0_PRST_ADD	0-FFFF FFFFh	Present writing address of RBR0 (read ring buffer channel 0).

4.38 Packet Counter Value Register (PKT_CNT)

The packet counter value register (PKT_CNT) is shown in Figure 57 and described in Table 42.

Figure 57. Packet Counter Value Register (PKT_CNT)

31	0
PKT_CNT	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 42. Packet Counter Value Register (PKT_CNT) Field Descriptions

Bit	Field	Value	Description
31-0	PKT_CNT	0-FFFF FFFFh	Packet counter value is reflected to this register. This register is used for debugging. Once the TSIF (or ARM) detects GOP header position (detail description is in INT_CTRL[1]) or boundary specific packet between plural programs of TS data, the counter value of the targeted packet value is reflected to this register.

Appendix A Revision History

Table A-1 lists the changes made since the previous version of this document.

Table A-1. Document Revision History

Reference	Additions/Modifications/Deletions
Section 2.1	Changed subsection.
Figure 5	Changed figure.
Figure 6	Changed figure.

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