TMS320DM646x DMSoC
Clock Reference Generator (CRGEN)

User's Guide

Literature Number: SPRUEQ1
December 2007

Texas Instruments

Contents

List of Figures

List of Tables

Read This First

About This Manual

Describes the operation of the clock reference generator (CRGEN) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUEP8 — ***TMS320DM646x DMSoC DSP Subsystem Reference Guide.*** Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRUEP9 — ***TMS320DM646x DMSoC ARM Subsystem Reference Guide.*** Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.

SPRUEQ0 — ***TMS320DM646x DMSoC Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).

SPRAA84 — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

Clock Reference Generator (CRGEN)

1 Introduction

This document describes the operation of the clock reference generator (CRGEN) in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

1.1 Purpose of the Peripheral

The clock reference generator (CRGEN) module aims to recover the 27-MHZ system clock from the program clock reference (PCR) value that is detected by the transport stream interface (TSIF) module, and also develops a system time clock (STC) counter value in both streaming (clock recovery with PCR) and video input cases. Each TSIF module has an associated CRGEN module, CRGEN0 may only be used with TSIF 0 and CRGEN 1 may only be used with TSIF 1.

1.2 Features

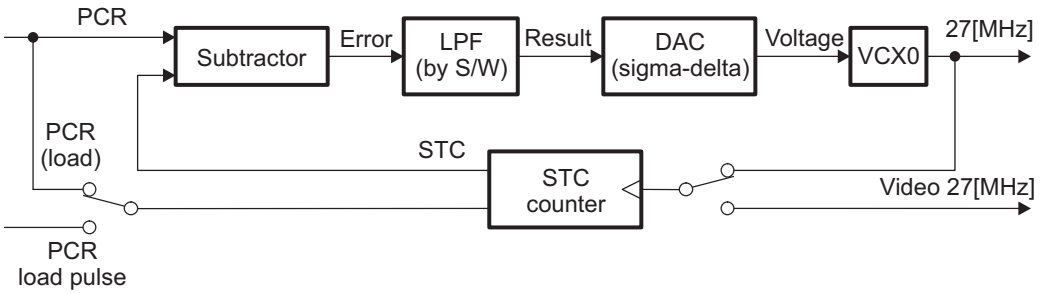
Each CRGEN module features:

- Automatic load of received PCR packet values from associated TSIF module
- Local system time clock (STC) counter
- PCR/STC difference generator (subtractor)
- Loop filter (LPF)
- 1-bit sigma/delta modulator digital-to-analog converter (DAC) output for external VCXO control

1.3 Functional Block Diagram

A block diagram of the CRGEN module is shown in Figure 1.

Figure 1. CRGEN Functional Block Diagram



1.4 Terminology Used in This Document

The following is a brief explanation of some terms used in this document:

Term	Meaning
CRGEN	clock reference generator
PCR	program clock reference
STC	system time clock
TSIF	transport stream interface

2 Architecture

This section discusses the architecture of the clock reference generator (CRGEN).

2.1 Clock Control

The CRGEN input clock is controlled by a system register. See the device-specific data manual for more information.

2.2 Signal Descriptions

The CRGEN provides the I/O signals listed in Table 1.

Table 1. CRGEN Signal Descriptions

Port Name	I/O	Description	To/From
CLK_27M	I	System main 27 MHZ clock	CLKC
CRGEN_PWM_OUT	O	Output signal to VCXO	VCXO
CRGEN_EMULSUSP	I	Emulation suspend signal (active high)	CPU
CRGEN_INT	O	Interrupt signal (1 pulse (high) on CLK_CFG)	INTC

2.3 Pin Multiplexing

On the DM646x DMSoC, extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the CRGEN.

2.4 Functional Description

This section discusses the CRGEN module.

2.4.1 Subtractor

The subtractor module takes the subtraction value between the input program clock reference (PCR) value and the internal system time clock (STC) counter value. With the PCR loading pulse comes from the transport stream interface (TSIF) module, the subtraction module works to take the subtraction value. The derived value is used as source data for the loop filter module and is reflected in the loop filter register (LOOP_FILTER) to be monitored by the CPU.

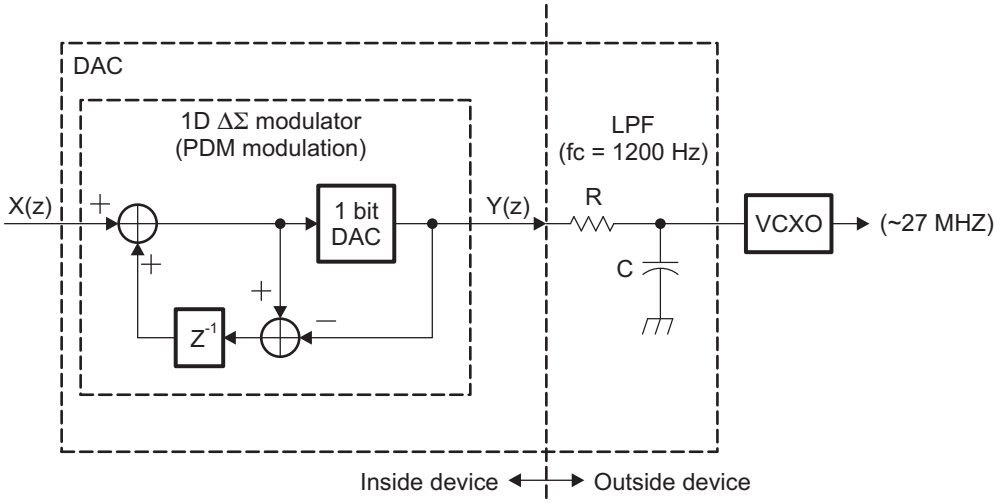
2.4.2 Loop Filter (LPF)

The loop filter module is part of the CPU and has a large effect on the PLL. The input value to the loop filter is the result of the subtraction module. The data width for the input to the loop filter is 7 bits (-63 to +63). The output value from the loop filter is the input for the sigma-delta DAC. The data width for the output from the loop filter is 16 bits (-32768 to +32768).

2.4.3 Sigma-Delta DAC

The sigma-delta DAC module is for analog voltage control. The result of the loop filter module is used as source data for the sigma-delta DAC module. The sigma-delta DAC module is shown in Figure 2. The output of the sigma-delta DAC module is Y(z).

Figure 2. Sigma-Delta DAC



2.4.4 VCXO

The output signal from the sigma-delta DAC module drives the VCXO. The VCXO generates the 27-MHZ system clock in cooperation with the input voltage value.

2.4.5 System Time Clock (STC) Counter

The system time clock (STC) counter module is driven by the 27-MHZ system clock or the video input 27-MHZ clock and provides the STC counter value to any of the peripherals inside the DM646x DMSoC. The STC value is reflected in the STC counter value registers to be monitored by the CPU.

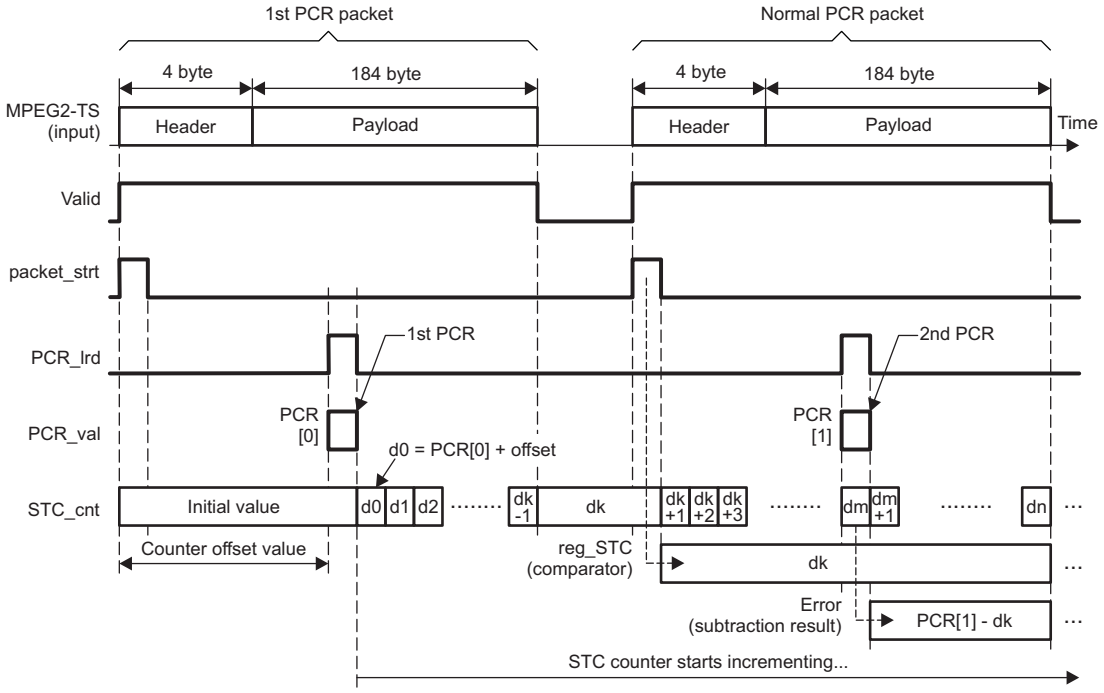
With the first program clock reference (PCR) loading pulse after the STC counter module is activated, the PCR value is detected as an initial value of the STC counter. When the STC counter module detects a PCR loading pulse from the transport stream interface (TSIF) module, the STC counter module asserts an interrupt pulse to the interrupt controller.

2.5 Processing Method of Clock Recovery

The CRGEN loads the STC counter value to the subtractor module with a packet start pulse of input TS packet. When the packet is a PCR packet, the PCR loading pulse is asserted from the transport stream interface (TSIF) module and the subtractor module derives the subtraction value of PCR value and stores the STC counter value to the register. This process is shown in Figure 3.

In Figure 3, the CRGEN compares the PCR value and the STC counter value on a packet start pulse. The STC counter value is advanced to the PCR value with a fixed offset value. From the MPEG system standard, the byte count of the PCR data from the start of the packet is a fixed value. This offset value can be defined by a module configuration register.

Figure 3. Waveform of Internal Signal Performance on CRGEN Module



2.6 Software Configuration

The CRGEN is required to be configured with the transport stream interface (TSIF) module. The example is written in the following.

- The STC_INIT_OFST_EXTENSION bits in the STC counter offset low value register (STC_OFFSET_LO) is set to the STC base counter offset value when one clock is described as 27 MHZ.
- The STC_INIT_OFST_BASE_H bits in the STC counter offset high value register (STC_OFFSET_HI) and the STC_INIT_OFST_BASE_L bits in STC_OFFSET_LO are set to the STC base counter offset value when one clock is described as 90 MHZ.
- The STC_LOAD_MODE bit in the CRGEN control register (CONTROL) is set to determine the STC counter load mode. This bit is cleared to 0 when the CRGEN loads the PCR value on the first loading pulse or set to 1 when the CRGEN loads the PCR value on each loading pulse from the TSIF module.
- The STC_LOAD_SEL bit in CONTROL is set to select the STC value hold timing. This bit is cleared to 0 when the CRGEN uses the TSIF packet start signal or set to 1 when the CRGEN uses the TSIF CRGEN PCR enable signal.

2.7 Hardware Reset Considerations

The CRGEN hardware reset is controlled by the DM646x DMSoC. See the device-specific data manual for more information.

2.8 Interrupt Events and Requests

With the first program clock reference (PCR) loading pulse after the STC counter module is activated, the PCR value is detected as an initial value of the STC counter. When the CRGEN detects a PCR loading pulse from the transport stream interface (TSIF) module, the CRGEN asserts an interrupt pulse (Table 2) to the interrupt controller.

Table 2. CRGEN Module Interrupts

ARM Event	Acronym	Source
8	CRGENINT0	CRGEN 0
9	CRGENINT1	CRGEN 1

2.9 Emulation Suspend Mode Support

The CRGEN module does support the emulation suspend signal from the CPU. The emulation suspend signal (a high indicates that the CPU is suspended) is asserted by the CPU when the CPU is halted with a breakpoint or any other reason during debug.

3 Registers

Table 3 lists the memory-mapped registers for the clock reference generator (CRGEN). See the device-specific data manual for the memory address of these registers. The module base address is 01C2 6000h for CRGEN0 and 01C2 6400h for CRGEN1.

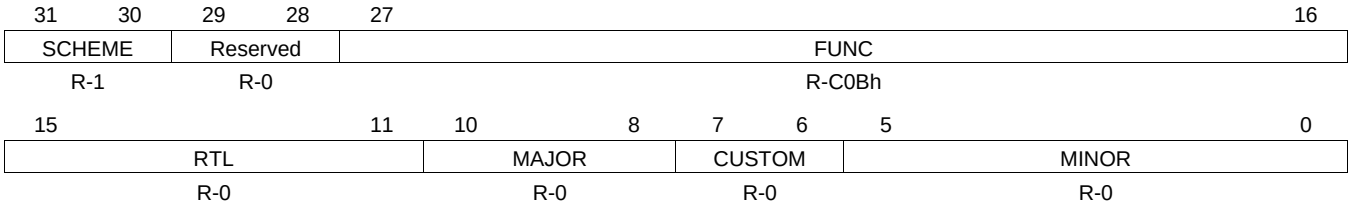
Table 3. Clock Reference Generator (CRGEN) Registers

Offset	Acronym	Register Description	Section
0h	PID	CRGEN Peripheral Identification Register	Section 3.1
4h	CONTROL	CRGEN Control Register	Section 3.2
8h	STC_HI	STC Counter Current High Value Register	Section 3.3
Ch	STC_LO	STC Counter Current Low Value Register	Section 3.4
10h	STC_VAL_HI	STC Counter High Value Register	Section 3.5
14h	STC_VAL_LO	STC Counter Low Value Register	Section 3.6
18h	PCR_HI	PCR Counter High Value Register	Section 3.7
1Ch	PCR_LO	PCR Counter Low Value Register	Section 3.8
20h	PCR_PKT_STAT	PCR Packet Status Register	Section 3.9
24h	LOOP_FILTER	Loop Filter Register	Section 3.10
28h	STC_OFFSET_HI	STC Counter Offset High Value Register	Section 3.11
2Ch	STC_OFFSET_LO	STC Counter Offset Low Value Register	Section 3.12
40h	INTEN	Interrupt Enable Register	Section 3.13
44h	INTEN_SET	Interrupt Enable Set Register	Section 3.14
48h	INTEN_CLR	Interrupt Enable Clear Register	Section 3.15
4Ch	INTSTAT	Interrupt Status Register	Section 3.16
50h	INTSTAT_CLR	Interrupt Status Clear Register	Section 3.17
54h	EMU_CTRL	Emulation Control Register	Section 3.18

3.1 CRGEN Peripheral Identification Register (PID)

The CRGEN peripheral identification register (PID) is shown in Figure 4 and described in Table 4.

Figure 4. CRGEN Peripheral Identification Register (PID)



LEGEND: R = Read only; -*n* = value after reset

Table 4. CRGEN Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	1	Used to distinguish between old scheme and current. Fixed to 01b.
29-28	Reserved	0	Reserved.
27-16	FUNC	0-FFFh	Function indicates a software-compatible module family.
		C0Bh	Current function number.
15-11	RTL	0	Indicates RTL version. In this module, fixed to 0.
10-8	MAJOR	0-7h	Major revision number.
		0	Current major revision.
7-6	CUSTOM	0	Indicates a special version for a particular device. In this module, fixed to 0.
5-0	MINOR	0-3Fh	Minor revision number.
		0	Current minor revision.

3.2 CRGEN Control Register (CONTROL)

The CRGEN control register (CONTROL) is shown in Figure 5 and described in Table 5.

Figure 5. CRGEN Control Register (CONTROL)

31	16
Reserved	
R–0	

15	3	2	1	0
Reserved		STC_LOAD_MODE	STC_LOAD_SEL	MODULE_EN
R–0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

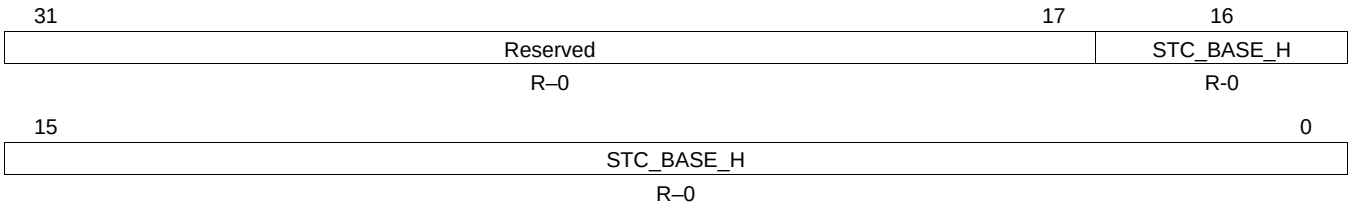
Table 5. CRGEN Control Register (CONTROL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved.
2	STC_LOAD_MODE		Defines loading mode for STC counter.
		0	CRGEN loads the PCR value on first loading pulse from TSIF module.
		1	CRGEN loads the PCR value on each loading pulse from TSIF module.
1	STC_LOAD_SEL		Defines hold timing select for STC value.
		0	CRGEN uses the TSIF packet start signal.
		1	CRGEN uses the TSIF CRGEN PCR enable signal.
0	MODULE_EN		Module enable. The first PCR loading pulse after activating this bit is used to initialize the STC counter value. If you would like to stall the STC counter module when the module is activated, you need to configure this bit to 0.
		0	CRGEN module stops.
		1	CRGEN module operates.

3.3 STC Counter Current High Value Register (STC_HI)

The system time clock (STC) counter current high value register (STC_HI) is shown in Figure 6 and described in Table 6.

Figure 6. STC Counter Current High Value Register (STC_HI)



LEGEND: R = Read only; -*n* = value after reset

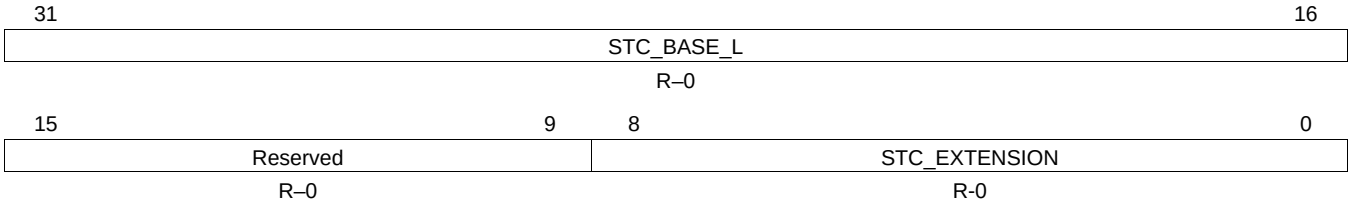
Table 6. STC Counter Current High Value Register (STC_HI) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved
16-0	STC_BASE_H	0-1FFFFh	STC counter current high value that is driven in 90 kHz. These bits hold the higher 17 bits (bits 32 to 16) of the current STC counter. The STC_BASE_L bit in the STC counter current low value register (STC_LO) holds the lower 16 bits (bits 15 to 0).

3.4 STC Counter Current Low Value Register (STC_LO)

The system time clock (STC) counter current low value register (STC_LO) is shown in Figure 7 and described in Table 7.

Figure 7. STC Counter Current Low Value Register (STC_LO)



LEGEND: R = Read only; -*n* = value after reset

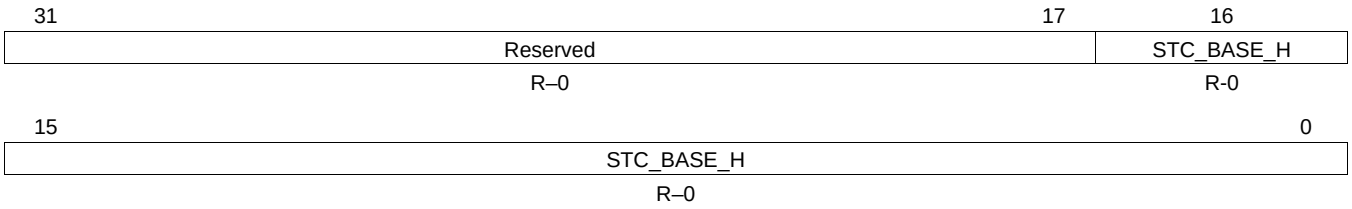
Table 7. STC Counter Current Low Value Register (STC_LO) Field Descriptions

Bit	Field	Value	Description
31-16	STC_BASE_L	0-FFFFh	STC counter current low value that is driven in 90 kHz. These bits hold the lower 16 bits (bits 15 to 0) of the current STC counter. The STC_BASE_H bit in the STC counter current high value register (STC_HI) holds the higher 17 bits (bits 32 to 16).
15-9	Reserved	0	Reserved
8-0	STC_EXTENSION	0-1FFh	STC counter extension value that is driven in 27 MHZ (maximum counter value is 299 (unsigned) = 12Bh).

3.5 STC Counter High Value Register (STC_VAL_HI)

The system time clock (STC) counter high value register (STC_VAL_HI) is shown in Figure 8 and described in Table 8.

Figure 8. STC Counter High Value Register (STC_VAL_HI)



LEGEND: R = Read only; -*n* = value after reset

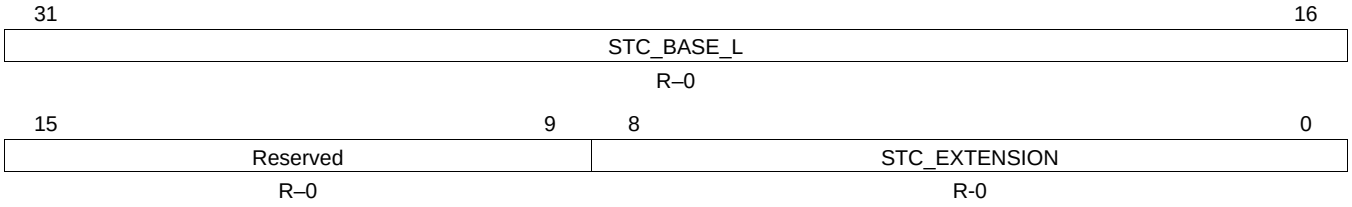
Table 8. STC Counter High Value Register (STC_VAL_HI) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved.
16-0	STC_BASE_H	0-1FFFFh	STC counter high value that is driven in 90 kHz. These bits hold the higher 17 bits (bits 32 to 16) of the STC counter. The STC_BASE_L bit in the STC counter low value register (STC_VAL_LO) holds the lower 16 bits (bits 15 to 0).

3.6 STC Counter Low Value Register (STC_VAL_LO)

The system time clock (STC) counter low value register (STC_VAL_LO) is shown in Figure 9 and described in Table 9.

Figure 9. STC Counter Low Value Register (STC_VAL_LO)



LEGEND: R = Read only; -*n* = value after reset

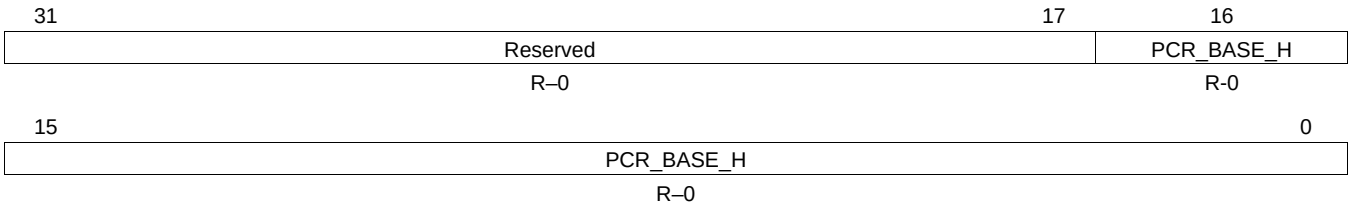
Table 9. STC Counter Low Value Register (STC_VAL_LO) Field Descriptions

Bit	Field	Value	Description
31-16	STC_BASE_L	0-FFFFh	STC counter low value that is driven in 90 kHz. These bits hold the lower 16 bits (bits 15 to 0) of the STC counter. The STC_BASE_H bit in the STC counter high value register (STC_VAL_HI) holds the higher 17 bits (bits 32 to 16).
15-9	Reserved	0	Reserved.
8-0	STC_EXTENSION	0-1FFh	STC counter extension value that is driven in 27 MHZ (maximum counter value is 299 (unsigned) = 12Bh).

3.7 PCR Counter High Value Register (PCR_HI)

The program clock reference (PCR) counter high value register (PCR_HI) is shown in Figure 10 and described in Table 10.

Figure 10. PCR Counter High Value Register (PCR_HI)



LEGEND: R = Read only; -*n* = value after reset

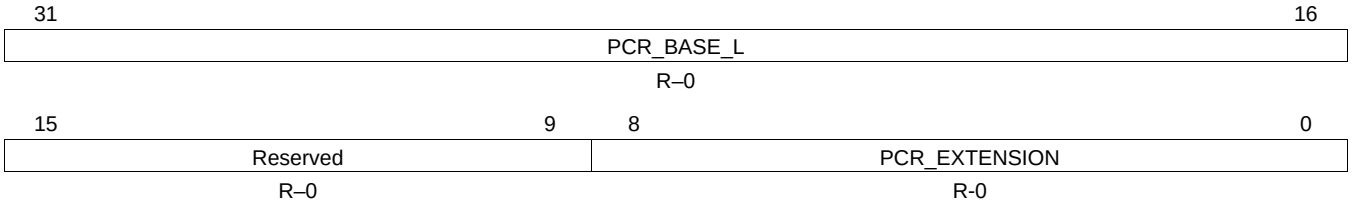
Table 10. PCR Counter High Value Register (PCR_HI) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved.
16-0	PCR_BASE_H	0-1FFFFh	PCR counter high value that is driven in 90 kHz. These bits hold the higher 17 bits (bits 32 to 16) of the PCR counter. The PCR_BASE_L bit in the PCR counter low value register (PCR_LO) holds the lower 16 bits (bits 15 to 0).

3.8 PCR Counter Low Value Register (PCR_LO)

The program clock reference (PCR) counter low value register (PCR_LO) is shown in Figure 11 and described in Table 11.

Figure 11. PCR Counter Low Value Register (PCR_LO)



LEGEND: R = Read only; -*n* = value after reset

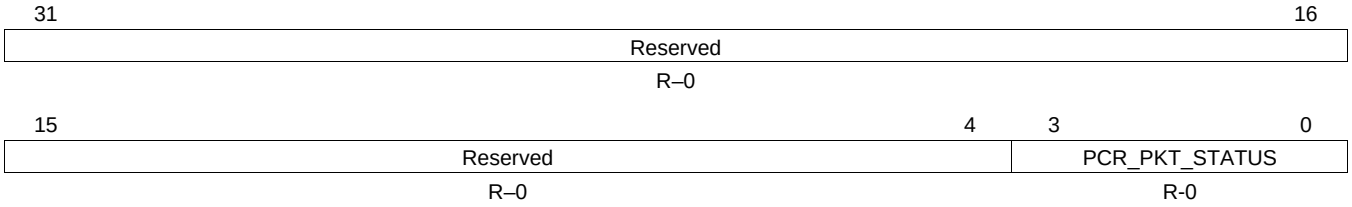
Table 11. PCR Counter Low Value Register (PCR_LO) Field Descriptions

Bit	Field	Value	Description
31-16	PCR_BASE_L	0-FFFFh	PCR counter low value that is driven in 90 KHz. These bits hold the lower 16 bits (bits 15 to 0) of the PCR counter. The PCR_BASE_H bit in the PCR counter high value register (PCR_HI) holds the higher 17 bits (bits 32 to 16).
15-9	Reserved	0	Reserved.
8-0	PCR_EXTENSION	0-1FFh	PCR counter extension value that is driven in 27 MHZ (maximum counter value is 299 (unsigned) = 12Bh).

3.9 PCR Packet Status Register (PCR_PKT_STAT)

The program clock reference (PCR) packet status register (PCR_PKT_STAT) is shown in Figure 12 and described in Table 12.

Figure 12. PCR Packet Status Register (PCR_PKT_STAT)



LEGEND: R = Read only; -*n* = value after reset

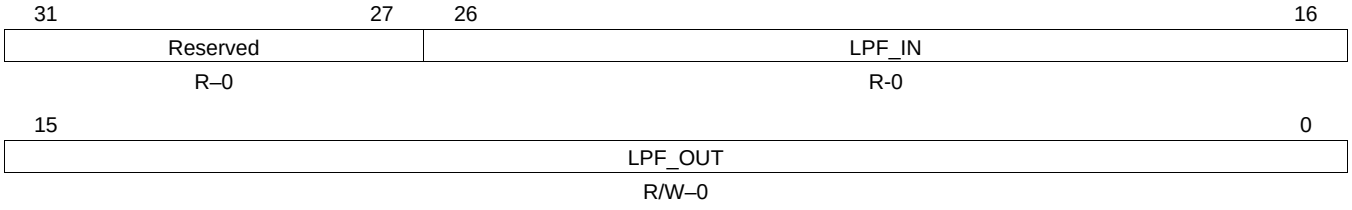
Table 12. PCR Packet Status Register (PCR_PKT_STAT) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Reserved.
3-0	PCR_PKT_STATUS	0-Fh	PCR packet status. Status value is detected by PCR loading pulse signal that comes from the TSIF module.
		0	No error
		1h	Transport error. Indicator in TS header.
		2h	Discontinuity. Indicator in adaptation field.
		3h	Fixed to 0
		4h-Fh	Reserved

3.10 Loop Filter Register (LOOP_FILTER)

The loop filter register (LOOP_FILTER) is shown in Figure 13 and described in Table 13.

Figure 13. Loop Filter Register (LOOP_FILTER)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

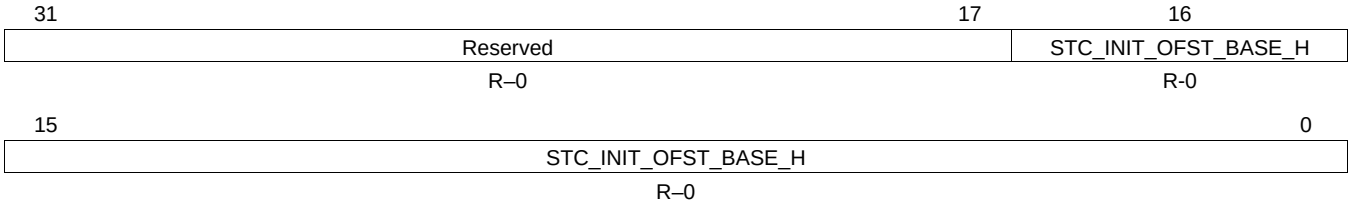
Table 13. Loop Filter Register (LOOP_FILTER) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved.
26-16	LPF_IN	0-7FFh	Loop filter in. Contains subtraction result between PCR value and STC counter value. Result data is clipped into -1024 to +1023 (11 bits).
15-0	LPF_OUT	0-FFFFh	Loop filter out. Configures loop filter output data that is derived from calculation result of ARM processor (-32768 to +32767). Do not write this bit when 27-MHZ clock is not supplied.

3.11 STC Counter Offset High Value Register (STC_OFFSET_HI)

The system time clock (STC) counter offset high value register (STC_OFFSET_HI) is shown in Figure 14 and described in Table 14.

Figure 14. STC Counter Offset High Value Register (STC_OFFSET_HI)



LEGEND: R = Read only; -*n* = value after reset

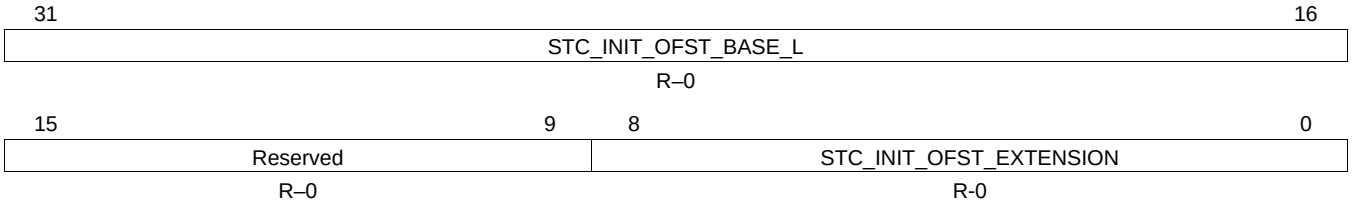
Table 14. STC Counter Offset High Value Register (STC_OFFSET_HI) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Reserved.
16-0	STC_INIT_OFST_BASE_H	0-1FFFFh	STC counter offset high value whose one clock is described as 90 kHz. This value is detected in the STC counter with the first PCR loading pulse signal. These bits hold the higher 17 bits (bits 32 to 16) of the STC counter offset. The STC_INIT_OFST_BASE_L bit in the STC counter offset low value register (STC_OFFSET_LO) holds the lower 16 bits (bits 15 to 0).

3.12 STC Counter Offset Low Value Register (STC_OFFSET_LO)

The system time clock (STC) counter offset low value register (STC_OFFSET_LO) is shown in Figure 15 and described in Table 15.

Figure 15. STC Counter Offset Low Value Register (STC_OFFSET_LO)



LEGEND: R = Read only; -*n* = value after reset

Table 15. STC Counter Offset Low Value Register (STC_OFFSET_LO) Field Descriptions

Bit	Field	Value	Description
31-16	STC_INIT_OFST_BASE_L	0-FFFFh	STC base counter offset low value whose one clock is described as 90 kHz. This value is detected in the STC counter with the first PCR loading pulse signal. These bits hold the lower 16 bits (bits 15 to 0) of the STC counter offset. The STC_INIT_OFST_BASE_H bit in the STC counter offset high value register (STC_OFFSET_HI) holds the higher 17 bits (bits 32 to 16).
15-9	Reserved	0	Reserved.
8-0	STC_INIT_OFST_EXTENSION	0-1FFh	STC counter offset extension value whose one clock is described as 27 MHZ. Maximum configured value should be 299(unsigned) = 12Bh, and must not be more than this value.

3.13 Interrupt Enable Register (INTEN)

The interrupt enable register (INTEN) is shown in Figure 16 and described in Table 16.

Figure 16. Interrupt Enable Register (INTEN)

31	16
Reserved	
R–0	

15	1	0
Reserved		CRGEN_INTEN
R–0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. Interrupt Enable Register (INTEN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved.
0	CRGEN_INTEN		This bit enables the interrupt from this module to the ARM processor. To activate the interrupt to the ARM, configure this bit to 1, and then configure the CRGEN_INTEN_SET bit in the interrupt enable set register (INTEN_SET) to 1.
		0	Interrupt is disabled.
		1	Interrupt is enabled.

3.14 Interrupt Enable Set Register (INTEN_SET)

The interrupt enable set register (INTEN_SET) is shown in Figure 17 and described in Table 17.

Figure 17. Interrupt Enable Set Register (INTEN_SET)

31	16
Reserved	
R–0	

15	1	0
Reserved		CRGEN_INTEN_SET
R–0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. Interrupt Enable Set Register (INTEN_SET) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved.
0	CRGEN_INTEN_SET		To enable the interrupt to the ARM processor, configure this bit to 1 and set the CRGEN_INTEN bit in the interrupt enable register (INTEN) to 1. While activated, this bit value remains set to 1. Notice that this bit is in effect only when the CRGEN_INTEN bit is activated; otherwise, any configured value to this bit is ignored and this bit remains cleared to 0. You can only write 1 and cannot write 0 to this bit. If you write 1 to the CRGEN_INTEN_CLR bit while this bit is activated, this bit is internally cleared to 0.
		0	Interrupt is inactivated (cannot write 0).
		1	Interrupt is activated.

3.15 Interrupt Enable Clear Register (INTEN_CLR)

The interrupt clear register (INTEN_CLR) is shown in Figure 18 and described in Table 18.

Figure 18. Interrupt Enable Register (INTEN_CLR)

31	16
Reserved	
R–0	

15	1	0
Reserved		CRGEN_INTEN_CLR
R–0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

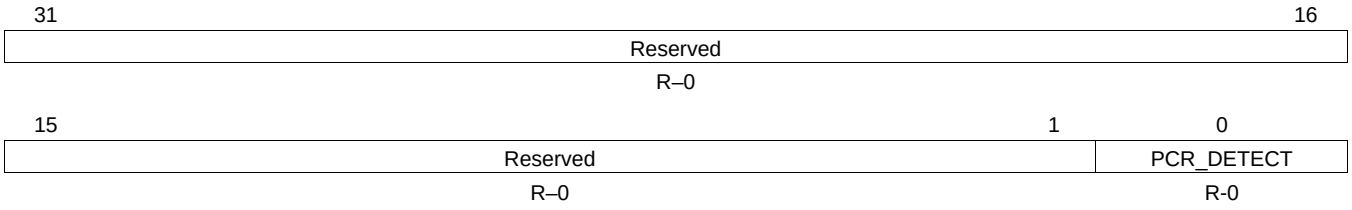
Table 18. Interrupt Clear Register (INTEN_CLR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved.
0	CRGEN_INTEN_CLR		To disable the interrupt to the ARM processor, configure this bit to 1 with the CRGEN_INTEN and CRGEN_INTEN_SET bits set to 1. Notice that this bit is in effect only when the CRGEN_INTEN and CRGEN_INTEN_SET bits are activated; otherwise, any configured value to this bit is ignored. You can only write 1 and cannot write 0 to this bit.
		0	No change
		1	Interrupt inactivated (cannot be read by ARM).

3.16 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 19 and described in Table 19.

Figure 19. Interrupt Status Register (INTSTAT)



LEGEND: R = Read only; -*n* = value after reset

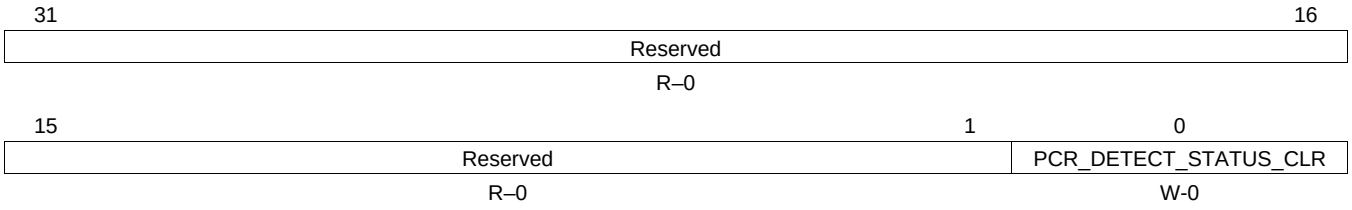
Table 19. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved.
0	PCR_DETECT		Interrupt status register. This bit works even if the following interrupt register is inactivated. Notice that this bit is read-only. To clear this bit, configure the PCR_DETECT_STATUS_CLR bit in the interrupt status clear register (INTSTAT_CLR) to 1.
		0	PCR loading pulse is not detected.
		1	PCR loading pulse is detected, and not checked yet.

3.17 Interrupt Status Clear Register (INTSTAT_CLR)

The interrupt status clear register (INTSTAT_CLR) is shown in Figure 20 and described in Table 20.

Figure 20. Interrupt Status Clear Register (INTSTAT_CLR)



LEGEND: R = Read only; W= Write only; -*n* = value after reset

Table 20. Interrupt Status Clear Register (INTSTAT_CLR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved.
0	PCR_DETECT_STATUS_CLR		Interrupt status clear register bit. To clear the PCR_DETECT bit in the interrupt status register (INTSTAT), configure this bit to 1. Notice that this bit is write-only, and a written value cannot be read by the ARM.
		0	No change.
		1	PCR_DETECT bit is cleared (write only: cannot be read).

3.18 Emulation Control Register (EMU_CTRL)

The emulation control register (EMU_CTRL) is shown in Figure 21 and described in Table 21.

Figure 21. Emulation Control Register (EMU_CTRL)

31	16
Reserved	
R–0	

15	2	1	0
Reserved		CRGEN_EMULSUSP_SOFT	CRGEN_EMULSUSP_FREE
R–0		R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 21. Emulation Control Register (EMU_CTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved.
1	CRGEN_EMULSUSP_SOFT		Defines whether a soft or hard stop is initiated whenever the EMUSUSP is asserted. Because this module generates a PWM output for a VCXO device outside the device and the VCXO device provides a system source clock (27 MHZ) to the device, the module asserts a DC component as an output for a VCXO device after the module stalls due to emulation suspend signal (same performance as if the LPF_OUT bit in the loop filter register (LOOP_FILTER) is configured to be 0).
		0	Hard stop (the CRGEN module immediately stops processing).
		1	Soft stop (the CRGEN module stops processing when next interrupt status is asserted).
0	CRGEN_EMULSUSP_FREE		Controls whether the peripheral responds to the emulation suspend signal that it has been programmed to monitor.
		0	Functions based on configuration of CRGEN_EMULSUSP_SOFT bit.
		1	Ignores any emulation suspend signal (non-stop).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265