TMS320C642x DSP 64-Bit Timer

User's Guide

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About This Manual

Describes the operation of the software-programmable 64-bit timer in the TMS320C642x Digital Signal Processor (DSP). The C642x DSP processor contains three software-programmable timers. Timer 0 and Timer 1 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode (operated independently), or dual 32-bit chained mode (operated in conjunction with each other). Timer 2 is used only as a Watchdog Timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct access (EDMA) synchronization events. The Watchdog Timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C642x Digital Signal Processor (DSP). Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the C642x DSP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUEM3 — ***TMS320C642x DSP Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320C642x Digital Signal Processor (DSP).

SPRAA84 — ***TMS320C64x to TMS320C64x+ CPU Migration Guide.*** Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.

SPRU732 — ***TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.

SPRU871 — ***TMS320C64x+ DSP Megamodule Reference Guide.*** Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

64-Bit Timer/Watchdog Timer

1 Introduction

This document describes the operation of the software-programmable 64-bit timer in the TMS320C642x Digital Signal Processor (DSP). The C642x DSP processor contains three software-programmable timers. Timer 0 and Timer 1 can be programmed in 64-bit mode, dual 32-bit unchained mode (operated independently), or dual 32-bit chained mode (operated in conjunction with each other). Timer 2 is used as a Watchdog Timer.

1.1 Purpose of the Peripheral

The timers support four modes of operation: a 64-bit general-purpose (GP) timer, dual unchained 32-bit GP timers, dual chained 32-bit timers, or a Watchdog Timer. The GP timer modes can be used to generate periodic interrupts, EDMA synchronization events, or external clock output. The Watchdog Timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop. The capabilities of each of the timers are summarized in Table 1.

Table 1. Supported Timer Features by Instantiation

Capability	Timer 0	Timer 1	Timer 2
64-bit general-purpose timer	√	√	-
Dual 32-bit general-purpose timer (unchained)	√	√	-
Dual 32-bit general-purpose timer (chained)	√	√	-
External clock input (TIN0 and TIN1 pins)	√	√	-
External clock output (TOUT0 and TOUT1 pins)	√	√	-
Watchdog Timer	-	-	√

1.2 Features

The 64-bit timer consists of the following features.

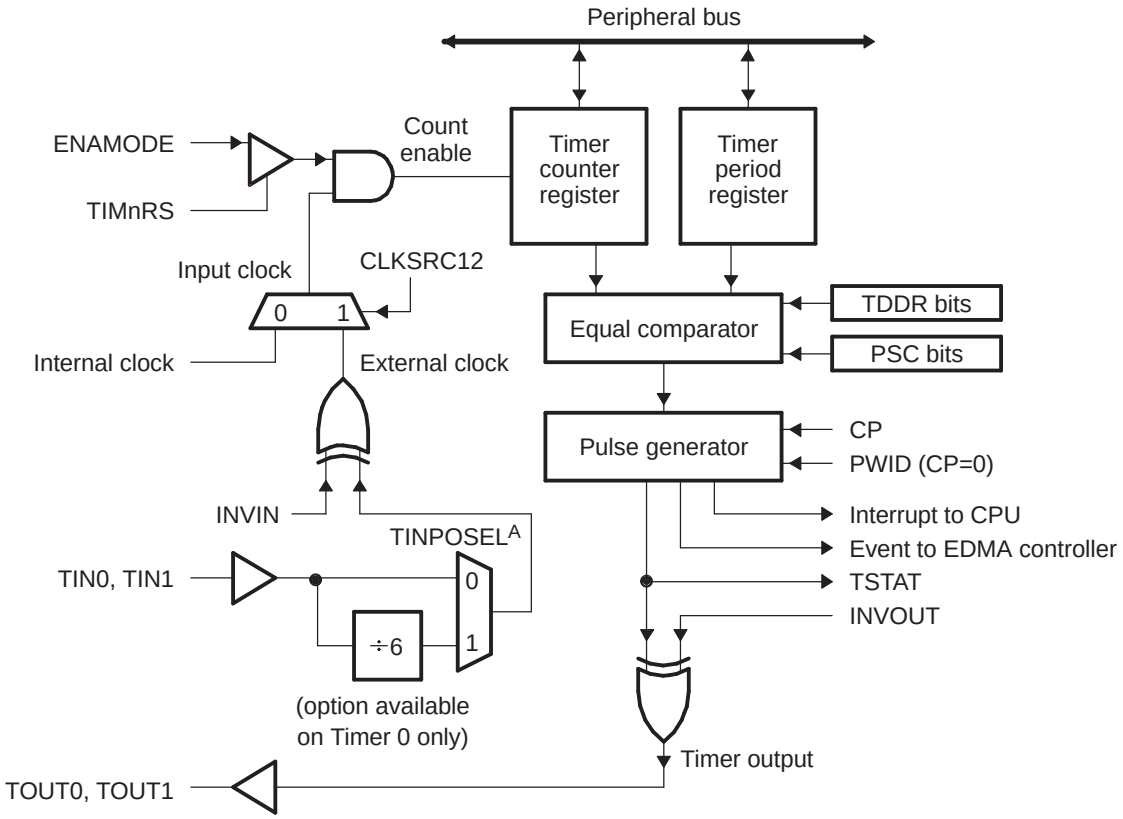
- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit general-purpose timer mode
  - Watchdog Timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock input via timer input pins TIN0 and TIN1 (Timer 0 and Timer 1 only)
- 2 possible output modes:
  - Pulse mode (configurable pulse width)
  - Clock mode
- 2 possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets after each period)

- Generates interrupts to DSP
- Generates sync event to EDMA

1.3 Functional Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the general purpose timers is in Section 2. For the detailed information and block diagram of the Watchdog Timer, reference Section 3.

Figure 1. Timer Block Diagram



A These options are set in the timer control register (TIMERCTL) within the System Module.

1.4 Industry Standard Compatibility Statement

This peripheral is not intended to conform to any specific industry standard.

2 Architecture – General-Purpose Timer Mode

This section describes general-purpose (GP) timers, Timer 0 and Timer 1. Timer 2 can only be used as a Watchdog Timer, for detailed information see Section 3.

2.1 Clock Control

Timer 0 and Timer 1 can use an internal or external clock source for the counter period. The following sections explain how to select the clock source. Table 2 shows which clock sources are supported on each timer.

Table 2. Supported Timer Clock Sources

Clock Source	Timer 0	Timer 1	Timer 2
Internal clock source	√	√	√
External clock input (TIN0 and TIN1 pins)	√	√	-

As shown in Table 3 and Figure 2, the timer clock source is selected using the clock source (CLKSRC12) bit in the timer control register (TCR). Two clock sources are available to drive the timer clock:

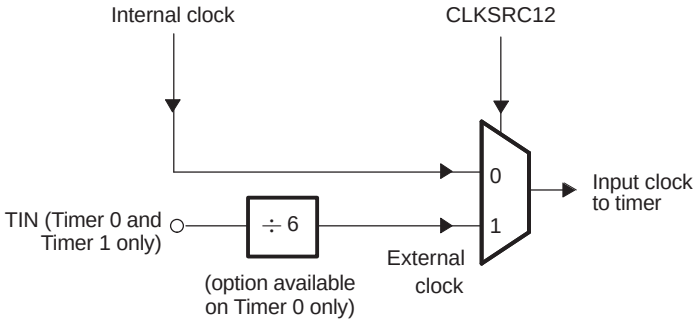
- Internal clock, by setting CLKSRC12 = 0
- External clock on Timer 0 and Timer 1 input pins (TIN0 and TIN1), by setting CLKSRC12 = 1 (This input signal is synchronized internally.)

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections.

Table 3. Timer Clock Source Selection

CLKSRC12	Input Clock
0	Internal clock (default)
1	External clock on timer input (TIN0 and TIN1 pin)

Figure 2. Timer Clock Source Block Diagram



2.1.1 Using the Internal Clock Source to the Timer

The internal clock source determines the speed of the timer since the timer counts up based on each cycle of the clock source. When determining the period and prescalers settings for the timer, choose the desired period in terms of number of clock cycles. For details on the generation of the on-chip clocks, see the device-specific data manual.

The CLKSRC12 bit in the timer control register (TCR) controls whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, the CLKSRC12 bit controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 1 in the timer global control register, TGCR), the CLKSRC12 bit controls the Timer 1:2 side of the timer. The Timer 3:4 side must use the internal clock.

To select the internal clock as the clock source for the timer, the CLKSRC12 bit must be cleared to 0.

2.1.2 Using the External Clock Source to the Timer (Timer 0 and Timer 1 only)

An external clock source can be provided to clock the timer via the TIN0 and TIN1 pins.

The CLKSRC12 bit in the timer control register (TCR) controls whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, the CLKSRC12 bit controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 1 in TGCR), the CLKSRC12 bit controls the Timer 1:2 side of the timer. The Timer 3:4 side must use the internal clock.

To select the external clock as the clock source for the timer, the CLKSRC12 bit must be set to 1.

2.2 Signal Descriptions

Input signals are available for Timer 0 and Timer 1 modules. The Timer 0 input (TIN0) and the Timer 1 input (TIN1) are connected to the input clock circuit to allow for timer synchronization. For audio applications, Timer 0 provides a ÷6 divider to ensure that the audio clock meets the timer module requirement of less than CLK/4, where CLK equals the 27 MHZ timer peripheral clock. The ÷6 divider on Timer 0 can be enabled by setting the Timer 0 input select (TINP0SEL) bit to 1. The TINP0SEL bit is located in the timer control register (TIMERCTL) within the System Module. When TINP0SEL = 1, enabling the ÷6 option, and the timer input inverter control (INVINP) option, in the timer control register (TCR), is set to 1, then the result of the ÷6 signal is inverted. If the TINP0SEL bit is cleared to 0 and INVINP option is set, then the input signal will come directly from the Timer 0 input (TINP0L) pin and the INVINP option inverts the input source signal. For more information on TIMERCTL, refer to your data manual.

Timer 0 and Timer 1 provides an external clock out and two timer output modes, pulse mode and clock mode. The timer output mode is selected using the Clock/Pulse mode (CP) bit in TCR. When in the pulse mode (CP = 0), the pulse width (PWID) bits can be configured to set pulse width to 1, 2, 3, or 4 timer clock cycles. The pulse width setting determines the number of timer clock cycles that pass before the timer status (TSTAT) goes inactive. The pulse can be inverted by setting the timer output inverter control (INVOUT) bit, located in TCR, to 1. When in the clock mode (CP = 1), the signal on the timer output pin has a 50% duty cycle. The signal toggles (from high to low or from low to high) each time the timer counter reaches zero. The value of the output pin is located in the TSTAT bits of TCR.

2.3 Pin Multiplexing

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings. Refer to the device-specific data manual to determine how pin multiplexing affects the Timer peripheral.

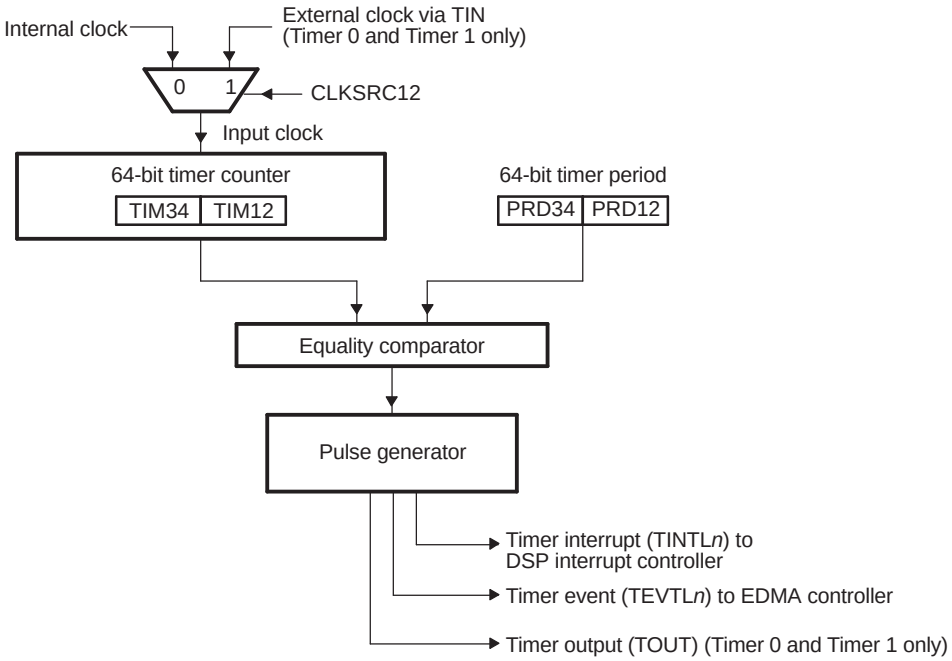
2.4 Timer Modes

The following section describes the general-purpose (GP) timer modes (Timer 0 and Timer 1 only). To use the timer as a Watchdog Timer (Timer 2 only), see Section 3.

2.4.1 64-Bit Timer Mode (Timer 0 and Timer 1)

The general-purpose timers can each be configured as a 64-bit timer (Figure 3) by clearing the TIMMODE bit in the timer global control register (TGCR) to 0. At reset, the default setting for the TIMMODE bit is for the 64-bit timer. In this mode, the timer operates as a single 64-bit up-counter. The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit timer period register. When the timer is enabled, the timer counter starts incrementing by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINTL*n*) , a timer EDMA sync event (TEVTL*n*), and an output signal (TOUT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using control bits in TGCR.

Figure 3. 64-Bit Timer Mode Block Diagram



2.4.1.1 Enabling the 64-Bit Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. For the timer to operate in 64-bit timer mode, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit field in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit field has no effect in 64-bit timer mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 4 shows the bit values in TGCR to configure the 64-bit timer.

Table 4. 64-Bit Timer Configurations

	TGCR Bit		TCR Bit
64-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 64-bit timer in reset	0	0	0
To disable the 64-bit timer (out of reset)	1h	1h	0
To enable the 64-bit timer for one-time operation	1h	1h	1h
To enable the 64-bit timer for continuous operation	1h	1h	2h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.4.1.2 Reading the Counter Registers

When reading the timer count in 64-bit timer mode, the CPU must first read TIM12 followed by TIM34. When TIM12 is read, the timer copies TIM34 into a shadow register. When reading TIM34, the hardware logic forces the reads from the shadow register. This ensures that the values read from the registers are not affected by the fact that the timer may continue to run as the registers are read. When reading the timers in 32-bit mode, TIM12 and TIM34 may be read in either order.

2.4.1.3 64-Bit Timer Configuration Procedure

To configure the GP timer to operate as a 64-bit timer, follow the steps below:

1. Perform the necessary device pin multiplexing setup (see the device-specific data manual).
2. Program the VDD3P3V_PWDN register to power up the IO pins for Timer 0 and Timer 1 (see the device-specific data manual).
3. Select clock source (CLKSRC bit in TCR).
4. Select output mode (CP bit in TCR).
5. Select pulse width mode (PWID bit in TCR).
6. Consider ÷6 requirements (TINP0SEL bit in TIMERCTL in system module).
7. Consider inverter requirements (INVINP and INVOUTP bits in TCR).
8. Select 64-bit mode (TIMMODE bit in TGCR).
9. Remove the timer from reset (TIM12RS and TIM34RS bits in TGCR).
10. Select the desired timer period (PRD12 and PRD34).
11. Enable the timer (ENAMODE12 bit field in TCR).

2.4.2 Dual 32-Bit Timer Modes (Timer 0 and Timer 1)

Each of the general-purpose timers can be configured as dual 32-bit timers by configuring the TIMMODE bit in the timer global control register (TGCR). In dual 32-bit timer mode, the two 32-bit timers can be operated independently (unchained mode) or in conjunction with each other (chained mode).

2.4.2.1 Chained Mode

The general-purpose timers can each be configured as a dual 32-bit chained timer (Figure 4) by setting the TIMMODE bit to 3h in TGCR.

In the chained mode, one 32-bit timer (Timer 3:4) is used as a 32-bit prescaler and the other 32-bit timer (Timer 1:2) is used as a 32-bit timer. The 32-bit prescaler is used to clock the 32-bit timer. The 32-bit prescaler uses one counter register (TIM34) to form a 32-bit prescale counter register and one period register (PRD34) to form a 32-bit prescale period register.

When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated and the prescale counter register is reset to 0 (see the example in Figure 5).

The other 32-bit timer (Timer 1:2) uses one counter register (TIM12) to form a 32-bit timer counter register and one period register (PRD12) to form a 32-bit timer period register. This timer is clocked by the output clock from the prescaler. The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINTL*n*), a timer EDMA event (TEVTL*n*), and an output signal (TOUT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS and TIM34RS bits in TGCR. In the chained mode, the upper 16-bits of the timer control register (TCR) are not used.

Figure 4. Dual 32-Bit Timers Chained Mode Block Diagram

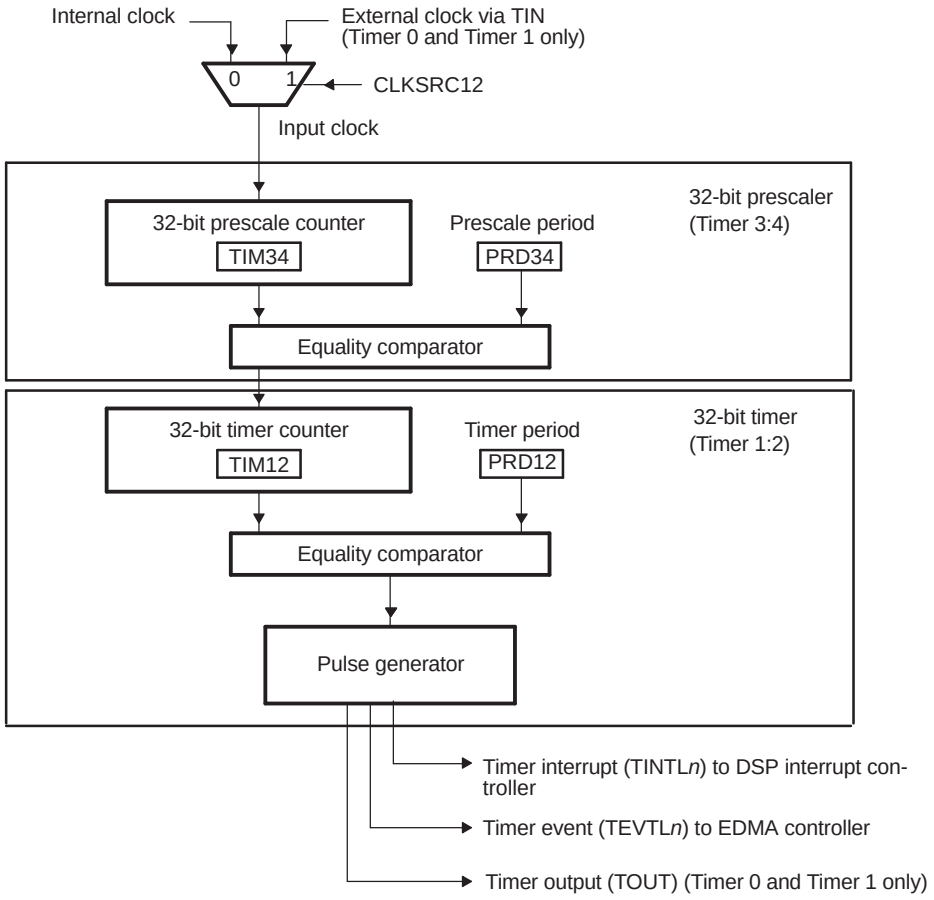
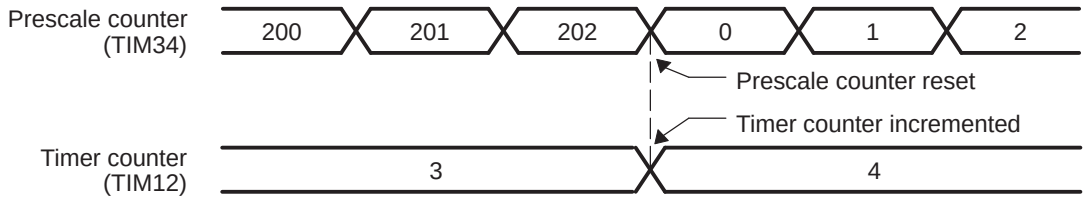


Figure 5. Dual 32-Bit Timers Chained Mode Example

32-bit prescaler settings: count = TIM34 = 200; period = PRD34 = 202
32-bit timer settings: count = TIM12 = 3; period = PRD12= 4



2.4.2.1.1 Enabling the 32-Bit Timer Chained Mode

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the Timer 1:2 side of the timer and the TIM34RS bits control the reset of the Timer 3:4 side of the timer. For the timer to operate, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit field in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit field has no effect in 32-bit timer chained mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 5 shows the bit values in TGCR to configure the 32-bit timer in chained mode.

Table 5. 32-Bit Timer Chained Mode Configurations

	TGCR Bit		TCR Bit
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 32-bit timer chained mode in reset	0	0	0
To disable the 32-bit timer chained mode (out of reset)	1h	1h	0
To enable the 32-bit timer chained mode for one-time operation	1h	1h	1h
To enable the 32-bit timer chained mode for continuous operation	1h	1h	2h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.4.2.1.2 32-Bit Timer Chained Mode Configuration Procedure

To configure the GP timer to operate as a dual 32-bit chained mode timer, follow the steps below:

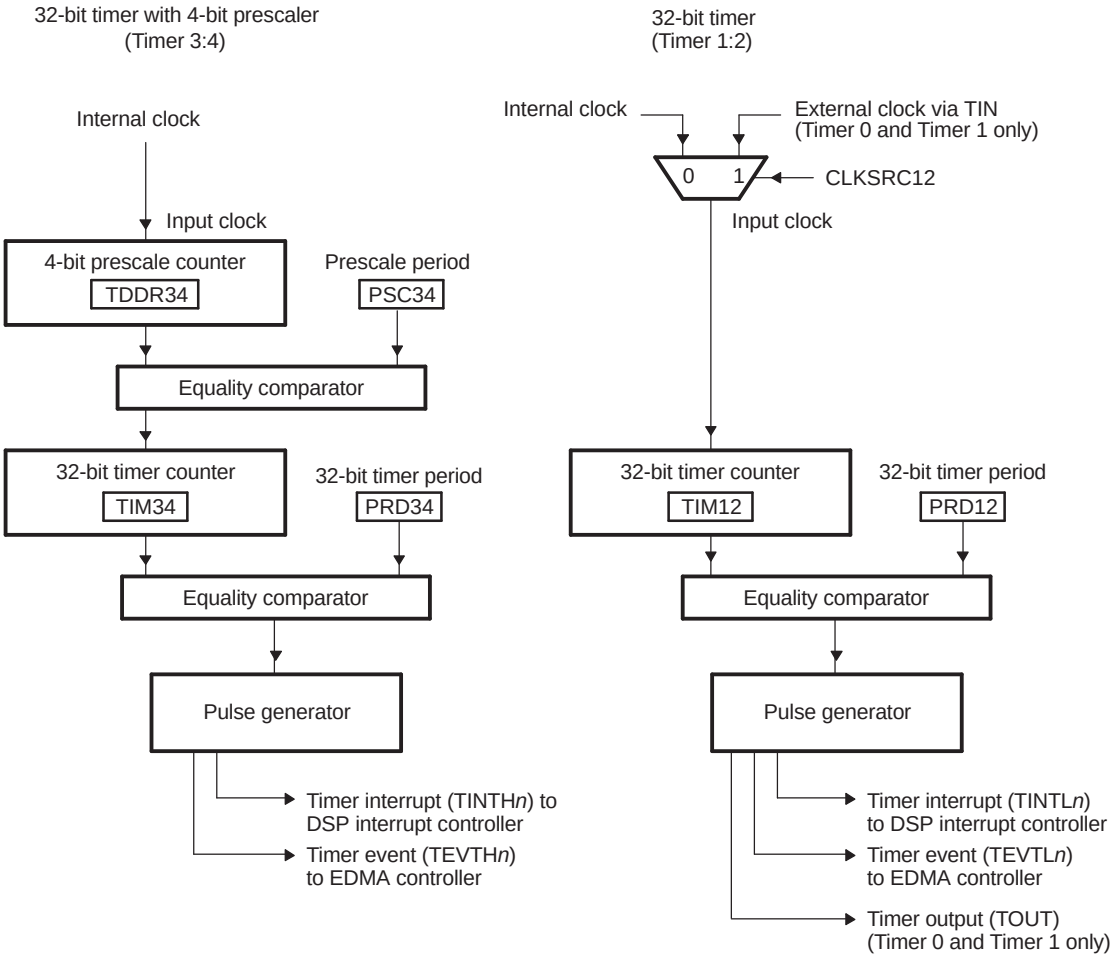
1. Perform necessary device pin multiplexing setup (see the device-specific data manual).
2. Program the VDD3P3V_PWDN register to power up the IO pins for Timer 0 and Timer 1 (see the device-specific data manual).
3. Select clock source (CLKSRC bit in TCR).
4. Select output mode (CP bit in TCR).
5. Select pulse width mode (PWID bit in TCR).
6. Consider ÷6 requirements (TINP0SEL bit in TIMERCTL in system module).
7. Consider inverter requirements (INVINP and INVOUTP bits in TCR).
8. Select 32-bit chained mode (TIMMODE bit in TCR).
9. Remove the timer from reset (TIM12RS and TIM34RS bits in TGCR).
10. Select the desired timer period (PRD12).
11. Select the desired timer prescaler value (PRD34).
12. Enable the timer (ENAMODE12 bit field in TCR).

2.4.2.2 Unchained Mode

The general-purpose timers can each be configured as a dual 32-bit unchained timers (Figure 6) by setting the TIMMODE bit to 1 in TGCR.

In the unchained mode, the timer operates as two independent 32-bit timers. One 32-bit timer (Timer 3:4) operates as a 32-bit timer being clocked by a 4-bit prescaler. The other 32-bit timer (Timer 1:2) operates as a 32-bit timer with no prescaler.

Figure 6. Dual 32-Bit Timers Unchained Mode Block Diagram

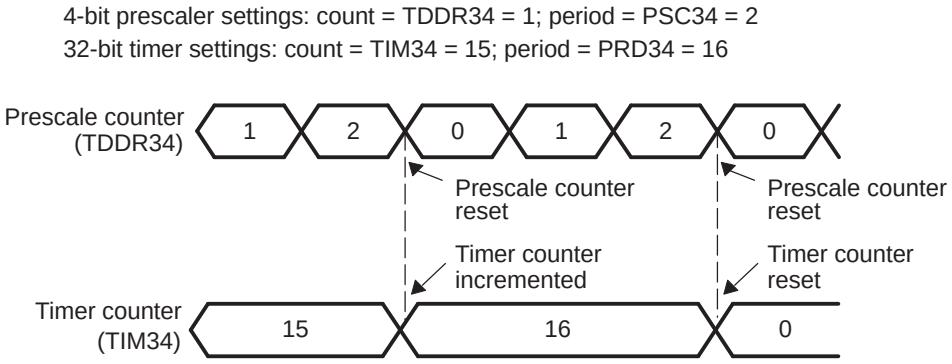


2.4.2.2.1 32-Bit Timer With a 4-Bit Prescaler

In the unchained mode, the 4-bit prescaler must be clocked by the internal clock; an external clock source cannot be used for Timer 3:4. The 4-bit prescaler uses the timer divide-down ratio (TDDR34) bit in TGCR to form a 4-bit prescale counter register and the prescale counter bits (PSC34) to form a 4-bit prescale period register (see Figure 6). When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated for the 32-bit timer.

The 32-bit timer uses TIM34 as a 32-bit timer counter register and PRD34 as a 32-bit timer period registers. The 32-bit timer is clocked by the output clock from the 4-bit prescaler (see the example in Figure 7). The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINTH*n* for TIM34), a timer EDMA sync event (TEVTH*n* for TIM34), and an output signal (TOUT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM34RS bit in TGCR. For Timer 3:4, the lower 16 bits of the timer control register (TCR) have no control.

Figure 7. Dual 32-Bit Timers Unchained Mode Example



2.4.2.2.2 32-Bit Timer with No Prescaler

The other 32-bit timer (Timer 1:2) uses TIM12 as the 32-bit counter register and PRD12 as a 32-bit timer period register (see Figure 6). When the timer is enabled, the timer counter increments by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINTL*n*), a timer EDMA sync event (TEVTL*n*), and an output signal (TOUT) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS bit in TGCR. For Timer 1:2, the upper 16 bit of the timer control register (TCR) have no control.

2.4.2.2.3 Enabling the 32-Bit Unchained Mode Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the Timer 1:2 side of the timer and the TIM34RS bit controls the reset of the Timer 3:4 side of the timer. For the timer to operate, the TIM12RS and/or TIM34RS bits must be set to 1.

The ENAMODE*n* bit field in the timer control register (TCR) controls whether the timer is disabled, enabled to run once or enabled to run continuously. When the timer is disabled (ENAMODE*n* = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE*n* = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE*n* = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 6 shows the bit values in TGCR to configure the 32-bit timer in unchained mode.

Table 6. 32-Bit Timer Unchained Mode Configurations

	TGCR Bit		TCR Bit	
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**	**ENAMODE34**
To place the 32-bit timer unchained mode with 4-bit prescaler in reset	x	0	x	0
To disable the 32-bit timer unchained mode with 4-bit prescaler (out of reset)	x	1h	x	0
To enable the 32-bit timer unchained mode with 4-bit prescaler for one-time operation	x	1h	x	1h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation	x	1h	x	2h
To place the 32-bit timer unchained mode with no prescaler in reset	0	x	0	x
To disable the 32-bit timer unchained mode with no prescaler (out of reset)	1h	x	0	x
To enable the 32-bit timer unchained mode with no prescaler for one-time operation	1h	x	1h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation	1h	x	2h	x

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock. External clock is only available on the Timer 1:2 side in unchained mode.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.4.2.2.4 32-Bit Timer Unchained Mode Configuration Procedure

To configure Timer 1:2, follow the steps below:

1. Perform necessary device pin multiplexing setup (see the device-specific data manual).
2. Program the VDD3P3V_PWDN register to power up the IO pins for Timer 0 and Timer 1 (see the device-specific data manual).
3. Select output mode (CP bit in TCR).
4. Select pulse width mode (PWID bit in TCR).
5. Consider ÷6 requirements (TINP0SEL bit in TIMERCTL in system module).
6. Consider inverter requirements (INVINP and INVOUTP bits in TCR).
7. Select 32-bit unchained mode (TIMMODE bit in TGCR).
8. Remove the Timer 1:2 from reset (TIM12RS bit in TGCR).
9. Select the desired timer period for Timer 1:2 (PRD12).
10. Select the desired clock source for Timer 1:2 (CLKSRC12 bit in TCR).
11. Enable Timer 1:2 (ENAMODE12 bit field in TCR).

To configure Timer 3:4, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE bit in TGCR).
2. Remove the Timer 3:4 from reset (TIM34RS bit in TGCR).
3. Select the desired timer period for Timer 3:4 (PRD34).
4. Select the desired prescaler value for Timer 3:4 (PSC34 bit in TGCR).
5. Enable Timer 3:4 (ENAMODE34 bit field in TCR).

2.4.3 Counter and Period Registers Used in GP Timer Modes

Table 7 summarizes how the counter registers (TIM*n*) and period registers (PRD*n*) are used in each GP timer mode.

Table 7. Counter and Period Registers Used in GP Timer Modes

Timer Mode	Counter Registers	Period Registers
64-bit general-purpose	TIM34:TIM12	PRD34:PRD12
Dual 32-bit chained		
Prescaler (Timer 3:4)	TIM34	PRD34
Timer (Timer 1:2)	TIM12	PRD12
Dual 32-bit unchained		
Timer (Timer 1:2)	TIM12	PRD12
Timer with prescaler (Timer 3:4)	TDDR34 bits	PSC34 bits

2.5 Timer Operation Boundary Conditions

The following boundary conditions affect the timer operation.

2.5.1 Timer Counter Overflow

Timer counter overflow can happen when the timer counter register is set to a value greater than the value in the timer period register. The counter reaches its maximum value (FFFF FFFFh or FFFF FFFF FFFF FFFFh), rolls over to 0, and continues counting until it reaches the timer period. An example is in Figure 8.

Figure 8. 32-Bit Timer Counter Overflow Example

2.5.2 Writing to Registers of an Active Timer

Writes to the timer registers are not allowed when the timer is active, except for stopping or resetting the timers. In the 64-bit and dual 32-bit timer modes, registers that are protected by hardware are:

- TIM12
- TIM34
- PRD12
- PRD34
- TCR (except the ENAMODE*n* bit field)
- TGCR (except the TIM12RS and TIM34RS bits)

2.6 General-Purpose Timer Power Management

The timer can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320C642x DSP Power and Sleep Controller (PSC) User's Guide* (SPRUEN8). The timer can be placed in an idle mode to conserve power when it is not being used.

2.7 Endianness Considerations

There are no endianness considerations for the Timer peripheral.

3 Architecture – Watchdog Timer Mode

This section describes the use of Timer 2 as a Watchdog Timer. Timer 0 and Timer 1 can only be used as general-purpose timers; to use Timer 0 or Timer 1 as general-purpose timers, see Section 2.

3.1 Watchdog Timer

Timer 2 can be configured only as a 64-bit Watchdog Timer. As a Watchdog Timer, it can be used to prevent system lockup when the software becomes trapped in loops with no controlled exit.

After a hardware reset, the Watchdog Timer is disabled. The timer should then be configured as a Watchdog Timer using the timer mode (TIMMODE) bit in the timer global control register (TGCR) and the watchdog timer enable (WDEN) bit in the watchdog timer control register (WDTCR). The Watchdog Timer requires a special service sequence to be executed periodically. Without this periodic servicing, the timer counter increments until it matches the timer period and causes a watchdog timeout event.

When the timeout event occurs, the Watchdog Timer could reset the entire processor depending on how the watchdog reset (WDRST) bit located in the timer control register (TIMERCTL) within the System Module is programmed. If the WDRST bit is set to 1, then a Watchdog Timer event causes a device reset. If the WDRST bit is cleared to 0, then a Watchdog Timer event does not cause a device reset. For more details on this feature and TIMERCTL, refer to your device data manual.

3.2 Watchdog Timer Mode Restrictions

The Watchdog Timer mode has the following restrictions:

- No external clock source
- No one-time enabling

3.3 Watchdog Timer Mode Operation

The Watchdog Timer mode is selected and enabled when:

- TIMMODE = 2h in TGCR
- WDEN = 1 in WDTCR

Figure 9 shows the Watchdog Timer. The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit period register. When the timer counter matches the timer period, the timer generates interrupt signal (WDINT) and a watchdog timeout event, which can reset the entire processor if the WDRST bit in the System Module's TIMERCTL register is set.

To activate the Watchdog Timer, a certain sequence of events must be followed, as shown in the state diagram of Figure 10.

Once the Watchdog Timer is activated, it can be disabled only by a watchdog timeout event, given that the WDRST bit in TIMERCTL is set to 1, or by a hardware reset. A special key sequence is required to prevent the Watchdog Timer from being accidentally serviced while the software is trapped in a loop or by some other software failure.

Figure 9. Watchdog Timer Mode Block Diagram

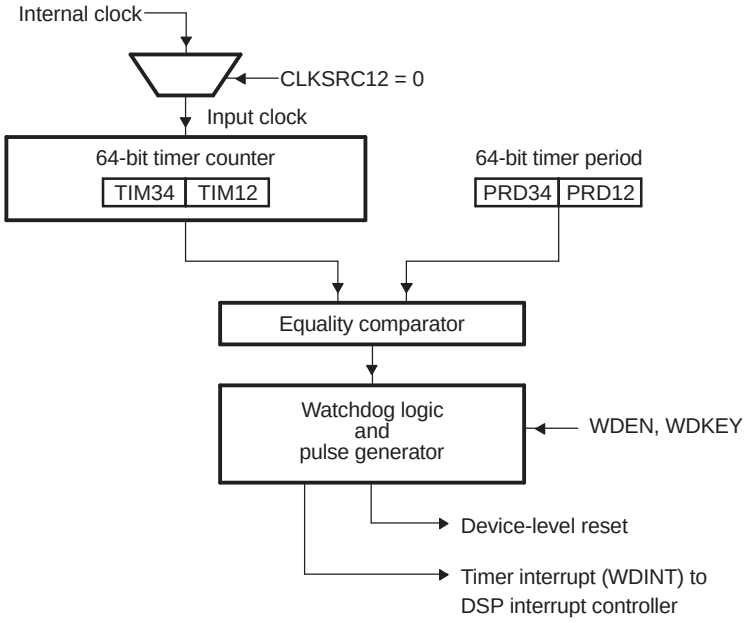
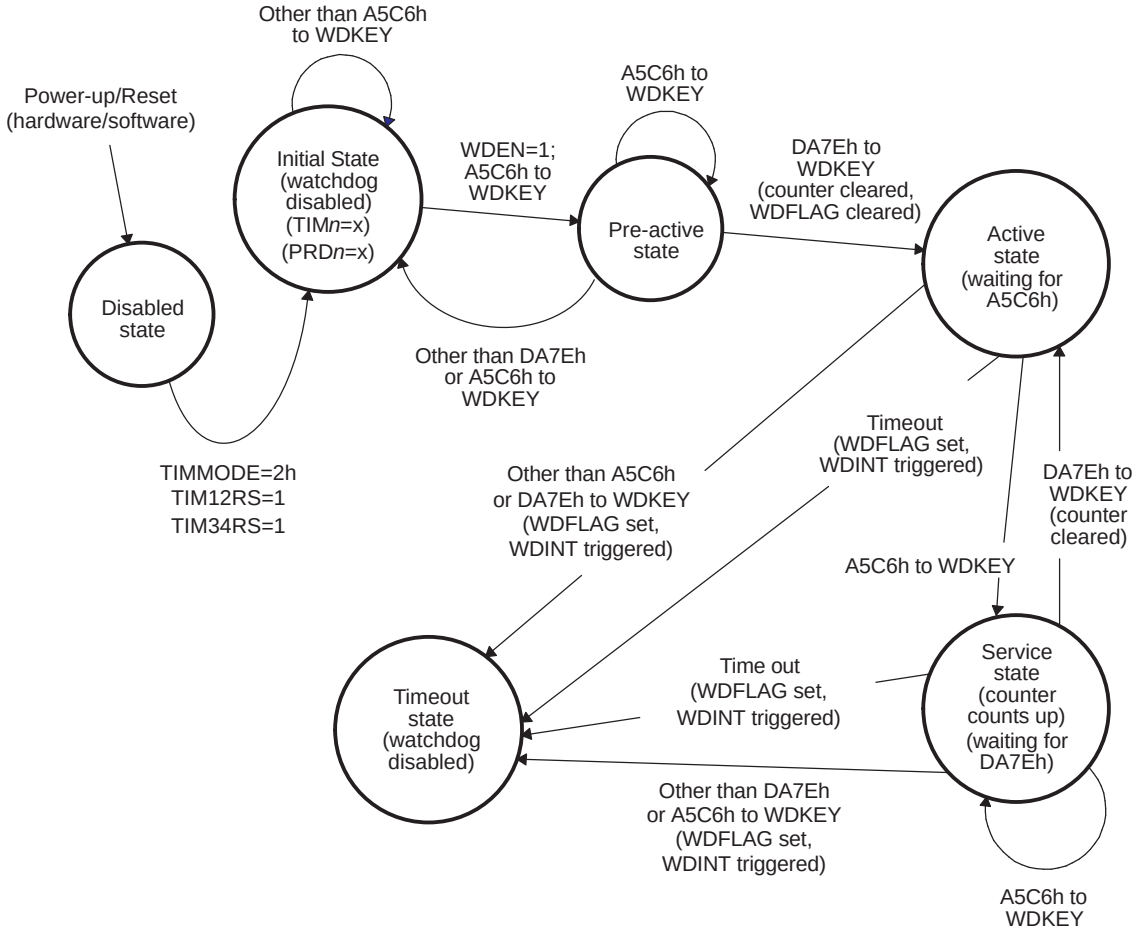


Figure 10. Watchdog Timer Operation State Diagram



To prevent a watchdog timeout event, the timer has to be serviced periodically by writing A5C6h followed by DA7Eh to the watchdog timer service key (WDKEY) bits in WDTCR before the timer finishes counting up. Both A5C6h and DA7Eh are allowed to be written to the WDKEY bits, but only the correct sequence of A5C6h followed by DA7Eh to the WDKEY bits services the Watchdog Timer. Any other writes to the WDKEY bits triggers the watchdog timeout event immediately.

When the Watchdog Timer is in the Timeout state, the Watchdog Timer is disabled, the WDEN bit is cleared to 0, and the timer is reset. After entering the Timeout state, the Watchdog Timer cannot be enabled again until a hardware reset occurs.

After a hardware reset, the Watchdog Timer is disabled; however, reads or writes to the Watchdog Timer registers are allowed. Once the WDEN bit is set (enabling the Watchdog Timer) and A5C6h is written to the WDKEY bits, the Watchdog Timer enters the Pre-active state. In the Pre-active state:

- A write to WDTCR is allowed only when the write comes with the correct key (A5C6h or DA7Eh) to the WDKEY bits.
- A write of DA7Eh to the WDKEY bits when the WDEN bit is set to 1 resets the counters and activates the Watchdog Timer.

The Watchdog Timer must be configured before the Watchdog Timer enters the Active state. The WDEN bit must be set to 1 before writing DA7Eh to the WDKEY bits in the Pre-active state. Every time the Watchdog Timer is serviced by the correct WDKEY sequence, the Watchdog Timer counter is automatically reset.

3.4 Watchdog Timer Register Write Protection

Once the Watchdog Timer enters the Pre-active state (see Figure 10), registers TIM12, TIM34, PRD12, PRD34, and WDTCR are write protected (except for the WDKEY field). While the Watchdog Timer is in the Timeout state, writing to the WDEN bit has no effect.

Once the Watchdog Timer enters its Initial state (see Figure 10), writes to the timer global control register (TGCR) are prohibited.

3.5 Watchdog Timer Power Management

The Watchdog Timer cannot be placed in power-down mode.

4 Reset Considerations

The timer has two reset sources: hardware reset and the timer reset (TIM12RS and TIM34RS) bits in the timer global control register (TGCR).

4.1 Software Reset Considerations

When the TIM12RS bit in TGCR is cleared to 0, the TIM12 register is held with the current value.

When the TIM34RS bit in TGCR is cleared to 0, the TIM34 register is held with the current value.

Emulator software reset: In the event of an emulator software reset, the timer register values are unaffected.

4.2 Hardware Reset Considerations

When a hardware reset is asserted, all timer registers are set to their default values.

5 Interrupt Support

Each of the timers can send either one of two separate interrupt events (TINT*n*) to the DSP, depending on the operating mode of the timer. The timer interrupts are generated when the count value in the counter register reaches the value specified in the period register.

Table 8 shows the interrupts generated in each mode on each instance of the timer.

Table 8. Timer Interrupts Generated

Timer Mode	Timer 0	Timer 1	Timer 2
64-bit mode	TINTL0	TINTL1	-
32-bit chained mode	TINTL0	TINTL1	-
32-bit unchained mode without prescaler (Timer 1:2)	TINTL0	TINTL1	-
32-bit unchained mode with prescaler (Timer 3:4)	TINTH0	TINTH1	-
Watchdog mode	-	-	WDINT

6 EDMA Event Support

Timer 0 and Timer 1 can send either one of two separate timer events (TEVT*n*) to the EDMA, depending on the operating mode the timer. The timer events are generated when the count value in the counters register reaches the value specified in the period register.

Table 9 shows the EDMA events generated in each mode on each instance of the timer.

Table 9. Timer EDMA Events Generated

Timer Mode	Timer 0	Timer 1	Timer 2
64-bit mode	TEVTL0	TEVTL1	-
32-bit chained mode	TEVTL0	TEVTL1	-
32-bit unchained mode without prescaler (Timer 1:2)	TEVTL0	TEVTL1	-
32-bit unchained mode with prescaler (Timer 3:4)	TEVTH0	TEVTH1	-
Watchdog mode	-	-	-

7 Emulation Considerations

Each timer has an emulation management register (EMUMGT). As shown in Table 10, the FREE and SOFT bits of EMUMGT determine how the timer responds to an emulation suspend event. An emulation suspend event corresponds to any type of emulator access where the emulator temporarily stops the processor.

Table 10. Timer Emulation Modes Selection

FREE	SOFT	Emulation Mode
0	0	The timer stops immediately.
0	1	The timer stops when the timer counter value increments and reaches the value in the timer period register.
1	x	The timer runs free regardless of SOFT bit status.

Note that during emulation, the timer count values will increment once every timer peripheral clock (not CPU clock). So when single-stepping though code, the timer values will not update on every CPU clock cycle.

8 Registers

Table 11 lists the memory-mapped registers for the 64-bit timer. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified. For details on using ÷6 mode for Timer 0 or watchdog reset enable that are set in the timer control register (TIMERCTL) within the System Module, refer to your device data manual.

Table 11. 64-Bit Timer Registers

Offset	Acronym	Register Description	Section
00h	PID12	Peripheral Identification Register 12	Section 8.1
04h	EMUMGT	Emulation Management Register	Section 8.2
10h	TIM12	Timer Counter Register 12	Section 8.3
14h	TIM34	Timer Counter Register 34	Section 8.3
18h	PRD12	Timer Period Register 12	Section 8.4
1Ch	PRD34	Timer Period Register 34	Section 8.4
20h	TCR	Timer Control Register	Section 8.5
24h	TGCR	Timer Global Control Register	Section 8.6
28h	WDTCR	Watchdog Timer Control Register	Section 8.7

8.1 Peripheral Identification Register 12 (PID12)

The peripheral ID register 12 (PID12) contains identification data (type, class, and revision) for the peripheral. The PID12 is shown in Figure 11 and described in Table 12.

Figure 11. Peripheral Identification Register 12 (PID12)

31	23	22	16
Reserved		TYPE	
R-0		R-01h	

15	8	7	0
CLASS		REVISION	
R-07h		R-01h	

LEGEND: R = Read only; -*n* = value after reset

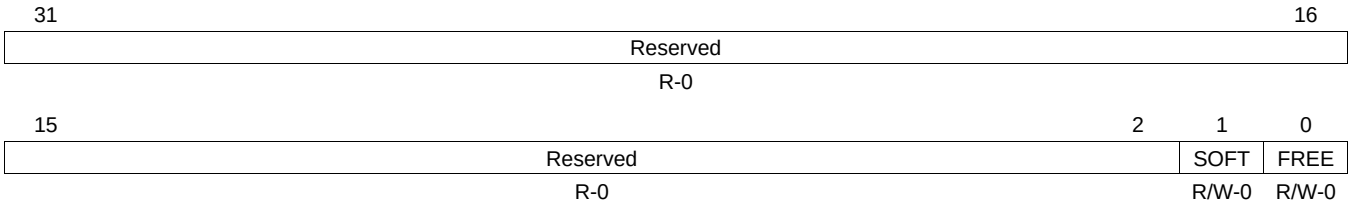
Table 12. Peripheral Identification Register 12 (PID12) Field Descriptions

Bit	Field	Value	Description
31-23	Reserved	0	Reserved
22-16	TYPE		Identifies type of peripheral
		01h	Timer
15-8	CLASS		Identifies class of peripheral
		07h	Timer
7-0	REVISION		Identifies revision of peripheral.
		01h	Current revision of peripheral.

8.2 Emulation Management Register (EMUMGT)

The emulation management register (EMUMGT) is shown in Figure 12 and described in Table 13.

Figure 12. Emulation Management Register (EMUMGT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Emulation Management Register (EMUMGT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	SOFT		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The timer stops immediately.
		1	The timer stops when the counter increments and reaches the value in the timer period register (PRD*n*).
0	FREE		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The SOFT bit selects the timer mode.
		1	The timer runs free regardless of the SOFT bit.

8.3 Timer Counter Registers (TIM12 and TIM34)

The timer counter register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, TIM12 and TIM34.

In the dual 32-bit timer mode, the 64-bit register is divided with TIM12 acting as one 32-bit counter and TIM34 acting as another. These two registers can be configured as chained or unchained.

8.3.1 Timer Counter Register 12 (TIM12)

The timer counter register 12 (TIM12) is shown in Figure 13 and described in Table 14

Figure 13. Timer Counter Register 12 (TIM12)

31	16
TIM12	
R/W-0	

15	0
TIM12	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 14. Timer Counter Register 12 (TIM12) Field Descriptions

Bit	Field	Value	Description
31-0	TIM12	0-FFFF FFFFh	TIM12 count bits. This 32-bit value is the current count of the main counter.

8.3.2 Timer Counter Register 34 (TIM34)

The timer counter register 34 (TIM34) is shown in Figure 14 and described in Table 15.

Figure 14. Timer Counter Register 34 (TIM34)

31	16
TIM34	
R/W-0	

15	0
TIM34	
R/W-0	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 15. Timer Counter Register 34 (TIM34) Field Descriptions

Bit	Field	Value	Description
31-0	TIM34	0-FFFF FFFFh	TIM34 count bits. This 32-bit value is the current count of the main counter.

8.4 Timer Period Registers (PRD12 and PRD34)

The timer period register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, PRD12 and PRD34.

Similar to TIM*n* in the dual 32-bit timer mode, PRD*n* can be divided into 2 registers: for Timer 1:2, PRD12 and for Timer 3:4, PRD34. These two registers can be used in conjunction with the two timer counter registers TIM12 and TIM34.

8.4.1 Timer Period Register (PRD12)

The timer period register 12 (PRD12) is shown in Figure 15 and described in Table 16.

Figure 15. Timer Period Register 12 (PRD12)

31	16
PRD12	
R/W-0	

15	0
PRD12	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 16. Timer Period Register (PRD12) Field Descriptions

Bit	Field	Value	Description
31-0	PRD12	0-FFFF FFFFh	PRD12 period bits. This 32-bit value is the number of timer input clock cycles to count.

8.4.2 Timer Period Register 34 (PRD34)

The timer period register 34 (PRD34) is shown in Figure 16 and described in Table 17.

Figure 16. Timer Period Register 34 (PRD34)

31	16
PRD34	
R/W-0	

15	0
PRD34	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 17. Timer Period Register (PRD34) Field Descriptions

Bit	Field	Value	Description
31-0	PRD34	0-FFFF FFFFh	PRD34 period bits. This 32-bit value is the number of timer input clock cycles to count.

8.5 Timer Control Register (TCR)

The timer control register (TCR) is shown in Figure 17 and described in Table 18.

Figure 17. Timer Control Register (TCR)

31	24	23	22	21	16
Reserved		ENAMODE34		Reserved	
R-0		R/W-0		R-0	

15	9	8	7	6	5	4	3	2	1	0
Reserved		CLKSRC12	ENAMODE12		PWID		CP	INVINP	INVOUTP	TSTAT
R-0		R/W-0	R/W-0		R/W-0		R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Timer Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-22	ENAMODE34	0-3h	ENAMODE34 determines the enabling modes of the timer. Note that ENAMODE34 is applicable only when the timer is configured in dual 32-bit unchained timer mode (TIMMODE = 1h in TGCR).
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.
21-9	Reserved	0	Reserved
8	CLKSRC12		CLKSRC12 determines the selected clock source for the timer.
		0	Internal clock
		1	Timer input pin
7-6	ENAMODE12	0-3h	ENAMODE12 determines the enabling modes of the timer.
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.
5-4	PWID	0-3h	Pulse width bits. PWID is only used in pulse mode (CP = 0). PWID controls the width of the timer output signal. The polarity of the pulse is controlled by the INVOUT bit. The timer output signal is recorded in the TSTAT bit and can be made visible on the timer output pin.
		0	The pulse width is 1 timer clock cycle.
		1	The pulse width is 2 timer clock cycle.
		2h	The pulse width is 3 timer clock cycle.
		3h	The pulse width is 4 timer clock cycle.
3	CP		Clock/pulse mode bit for timer output. In the Watchdog Timer mode (TIMMODE = 2h in TGCR), the pulse mode is selected automatically and the CP bit is a don't care.
		0	Pulse mode. When the timer counter reaches the timer period, the timer output appears as a pulse with the width defined by the PWID bits and the polarity defined by the INVOUT bits.
		1	Clock mode. The timer output signal has a 50% duty cycle signal. When the timer counter reaches the timer period, the level of the timer output signal is toggled (from high to low or from low to high).
2	INVINP		Timer input inverter control. Only affects operation if CLKSRC12 = 1. This mode is affected when ÷6 is enabled, TINP0SEL = 1 in TIMERCTL (in the System Module). This will cause the divided result to be inverted.
		0	A noninverted timer input drives the timer.
		1	An inverted timer input drives the timer.

Table 18. Timer Control Register (TCR) Field Descriptions (continued)

Bit	Field	Value	Description
1	INVOUTP		Timer output inverter control bit.
		0	The timer output is not inverted.
		1	The timer output is inverted.
0	TSTAT		Timer status bit. This is a read-only bit that shows the value of the timer output. TSTAT drives the timer output pin and may be inverted by setting INVOUTP = 1.
		0	Timer output is low.
		1	Timer output is high.

8.6 Timer Global Control Register (TGCR)

The timer global control register (TGCR) is shown in Figure 18 and described in Table 19.

Figure 18. Timer Global Control Register (TGCR)

31					16
Reserved					
R-0					
15	12	11			8
TDDR34		PSC34			
R/W-0		R/W-0			
7	4	3	2	1	0
Reserved		TIMMODE		TIM34RS	TIM12RS
R-0		R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Timer Global Control Register (TGCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	TDDR34	0-Fh	Timer linear divide-down ratio specifies the timer divide-down ratio for Timer 3:4. When the timer is enabled, TDDR34 increments every timer clock. The TIM34 counter increments on the cycle after TDDR34 matches PSC34. TDDR34 resets to 0 and continues. When TIM34 matches PRD34, Timer 3:4 stops, if Timer 3:4 is enabled one time; TIM34 resets to 0 on the cycle after matching PRD34 and Timer 3:4 continues, if Timer 3:4 is enabled continuously.
11-8	PSC34	0-Fh	TIM34 pre-scalar counter specifies the count for Timer 3:4.
7-4	Reserved	0	Reserved
3-2	TIMMODE	0-3h	TIMMODE determines the timer mode.
		0	The timer is in 64-bit GP timer mode.
		1h	The timer is in dual 32-bit timer unchained mode.
		2h	The timer is in 64-bit Watchdog Timer mode.
		3h	The timer is in dual 32-bit timer, chained mode.
1	TIM34RS		Timer 3:4 reset.
		0	Timer 3:4 is in reset.
		1	Timer 3:4 is not in reset. Timer 3:4 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.
0	TIM12RS		Timer 1:2 reset.
		0	Timer 1:2 is in reset.
		1	Timer 1:2 is not in reset. Timer 1:2 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.

8.7 Watchdog Timer Control Register (WDTCR)

The watchdog timer control register (WDTCR) is shown in Figure 19 and described in Table 20.

Figure 19. Watchdog Timer Control Register (WDTCR)

31	16
WDKEY	
R/W-0	

15	14	13 12	11 0
WDFLAG	WDEN	Reserved	Reserved
R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Watchdog Timer Control Register (WDTCR) Field Descriptions

Bit	Field	Value	Description
31-16	WDKEY	0-FFFFh	16-bit watchdog timer service key. Only the sequence of an A5C6h followed by a DA7Eh services the Watchdog Timer. Not applicable in general-purpose timer mode.
15	WDFLAG		Watchdog flag bit. WDFLAG can be cleared by enabling the Watchdog Timer, by device reset, or being written with 1. It is set by a watchdog time-out.
		0	No watchdog time-out occurred.
		1	Watchdog time-out occurred.
14	WDEN		Watchdog timer enable bit.
		0	Watchdog disabled.
		1	Watchdog enabled.
13-12	Reserved	0-3h	Reserved. This bit field must be written as 00b.
11-0	Reserved	0	Reserved

Appendix A Revision History

Table 21 lists the changes made since the previous version of this document.

Table 21. Document Revision History

Reference	Additions/Modifications/Deletions
Section 2.1.1	Changed first paragraph.

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