TMS320C645x DSP Peripherals Overview

Reference Guide

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Read This First

About This Manual

This document provides an overview and briefly describes the peripherals available on the TMS320C645x DSP.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C6455 Technical Reference (literature number SPRU965) gives an introduction to the TMS320C6455™ DSP and discusses the application areas that are enhanced.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C64x+ Megamodule Reference Guide (literature number SPRU871) describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

TMS320C645x DSP Peripherals Overview Reference Guide (literature number SPRUE52) provides a brief description of the peripherals available on the TMS320C645x digital signal processors (DSPs).

TMS320C6455 Chip Support Libraries (CSL) (literature number SPRC234) is a download with the latest chip support libraries.

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TMS320C645x DSP Peripherals Overview

1 Overview

The new C64x+ core extends the performance leadership by offering more multiplication bandwidth, higher data bandwidth, and smaller code size than the C64x core. The TMS320C6455 DSP, one of the first devices to employ the C64x+ core, has several high bandwidth external interfaces. The C6455 device is the first broad market DSP to incorporate a serial rapid I/O (SRIO) interface to provide inter-DSP communication. The SRIO interface can operate as a 4x serial bi-directional link at 12.5 Gbits/sec which is fast enough to transmit an uncompressed high-definition 1080p video stream between processors. There are two external memory interfaces; one is a 32-bit double data rate (DDR2) interface that provides up to 2GB/sec of memory bandwidth and the other is a 64-bit interface to both synchronous and asynchronous memories. Additionally, C6455 DSP developers can use a 1Gbit Ethernet interface to network to an IP backplane with eight independent transmit and receive channels. A 66MHz PCI interface is also provided to connect to a PCI host. Data movement in the system is facilitated by an internal enhanced direct memory access (EDMA3) engine capable of providing over 5GB/sec with 64 independent channels.

The C6455 DSP utilizing the C64x+ core is object code-compatible with the C64x generation, yet extends the performance leadership by offering greater multiplication bandwidth, higher I/O bandwidth, and larger and more flexible on-chip memory while addressing code size and system issues such as memory protection and privilege.

The user-accessible peripherals available on the C645x DSP are configured using a set of memory-mapped control registers. Peripherals available on the C645x DSP and their associated literature numbers are listed in Table 1.

Table 1. TMS320C645x DSP Peripherals Documentation

Peripheral/Module	Acronym	Lit #
General-Purpose Input/Output	GPIO	SPRU724
Enhanced Direct Memory Access (EDMA3) Controller	EDMA	SPRU966
64-Bit Timer	Timer	SPRU968
Host Port Interface	HPI	SPRU969
DDR2 Memory Controller	DDR2	SPRU970
External Memory Interface	EMIF	SPRU971
Inter-Integrated Circuit Module	I2C	SPRU974
Ethernet Media Access Controller/Management Data Input/Output Module	EMAC/MDIO	SPRU975
Universal Test & Operations PHY Interface for ATM 2	UTOPIA2	SPRUE48
Software-Programmable Phase-Locked Loop	PLL	SPRUE56

2 General-Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA synchronization events in different interrupt/event generation modes.

3 Enhanced Direct Memory Access (EDMA) Controller

This document describes the features and operations of the enhanced direct memory access (EDMA3) controller in the TMS320C645x digital signal processor (DSP). The EDMA3 is a high-performance, multichannel, multithreaded DMA controller that allows you to program a wide variety of transfer geometries and transfer sequences.

The enhanced direct memory access (EDMA3) controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the device. Typical usage includes, but is not limited to:

- Servicing software driven paging transfers (for example, from external memory such as SDRAM to internal device memory such as DSP L2 SRAM)
- Servicing event driven peripherals, such as a serial port or UTOPIA peripheral
- Performing sorting or subframe extraction of various data structures
- Offloading data transfers from the main device CPU(s) or DSP(s)
- See the device data manual for specific peripherals that are accessible via EDMA3 controller

The EDMA3 controller has a different architecture from the previous EDMA2 controller on the TMS320C621x/C671x DSPs and TMS320C64x DSPs. (See the *EDMA v3.0 (EDMA3) Migration Guide for TMS320C645x DSP* (SPRAAB9) for more details on new/advanced features.)

4 64-Bit Timer

The timer can be configured as a general-purpose 64-bit timer, dual general-purpose 32-bit timers, or a watchdog timer. When configured as a dual 32-bit timers, each half can operate in conjunction (chain mode) or independently (unchained mode) of each other.

The timer can be configured in one of three modes using the timer mode (TIMMODE) bits in the timer global control register (TGCR): a 64-bit general-purpose (GP) timer, dual 32-bit timers (TIMLO and TIMHI), or a watchdog timer. When configured as dual 32-bit timers, each half can operate dependently (chain mode) or independently (unchained mode) of each other. At reset, the timer is configured as a 64-bit GP timer. The watchdog timer function can be enabled if desired, via the TIMMODE bits in timer global control register (TGCR) and WDEN bit in the watchdog timer control register (WDTCR). Once the timer is configured as a watchdog timer, it cannot be re-configured as a regular timer until a device reset occurs. The timer has one input pin (TINPL) and one output pin (TOUTL). The timer control register (TCR) controls the function of the input and output pin.

5 Host Port Interface (HPI)

The HPI provides a parallel port interface through which an external host processor (host) can access DSP resources. The HPI enables a host device and CPU to exchange information via internal or external memory. Dedicated address and data registers (HPIA and HPID respectively) within the HPI provide the data path between the external host interface and the processor resources. An HPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions. The host functions as a master to the HPI. Host activity is asynchronous to the internal clock that drives the HPI. When HPI resources are temporarily busy or unavailable, the HPI informs the host by deasserting the HPI-ready (HRDY) output signal.

The HPI uses multiplexed operation, meaning the data bus carries both address and data. When the host drives an address on the bus, the address is stored in the address register (HPIA) in the HPI, so that the bus can then be used for data. The HPI supports two interface modes: HPI16 and HPI32 mode. DSP selects either HPI16 or HPI32 mode via the HPI_WIDTH device configuration pin at reset.

6 DDR2 Memory Controller (DDR2)

The DDR2 memory controller interfaces with JESD79D-2A standard compliant DDR2 SDRAM devices. Memory types such as DDR1 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR2 memory controller SDRAM can be used for program and data storage.

The DDR2 memory controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM
- 256 Mbyte memory space
- Data bus width of 32 or 16 bits
- CAS latencies: 2, 3, 4, and 5
- Internal banks: 1, 2, 4, and 8
- Burst length: 8
- Burst type: sequential
- 1 CE signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little-endian and big endian transfers

7 External Memory Interface (EMIF)

The C645x DSP External Memory Interface (EMIF) can interface to a variety of external devices, including:

- Pipelined and flow-through synchronous-burst SRAM (SBSRAM)
- ZBT (zero bus turnaround) SRAM and Late Write SRAM
- Synchronous FIFOs
- Asynchronous memory, including SRAM, ROM, and Flash

In this document, the term EMIF refers to the EMIFA of C645x devices. The EMIF services requests of the external bus from on-chip masters such as the enhanced direct-memory access (EDMA) controller and the C64x+ Megamodule, as well as external shared-memory device controllers (through the hold interface). On-chip masters place requests to the EMIF through the switched control resource (SCR). For more information on the SCR, see the device data manual.

8 Viterbi Decoder Coprocessor (VCP)

Channel decoding of voice and low bit-rate data channels found in third generation (3G) cellular standards requires decoding of convolutional encoded data. The Viterbi-decoder coprocessor 2 (VCP2) provided in C645x devices performs Viterbi-Decoding for IS2000 and 3GPP wireless standards. The VCP2 coprocessor also performs forward error correction for 2G and 3G wireless systems. The VCP2 coprocessor offers a very cost effective and synergistic solution when combined with Texas Instruments (TI) DSPs. The VCP2 can support 1941 12.2 Kbps class A 3G voice channels running at 333 MHz.

The VCP2 provides:

- High flexibility
  - Variable constraint length, K = 5, 6, 7, 8, or 9
  - User-supplied code coefficients
  - Code rates (½, 1/3, or 1/4)
  - Configurable trace back settings (convergence distance, frame structure)
  - Branch metrics calculation and depuncturing done in software by the DSP
- System and development cost optimization
  - The VCP2 releases DSP resources for other processing
  - Reduces board space and power consumption by performing decoding on-chip
  - Communication between the DSP and the VCP2 is performed through the high performance EDMA engine
  - Uses its own optimized working memories
  - Provides debug capabilities during frame processing
  - Libraries are provided for reduced development time

9 Turbo Decoder Coprocessor (TCP)

Channel decoding of high bit-rate data channels found in third generation (3G) cellular standards requires decoding of turbo-encoded data. The turbo-decoder coprocessor (TCP2) in some of the digital signal processor (DSPs) of the TMS320C6000 DSP family has been designed to perform this operation for IS2000 and 3GPP wireless standards. This document describes the operation and programming of the TCP2.

The TCP2 provides:

- High performance
  - Very low processing delay because of the highly paralleled architecture allowing 8 iterations of a 2Mbps 3GPP channel to be decoded in less than 1.2 ms and a IS-2000 channel in less than 1.2 ms.
  - Processing delay can be further reduced by enabling a stopping criteria algorithm while achieving optimal BER performance.
  - TCP2 and DSP can run full speed in parallel.
- System cost optimization
  - Reduces board space and power consumption by performing turbo-decoding on-chip.
  - Communication between the DSP and the TCP2 is performed through a high performance DMA engine, the enhanced DMA (EDMA).
  - TCP2 uses its own optimized memories, reducing system memory overhead and yielding higher overall performance.
  - Increased programmability
  - Power efficient, memory sleep mode, and module powersaver capabilities.

10 Inter-Integrated Circuit (I2C) Module

The inter-integrated circuit (I2C) module provides an interface between the TMS320C645x DSP and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the C645x DSP through the I2C module.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1)
  - Support for byte format transfer
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers mode
  - Support for multiple slave-transmitters and master-receivers mode
  - Combined master transmit/receive and receive/transmit mode
  - I2C data transfer rate of from 10 kbps up to 400 kbps (Philips I2C rate)
- 2 to 7 bit format transfer
- Free data format mode
- One read DMA event and one write DMA event that can be used by the DMA
- Seven interrupts that can be used by the CPU
- Interface to V-bus (32-bit synchronously slave bus)
- Module enable/disable capability

11 Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO) Module

This document provides a functional description of the Ethernet Media Access Controller (EMAC) and Physical layer (PHY) device Management Data Input/Output (MDIO) module integrated with the devices of the C645x family. Included are the features of the EMAC and MDIO modules, a discussion of their architecture and operation, how these modules connect to the outside world, and the registers description for each module.

The EMAC controls the flow of packet data from the processor to the PHY. The MDIO module controls PHY configuration and status monitoring. Both the EMAC and the MDIO modules interface to the DSP through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral.

12 Serial RapidIO (SRIO)

The RapidIO peripheral used in the TMS320C645x is serial RapidIO (SRIO).

RapidIO is a non-proprietary high-bandwidth system level interconnect. It is a packet-switched interconnect intended primarily as an intra-system interface for chip-to-chip and board-to-board communications at Gigabyte-per-second performance levels. Uses for the architecture can be found in connected microprocessors, memory, and memory mapped I/O devices that operate in networking equipment, memory subsystems, and general purpose computing. Principle objectives of RapidIO include:

- Flexible system architecture allowing peer-to-peer communication
- Robust communication with error detection features
- Frequency and port width scalability
- Non-software intensive
- High bandwidth interconnect with low overhead
- Low pin count
- Low power
- Low latency

13 Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2)

This document describes the universal test and operations PHY interface for asynchronous transfer mode [ATM] 2 (UTOPIA2) in the TMS320C645x digital signal processors (DSPs) of the TMS320C6000 DSP family.

The UTOPIA is an ATM controller (ATMC) slave device that interfaces to a master ATM controller. The UTOPIA port conforms to the ATM Forum standard specification af-phy-0039.000. Specifically, this interface supports the UTOPIA Level 2 interface that allows 8-bit slave operation up to 50 MHz for both transmit and receive operations.

The UTOPIA slave interface relies on the master ATM controller to provide the necessary control signals such as the clock, enable and address values. Only cell-level handshaking is supported.

The enhanced DMA (EDMA) controller can service the UTOPIA. The ATM Adaptation Layer (AAL) commonly called as Segmentation and Reassembly (SAR) functions should be performed in software.

14 Software Programmable Phase-Locked Loop (PLL) Controller

The PLL controller features a software-configurable PLL multiplier controller (PLLM) and dividers (PREDIV and D1-D16). The PLL controller offers flexibility and convenience with software-configurable multiplier and dividers to modify the input clock signal (CLKIN) internally. The resulting clock outputs are passed to the DSP core, peripherals, and other modules inside the DSP.

The PLL controller has one input clock and several output clocks.

- Input reference clock to the PLL controller:
  - CLKIN: Input signal from external oscillator
- Resulting output clocks from the PLL controller:
  - AUXCLK: Internal clock output signal directly from CLKIN
  - SYSCLK1 to SYSCLK16: System domain clocks, each output from its own divider

15 Peripheral Component Interconnect (PCI)

The peripheral component interconnect (PCI) module supports the following features:

- PCI Local Bus Specification (revision 2.3) compliant
- Provides single function PCI interface
- 32-bit address/data bus width
- Operation up to 66 MHz
- Supports optimized burst behavior for system cache line sizes of 16, 32, 64 and 128 bytes

The PCI operates as a PCI slave device for configuration cycles and memory cycles. It also acts as a PCI master device for configuration cycles, IO cycles, and memory accesses to other devices.

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