Application Note

Power Optimization Techniques for the AWR294x

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ABSTRACT

This application note help users with varying power constraints using the TI AWR2944 mmWave Sensor. Varying degrees of power optimization are possible on the sensor depending on the application and use case. Power optimization can be implemented in many different forms depending on what is appropriate for the use case. This document describes the implementation of different optimization techniques along with both the degree of power savings and associated design tradeoffs.

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Trademarks

1 Definitions, Abbreviations, Acronyms

Term	Definition
FMCW	Frequency Modulated Continuous Wave
SDK	Software Development Kit
MSS	Main subsystem
DSS	Digital signal processing subsystem
RSS	Radio Processing Subsystem
WFI	Wait for Interrupt
PLL	Phase-Locked Loop

2 Introduction

The AWR294x is a single-chip mmWave sensor composed of an FMCW transceiver, capable of operation in the 76GHz to 81GHz band, radar data processing elements, and peripherals for in-vehicle networking. TI mmWave Sensors enable high-performance measurement and object detection over a variety of applications, but some designs require minimal power consumption. This application note discusses various power-saving techniques on the mmWave sensor, where power consumption concerns are critical. This guide helps users to implement various optimizations for evaluation. Moreover, this document discusses the tradeoffs involved as well. The power-saving techniques discussed in this document can be implemented exclusively through software.

3 Device Architecture Overview

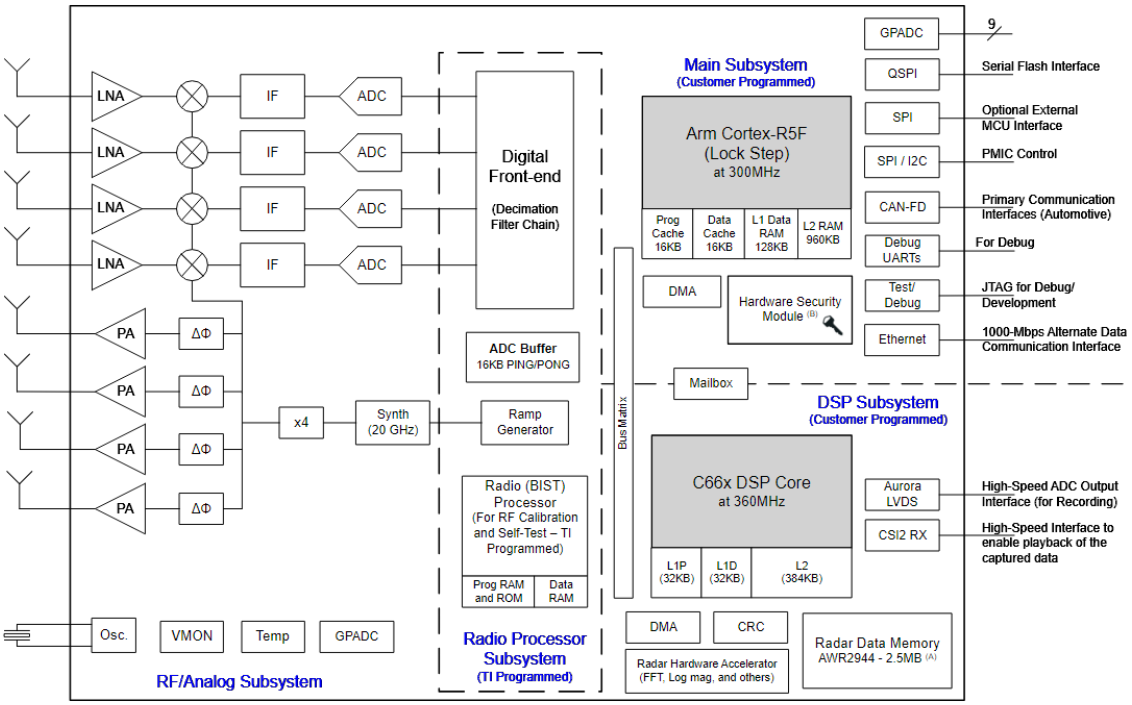

Figure 3-1. Device Block Diagram

The power consumption of AWR294x can be reduced by some techniques. These power reduction techniques can be achieved through appropriate programming of the MSS and DSP. The architecture of the AWR2944 allows the radar device to completely or partially power off specific blocks in different subsystems.

4 Key Power Consuming Blocks In AWR2944 Device

The AWR2944 device, a highly integrated single-chip radar sensor, incorporates several key power-consuming elements that are essential for advanced signal processing and transmission capabilities.

The main power-consuming components are as follows:

1. Transmitter (Tx) and Receiver (Rx) or Radar Front End: These blocks are responsible for generating and processing radar signals, and consume significant power due to high-frequency operations.
2. Digital signal processing subsystem (DSP SS): The C66x DSP core handles complex computations required for radar signal processing. The C66x DSP is one of the primary power consumers due to high processing capabilities.
3. Radar Hardware Accelerator (HWA): This component accelerates operations like Fast Fourier Transform (FFT), log magnitude calculations, and memory compression, which are essential for radar signal processing.
4. Arm® Cortex®-R5F Core: This core supports lock-step operation and is used for control and configuration tasks. This core also contributes significantly to the overall power consumption.
5. Phase-Locked Loop (PLL): The integrated PLL is used for frequency synthesis and contributes to power consumption, especially during signal transmission.
6. Analog-to-Digital Converters (ADCs): Multiple ADC channels are used to convert analog radar signals into digital form for processing. These converters also consume a considerable amount of power.

Understanding these components can help optimize power consumption and enhance the overall efficiency of the device.

5 Fundamental Power Optimization Strategies

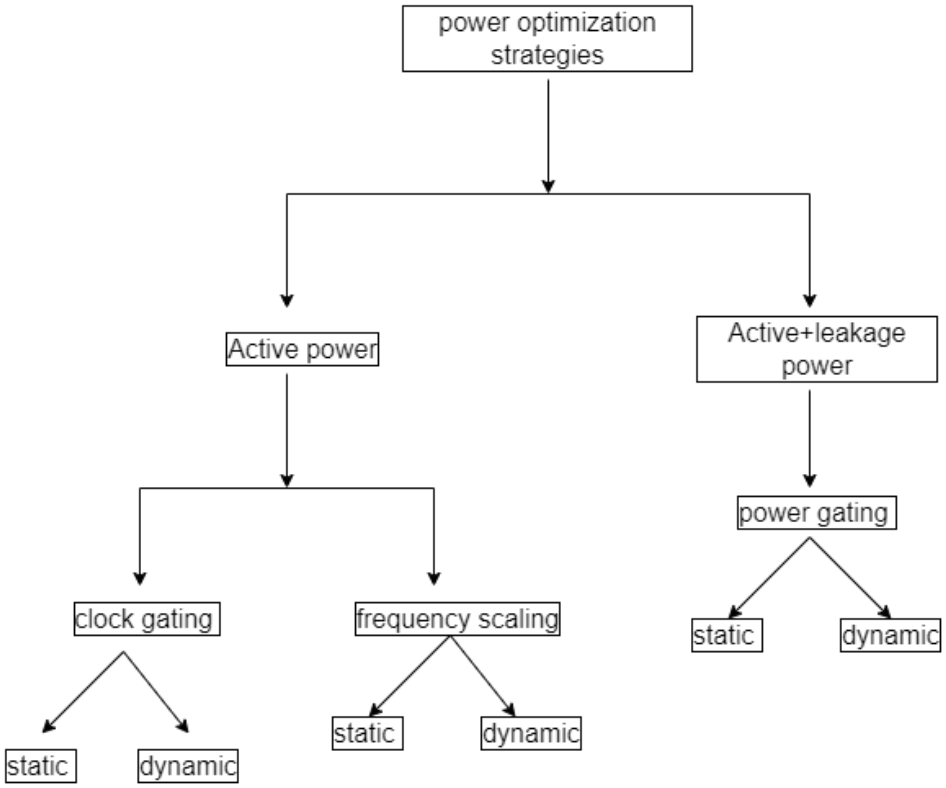

Figure 5-1. Basic Power Optimization Strategies

Following are the main techniques that can be used for power optimization as shown in the above fig –

1. Clock gating technique: clock gating is a power-saving technique used in digital circuits to reduce power consumption. Clock gating works by disabling the clock signal to certain parts of the circuit when those certain parts are not in use. This gating technique can further be divided into two types static and dynamic clock gating.

   In static clock gating, the clock to the unused modules, peripherals, and blocks has been disabled. In dynamic clock gating, the disabling or gating of the clock is being done for a specific duration. After that period of time, the clock can be restored to the previous state.

2. Frequency scaling technique: frequency scaling is a power management technique, where the frequency can be adjusted based on the use-case to save the power. This gating technique can further be divided into two types static and dynamic frequency scaling.

   In static frequency scaling, the frequency of a specific block or module is reduced based on the use case. In dynamic frequency scaling, the frequency of a specific module can be controlled for a particular duration and after that the frequency can be restored to the previous state.

3. Power gating technique: power gating is used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. Power gating technique can also be divided into two types, static and dynamic power gating.

   In static power gating, the current has been cut off from the unused blocks or memories depending on the use case. In the dynamic power gating, the supply of current can be controlled for a specific duration for a particular module. After that period of time, the previous state can be restored.

6 SDK-based Power Optimization methods for AWR2944 Device

The power consumption of AWR294x can be reduced by some techniques. These power reduction techniques can be achieved through appropriate programming of the MSS and DSP. These techniques are designed for applications with a significant time gap between successive radar measurement cycles or chirp transmissions. The techniques include static programming of the digital cores, peripherals and RF or analog circuits of the device in appropriate high-performance and low-power states, and dynamic transitions between the states. Low power states are generally achieved by switching off the bias current, or power supply, or clock inputs of a component, or significantly reducing the clock frequency.

During the operation of the radar sensor, identifying avenues to enter low power operations is important. The window of opportunity depends on the module and the nature of the processing being performed. The opportunities during the radar cycles include during the inter-chirp and inter-frame durations.

6.1 Typical Radar Measurement Cycle

Figure 6-1 shows a typical radar application flow during one frame of operation.

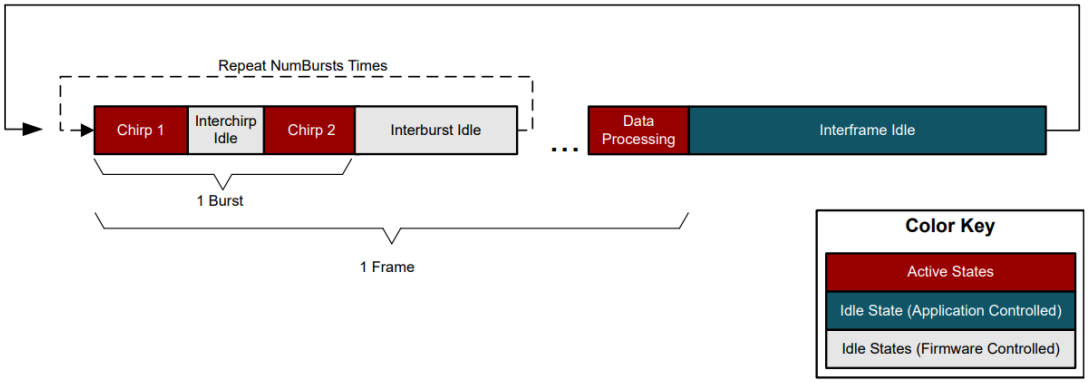

Figure 6-1. Typical Radar Measurement Cycle For One Frame

The different states during one frame of operation are shown in Table 6-1.

Table 6-1. Different States During Operation

State	Description
Chirp	The period of time in which one or more transmitters emits/receives an FMCW wave.
Burst	A sequence of chirps.
Frame	A time period that consists of a sequence of bursts followed by data processing. Frames are periodic on a defined interval.
Inter chirp idle	The time period between chirps
Inter burst idle	The time period between bursts
Inter frame idle	The time period between the end of one frame and the beginning of the next frame
Data processing	The time period in which the device processes the radar data collected in the previous frame

6.2 Power States During a Typical Radar Measurement Cycle

By default, the device boots at power on, chirps based on the front end configuration provided by the user, and leaves all subsystems running (even if the subsystems are not used). In many cases, this default behavior is fine. However, for power-sensitive applications, action can be taken to reduce the power consumption in both the acquisition and inter-frame periods.

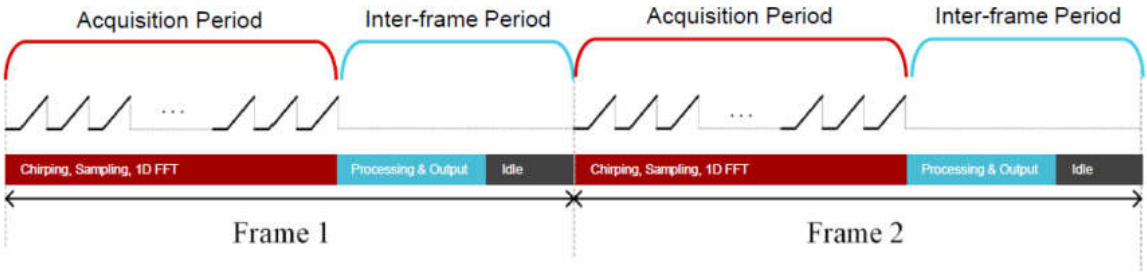

Figure 6-2. Power State During a Typical Radar Operation

The power optimization techniques can be mainly classified into two types.

1. Active mode optimization: the Active state is when the device is chirping or processing chirp data. In this state, the device can either be in a Data Acquisition substate, which is when data is being collected by transmitting and receiving chirps, or in a Data Processing substate, when the samples recorded in the Data Acquisition substate are being processed together. Here, the power optimization techniques are mainly focused on the acquisition period, that is, the time when the sensor is chirping, followed by the sampling and 1D-FFT processing.
2. Idle mode optimization: the Idle state occurs when the device is not actively chirping or processing data. There are three types of Idle states (Interchirp Idle, Interburst Idle and Interframe Idle). The Interchirp Idle and Interburst Idle states are completely handled by the device firmware. As the device cycles between chirps and bursts, the device goes to these states automatically. By comparison, the Interframe Idle state that the device enters between frames can be configured and modified by the user. Here, the power optimization techniques are mainly focused on the interframe idle state.

6.3 Power Reduction Techniques Implemented In Mililmeter Wave Demo

To reduce the power consumption of the Radar device, the following optimizations can be done:

1. Clock gating of unused modules: This method comes under static clock gating technique. The device includes several peripherals and modules, and several instances. Depending on the application, some of these can be active while others remain unused. The unused peripherals can be clock-gated to save power. In the SDK power measurement example (mmwave_mcuplus_sdk\ti\demo\awr294x\power_measurement), the following are the unused peripherals which have been clock gated:
   a. MSS: SPIA , I2C, MII100, MII10CSIRX, OBSCLKOUT, PMICCLKOUT, TRCCLKOUT
   b. DSS: RTIB, SCIA, CBUFF
   c. RSS: CSI2A

Figure 6-3. Example Snippet From Power Measurement Demo

2. Dynamic Clock Gating: This type of clock gating can be implemented in two ways, as shown below:
   a. Clock gating using the WFI instruction: the clock gating of the processing core can be done by the invocation of WFI instruction. The applicable cores are MSS ARM Cortex R5F, HSM ARM Cortex M4F and DSS ARM Cortex C66X. The HW-based clock gating of the logic is supported, and any interrupt ungates the logic and wakes up the core.
   b. Explicit clock gating: the modules explicit clock gating can be done using a control processing core.

      For example, the SDK power measurement example ((mmwave_mcuplus_sdk\ti\demo\awr294x\power_measurement)) demonstrates the dynamic clock gating of the hardware accelerator. This enables the capability to clock gate the 4 radar accelerator core IPs (FFT datapath, CFAR, memory compression, local maxima) based on the paramset being executed.

      The example also demonstrates the clock gating of HWA after the frame processing. The HWA is clock-gated once the angle of arrival frame processing is done. The clock is ungated in the frame start ISR.

```
/* Check if DSP Clock Gate option is enabled*/
if((gMmwMssMCB.powerMeas.isdspclkgate) && (gMmwMssMCB.powerMeas.dspStateAfterFrameProc == 1))
{
    /* Wait till DSP goes to Power OFF State. */
    while(((*(volatile uint32_t *)0x06000020 & 0x30) != 0x00))
    {
        ;
    }
    *((volatile uint32_t *)0x060000B8) = 0x7U; // Gate DSP Clock
}
```

```
if((ptrDssRcmRegs->DSP_PD_STATUS & 0x30) == 0x00)
{
    if(gMmwMssMCB.powerMeas.isdspclkgate == MMWDEMO_DSS_CG_ENABLE)
    {
        /* Un-Gate DSP Clock */
        ptrDssRcmRegs->DSS_DSP_CLK_GATE = 0x0;
    }

    /* Restore DSP Clock */
    ptrDssRcmRegs->DSS_DSP_CLK_SRC_SEL = MMWDEMO_DSP_CLK_SRC_DSP_PLL_MUX;
```

Figure 6-4. Example Snippets From Power Measurement Demo

3. Dynamic Frequency Scaling: the power measurement example in the SDK (mmwave_mcuplus_sdk\ti\demo\awr294x\power_measurement), demonstrates the dynamic frequency scaling for both DSS and RSS/BSS. The main objective is to lower the frequency during a specific period of time when the higher frequencies are not needed.
   a. DSS dynamic frequency scaling: in Radar devices, the DSS subsystem is mainly used for the computations. Typically, the DSP computations for one measurement cycle gets completed before the computations for the next measurement cycle start. If DSP runs on the same frequency throughout the processing, then DSP results in more power consumption. A better way to optimize is to adjust the frequency during the intermittent time.

      In intermittent time, the DSP clock rate can be reduced from the normal rates to the XTAL frequency (40MHz) to keep the DSP clock rate active and responsive to interrupts, while saving power.

      There are two ways to lower the frequency:

      i. By modifying the clock divider value.
      ii. By switching the clock source to a lower frequency.

      For example, in the power measurement example present in the SDK, the DSP clock is switched to the XTAL clock after the DSS Loading time elapses.

   b. BSS dynamic frequency scaling: for this type of frequency scaling, the TI Firmware supports dynamic frequency scaling by enabling the *BSS Underclocking feature*. This feature requires the following actions:
      i. First, the necessary clock configurations of the RSS clock and FRC clock sources need to be done.
      ii. Reserve MSS RTIC for BSS use for maintaining ticks across the modes.
      iii. Handle the functional safety aspects of FRC and WDT.
      iv. This can be achieved by performing a *Logical monitoring of the Frame timing* in the application.
      v. Enable the feature and necessary configurations before unhalting the BSS core.

For example, in the power measurement present in the SDK (mmwave_mcuplus_sdk\ti\demo\awr294x\power_measurement), the BSS clock source switches to the XTAL (40MHz) clock when the core is idle. This feature cannot be configured through CLI since the feature is enabled in the SBL. Refer to SOC_rcmPopulateBSSControl API in mcu_plus_sdk_awr294x_<ver>.c to enable or disable the BSS Dynamic clocking feature. The 3rd bit of RSS_CR4_BOOT_INFO_REG5 is set to 1 to enable Dynamic clocking. The bit needs to be set to 0 for disabling the feature. MSS RTIC is used by the BSS when the Dynamic clocking feature is enabled.

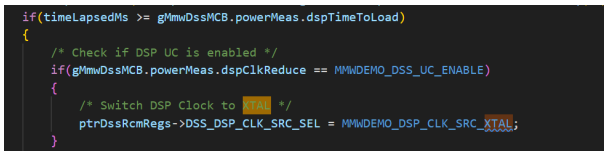

Figure 6-5. Example Snippet From Power Measurement Demo

4. Dynamic Power Gating: the power measurement example in the SDK (mmwave_mcuplus_sdk\ti\demo\awr294x\power_measurement), demonstrates the different ways in which power gating can be done. Some of the examples are shown below.
   a. Dynamic power gating of the HWA module: in the device, there is a dedicated power switch available for the HWA module, for which the HWA power supply can be gated off.

      In comparison with the dynamic under-clocking explained earlier, dynamic power-gating needs a reconfiguration of the HWA and consumes more state-transition time (a few micro-seconds more), but provides more power saving.

      For example, HWA is powered down after the AoA frame processing is completed. Hence, HWA needs to be powered up and reconfigured before the next frame start interrupt. In the provided example, this feature works in conjunction with DSS Power Gate. The DSP wakes up, powers up HWA and reconfigures HWA.

   b. Dynamic power gating of the DSP core: in addition to dynamic under-clocking as explained earlier, the power supply of the DSP can be gated off using a power switch dedicated to the DSP core. In comparison with the dynamic under-clocking explained earlier, dynamic power-gating needs more sophisticated implementation, consumes more state-transition time (a few micro-seconds more), but provides additional power saving.

Note

The contents of the L1 memory are not retained when powered down. Hence, TI recommend to use the L1 memories as a cache and writeback the dirty lines before powering down the DSP. The L2 memory contents are retained.

For example, the power measurement example provided in the SDK, demonstrates the power gating of the DSP core. DSP is power gated after the DSS loading time is elapsed. DSP is powered up by MSS once the DSP receives the interrupt from the RTIB timer. This timer is configured according to the wakeup time given by the user through CLI. Please make sure the DSP is powered up before the next frame start.

Note

DSS starts execution from the reset vector when DSS is powered up.

Note

DSP Gating concerns:

i. An observation is that in typical use cases for long DSP idle periods (> 8ms), DSP powering down gives benefits over dynamic frequency scaling.
ii. The savings is a function of the save-restore routines as these routines keep the DSP in active mode additionally.
iii. TI recommends to lower the overall device power consumption in thermal shutdown situations.

5. Transmitters and receivers: the dynamic power saving option can be enabled during the inter chirp idle time to save power. This is done by turning off various circuits. For example, the TX, RX, LO Distribution blocks. The RF, analog sections can be switched OFF between chirps if there is sufficient inter-chirp idle time to save power.
6. APLL and FMCW Synthesizer: the APLL supplies the clock to the RX ADCs and the FMCW synthesizer. The FMCW synthesizer generates the chirp waveform supplied to the TX and RX circuits. These circuits need to be ON during chirps and bursts in a frame. In AWR2944, the APLL and FMCW synthesizer can be switched OFF in interburst and interframe times to conserve power.
7. RX ADC Low Power Mode: the RX ADC and IFA can operate in two modes: regular and low power ADC mode, which is configurable based on the use case. The low power mode is natively supported for lower sampling rates. If the user's RX sampling rate requirement is low (<7.5MHz IF Bandwidth), then the low power mode can be enabled to conserve power by lowering the operation clock frequency.
8. RF Monitors: this method can be used in conserving the monitoring power. The front-end monitors of the device use TXs and RXs to monitor each other with an RF loopback. The set of RXs to be used during RF loopback-based TX monitors is configurable along with other monitoring parameters. This is true for inter-TX mismatch monitors, and phase shifter monitors. Enabling only a single RX can be sufficient to monitor the TXs while also conserving power in comparison with enabling all RXs.

7 Equipment Needed For Evaluation

The hardware and software requirements to evaluate the power optimization techniques discussed in this document are shown below.

Required Hardware for Evaluation: all of the power saving techniques discussed in this document can be evaluated using the AWR2944EVM.

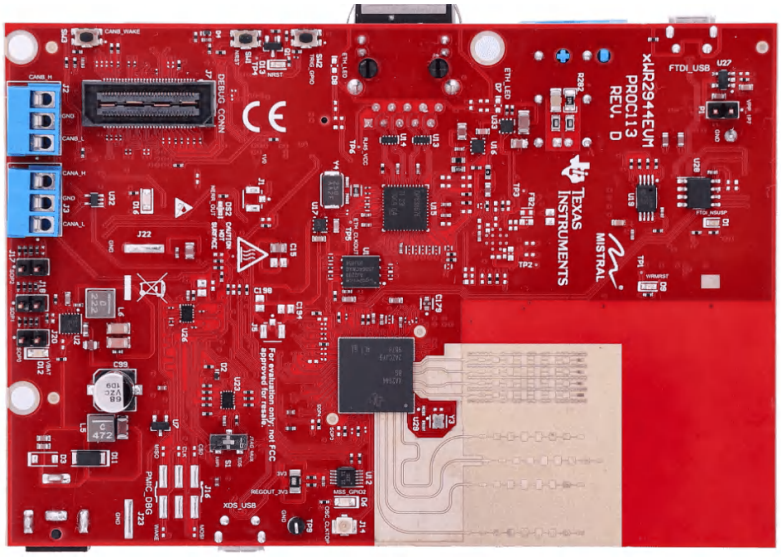

Figure 7-1. AWR2944EVM

Software Requirement: a power measurement demo is available in the device SDK: MMWAVE-MCUPLUS-SDK. This millimeter wave demo shows how the power reduction techniques can be implemented.

8 Summary

The key techniques of power saving such as clock gating, frequency scaling and power gating and so forth are discussed in this document. Implementing this techniques offers a significant advantages, including improved energy efficiency, reduced heat generating, cost savings and so forth.

9 References

- Texas Instruments, AWR2943/AWR2944 Single-Chip 76 to 81GHz FMCW Radar Sensor, data sheet
- Texas Instruments, AWR294x and AWR2944LC Technical Reference Manual
- Texas Instruments, Programming Chirp Parameters in TI Radar Devices, application note
- Texas Instruments, AWR2944EVM, webpage
- Texas Instruments, MMWAVE-MCUPLUS-SDK, webpage

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