Application Note

AM273x Hardware Design Guide

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ABSTRACT

This application note intends to serve as a guide for hardware designers creating PCB systems based on the AM273x family of MCU devices. This document serves to integrate device-specific schematic and PCB layout recommendations and examples from the AM273x evaluation modules (EVM), the TMDS273GPEVM, with the *AM273x Sitara™ Microcontroller Data Sheet*, *AM273x Sitara™ Microcontroller Technical Reference Manual* and other collateral documents and tools, as shown in Section 12.

Project collateral and source code discussed in this application note can be downloaded from the following link https://www.ti.com/lit/zip/sprad61.

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Trademarks

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1 Introduction

The AM273x family of microcontrollers is a highly-integrated, high performance microcontroller based on the Arm Cortex-R5F and a C66x floating-point DSP cores. The device enables Original-Equipment Manufacturers (OEM) and Original-Design Manufacturers (ODM) to quickly bring to market devices with robust software support, rich user interfaces, and high performance, through the maximum flexibility of a fully integrated, mixed processor solution. A typical AM273x based design is shown in Figure 1-1. This diagram is excerpted from the AM273x EVM (TMDS273GPEVM) system block diagram. As can be seen below the AM273x devices offer designers a wide range of digital connectivity, audio, radar and analog sensor feedback options.

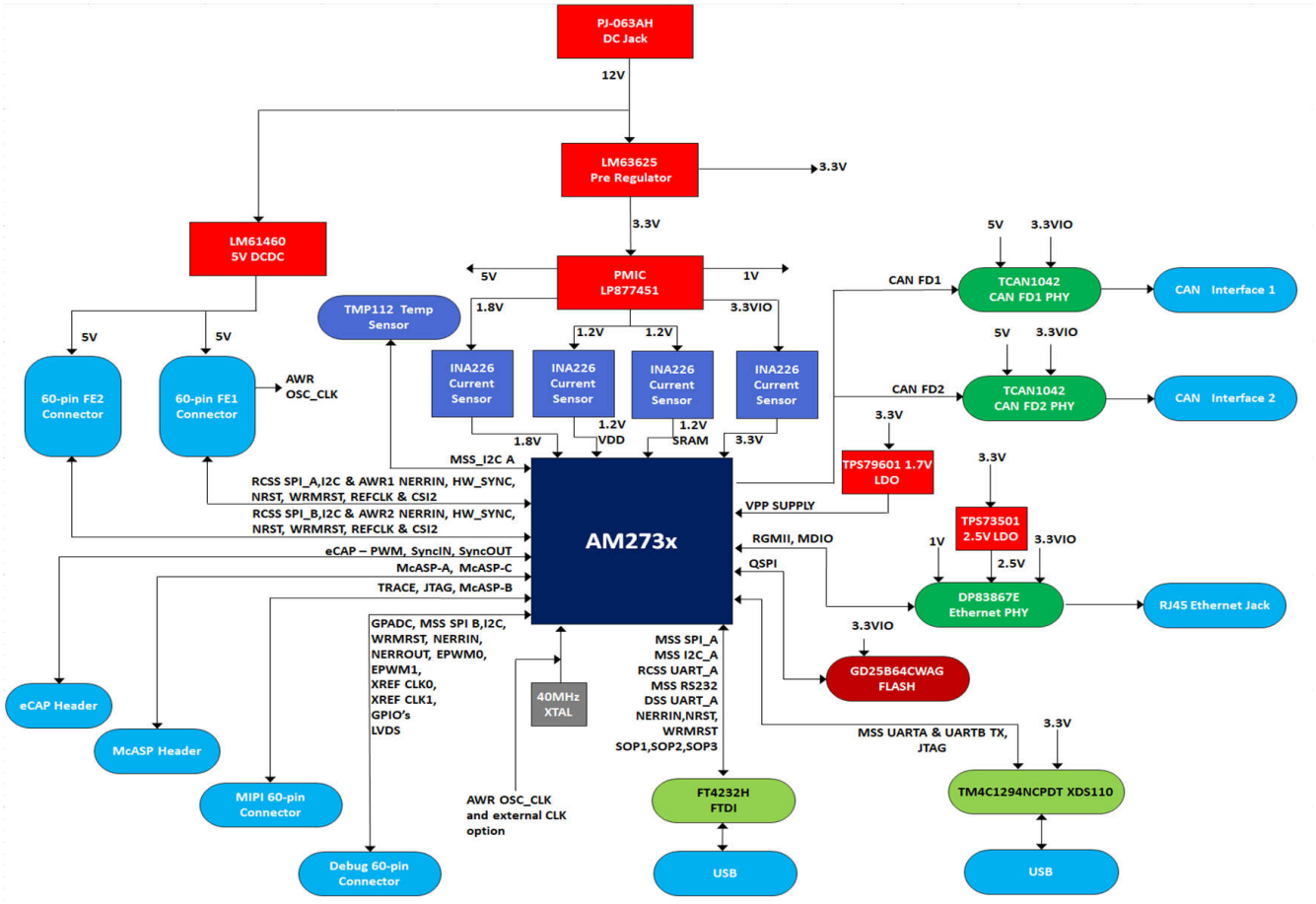

Figure 1-1. Typical AM273x System Block Diagram (Based on TMDS273GPEVM Design)

To quickly achieve a working system with the numerous cores peripherals and pin multiplexing options available on the AM273x MCU, this document should be referenced along with the other key AM273x collateral references. These include:

- The *AM273x Sitara™ Microcontroller Data Sheet* [11] is the primary resource for all device pinout and pin-level multiplexing options.
- The SYSCONFIG [24] pinmux planning tool should be utilized when starting a new AM273x pinout and driver utilization.
- The *AM273x Sitara™ Microcontroller Technical Reference Manual* [22] documents detail each core and peripheral subsystem from a conceptual, usage and programming model perspective.
- The AM273x MCU-SDK [7] ties the data sheet and technical reference manual together with software system and peripheral usage examples.

1.1 Acronyms

Table 1-1. Acronyms Used in This Document

Acronym	Description
EVM	Evaluation Module. Referencing TI PCB assemblies such as the AM273x GP EVM (TMDS273GPEVM)
PDN	Power Distribution Network. The active and passive components providing regulated power to a load such as the AM273x MCU power pins.
EMI	Electromagnetic Interference
PI	Power Integrity
SI	Signal Integrity
BOM	Bill of Materials

2 Power

2.1 Discrete DC-DC Power Solution

To support discrete DC-DC power solutions, separate power converter ICs can be selected for each power rail needed by the AM273x. The power converter ICs should be chosen to ensure each is capable of supporting the current needs for the generated power rails. The Power Good signals for each rail should be combined into a single PG signal that is connected to the nRESET pin on the AM273x.

2.2 Integrated PMIC Power Solution

The AM273x GP EVM integrates a Power Management Integrated Circuit (PMIC) based power solution that may be used as a reference solution for some systems. The solution consists of a LM63625 voltage converter pre-regulator and a LP877451 PMIC to generate the MCU core, SRAM, system digital and analog I/O power. A TPS73501 Low Drop Out (LDO) regulator is used for the Ethernet PHY.

The power good generation circuits available on the PMIC and DC-DC regulators should be combined to a single line and used to drive the reset (nRESET) of the AM273x device.

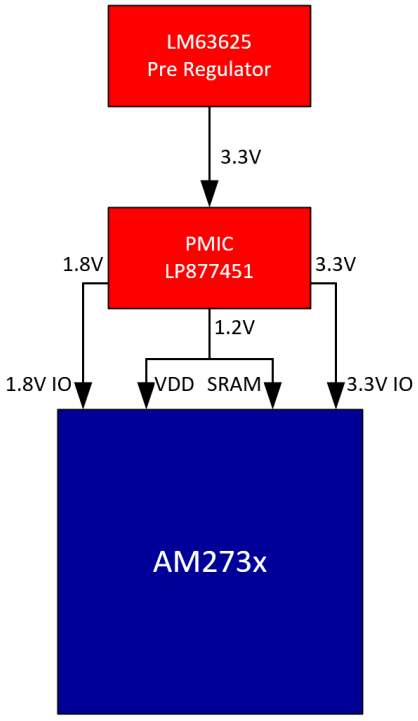

Figure 2-1. AM273x PMIC Example Solution

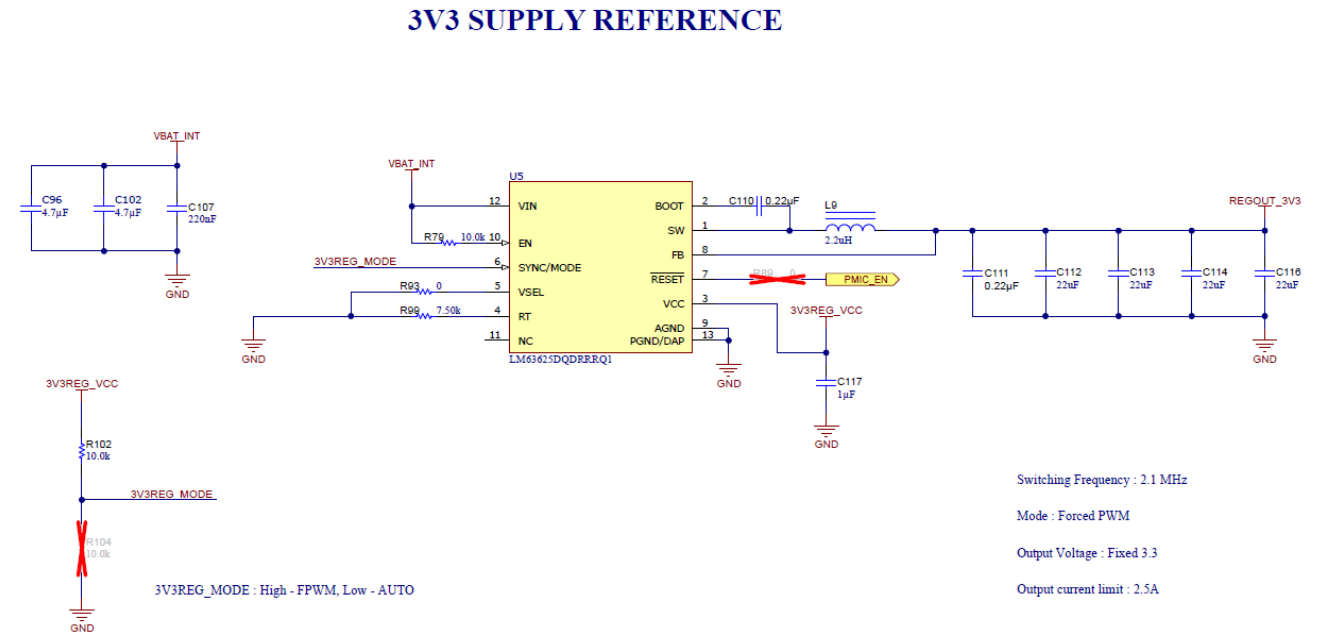

Figure 2-2. AM273x PMIC 3.3V Pre-Regulator Implementation

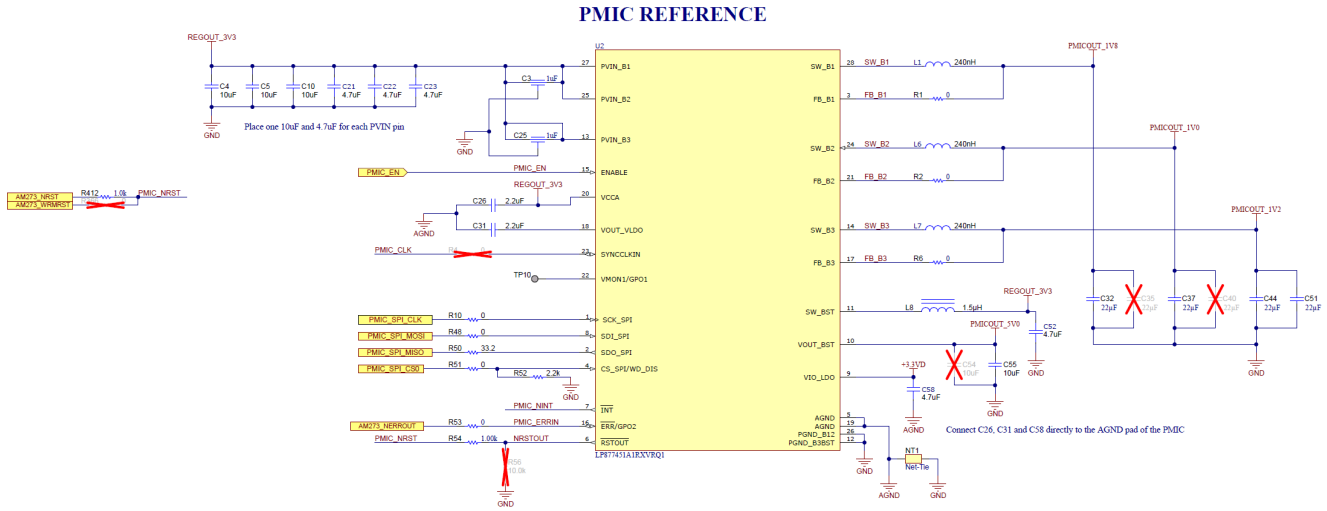

Figure 2-3. AM273x PMIC Implementation

2.3 Power Decoupling and Filtering

Table 2-1 describes the initial BGA decoupling and power filtering required for the AM273x. These were based on the initial simulation feedback of the AM273 GPEVM PCB and AM273x package with the above transient use-cases.

The decoupling network presented in the below sections and in the AM273x EVM schematics and layouts are reasonable starting points for any AM273x PCB design. Additional placement guidance for the decoupling network is provided in Section 11. However, due to specific PCB routing differences and the resulting plane capacitance and decoupling mounting inductances and other parasitics, it is highly recommended that designers simulate and measure their specific power distribution network performance. Simulations and measurements should ideally be done with target application software active and intended operating environment conditions applied to the system.

Table 2-1. AM273x Recommended Decoupling per Power Net

Device Supply	Quantity	Comment	Part Number	Manufacturer
1.2-V VDD_CORE	2	2.2 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	5	0.22 µF, 16 V,± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	3	0.01 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
1.2-V SRAM	1	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
	2	0.1 µF, 16 V, ± 10%, X7R, 0402	GCM155R71C104KA55D	Murata
1.8-V IO Supply	4	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
3.3-V IO Supply	1	2.2 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	GCM188R70J225KE22D	Murata
	6	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
1.8-V ADC Supply	1	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
1.8-V Clock Supply	1	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
1.8-V CSI Supply	1	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
1.8-V LVDS Supply	1	0.22 µF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	GCM155R71C224KE02D	Murata
VNWA Supply	1	0.1 µF, 16 V, ± 10%, X7R, 0402	GCM155R71C104KA55D	Murata
Bandgap Supply	1	0.047 µF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H473K050BB	TDK
VPP Supply	1	0.1 µF, 16 V, ± 10%, X7R, 0402	GCM155R71C104KA55D	Murata

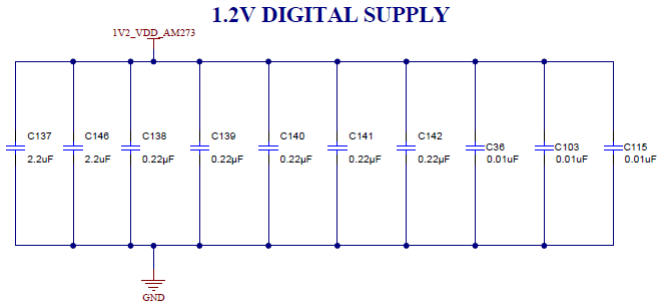

Figure 2-4. AM273x GPEVM Excerpt – 1.2 V Power Decoupling Schematic

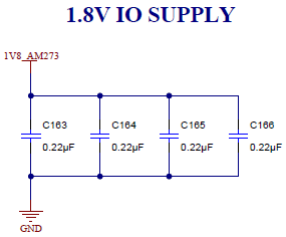

Figure 2-5. AM273x GPEVM Excerpt – 1.8 V Digital I/O Decoupling Schematic

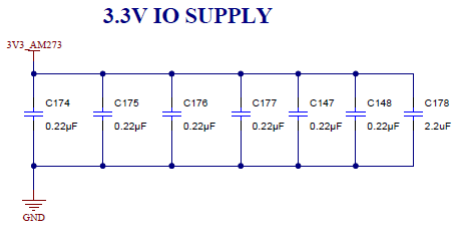

Figure 2-6. AM273x GPEVM Excerpt – 3.3 V Digital I/O Decoupling Schemati

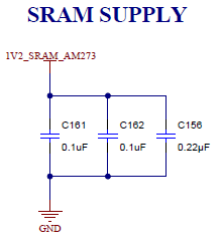

Figure 2-7. AM273x GPEVM Excerpt – SRAM Decoupling Schematic

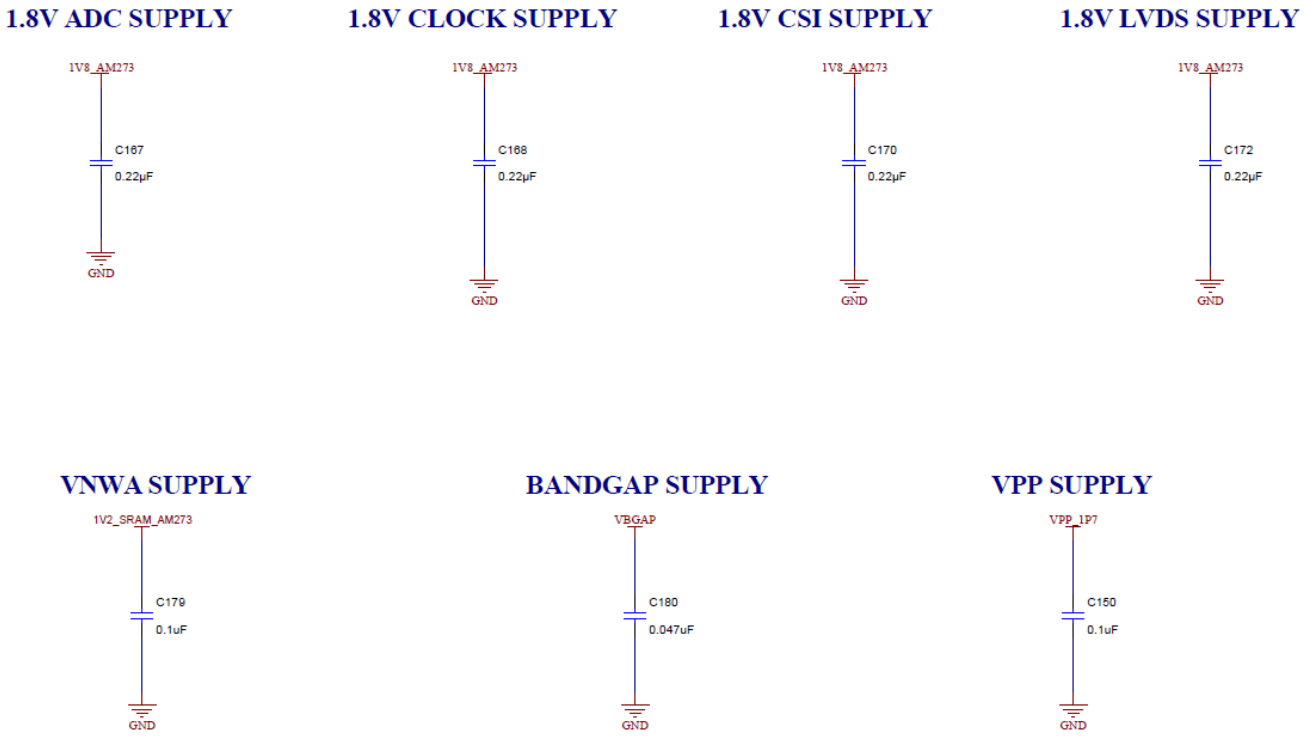

Figure 2-8. AM273x GPEVM Excerpt – Additional Decoupling Schematic

2.4 Power Consumption

This section outlines the latest estimates of the AM273x power consumption on a per device power net basis. These values may change as more power modeling and characterization is performed. This data can be used to scale peak DC-DC conversion power margin, perform IR drop analysis of the PCB layout, and help with thermal loading analysis.

These estimates are based on initial power simulations of the device. For the latest characterized, peak power numbers, see the *AM273x Sitara™ Microcontroller Data Sheet*.

Also, a use-case based power estimation tool (PET) is provided for the AM273x MCU. This tool can help further bound the peak power based on specific core and peripheral utilization duty-cycle.

Table 2-2. AM273x Estimated Peak Power Consumption

Device Supply	V	Average Power (mW)	Average Current (mA)	Peak Current (mA)	Comments
VDD	1.2	693	576	2315	1.2-V Core Digital Power
VDD_SRAM	1.2	3	3	75	1.2-V SRAM Power
VIOIN	1.8 or 3.3	12	4	74	1.8-V or 3.3-V Digital I/O Power
VIOIN_18	1.8	0	0	1	1.8-V Digital I/O Power
VIOIN_18CLK	1.8	32	18	18	1.8-V Clocking Power
VIOIN_18ADC	1.8	3	2	2	1.8-V ADC Power
VIOIN_18CSI	1.8	40	22	23	1.8-V CSI Power
VIOIN_18LVDS	1.8	125	69	70	1.8-V LVDS Power
Device Peak Power		**908**	**694**	**2578**	

3 Clocking

3.1 Crystal and Oscillator Input Options

The AM273x primary clock interface, CLKM and CLKP (ZCE pins U1 and V1, NZN pins N1 and P2), can be sourced from either an attached crystal or a single-ended oscillator output. The attached crystal should be a fundamental mode crystal operating at 40 MHz. If operating from a single-ended oscillator output, the CLKP pin should be connected to the oscillator and the CLKM pin must be connected to ground. In oscillator input mode, the CLKP pin can be tied to either a 1.8 V DC-coupled square wave or AC-coupled sine wave oscillator. For full crystal and oscillator input requirements, see the *AM273x Sitara™ Microcontroller Data Sheet*.

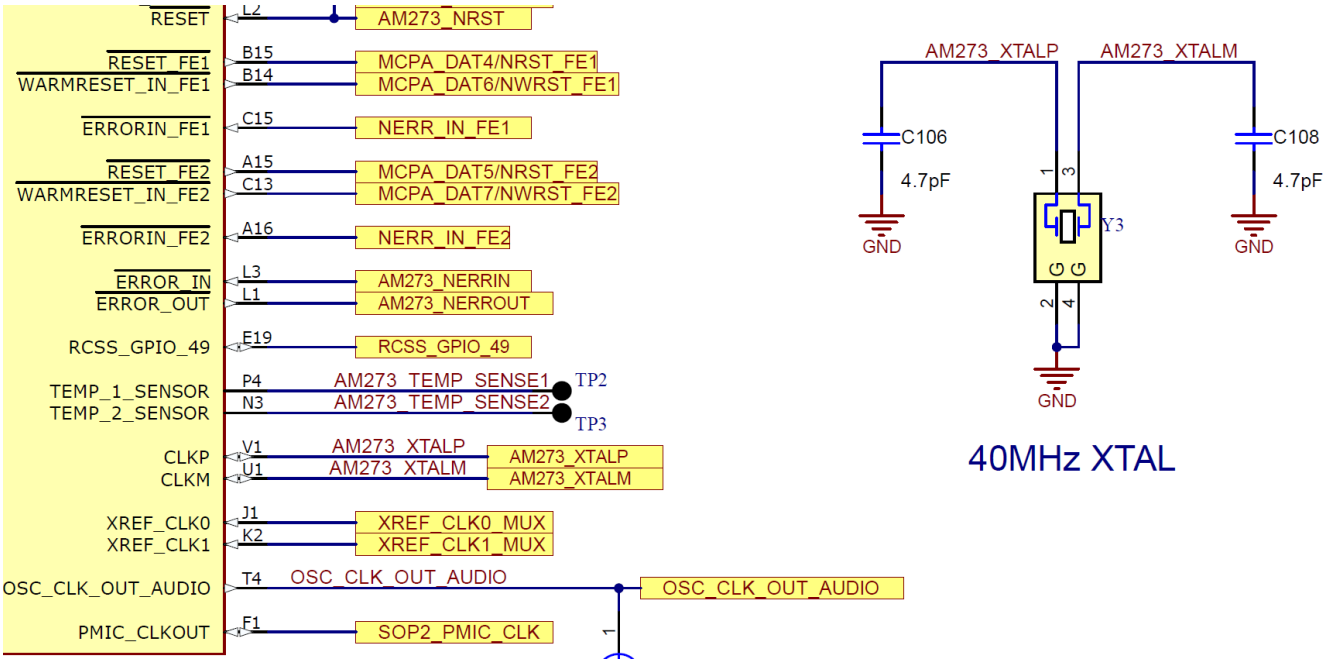

Figure 3-1. Excerpt From AM273x GPEVM Schematics

Additional clock inputs for the AM273x include:

- Two external reference clock inputs, XREF_CLK0 and XREF_CLK1 (ZCE pins J1 and K2, NZN pins G1 and G2), that can be used as dedicated peripheral clock sources for system synchronization.
- Two Camera Subsystem 2.0 (CSI2.0) Clock inputs, CSI2_RX0CLKM/CSI2_RX0CLKP (ZCE pins B6 and A6) for CSI2.0 Receiver #1 and CSI2_RX1CLKM/CSI2_RX1CLKP (ZCE pins A11 and B11) for CSI2.0 Receiver #2.

3.2 Output Clock Generation

The AM273x devices include four output clock sources:

- Oscillator output reference clock, OSC_CLK_OUT_AUDIO (ZCE pin T4, NZN pin R2)
- PMIC output reference clock, PMIC_CLKOUT (ZCE pin F1)
- LVDS/Aurora bit clock, LVDS_CLKM and LVDS_CLKP (ZCE pins W7 and V7)
- LVDS/Aurora frame clock, LVDS_FRCLKM and LVDS_FRCLKP (ZCE pins W8 and V8)

3.3 Crystal Selection and Shunt Capacitance

In crystal operating mode, the AM273x can be interfaced to a wide variety of compatible crystals. Based on PCB parasitic capacitance and crystal selected, the additional load capacitance needs to be modified to achieve the best start-up stability and frequency accuracy.

For full crystal loading tolerances, see the *AM273x Sitara™ Microcontroller Data Sheet*.

3.4 Crystal Placement and Routing

Crystal oscillator input should be placed as close as possible to the AM273x CLKM/P pads with minimal length traces between crystal and AM273x pads. A ground ring shorted to the local VSS plane should be placed adjacent and between the CLKM and CLKP traces to help prevent coupling from adjacent signals onto the clock higher impedance crystal input paths.

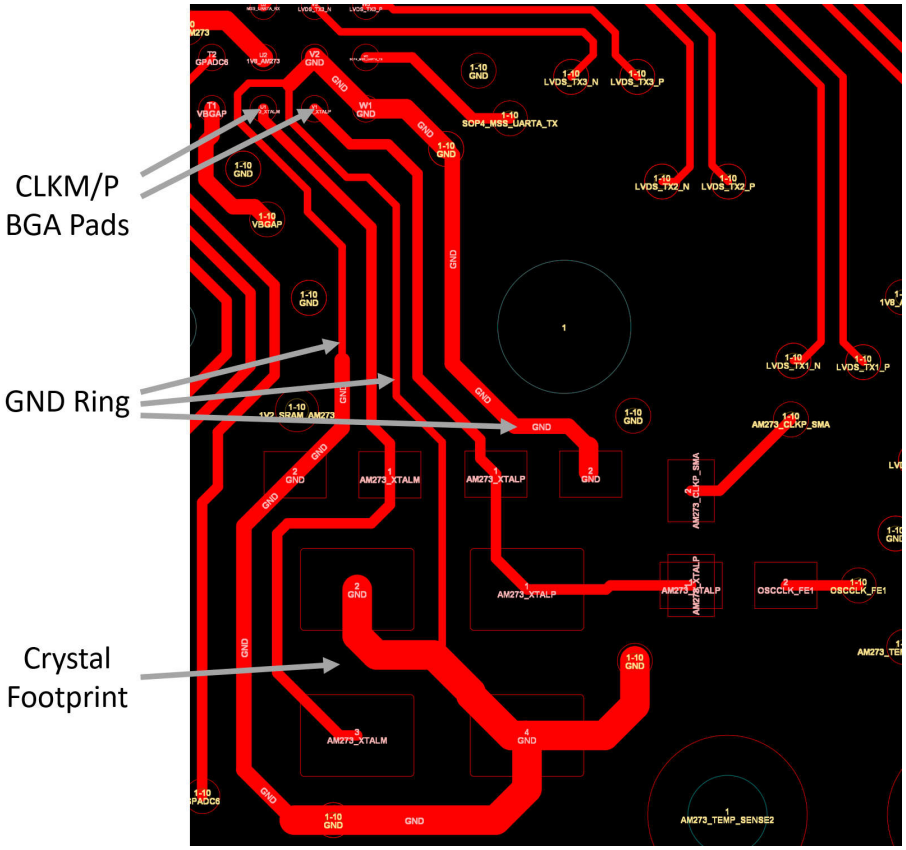

Figure 3-2. Excerpt From AM273x GPEVM Layout - Crystal Layout and Ground Ring Structure

4 Resets

The AM273x MCU has two hardware reset sources:

- NRESET: Power on reset (logic low enable) signal, ZCE pin L2, NZN pin J3
  - The power-on default configuration sets this pin as an LVCMOS, Failsafe, open-drain output.
  - Should be driven from the power-good circuits of the associated 1.2 V core and 3.3 V I/O regulators or PMIC Reset Out output
- WARM_RESET: Warm reset input and reset status output signal, ZCE pin K1, NZN pin H3
  - The power-on default configuration sets this pin as an LVCMOS open-drain output with the internal pull status disabled
  - When the device enters reset, this signal is driven logic low.
  - When the device is fully out of reset, this signal is driven logic high.

The NRESET is intended to be kept at logic low at initial startup of the system. Once each regulator or PMIC sourcing the AM273x power pins has been verified to be operating at nominal output voltage, then the NRESET signal can be brought up to logic high. This action will start the AM273x boot ROM execution, beginning with sampling of the SOP pins. The AM273x GPEVM implementation does this with the nRSTOUT pin of the LP877451A PMIC. A weak pull-down resistor is recommended on the PORZ signal to keep the signal low before startup of the system. PORz should be forced low if either 1.2 V or 3.3 V rail power goes below the nominal operating range.

For a full description of the power-on and power-off reset sequencing requirements, see the *AM273x Sitara™ Microcontroller Data Sheet*.

The WARMRSTN pin is a multi-purpose software reset input and hardware reset status pin. In the power-on-default configuration, this pin is configured as an open-drain output and requires an external pull-up resistor to VIOIN 1.8/3.3 V I/O voltage rail. In this mode, WARMRSTN can be used as an MCU reset indicator and can be used to drive reset input for attached peripheral IC such as Ethernet PHY and memories.

WARMRSTN can also be configured by software as software reset. Additional software reset sources are also available on the AM273x devices. For more information on reset functionality, see the *Reset* chapter in the *AM273x Sitara™ Microcontroller Technical Reference Manual*.

Because of the default open-drain configuration of this pin, if both the reset status output mode and the software reset input mode are needed in a design, it is recommended that open-drain buffers be used to drive the optional reset input status.

5 Bootstrapping

The start-on-power (SOP) signals are used to latch in the selected boot mode into the AM273x device. During the NRESET rising edge (low to high logic transition) the SOP[4:0] signals are sampled. The resulting 5 bits are used to select the XTAL Frequency and to branch the boot ROM into the selected boot mode. Not all combinations are supported. For a full description of the SOP pin states and supported boot modes, see the *AM273x Sitara™ Microcontroller Data Sheet*.

5.1 SOP Signal Implementation

Each SOP[n] signal is multiplexed with different peripheral functional mode signals as well. For more information, see the signal description tables in the *AM273x Sitara™ Microcontroller Data Sheet*. The SOP signal descriptions are excerpted below.

Table 5-1. SOP and Functional Mode Signal Mapping

Pin Number - ZCE	Pin Number - NZN	Primary Pinmux Signal	SOP Mode Signal
D6	C6	TDO	SOP[0]
E17	C14	MSS_MIBSPIB_CS2	SOP[1]
F1	D3	PMIC_CLKOUT	SOP[2]
V9	P4	MSS_UARTB_TX	SOP[3]
W2	R4	MSS_UARTA_TX	SOP[4]

Because of this SOP/functional-mode multiplexing additional care must be taken in schematic and layout to ensure that the SOP mode selection resistors, jumpers or switch paths are routed in such a way that the SOP mode branches do not present inductive stubs to the functional mode signal paths. Failing to take care of this may result in non-functional interfaces during normal operation.

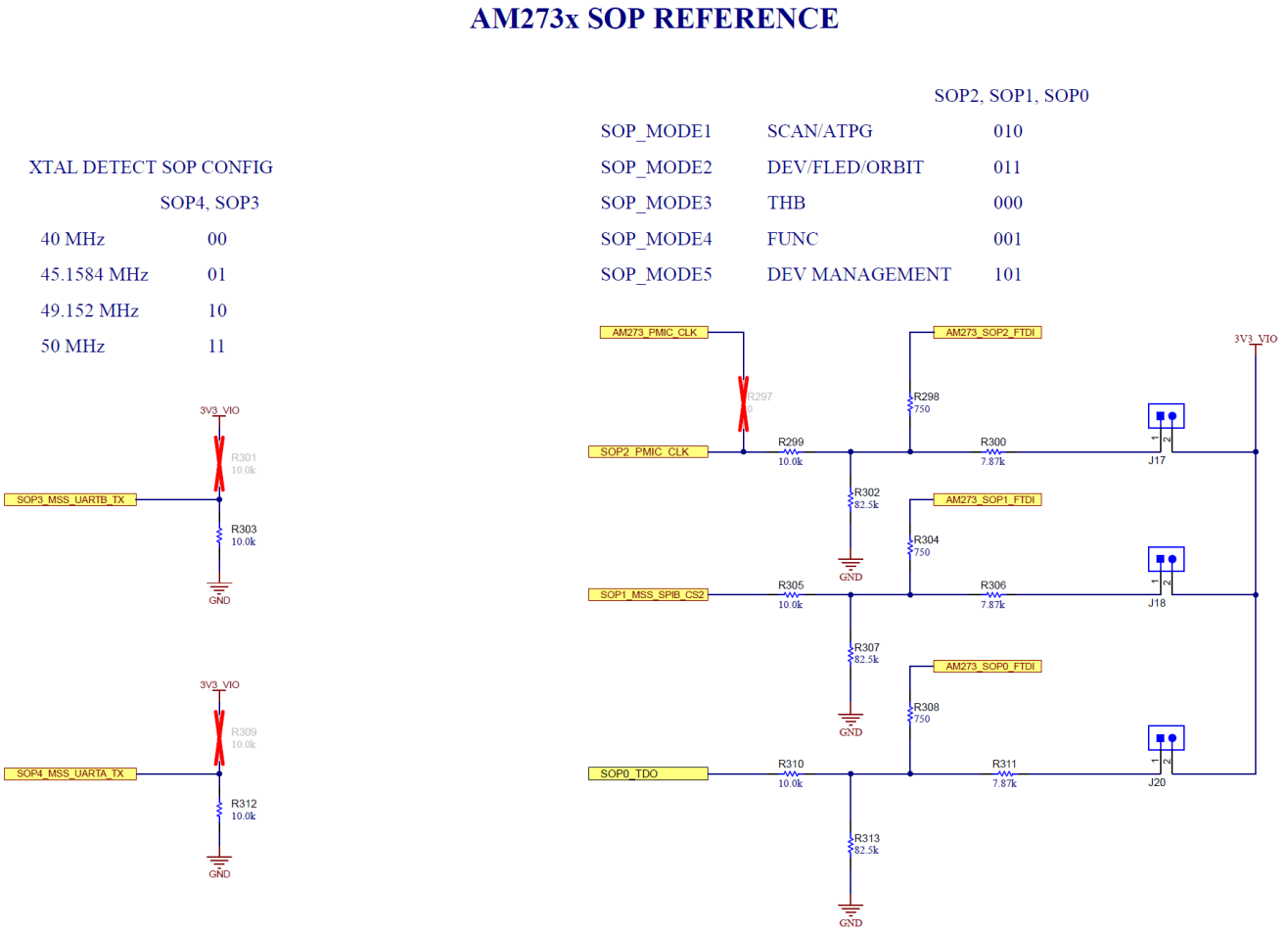

Figure 5-1. Excerpt From AM273x GPEVM Schematic – SOP[4:0] Functional and SOP Paths

In the AM273x GPEVM design this SOP mode isolation is accomplished by including a 10KΩ resistor in the SOP signal path for SOP[2:0]. For SOP[4:3], the 10KΩ pulldown resistor setting the SOP bit to 0 does not impact the function of the UART TX lines, so no isolating 10KΩ resistor is necessary. Ideally, the resistor is placed such as one pad is as close to the AM273x BGA pad and in-line with the functional mode path. This creates a layout where the additional stub length necessary to breakout the SOP path will only minimally impact the functional mode operation of the signals.

5.2 QSPI Memory Controller Implementation

The QSPI memory is the primary boot memory location for the AM273x MCU. Good signal integrity of this memory interface is critical for basic QSPI boot operations of the AM273x MCU. Additional pull-up resistors are also necessary.

- Include a chip-select pull-up resistor to ensure that the device is normally read/write disabled until the AM273x QSPI controller drives chip-select low at the start of a new read/write transaction.
- Include a pull resistor to disable write protect mode by default
- Include a pull resistor to disable hold mode by default

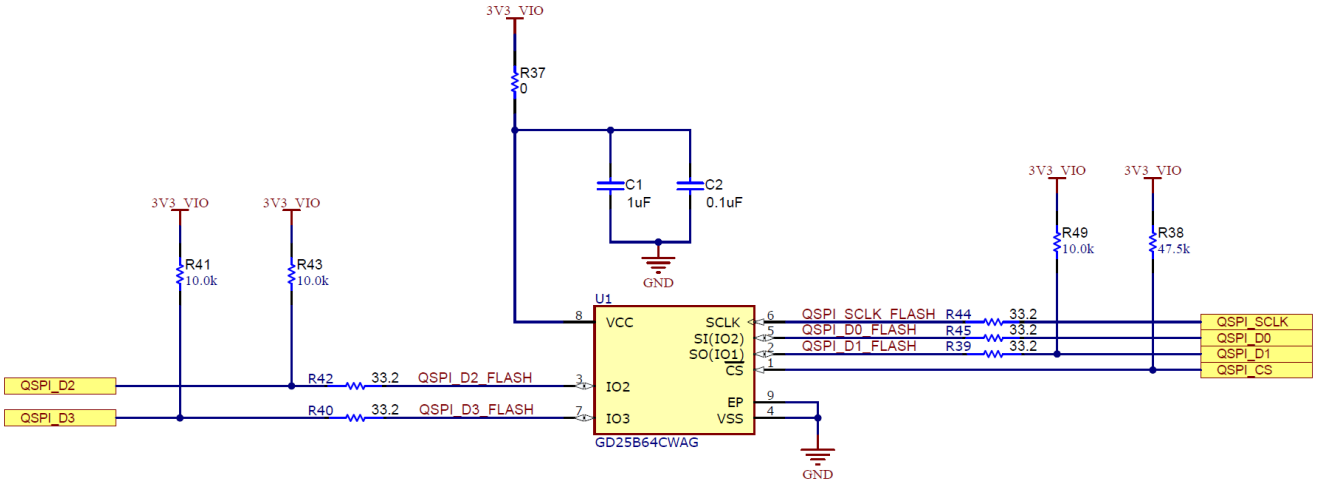

Figure 5-2. Excerpt From AM273x GPEVM Schematic – AM273x QSPI Controller and GD25B64CWAG NOR Flash Memory

Additional routing guidelines for the QSPI memory interface are provided in Figure 5-3 and Table 5-2 These should be used as maximum routing and skew match limits.

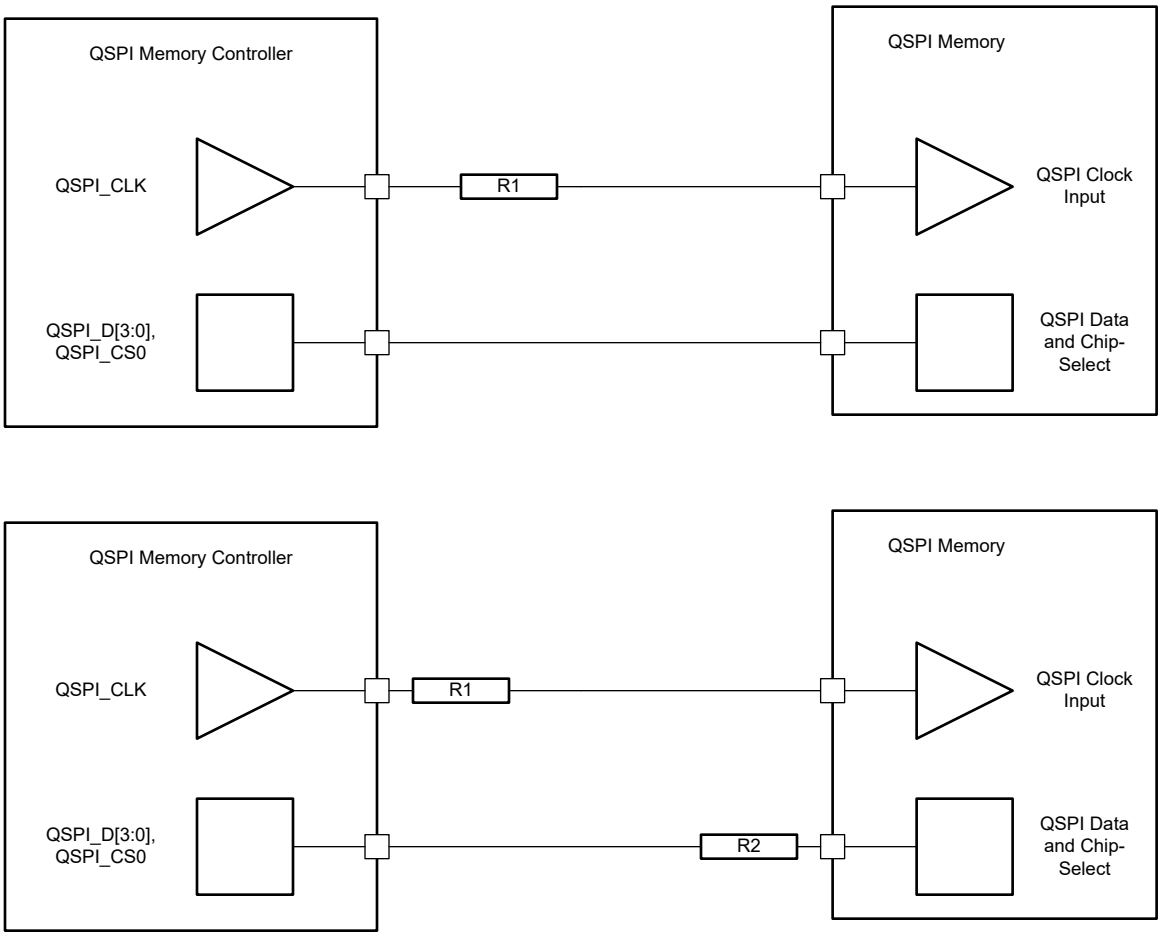

Figure 5-3. AM273x QSPI - Routing Rules Diagram

Table 5-2. AM273x QSPI – Recommended Routing Rules

Spec No.	Specification	Value	Unit
1	QSPI_CLK, QSPI_CS0, QSPI_D[3:0] maximum delay	450	ps
2	QSPI_CLK to QSPI_D[3:0] maximum skew	50	ps
3	Approximate maximum routing distances	3214	mils
4	Approximate maximum routing skew	357	mils
5	A series termination resistor (R1 in diagram above) should be placed close to the QSPI_CLK transmit pin of the AM273x to control rise-time and reflections of the clock line.	Variable, 0 to 40	Ω
6	A series termination resistor (R2 in diagram above) should be placed close to the QSPI data pins of the attached memory to control rise-time and reflections of the data lines.	Variable, 0 to 40	Ω

Note

Approximate routing distances computed assuming a typical 140 ps/inch propagation delay in 50-Ω FR4 Microstrip or Stripline transmission lines. A 2D field solver or appropriate closed-form approximate impedance equations should be used to find more exact propagation delay for a specific given stackup and routing.

It is recommended that the QSPI memory be co-located close to the AM273x BGA footprint, which allows for routing that maximizes the delay margins and skew margins. As seen in Figure 5-3 it is also recommended to include a series termination resistor near the QSPI controller clock transmit pin. Similarly, series terminations should be added at the data pins of the QSPI device as well. During read quad-read operations, which will be the most used mode of operation of the memory, this helps create well controlled edges on the data lines.

5.3 ROM QSPI Boot Requirements

For the AM273x device, ROM code expects the following QSPI flash memory features:

- The flash device should be compatible with 3.3V LVCMOS signaling levels provided by the AM273x device
- Ensure the flash device is set to write-protect mode disabled and hold-mode disabled.
  - This is usually a pull-up resistor option on the D1 and D2 pins of the flash device.
  - Ensure proper pull-up resistors are applied such that this correct operating state is selected.
- The flash device be able to support Quad Output Fast Read (opcode 0x6B)
- Flash must be able to support Fast Read in Single Mode (opcode 0x0B)
- Device should allow 8 “dummy” clock cycles for setting up the initial address during the previously mentioned read operations
- Flash must support 3-byte (24 bit) addressing mode by default
- Flash memory size should be in the 2.5MB-4MB range, but it is not recommended to exceed the 16MB range to ensure correct operation

The following list of flash memory devices have been tested with the AM273x MCU for compatibility. For the above compatibility requirements, check the specific flash device-specific data sheet.

Table 5-3. QSPI Devices Compatible with AM273x

Manufacturer	Flash Memory Devices
Infineon	S25FL128S/S25FL256S series
Winbond	W25Q series
GigaDevice	GD25 series
Macronix	MX25xxx35 series

Note

The GD25B64CWAG device from GigaDevice was utilized on the AM273x GPEVM.

6 JTAG Emulators and Trace

The AM273x MCU supports multiple different classes of JTAG emulators with or without additional ARM Trace capture capabilities.

For out of box convenience the TMDS273GPEVM implements an onboard XDS110 emulator with JTAG and auxiliary UART-USB bridge using a TI TM4C MCU. However, for actual custom systems, a simpler JTAG/Trace debug header should be implemented. This allows for external JTAG and Trace pods to be attached to the system as needed during development. The header can then be removed entirely or depopulated for full production of the system to save cost.

One popular JTAG and Trace implementation is the MIPI industry standard MIPI-60 shown in [5]. This is based on the Samtec QSH-030-01-L-D-A. This implementation is compatible with TI XDS560v2 JTAG/Trace pods as well as other third-party JTAG/Trace pods. Additional TI JTAG debugger connections can be found in [6].

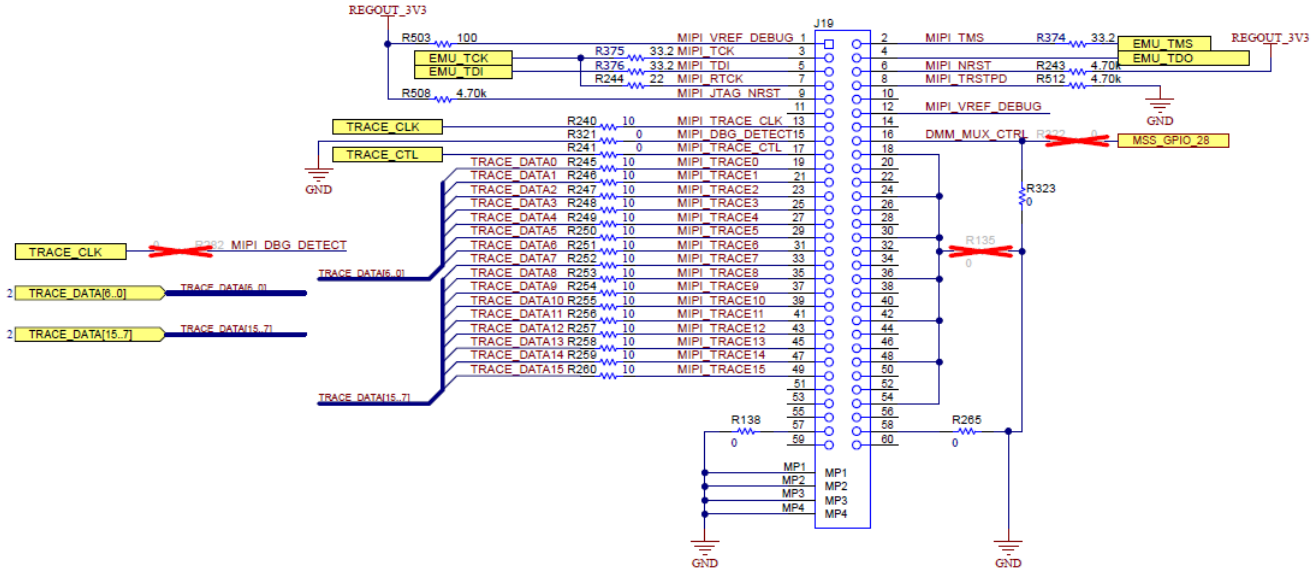

Figure 6-1. Example MIPI-60 JTAG and 16-Bit Trace Implementation

Additional, non-TI JTAG debug and Trace systems are still being tested. Further guidance is planned in future revisions of this document.

7 Multiplexed Peripherals

With the large number of multiplexed digital I/O present on the AM273x MCU IOMUX, designers should make full use of the TI System Configuration tool (SYSCONFIG) to experiment and plan different pin multiplexing scenarios before committing the design to hardware. The resulting SYSCONFIG pin multiplexing configurations can then be used for schematic capture, layout, and software driver creation.

For more details, see https://www.ti.com/tool/SYSCONFIG.

8 Digital Peripherals

8.1 General Digital Peripheral Routing Guidelines

The following general routing recommendations should be followed throughout an AM273x PCB design. The 45nm LVCMOS process I/O can produce relatively fast edge-rates. Without transmission-line effects planned for, this can result in severe overshoot/undershoot even with relatively short traces on the PCB.

These uncontrolled level transitions can damage associated components by presenting attached I/O with over/under-voltage conditions. Additionally, these uncontrolled transitions can radiate excessively which creates cross-talk and EMI compliance problems.

To mitigate these problems:

- Route all digital I/O as controlled impedance transmission-lines (Microstrip/Stripline)
- Place series termination near each AM273x transmit pin and attached transmit pins of associated IC
  - The values and performance of these termination resistors should be validated during wake-up of new PCB hardware.
  - In some cases, these termination resistors may not be required, but they should only be removed or eliminated from the design after testing
- Route with solid ground return planes on adjacent layers
- Route with ground return rings surrounding constantly switching signals (clocks, EPWM)
- Route with ground return rings surrounding sensitive analog signals (ADC/DAC channels, VREF)

9 Layer Stackup

The AM273x MCU is packaged in either a ZCE0285A 285 ball, 0.65mm pitch, 19 x 19 NFBGA array [1] with select balls strategically removed or a NZN0225 225 ball 0.8mm pitch 15 x 15 full NFBGA array. The strategically removed balls on the ZCE package allow for easier escape routing by allowing for more and larger vias to be placed underneath the package. The larger pitch on the NZN package allows for larger trace and clearance routing rules in escape routing.

9.1 TMDS273GPEVM Layer Stackup

In the AM273 GPEVM, a 10-layer stackup design is used to fully route all power and signal pins across the ZCE package device for the EVM.

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		2mil	3.9
1	Top Layer		Signal	1oz	1.85mil	
	Dielectric 1	FR-4 High Tg	Prepreg		3.696mil	3.79
2	GND1		Signal	1oz	1.26mil	
	Dielectric 2	FR-4 High Tg	Core		6mil	4.46
3	SIG1		Signal	1oz	1.26mil	
	Dielectric 3	FR-4 High Tg	Prepreg		7.104mil	3.79
4	GND2		Signal	1oz	1.26mil	
	Dielectric 4	FR-4 High Tg	Core		4mil	4.4
5	PWR1		Signal	1oz	1.26mil	
	Dielectric 5	FR-4	Prepreg		5.292mil	3.79
6	PWR2		Signal	1oz	1.26mil	
	Dielectric 6	FR-4 High Tg	Core		4mil	4.4
7	GND3		Signal	1oz	1.26mil	
	Dielectric 7	FR-4 High Tg	Prepreg		7.104mil	3.79
8	SIG2		Signal	1oz	1.26mil	
	Dielectric 8	FR-4 High Tg	Core		6mil	4.46
9	GND4		Signal	1oz	1.26mil	
	Dielectric 9	FR-4 High Tg	Prepreg		3.696mil	3.79
10	Bottom Layer		Signal	1oz	1.85mil	
	Bottom Solder	Solder Resist	Solder Mask		2mil	3.9
	Bottom Overlay		Overlay			

Figure 9-1. AM273 GPEVM Layer Stackup

Lower layer count stackup solutions are possible, especially when considering partial signal fan-out designs. When utilizing designs with fewer layer counts, signal return paths and power and ground plane designs become more challenging to ensure reliable performance and minimal radiated emissions.

9.1.1 TMDS273GPEVM Key Stackup Features

- Standard 62 mil total thickness
- 4 optionally controlled impedance routing layers on L1, L3, L8 and L10.
- All signal and power layers have adjacent ground reference for controlled impedance planning and EMI performance
- Minimal dielectric thickness between L5 power and L4 GND return layers as well as L6 power and L7 GND return layers for best plane capacitance performance, aiding power integrity and EMI.
- Example fan-out with all through-hole via layer transitions – no micro-via or via-in-pad necessary.

Table 9-1. TMDS273GPEVM Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane
Copper 3	Embedded Microstrip/Stripline signal routing and power routing
Copper 4	Ground return plane
Copper 5	Power routing
Copper 6	Power routing
Copper 7	Ground return plane
Copper 8	Embedded Microstrip/Stripline signal routing and power routing
Copper 9	Ground return plane
Copper 10 (Bottom)	Bottom layer mounting and signal routing

9.2 Four Layer ZCE Example Layer Stackup

A proof-of-concept, full signal, escape routing of the 0.65 mm pitch ZCE package in four layers is shown in https://www.ti.com/lit/zip/sprad61.

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.394mil	3.3
1	Top Layer		Signal	1oz	1.378mil	
	Dielectric 1	FR-4 High Tg	Prepreg		3.937mil	4.3
2	GND		Signal	1oz	1.378mil	
	Dielectric 2	FR-4 High Tg	Core		47.244mil	4.3
3	Power		Signal	1oz	1.378mil	
	Dielectric 3	FR-4 High Tg	Prepreg		3.937mil	4.3
4	Bottom Layer		Signal	1oz	1.378mil	
	Bottom Solder	Solder Resist	Solder Mask		0.394mil	3.3
	Bottom Overlay		Overlay			

Figure 9-2. AM273 ZCE Four Layer Example Layer Stackup

9.2.1 ZCE Four Layer Example Key Stackup Features

- Standard 62 mil total thickness
- Only top layer has adjacent ground reference for controlled impedance planning
- Single GND plane on layer 2 as most signals are routed on layer 1, allowing the best signal return paths for the most signals possible
- Larger dielectric thickness between L3 power and L2 GND return layers has reduced plane capacitance performance compared to higher layer count stackups, potentially impacting power integrity and EMI.
- Example fan-out with all through-hole via layer transitions – no micro-via or via-in-pad necessary.

Table 9-2. ZCE Four Layer Example Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane with cutouts for 3.3V plane sections
Copper 3	Power routing
Copper 4 (Bottom)	Bottom layer mounting and signal routing

9.3 Four Layer NZN Example Layer Stackup

A proof-of-concept, full signal, escape routing of the 0.8mm pitch NZN package in four layers is shown in .

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.394mil	3.3
1	Top Layer		Signal	1oz	1.378mil	
	Dielectric 1	FR-4 High Tg	Prepreg		3.937mil	4.3
2	GND		Signal	1oz	1.378mil	
	Dielectric 2	FR-4 High Tg	Core		47.244mil	4.3
3	Power		Signal	1oz	1.378mil	
	Dielectric 3	FR-4 High Tg	Prepreg		3.937mil	4.3
4	Bottom Layer		Signal	1oz	1.378mil	
	Bottom Solder	Solder Resist	Solder Mask		0.394mil	3.3
	Bottom Overlay		Overlay			

Figure 9-3. AM273 NZN Four Layer Example Layer Stackup

9.3.1 NZN Four Layer Example Key Stackup Features

- Standard 62 mil total thickness
- Only top layer has adjacent ground reference for controlled impedance planning
- Single GND plane on layer 2 as most signals are routed on layer 1, allowing the best signal return paths for the most signals possible
- Larger dielectric thickness between L3 power and L2 GND return layers has reduced plane capacitance performance compared to higher layer count stackups, potentially impacting power integrity and EMI.
- Example fan-out with all through-hole via layer transitions – no micro-via or via-in-pad necessary.

Table 9-3. NZN Four Layer Example Layer Utilization

Layer Number	Comment
Copper 1 (Top)	Top layer mounting and signal routing
Copper 2	Ground return plane with cutouts for 3.3V plane sections
Copper 3	Power routing
Copper 4 (Bottom)	Bottom layer mounting and signal routing

10 Vias

The AM273 GPEVM and ZCE/NZN 4 Layer Escape Routing Examples show PTH via only construction. Via-in-pad construction can also be used to provide minimal decoupling capacitor mounting distance from the BGA. This results in a more optimal power distribution network at the cost of additional fabrication cycle time per PCB.

Table 10-1. AM273x Hardware Via Types

EVM	Via Type	Via Diameter (mils)	Via Drill (mils)
AM273 GPEVM	PTH	18.000	8.000
AM273x ZCE 4 Layer Escape Routing Example	PTH	18.000	8.000
AM273 NZN 4 Layer Escape Routing Example	PTH	18.000	8.000

11 BGA Power Fan-Out and Decoupling Placement

45 nm CMOS technology allows for faster core and SRAM clock rates, and faster edge rates for LVCMOS I/O buffers. Therefore, in comparison with previous MCU process nodes, careful power and ground return placement is critical to achieving the best power integrity, signal integrity, and EMI performance with AM273x designs.

It is recommended that designers follow a similar power distribution layout as implemented in the AM273x GPEVM or 4-layer ZCE or NZN escape routing designs to achieve good power integrity results across all operating conditions and EMI testing conditions.

The AM273 GPEVM represents the most optimized and scrutinized power distribution layout example so far and is referenced in this section.

11.1 Ground Return

All available ground return BGA balls should be utilized to create the best possible electrical and thermal connection between the AM273x package and the attached PCB. Roughly the center 7 x 7 BGA balls on the ZCE package and 5x6 BGA balls on the NZN package are dedicated to ground return with a few other I/O return paths placed near the edges of the BGA. For best thermal performance, solid ground return planes should be used directly under the BGA on as many layers as possible.

The AM273x contains both analog and digital ground return pins. Both analog and digital ground return pins should be shorted to a common set of ground return planes on the PCB for best noise and EMI performance as this creates the lowest possible impedance path for all return currents to follow. It is not recommended to separate these two return paths as this typically ends up with lower performance return paths for both digital and analog signal paths.

11.1.1 Ground Return - TMDS273GPEVM

On the AM273x GPEVM, the top layer has a central ground pour that connects to as many vias as possible between the adjacent ground pads. On the bottom layer, these vias are enclosed in a central ground pour that connects to many of the decoupling capacitor footprints.

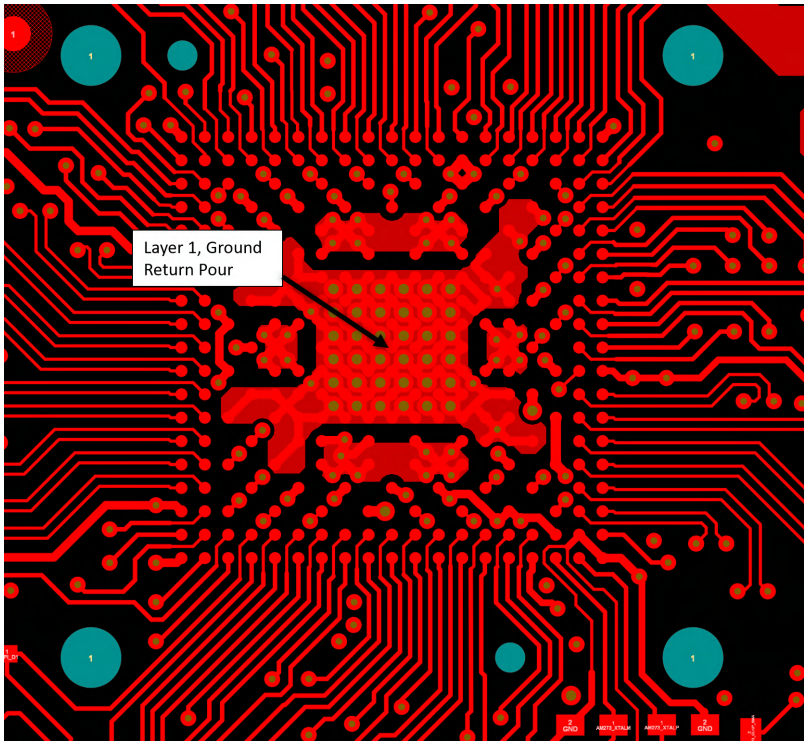

Figure 11-1. AM273 GPEVM Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 1

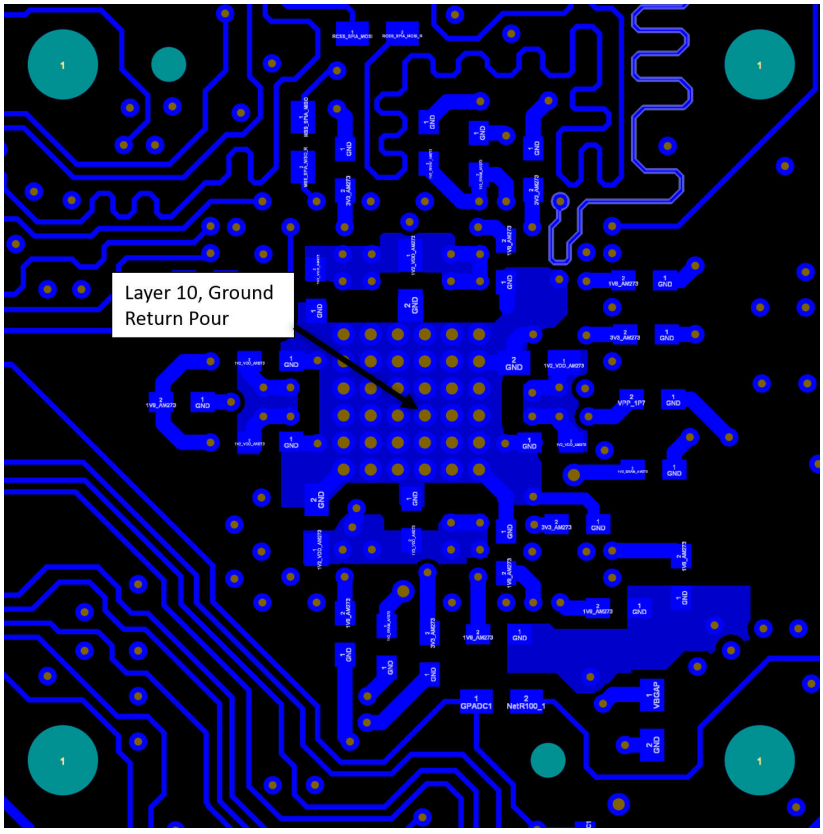

Figure 11-2. AM273 GPEVM Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 10

11.1.2 Ground Return - ZCE Four Layer Example

On the AM273x ZCE 4 Layer Escape Routing example, the top layer has a central ground pour that connects to as many vias as possible between the adjacent ground pads. On the bottom layer, these vias are enclosed in a central ground pour that connects to many of the decoupling capacitor footprints.

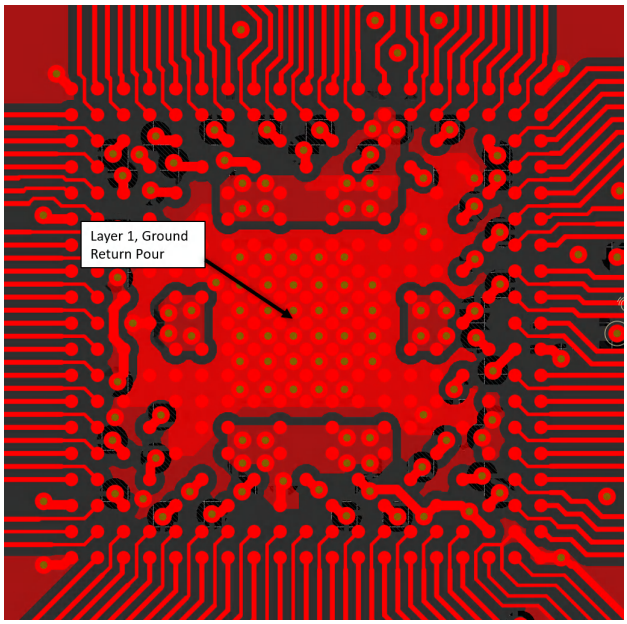

Figure 11-3. ZCE 4 Layer Example Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 1

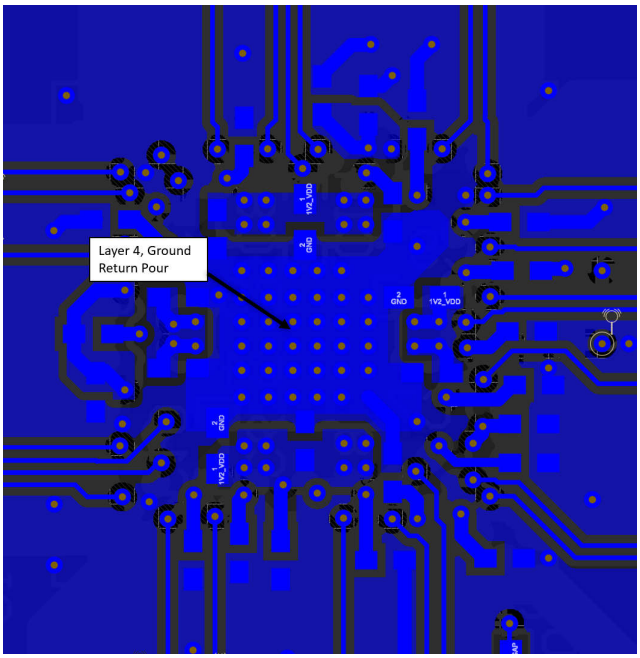

Figure 11-4. ZCE 4 Layer Example Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 4

11.1.3 Ground Return - NZN Four Layer Example

On the AM273x NZN 4 Layer Escape Routing example, the top layer has a central ground pour that connects to as many vias as possible between the adjacent ground pads. On the bottom layer, these vias are enclosed in a central ground pour that connects to many of the decoupling capacitor footprints.

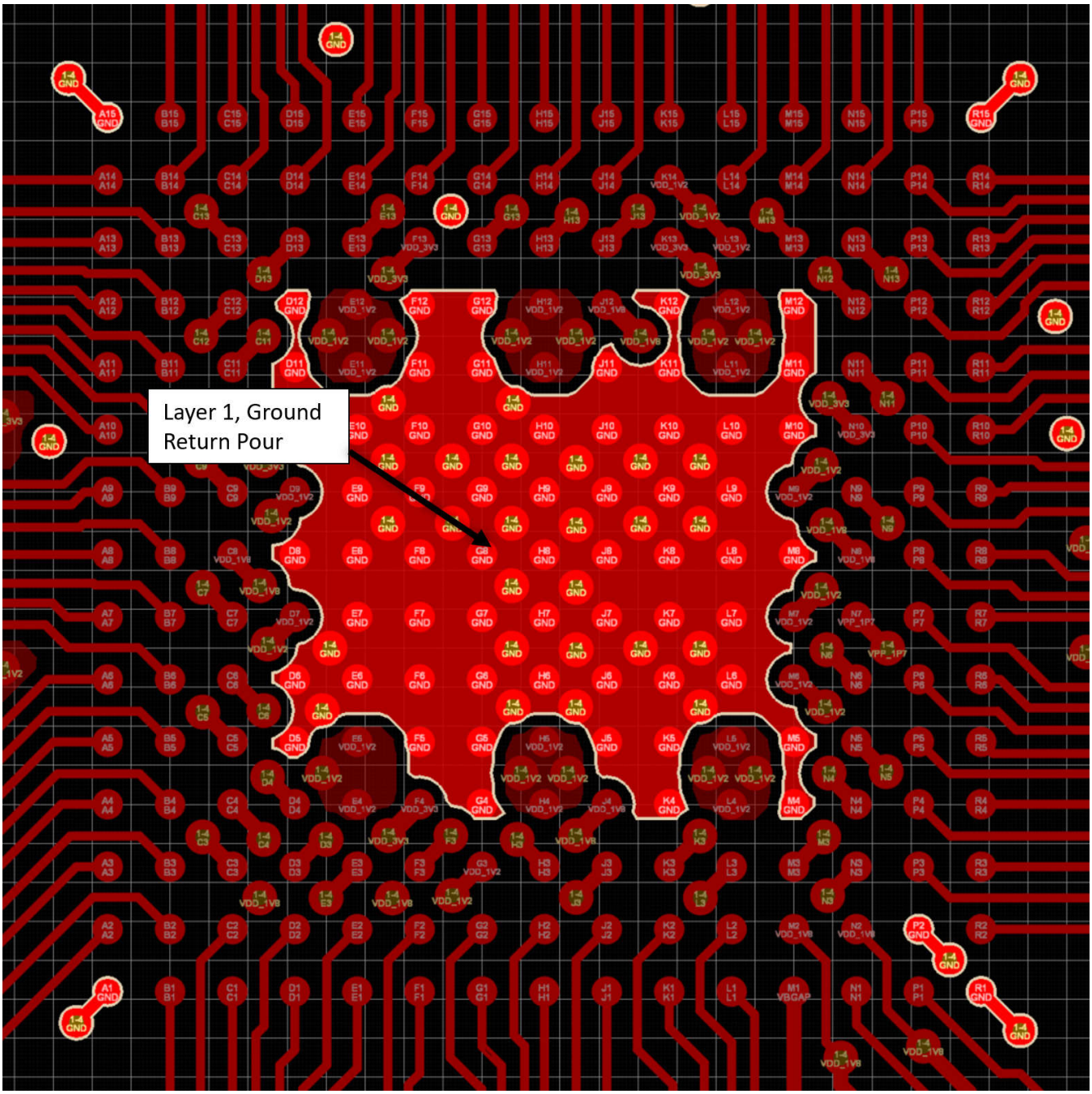

Figure 11-5. NZN 4 Layer Example Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 1

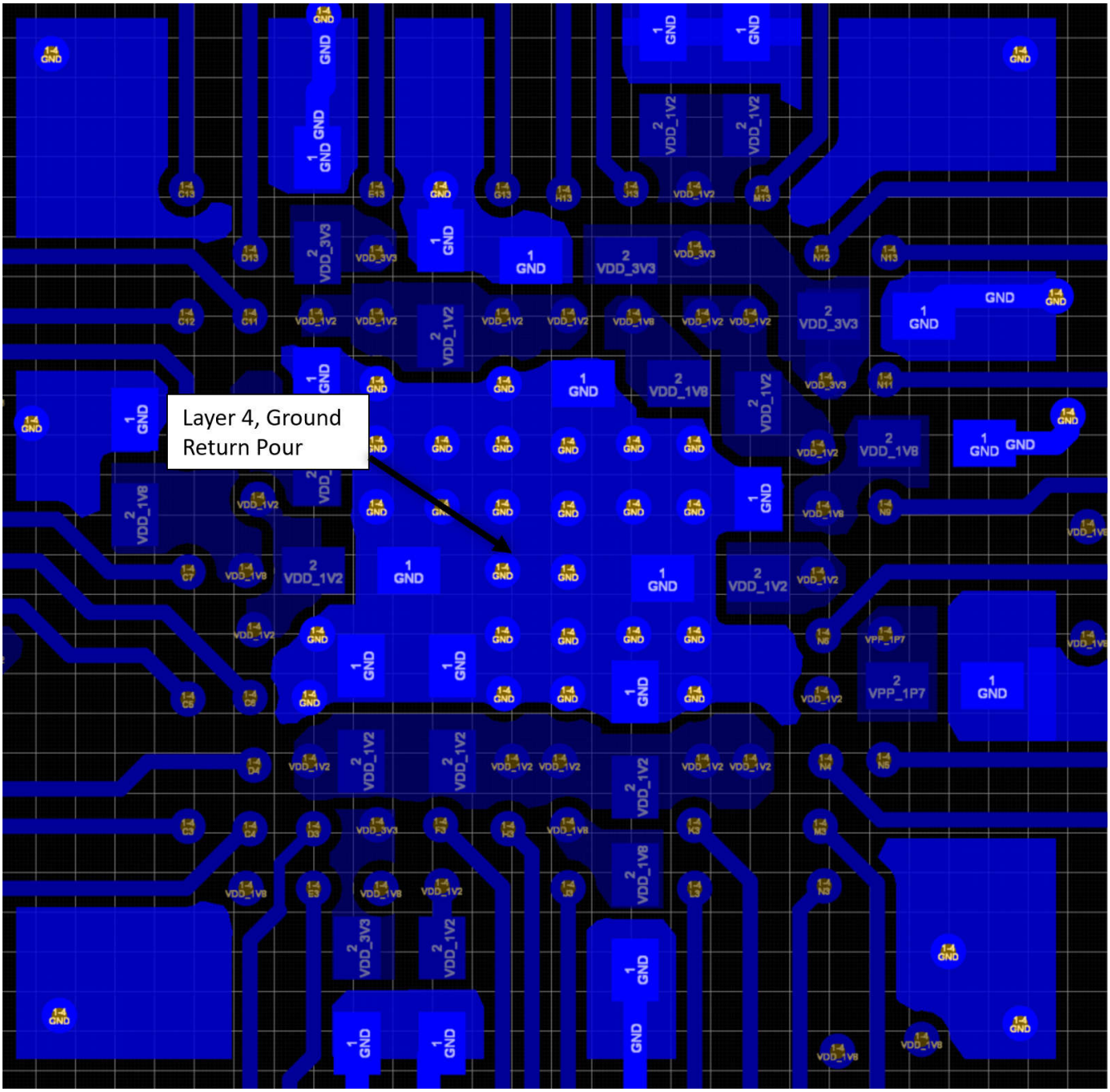

Figure 11-6. NZN 4 Layer Example Excerpt – Ground Return Pour and Vias Under AM273x BGA Layer 4

11.2 1.2 V Core Digital Power

This section summarizes the main elements of the 1.2 V core digital power routing of the AM273x device from the 1.2 V output of the power subsystem on the board through the board power planes and ending at the BGA bulk and per pin decoupling capacitor array.

11.2.1 1.2 V Core Digital Power Key Layout Considerations

- AM273x should be co-located with the 1.2 V core digital regulator or PMIC to allow for minimal IR drop from the regulator to the BGA power pins.
- Wide 15 mil traces should be used for all power and ground return via fan-out.
- A dedicated power layer with tightly coupled ground return reference plane should be used for best transient performance and EMI coupling

- A wide power plane entry into the center of the BGA 1.2 V power pin areas should be used for minimal IR drop and best transient performance
- Larger packaged, lower-frequency, bulk capacitance should be placed adjacent to AM273x BGA with vias directly to power plane paths
- Smaller packaged, higher-frequency, decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

11.2.1.1 1.2V Core Layout - TMDS273GPEVM

On the AM273 GPEVM, the 1.2 V plane is primarily located on layer 6, with a filter and current sense shunt resistor on layer 1 adjacent to the AM273 device. After passing through the shunt resistor the 1.2 V plane moves to layer 5 underneath the AM273 where the vias connect to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

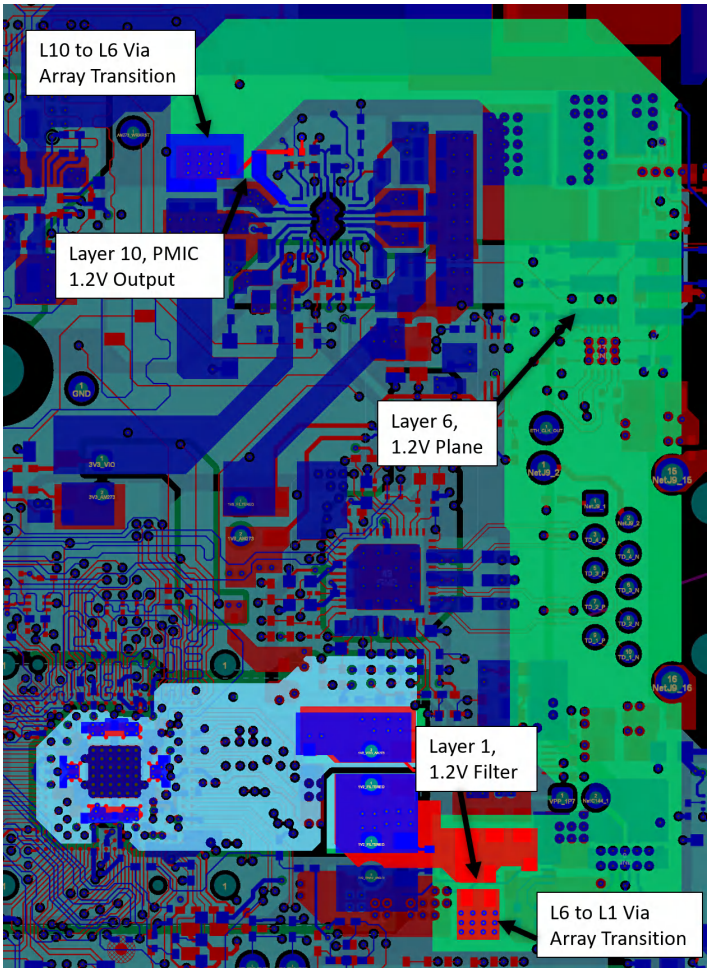

Figure 11-7. AM273 GPEVM Excerpt – 1.2 V Core Power Output from PMIC, Power Plane Vias, and BGA Vias

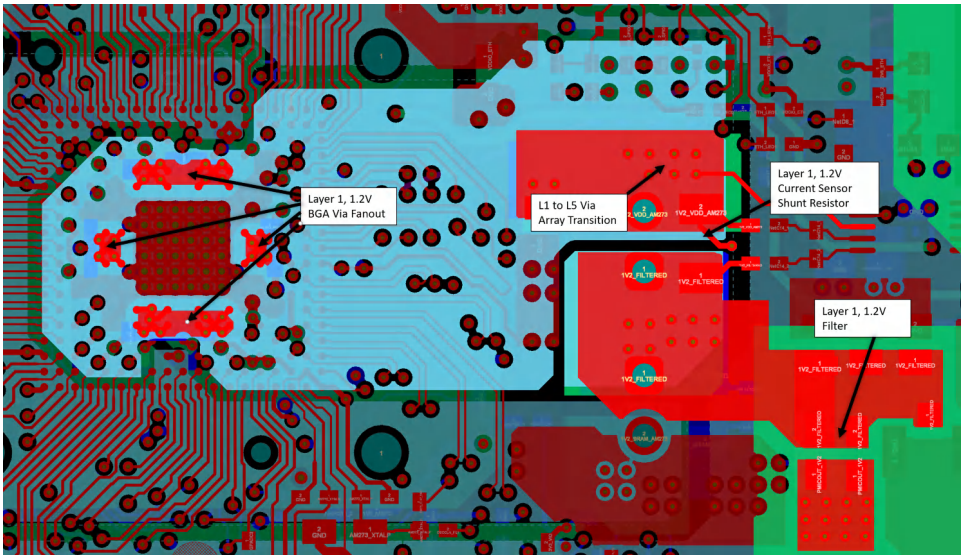

Figure 11-8. AM273 GPEVM Excerpt – 1.2 V Core Power Plane and Vias into BGA

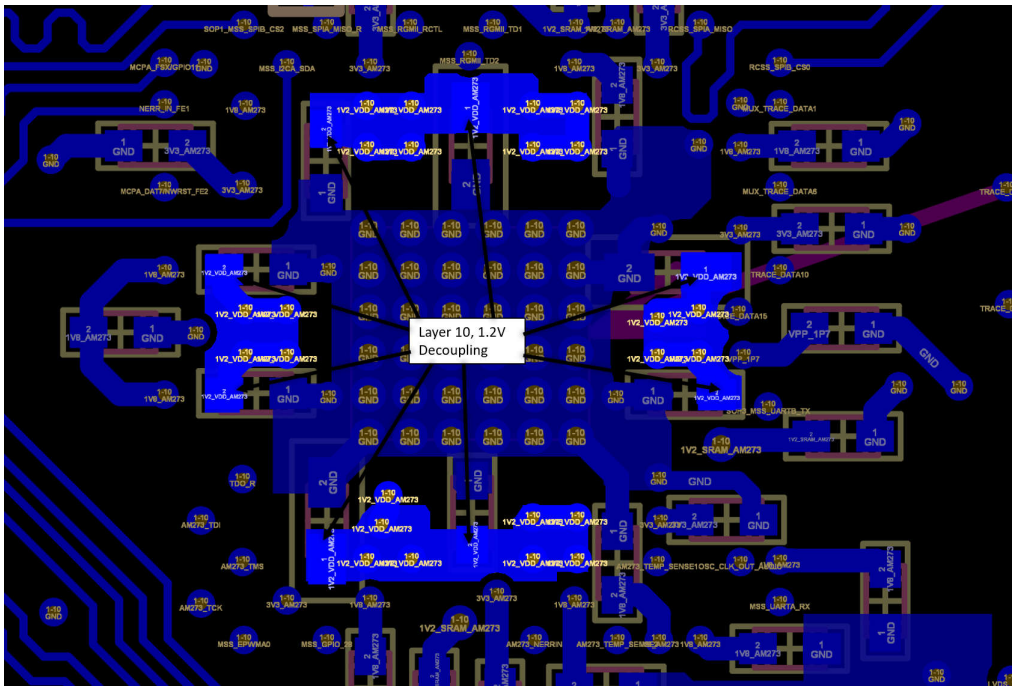

Figure 11-9. AM273 GPEVM Excerpt – 1.2 V Core Power Decoupling Mounting, Layer 10

11.2.1.2 1.2V Core Layout - ZCE Four Layer Example

On the AM273 NZN Four Layer Example, the 1.2 V plane is shown routing to and underneath the AM273 device on layer 3. Vias connect the plane on layer 3 to the BGA ball pads on layer 1 and the decoupling capacitors on the bottom layer.

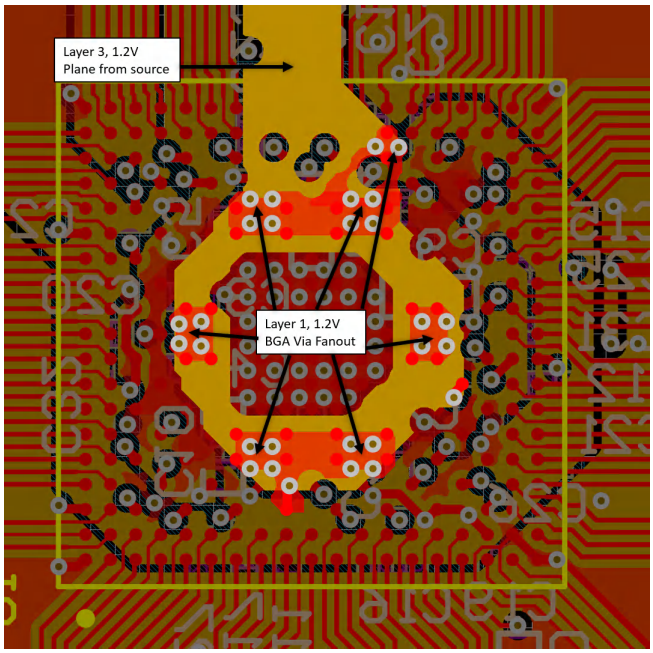

Figure 11-10. ZCE 4 Layer Example Excerpt – 1.2 V Core Power Output From Source and BGA Vias

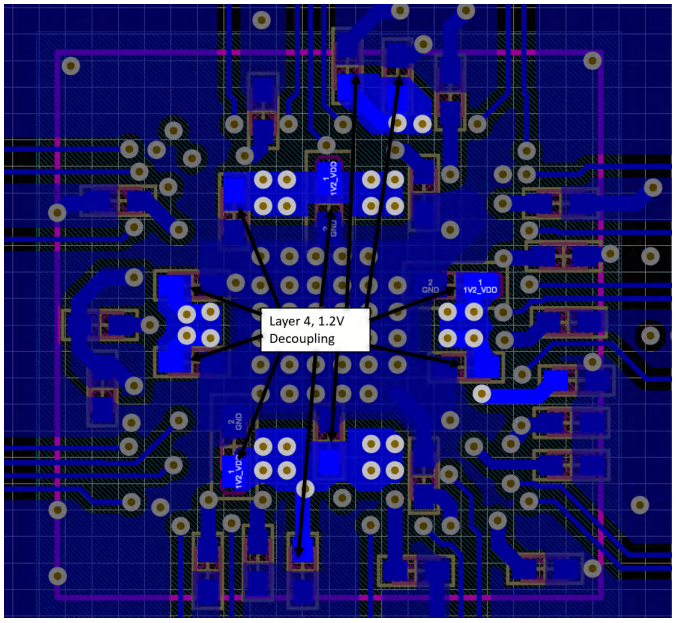

Figure 11-11. ZCE 4 Layer Example Excerpt – 1.2 V Core Power Decoupling Mounting, Layer 4

11.2.1.3 1.2V Core Layout - NZN Four Layer Example

On the AM273 NZN Four Layer Example, the 1.2 V plane is shown routing to and underneath the AM273 device on layer 3. Vias connect the plane on layer 3 to the BGA ball pads on layer 1 and the decoupling capacitors on the bottom layer.

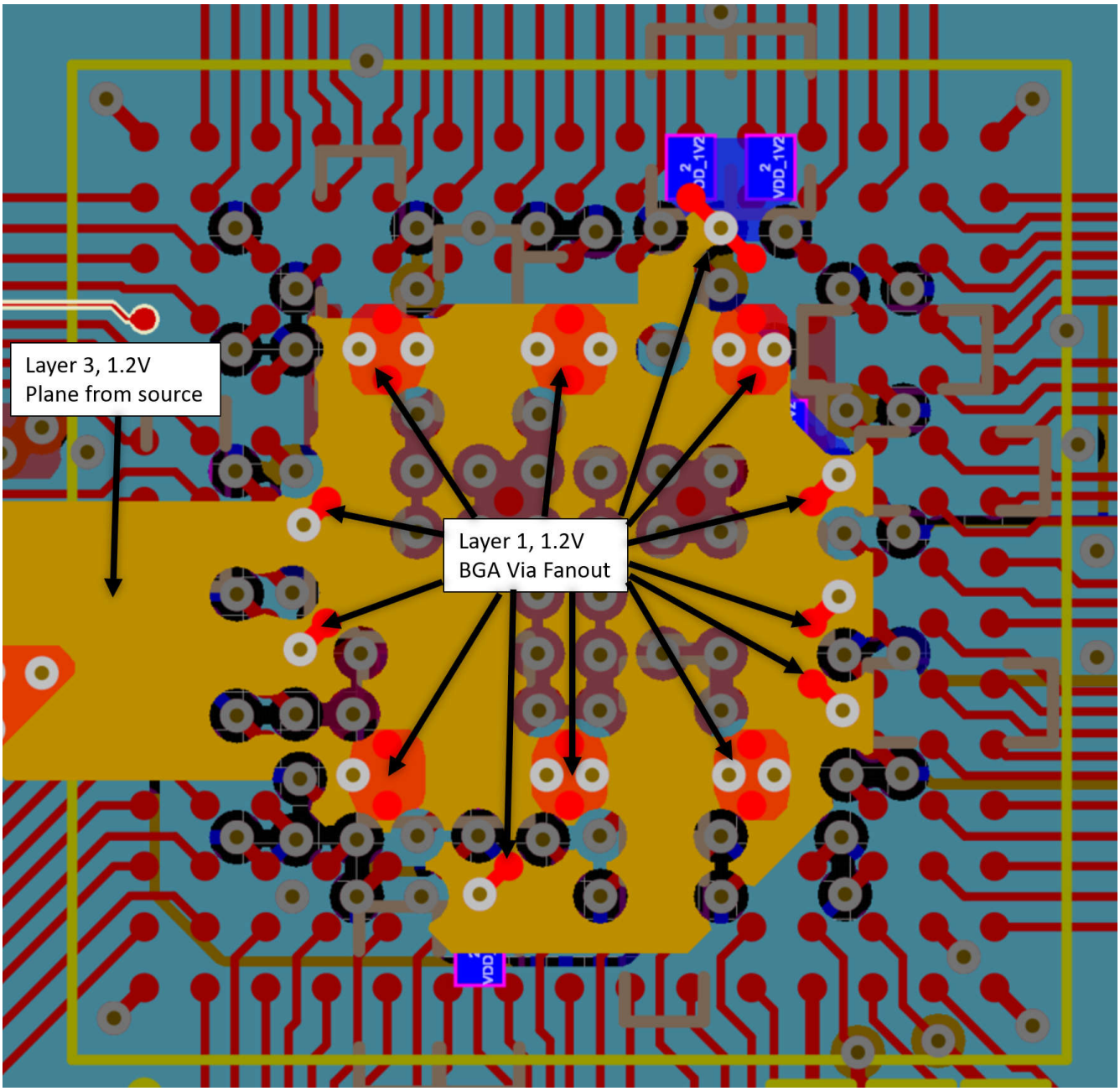

Figure 11-12. NZN 4 Layer Example Excerpt – 1.2 V Core Power Output from source and BGA Vias

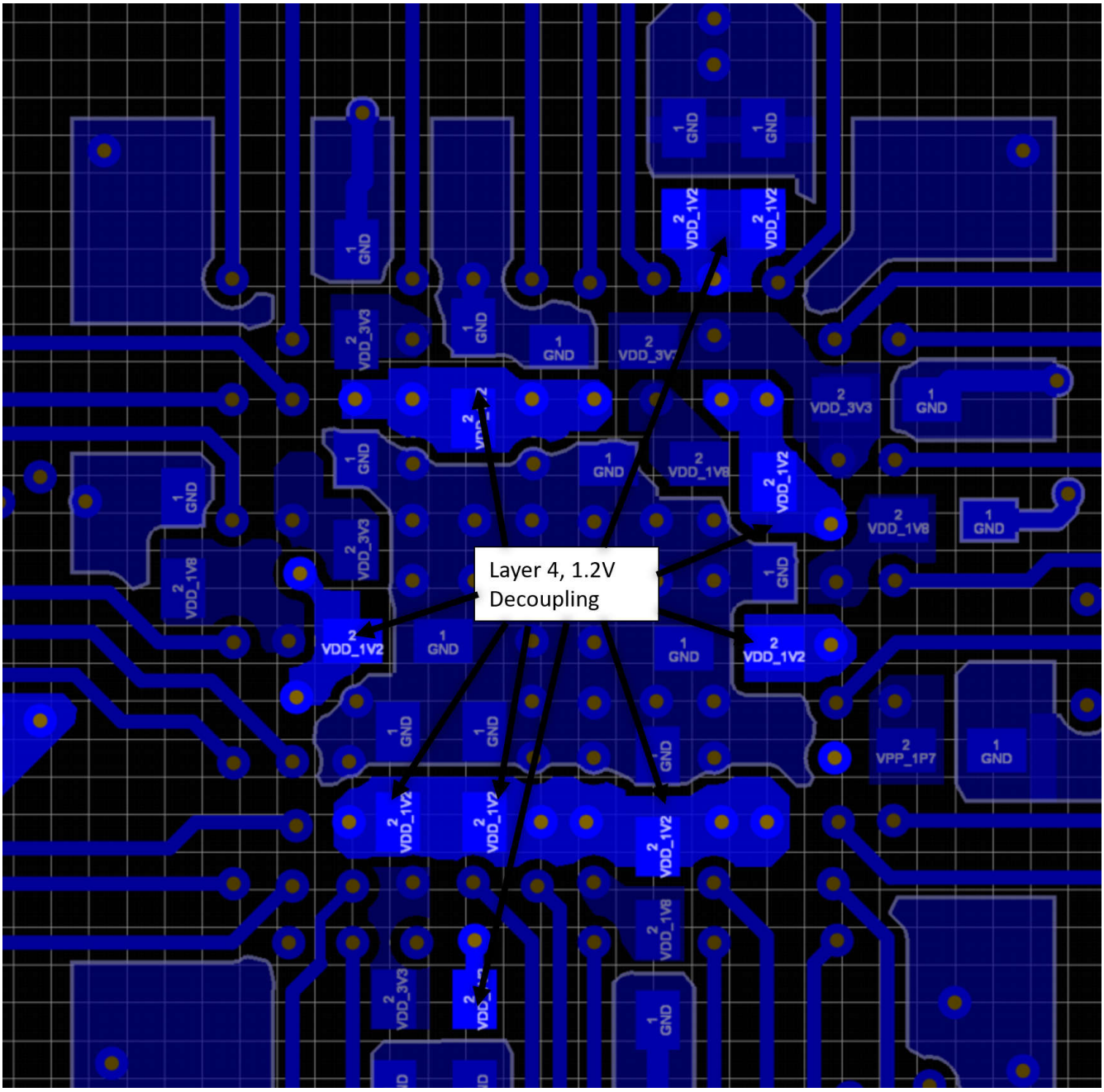

Figure 11-13. NZN 4 Layer Example Excerpt – 1.2 V Core Power Decoupling Mounting, Layer 4

11.3 3.3 V Digital and Analog Power

This section summarizes the main elements of the 3.3 V digital I/O and analog I/O power routing of the AM273x device from the 3.3 V output of the power subsytem through the board power planes and ending at the BGA bulk and per pin decoupling capacitor array.

11.3.1 3.3 V Digital and Analog Power Key Layout Considerations

- Wide 15 mil traces should be used for all power and ground return via fan-out.
- 3.3 V I/O power tends to be shared across multiple devices in the system, recommend routing with very wide power planes across the PCB to minimize IR drops to all components including the AM273x
- A tightly coupled, adjacent ground return, reference plane should be used for best transient performance and EMI coupling

- A wide power plane entry that covers the BGA 3.3 V power pin areas should be used for minimal IR drop and best transient performance
- Larger packaged, lower-frequency, bulk capacitance should be placed adjacent to AM273x BGA with vias directly to power plane paths
- Smaller packaged, higher-frequency, decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

11.3.1.1 3.3V Digital and Analog Layout - TMDS273GPEVM

A common step-down-converter generates a 3.3 V rail that is supplied to the PMIC on the AM273x GPEVM as well as the peripheral 3.3 V system needs and LDOs for the 2.5 V Ethernet and 1.7V VPP power rails. The PMIC generates a 3.3 V rail on the VIO_LDO output, which supplies the 3.3 V analog and digital supplies for all of the AM273x digital I/O and analog I/O loads. This is common in most designs where all 3.3 V digital level I/O share a common power supply.

On the AM273 GPEVM, the 3.3 V rail is generated by the PMIC on layer 10, but transitions to layer 6 to spread across the board. There is a current sense shunt resistor on layer 1 between the main 3.3 V plane on the board and the 3.3 V plane to the AM273 device on layer 6. Vias underneath the AM273 device connect the plane to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

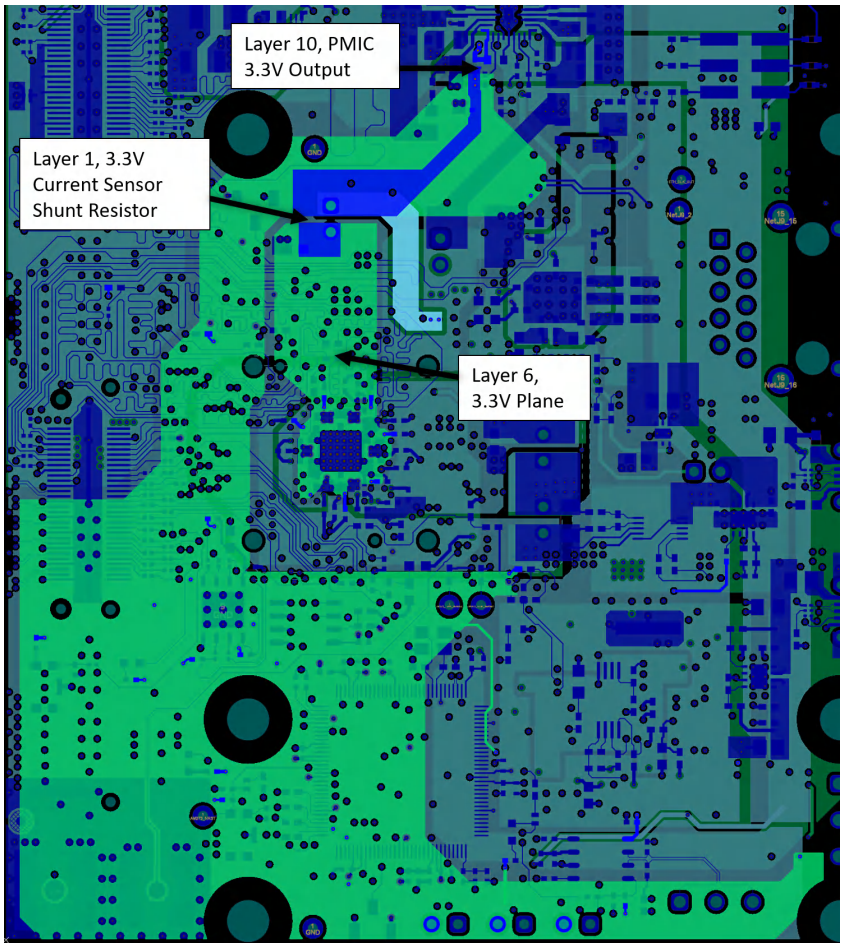

Figure 11-14. AM273 GPEVM Excerpt – 3.3 V Digital and Analog Power Planes on Layer 6

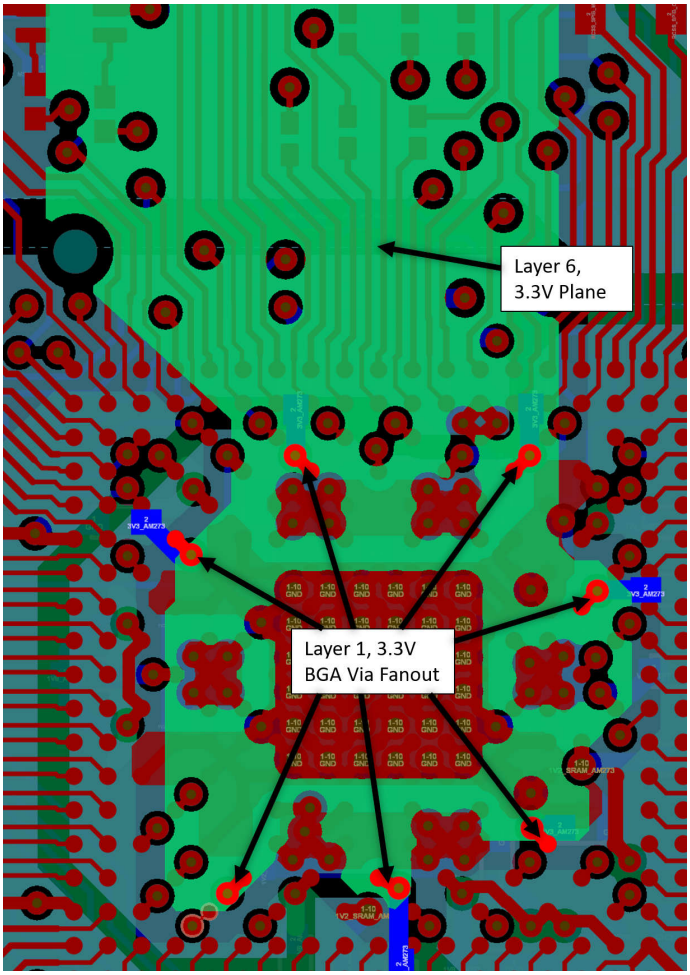

Figure 11-15. AM273 GPEVM Excerpt – 3.3 V Digital I/O and Analog I/O BGA Pinout

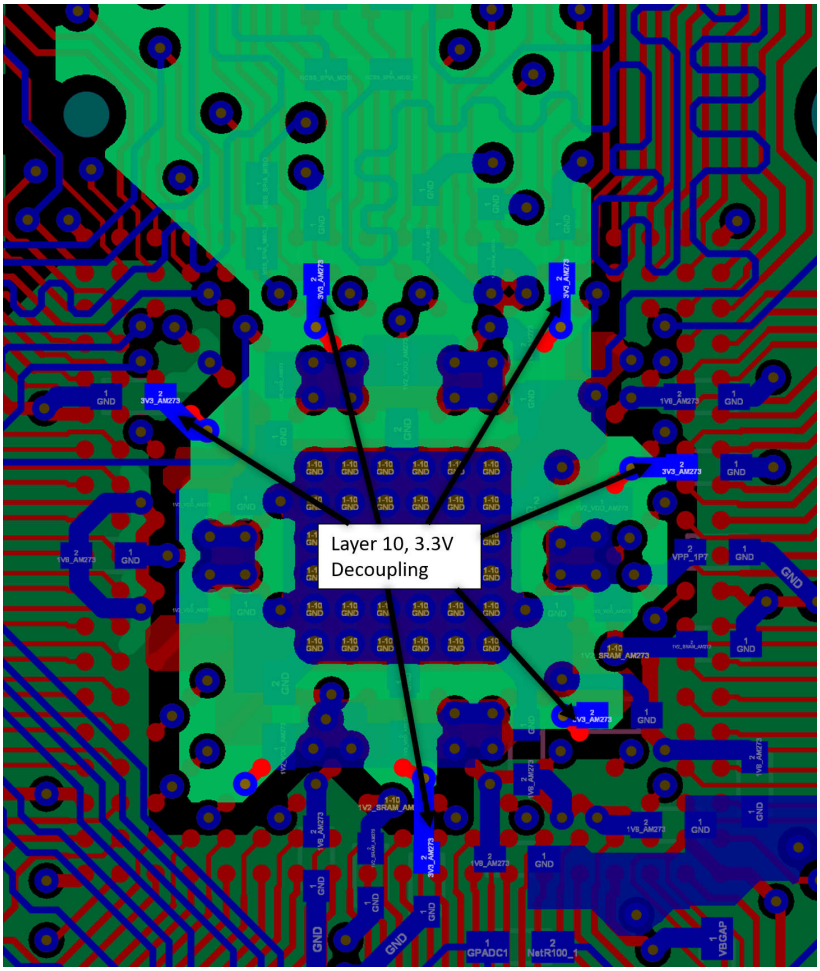

Figure 11-16. AM273 GPEVM Excerpt – 3.3 V Decoupling

11.3.1.2 3.3V Digital and Analog Layout - ZCE Four Layer Example

On the AM273 NZN Four Layer Example, the 3.3 V plane is shown routing to and underneath the AM273 device primarily on layer 3. Due to routing limitations caused by a four layer PCB, underneath the AM273 device the 3.3 V plane is split between layer 2 and layer 3.

The 3.3 V planes on layer 2 break up the otherwise solid ground pour on layer 2. The placement of these cutouts was chosen to minimize the impact to the signal return paths for as many GPIO pins as possible. Vias connect the planes on layers 2 and 3 to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

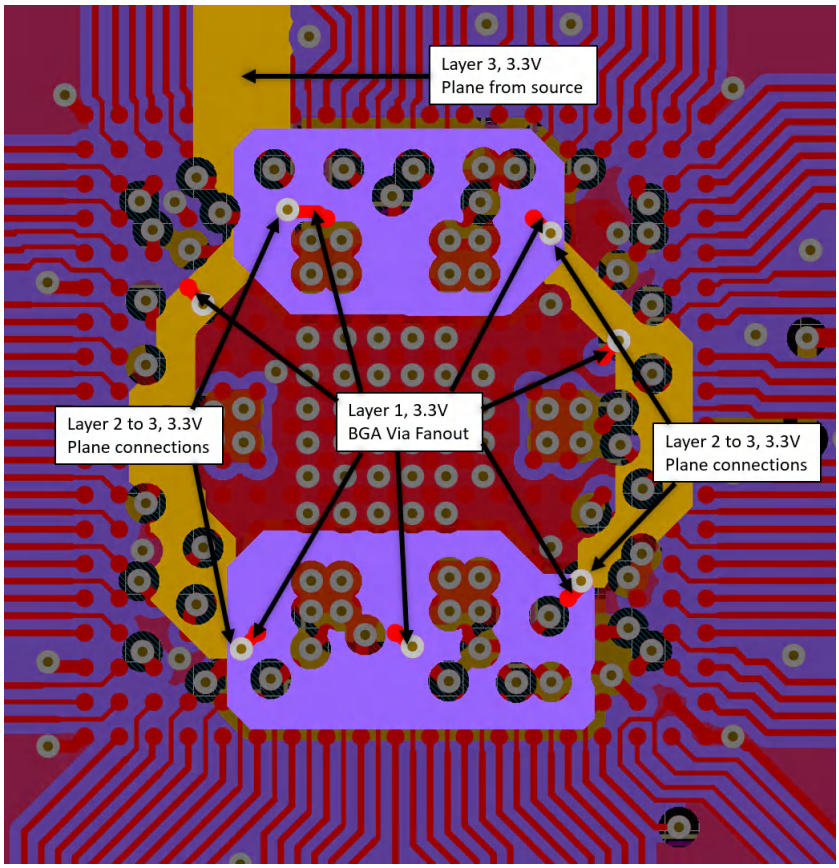

Figure 11-17. ZCE 4 Layer Example Excerpt – 3.3 V Digital and Analog Power Planes on Layers 2 and 3 and BGA Vias

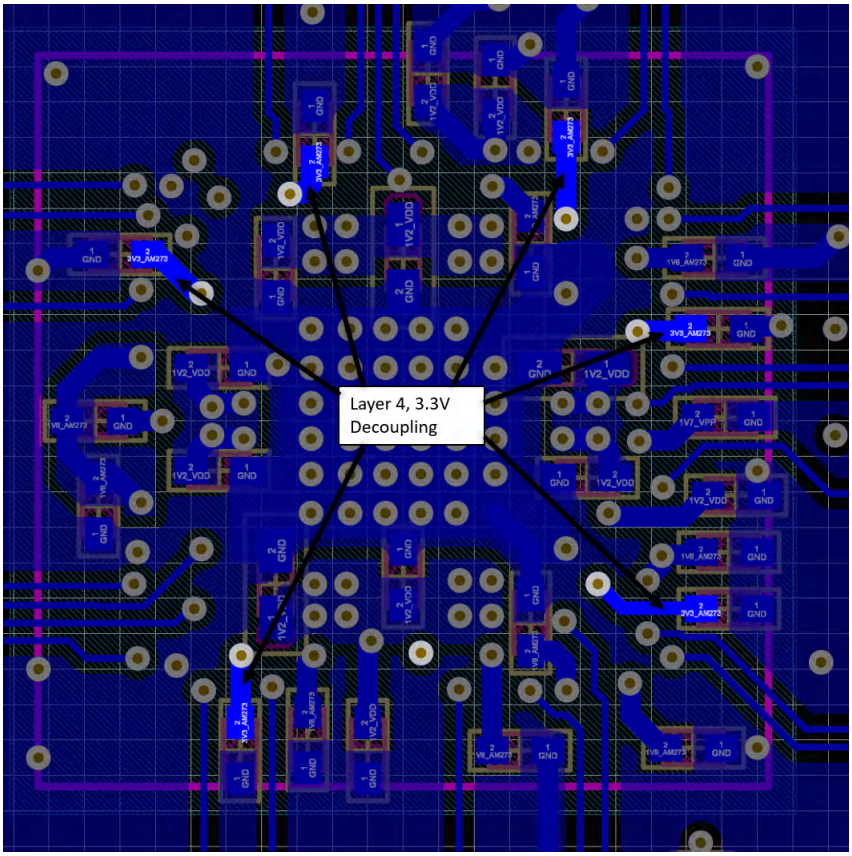

Figure 11-18. ZCE 4 Layer Example Excerpt – 3.3 V Decoupling

11.3.1.3 3.3V Digital and Analog Layout - NZN Four Layer Example

On the AM273 NZN Four Layer Example, the 3.3 V plane is shown routing to and underneath the AM273 device primarily on layer 3. Due to routing limitations caused by a four layer PCB, underneath the AM273 device the 3.3 V plane is split between layer 2 and layer 3.

The 3.3 V plane on layer 2 break up the otherwise solid ground pour on layer 2. The placement of the cutout was chosen to minimize the impact to the signal return paths for as many GPIO pins as possible. Vias connect the planes on layers 2 and 3 to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

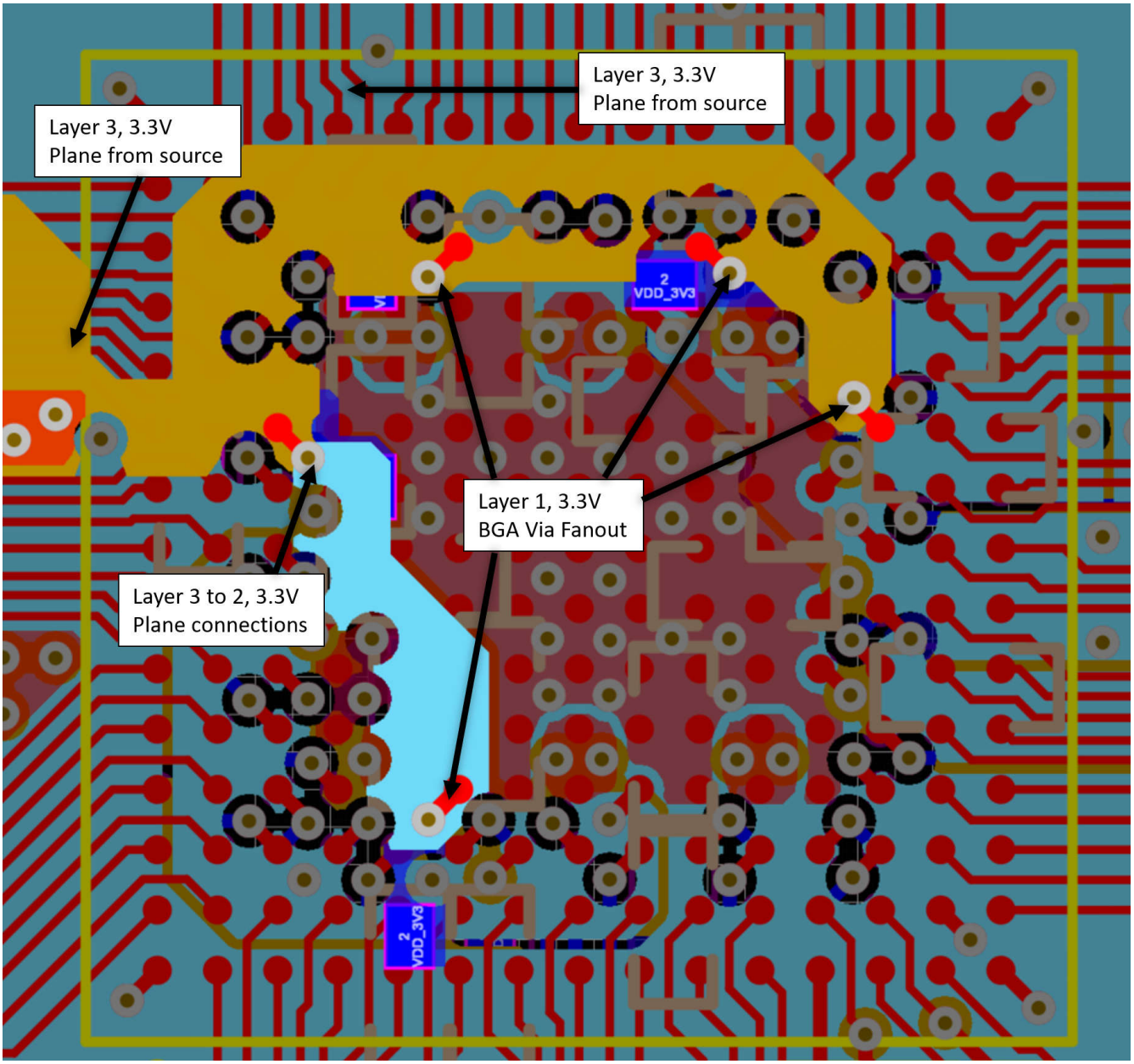

Figure 11-19. NZN 4 Layer Example Excerpt – 3.3 V Digital and Analog Power Planes on Layers 2 and 3 and BGA Vias

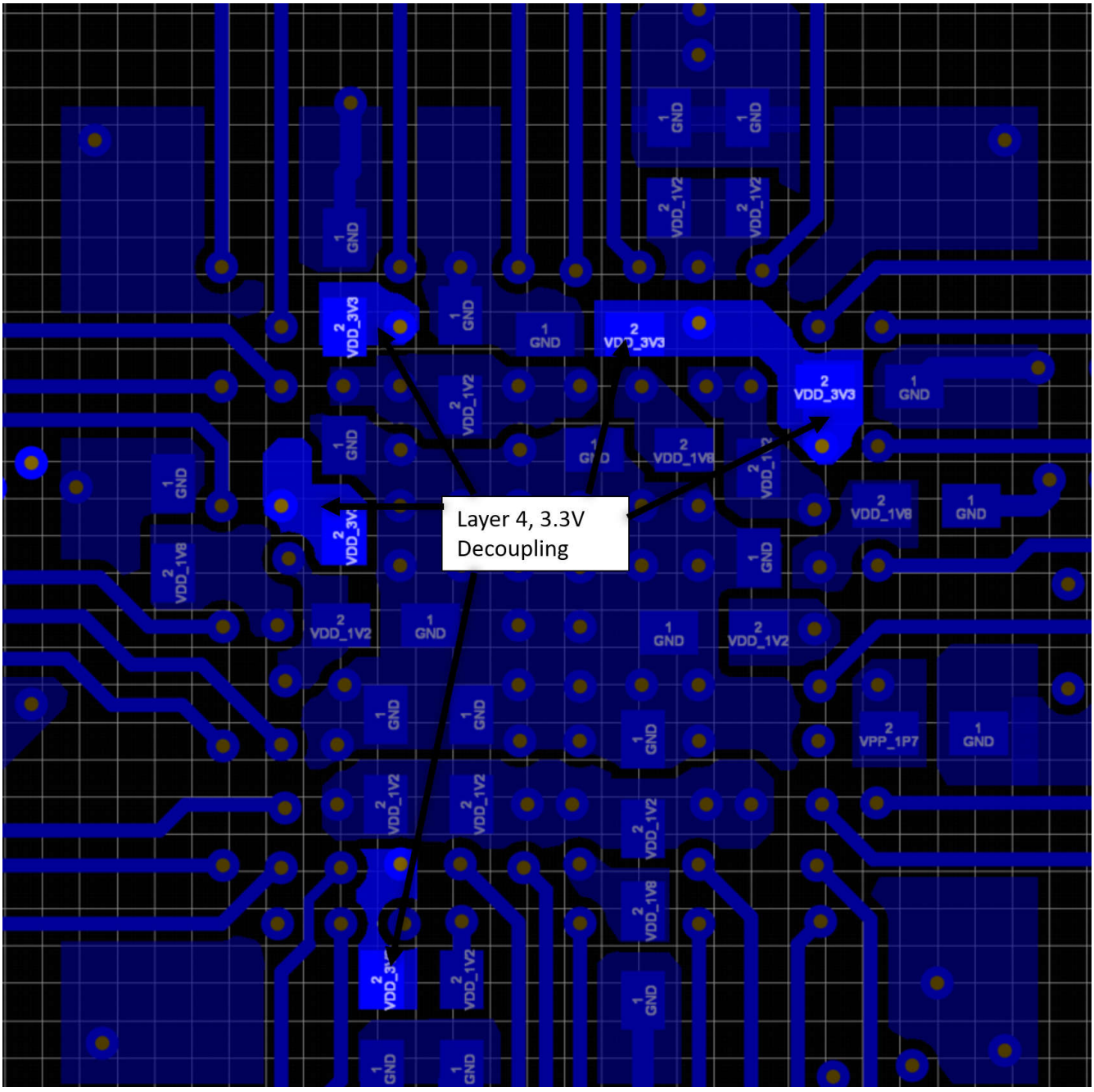

Figure 11-20. NZN 4 Layer Example Excerpt – 3.3 V Decoupling

11.4 1.8 V Digital and Analog Power

This section summarizes the main elements of the 1.8 V digital I/O and analog I/O power routing of the AM273 device. A single 1.8 V power net is generated from the power subsystem on the board and is connected to both the digital I/O and analog I/O 1.8 V power pins on the BGA.

11.4.1 1.8 V Digital and Analog Power Key Layout Considerations

- Wide 15 mil traces should be used for all power and ground return via fan-out.
- AM273x should be co-located with the 1.8 V regulator or PMIC to allow for minimal IR drop from the regulator to the BGA power pins.
- A tightly coupled, adjacent ground return, reference plane should be used for best transient performance and EMI coupling

- Smaller power planes or wider traces should be used for minimal IR drop and best transient routing across the associated BGA pins
- Smaller packaged, higher-frequency, decoupling capacitance should be placed directly on BGA fan-out vias with as small of a dog-bone to power and ground return vias as possible

11.4.1.1 1.8V Digital and Analog Layout - TMDS273GPEVM

On the AM273 GPEVM, the 1.8 V plane is located on layer 10 from the output of the PMIC to the current sense shunt resistor located on layer 1. From the shunt resistor, the 1.8 V plane is routed on layer 6 to the AM273 device where the vias connect to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

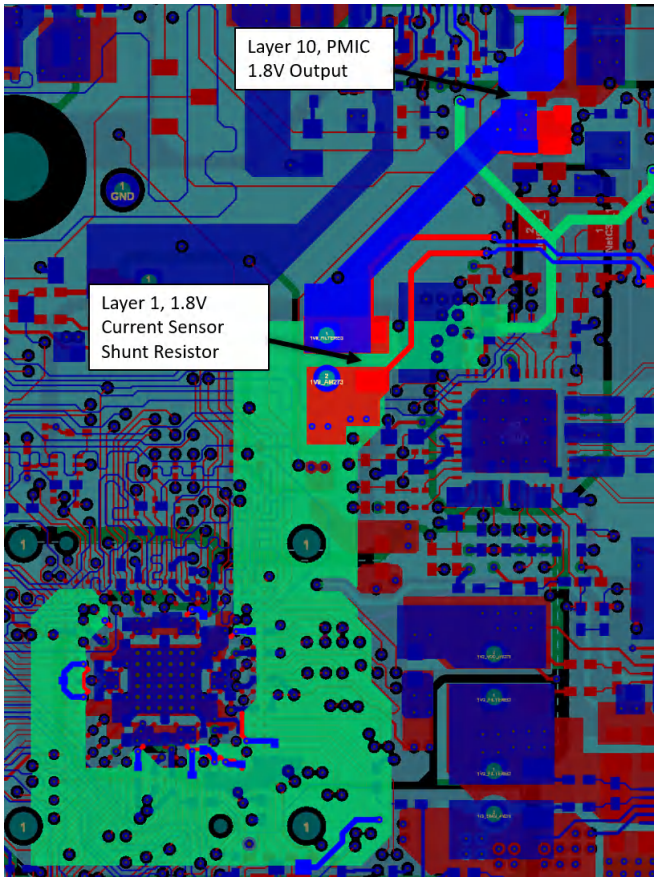

Figure 11-21. AM273 GPEVM Excerpt – 1.8 V Digital Power Via Fan-Out and Plane Routing Layer 6

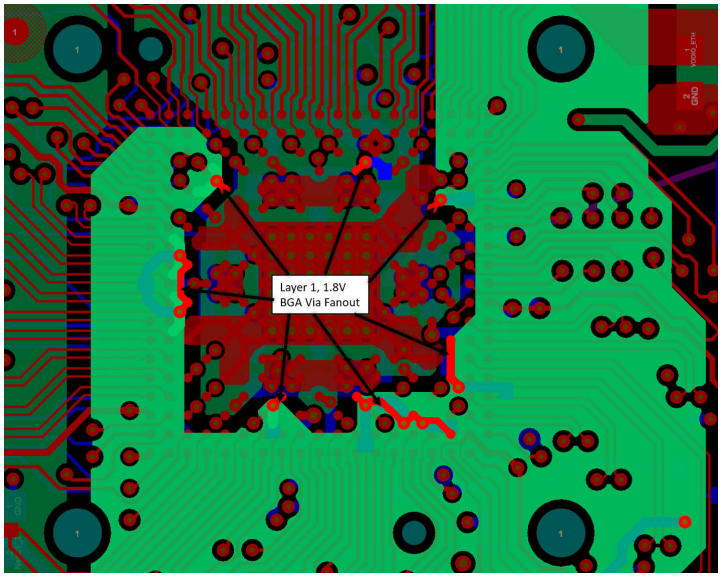

Figure 11-22. AM273 GPEVM Excerpt – 1.8 V Power Via Fan-Out and Plane Routing Layer 6

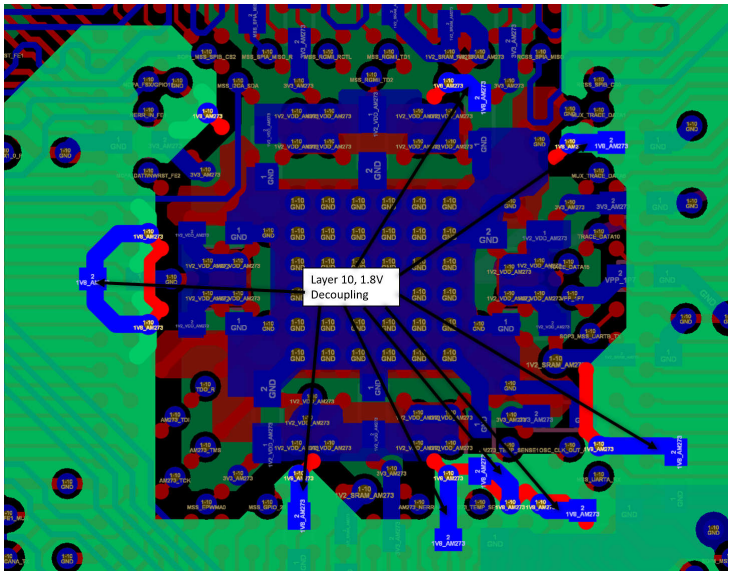

Figure 11-23. AM273 GPEVM Excerpt – 1.8 V Power Decoupling on Layer 10

11.4.1.2 1.8V Digital and Analog Layout - ZCE Four Layer Example

On the AM273 NZN Four Layer Example, the 1.8 V plane is shown routing to and underneath the AM273 device on layer 3. Vias connect the plane on layer 3 to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

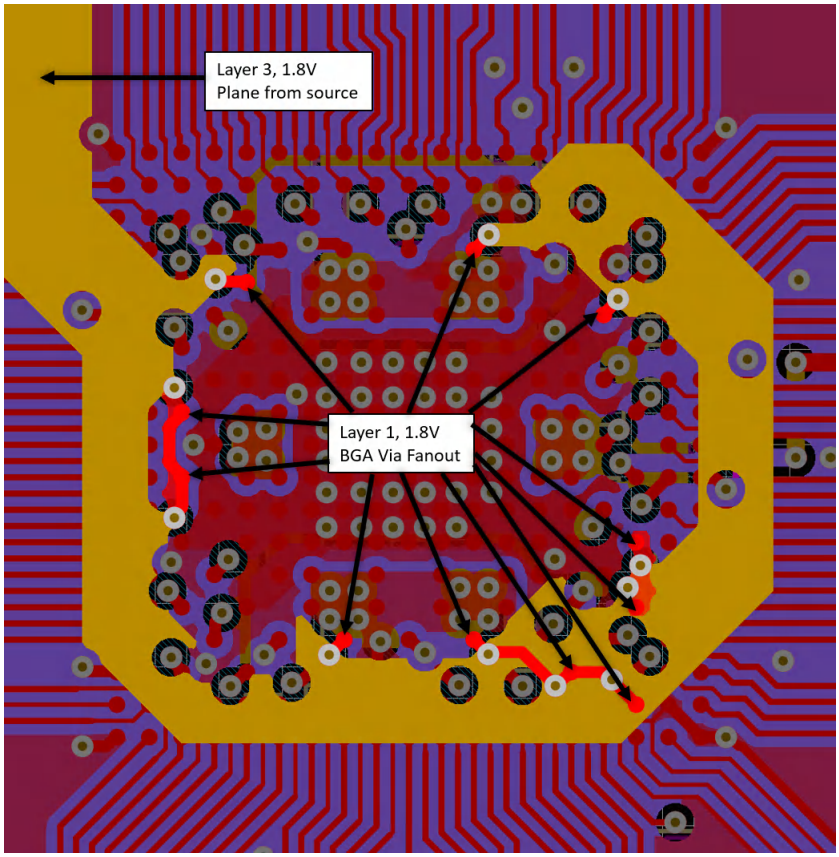

Figure 11-24. ZCE 4 Layer Example Excerpt – 1.8 V Power Via Fan-Out and Plane Routing Layer 3

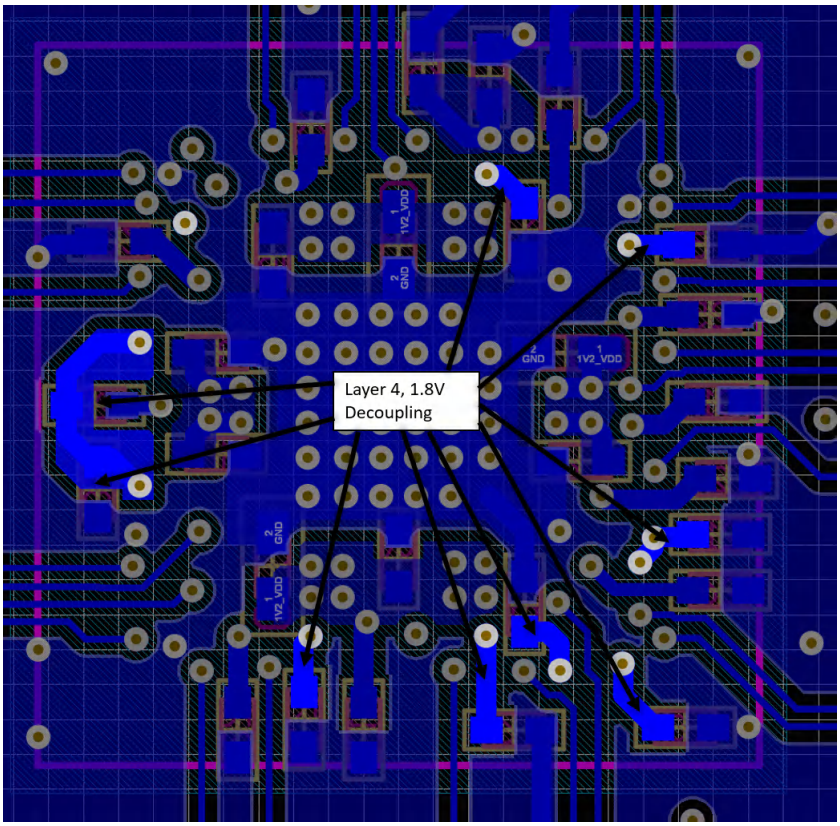

Figure 11-25. ZCE 4 Layer Example Excerpt – 1.8 V Power Decoupling on Layer 4

11.4.1.3 1.8V Digital and Analog Layout - NZN Four Layer Example

On the AM273 NZN Four Layer Example, the 1.8 V plane is shown routing to and underneath the AM273 device primarily on layer 3. Due to routing limitations caused by a four layer PCB, underneath the AM273 device the 1.8 V plane is split between layers 2 and 3.

The 1.8V planes on layer 2 split up an otherwise solid ground pour on layer 2. The placement of these cutouts was chosen to minimize the impact to the signal return paths for as many GPIO pins as possible. Vias connect the plane on layers 2 and 3 to the BGA ball pads on the top layer and the decoupling capacitors on the bottom layer.

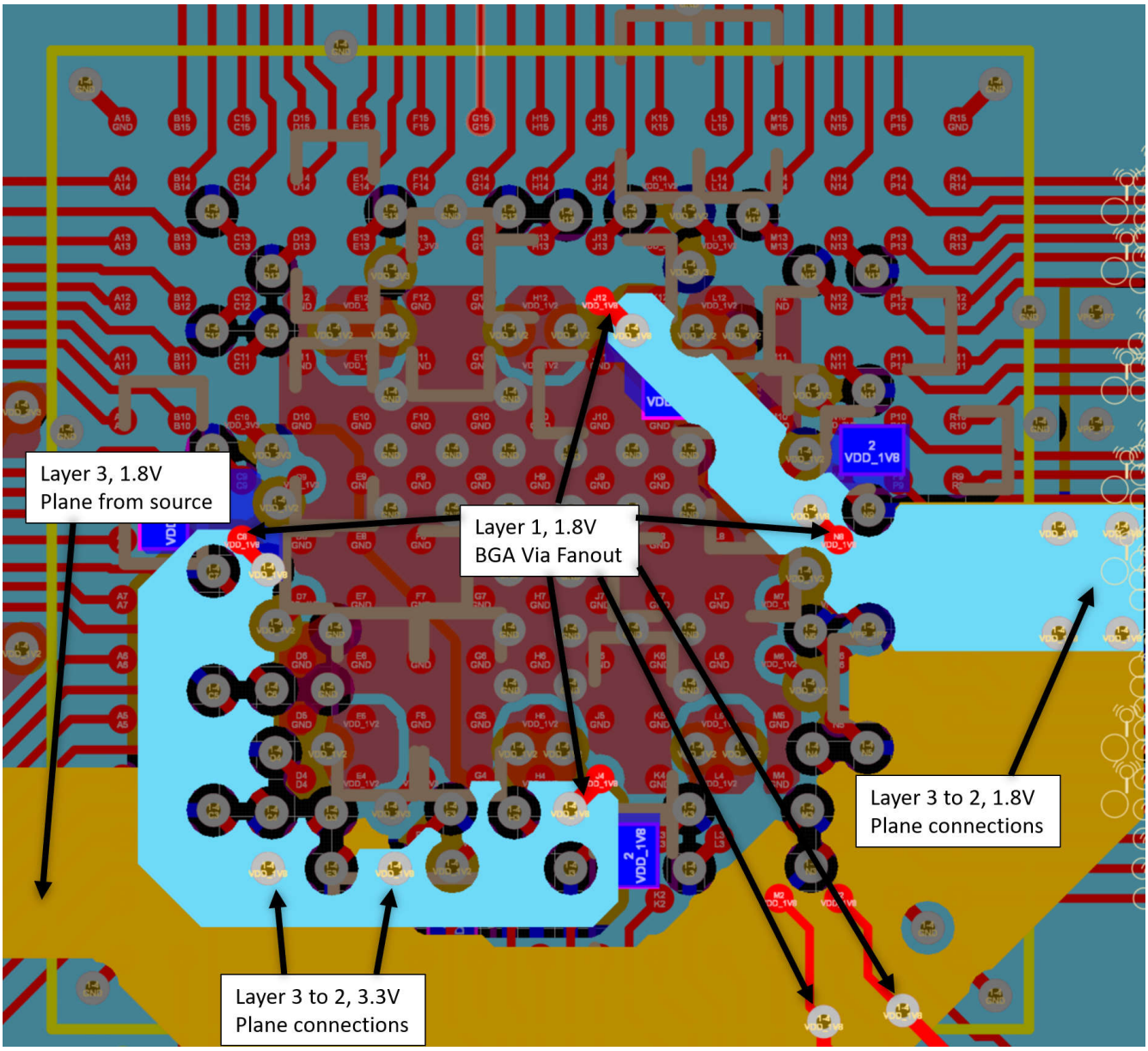

Figure 11-26. NZN 4 Layer Example Excerpt – 1.8 V Power Via Fan-Out and Plane Routing Layer 3

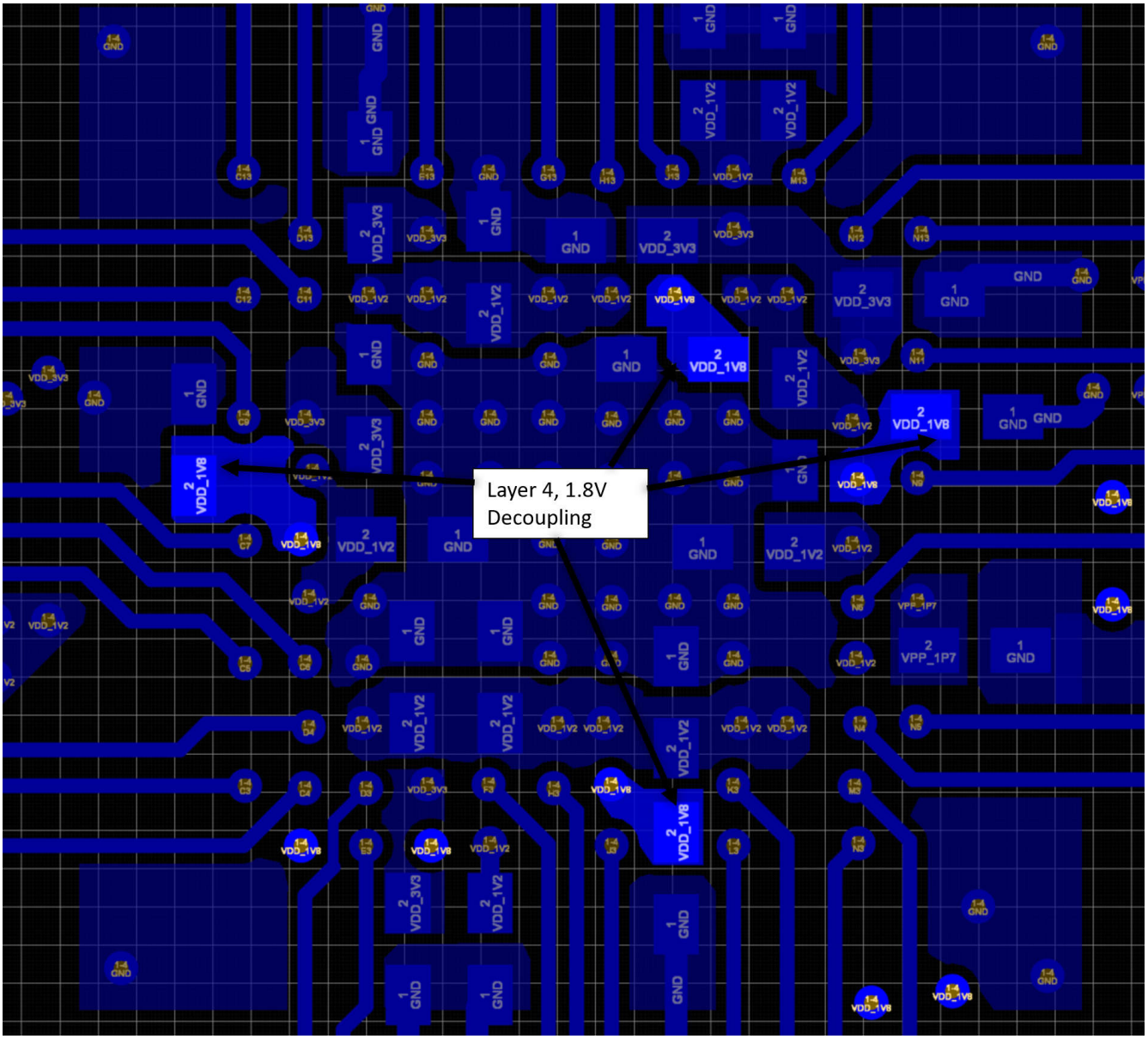

Figure 11-27. NZN 4 Layer Example Excerpt – 1.8 V Power Decoupling on Layer 4

12 References

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2. Texas Instruments: *AM273x Sitara™ Microcontroller Technical Reference Manual*
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4. Texas Instruments System Configuration Tool (SYSCONFIG): https://www.ti.com/tool/SYSCONFIG
5. MIPI Alliance Recommendation for Debug and Trace Connectors: https://www.mipi.org/sites/default/files/MIPI-Alliance-Recommendation-Debug-Trace-Connectors.pdf
6. JTAG Connectors and Pinout: https://software-dl.ti.com/ccs/esd/documents/xdsdebugprobes/emu_jtag_connectors.html
7. AM273 MCU Software Development Kit: https://www.ti.com/tool/MCU-PLUS-SDK-AM273x.

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2023) to Revision A (November 2023)	Page
• Global: Added NZN package details throughout document	3

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