

# TMS320DM6467 to TMS320DM6467T Migration Guide

DSPS Applications

## ABSTRACT

This application report describes an overview of the necessary changes to migrate a DM6467-based design from a DM6467 device (594 MHz or 729 MHz) to a DM6467T (1GHz) device. The DM6467T device requires the changes listed in this document for proper operation. Other system changes may be required to accommodate new speeds or capabilities in the system.

More information on these two devices is available from their respective TI product folders located at:

- TMS320DM6467: <http://focus.ti.com/docs/prod/folders/print/tms320dm6467.html>
- TMS320DM6467T: <http://focus.ti.com/docs/prod/folders/print/tms320dm6467t.html>

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## 1 Pin Map and Memory Map

The pin and memory maps are the same for both the DM6467 and DM6467T devices.

## 2 Feature Differences

Table 1 shows the feature differences between the DM6467 and DM6467T devices.

**Table 1. DM6467 and DM6467T Feature Differences**

	DM6467 (594MHz)	DM6467T
DSP/ARM Speed	594 MHz/297 MHz	1 GHz/500 MHz
DDR2 Speed	297 MHz	400 MHz
VPIF	99 MHz	150 MHz
PCI	33 MHz	66 MHz

### 3 Board Hardware Changes

This section describes the hardware changes needed to migrate from DM6467 to DM6467T.

#### 3.1 Minimum Required Changes

Table 2 summarizes the minimum required changes for DM6467T 1GHz operation. These changes are required in all systems, unless the current DM6467 design already meets or exceeds the new requirement.

**Table 2. Minimum Required Changes**

Component	Change To	Comments
CV <sub>DD</sub> Core Power Supply	Core power supply is changed from 1.2 V to 1.3 V for DM6467T device.  Furthermore, the power will nearly double (3-4W applications now in the 6-7W range), so the power supply design needs to account for the additional current.	DM6467T 1GHz operation has higher CV <sub>DD</sub> power demands than 594 MHz parts. Systems where the power supply was barely adequate to supply DM6467 (594-/729-MHz) parts will require larger power supplies for DM6467T (1 GHz).
DDR2	DDR2-800	
DEV_MXI Input Clock	33 MHz or 33.3 MHz oscillator or fundamental-mode crystal, e.g., CS10-33.000MABJ-UT or equivalent	<p>To achieve 1 GHz speed, input frequency above 31.25 MHz is required. (Note: Max PLL multiplier (PLLM) value is 32). The DM6467 can accept a clock up to ~55 MHz from external oscillators, but only up to 35 MHz from external crystals.</p> <p>Recommendation is to use the same crystal speed as used on the DM6467T EVM, which is 33 MHz. For more information regarding the DM6467T EVM, see <a href="http://support.spectrumdigital.com/boards/evmdm6467t">http://support.spectrumdigital.com/boards/evmdm6467t</a>.</p> <p>Other crystal speeds between 31.25 MHz and 35 MHz can be used with software changes to set appropriate PLL multiplier.</p> <p>The 27 MHz crystal can be used with the DM6467T to maintain backward compatibility with DM6467. However, with 27 MHz input clock, maximum device operating speed and DDR2 operating speed can not be achieved due to PLL multiplier limitation (maximum PLLM value is 32). The maximum frequency that can be achieved with 27 MHz input crystal is: 27 MHz * 32 = 864 MHz.</p>

#### 3.2 Probable Changes

Table 3 summarizes other changes that are likely to be required by systems of a typical design. These changes will not necessarily be required in all systems. Therefore, each of these probable changes should be evaluated to determine if they are necessary for any given design.

**Table 3. Probable Changes**

Component	Change To	Comments
Video Port Clock	External clock source: 27 MHz for SD video 74.25 MHz for HD video	<p>At 1GHz, the DM6467T can not produce standard 27, 74.25, or 148.5 MHz frequencies. In systems where the VPBE or other parts are relying on internal clock sources to generate these frequencies, a change to external clocks will be required.</p> <p>The external clock source can be an existing clock source in the design of the correct frequency, a fixed-frequency Oscillator or Crystal Clock Generator, or an external programmable PLL such as the CDCE949.</p>

**Table 3. Probable Changes (continued)**

Component	Change To	Comments
PCI-66	Pull up M66EN pin (see the DM6467T EVM schematic located at: <a href="http://support.spectrumdigital.com/boards/evmdm6467t">http://support.spectrumdigital.com/boards/evmdm6467t</a> ) Ensure other PCI components on the bus are 66 MHz capable Change to 66 MHz clock source for PCI	In systems where 66 MHz PCI operation is desired, these changes must be made. In systems not using PCI or remaining at 33 MHz PCI, these changes are not necessary.

### 3.3 Other Potentially Required Changes

Table 4 summarizes other changes that may be required in some systems. These changes will not necessarily be required in all systems. Therefore, each of these changes should be evaluated to determine if they are necessary for any given design.

**Table 4. Other Potentially Required Changes**

Component	Change To	Comments
Heat Sink	Larger capacity heat sink	Systems where the heat sink was barely adequate to cool DM6467 (594-/729-MHz) device requires larger heat sinks for the DM6467T (1 GHz) device. Note that a head sink is installed on the DM6467T EVMs (Revision C or later).

## 4 Software/Firmware Changes

This section describes software/firmware changes needed to migrate from TMSDM6467 to TMSDM6467T.

### 4.1 Software Minimum Required Changes

Table 5 summarizes the minimum required changes in software/firmware for DM6467T 1 GHz operation. These changes are required in all systems, unless the current DM6467 design already meets or exceeds the new requirement.

**Table 5. Software Minimum Required Changes**

Component	Change To	Comments
UBL	Correct PLL settings for DEV_MXI input clock	TI will supply a new UBL with the correct programming for 990 MHz DSP and 396 MHz DDR with 33 MHz input clock. Users of other frequencies need to change the PLL multiply, divide, and DDR timing parameters as appropriate.
Kernel VPIF Clock Muxing	External clock source	To use the external video port clocks provided by the hardware, the clock muxing must be set to use the external clocks. TI provides a kernel that includes this change.

### 4.2 Migration from LSP 2.00 (DM6467) to PSP 3.02 (DM6467T)

The migration details from LSP 2.00 (DM6467) to PSP 3.02 (DM6467T) are available on the wiki at:

[http://wiki.davincidsp.com/index.php/DaVinci\\_PSP\\_3.02\\_Linux\\_Installation\\_User\\_Guide#Migration\\_to\\_DaVinci\\_PSP\\_3.02](http://wiki.davincidsp.com/index.php/DaVinci_PSP_3.02_Linux_Installation_User_Guide#Migration_to_DaVinci_PSP_3.02)

### 4.3 Software Codec Migration From DM6467 to DM6467T

There are no known considerations for the software codecs when migrating from DM6467 to DM6467T.

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