Application Report
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TMS320C6747/45/43 and OMAP-L1x7 Universal Serial Bus Downstream Host Compliance Testing

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ABSTRACT

This application report describes the TMS320C6747/45/43 and OMAP-L1x7 embedded Host electrical compliance of a high-speed (HS) universal serial bus (USB) operation conforming to the USB 2.0 specification. The OTG controller supports the USB 2.0 device and host mode at high-speed (HS), full-speed (FS) and low-speed (LS).

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1 Introduction

The C6747/45/43 and OMAP-L1x7 Host high-speed electrical test of the USB is performed on a verification and debug board (VDB), which is used to validate the device feature and is not optimized for USB characterization. Better results are expected when using test boards that are optimized for characterization purposes. These optimized boards follow the board design guidelines as recommended by the USB-IF.

The USB functional block diagram is shown in Figure 1.

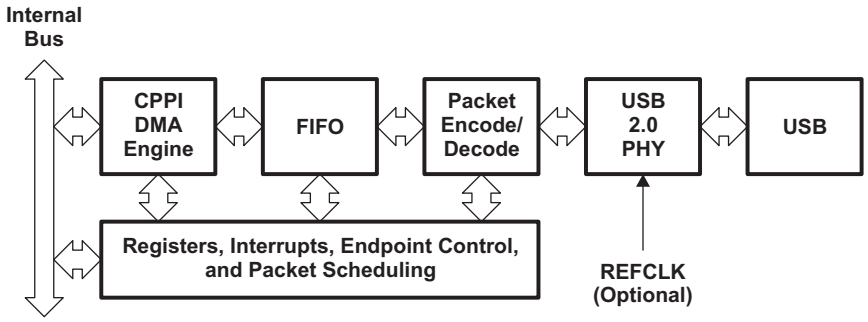

Figure 1. USB Functional Block Diagram

2 Test Items

Table 1 shows a summary of the test listings results of the compliance tests performed to evaluate the USB controller operation while operating in Host mode.

Table 1. Host Electrical Tests Result Summary

Test#	Test Items	Result
USB_EL_2	HS Host transmitter data rate 480 Mb/s ± 0.05%	PASS
USB_EL_3	HS Host signal quality test measured at the near end	PASS
USB_EL_6	10% to 90% differential rise and fall time > 500 ps	PASS
USB_EL_7	Monotonic data transitions over the vertical openings in the appropriate EYE pattern template	PASS
USB_EL_21	SYNC field (packet originating from Host)	PASS
USB_EL_22	Inter-packet gap field (device and Host)	PASS
USB_EL_23	Inter-packet gap field (back-to-back Host)	PASS
USB_EL_25	EOP field (non-SOF packets)	PASS
USB_EL_55	EOP field (SOF packets)	PASS
USB_EL_33	Chirp response time	PASS
USB_EL_29	Chirp-K and chirp-J duration	PASS
USB_EL_31	Time between SOF and last chirp-(JorK)	PASS
USB_EL_39	Host suspend capability/timing	PASS
USB_EL_41	Host resume capability/timing	PASS
USB_EL_8	Test J/K (controller transmits continuous J)	PASS
USB_EL_8	Test K (controller transmits continuous K)	PASS
USB_EL_9	Test_SE0 (controller does not drive data lines)	PASS
---------	Legacy compliance (full-speed signal quality)	PASS
---------	Legacy compliance (low-speed signal quality)	PASS

The tests are classified into six categories (see Table 2). These categories correspond to the electrical test in the USB2.0 compliance test.

Table 2. Test Categories

Test Items	Categories
HS Host transmitter data rate 480 Mb/s ± 0.05%	HS downstream signal quality test
HS Host signal quality test measured at the near end	
10% to 90% differential rise and fall time > 500ps	
Monotonic data transitions over the vertical openings in the appropriate EYE pattern template	
SYNC field (packet originating from Host)	Host packet parameters
Inter-packet gap field (device and Host)	
Inter-packet gap field (back-to-back Host)	
EOP field (non-SOF packets)	
EOP field (SOF packets)	
Chirp response time	Host chirp timing
Chirp-K and chirp-J duration	
Time between SOF and last chirp-(JorK)	
Host suspend capability/timing	Host suspend/resume timing
Host resume capability/timing	
Test J (controller transmits continuous J)	Host test_J/K/SE0
Test K (controller transmits continuous K)	
Test_SE0 (Host stops driving data lines)	

Table 2. Test Categories (continued)

Test Items	Categories
Full-speed signal quality	Legacy USB compliance testing
Low-speed signal quality	

3 Required Instruments

This section discusses the required instruments used for performing compliance tests. USB characterization tests are performed using test fixtures produced by Tektronix®.

Note: It is recommended that you use a scope with a 2 GHz bandwidth for performing the tests. This will not allow noise magnification to disturb the test. The DSA71604 is a very fast scope with a maximum operating bandwidth of 16 GHz. Even though the bandwidth needed is user selectable, during the time this test was performed, the TDSUSB2 software re-configures the user set bandwidth to the default 16 GHz speed configuration, disrupting the user settings. This is more important when performing low-speed signal quality testing since the test result captures differ heavily with a low bandwidth configuration yielding a much better result.

The high-speed electrical test (HSET) is not applicable for use with this solution since it requires an EHCI USB controller with Windows® XP/2000 running on the device. The C6747/45/43 and OMAP-L1x7 USB controller is not an EHCI controller, nor is it not running the required operating system (O/S). For this reason, you are required to create a similar application to the HSET utility furnished by the USB-IF. This utility should put the USB controller into the required test modes or configure the USB controller to perform transfers to create the right test conditions applicable for the test. The method used to invoke these tests is a Host test program running under Code Composer Studio™ software with test options controlled by variables where you select the desired test by modifying the variables within the watch window.

Table 3. Required Instruments

Type	Manufacturer	Product	Use
Oscilloscope	Tektronix	DSA71604	To measure USB signals
Differential probe (1)	Tektronix	P7313	Signal quality/receiver sensitivity tests
Single ended FET probe (2)	Tektronix	P6243	Packet parameters/Chirp timings
Measurement application (USB test software that is part of the scope application)	Tektronix	TDSUSB	USB compliance test software specifically used for USB
Test fixture	Tektronix	TDSUSBF	For USB test
Power Supply	Agilent	E3633A	5 V power supply for TDSUSBF
Digital multimeter	Fluke	Fluke 45 Series	Actual voltage monitor
Test board (VDB) (1)	TI	EVM like board	Non-optimized test board used for C6747/45/43 and OMAP-L1x7 device validation
Four self powered USB certified high-speed hubs	Digitus	Hub Twister	For full-speed signal quality testing
One self powered USB certified full-speed hub	ABB	-	For full-speed signal quality testing
One known good USB 2.0 certified compliant device	-	-	For high-speed testing
One known good USB 1.1 certified complaint device	-	-	For full-speed signal quality testing
One USB mouse	-	-	For low-speed signal quality test
Six 5 meter USB cables	-	-	For full-speed signal quality testing

(1) Results could change for the better if using an optimized test board.

4 Test Condition

4.1 Power Supply Voltage/Temperature

Table 4 shows the power supply voltage and temperature conditions:

Table 4. Power Supply Voltage and Temperature Condition

Parameter	Min	Typ	Max	Unit
USB_VDDA1P2LDO	1.14	1.2	1.26	V
USB_VDDA3P3	3.1	3.3	3.5	V
Operating Temperature	-10	25	95	°C

4.2 HS Downstream Signal Quality Test

The HS downstream signal quality test uses the *TEST_PACKET* to place the C6747/45/43 and OMAP-L1x7 USB controller in a test mode where the controller continuously transmits a fixed defined format test packet, which is defined in the USB 2.0 specification, Section 7.1.20. Even though there are many ways to achieve this task, the method used here is for the C6747/45/43 and OMAP-L1x7 to enumerate a known good device (a HS USB Flash drive); at the end of enumeration, you will force the device to go into TEST_PACKET test mode via the Code Composer Studio watch window. When this test mode is entered, the device continually transmits the data packet shown in Table 5.

The oscilloscope, along the embedded TDSUSB2 software, automatically analyzes the test packet signal quality as observed on the USB bus. For detailed procedures on how to configure the scope as well as the TDSUSB2 software, see the *Host High-Speed Electrical Test Procedure* documentation issued by the USB Implementers Forum (http://www.usb.org/home).

Table 5. Test Packet Data

Data Used for Generating Test Packet	00 00 00 00 00 00 00 00 00 AA AA AA AA AA AA AA AA EE EE EE EE EE EE EE EE FE FF FF FF FF FF FF FF FF FF FF FF 7F BF DF EF F7 FB FD FC 7E BF DF EF F7 FB FD 7E

Figure 2 displays the equipment setup for high-speed downstream signal quality test.

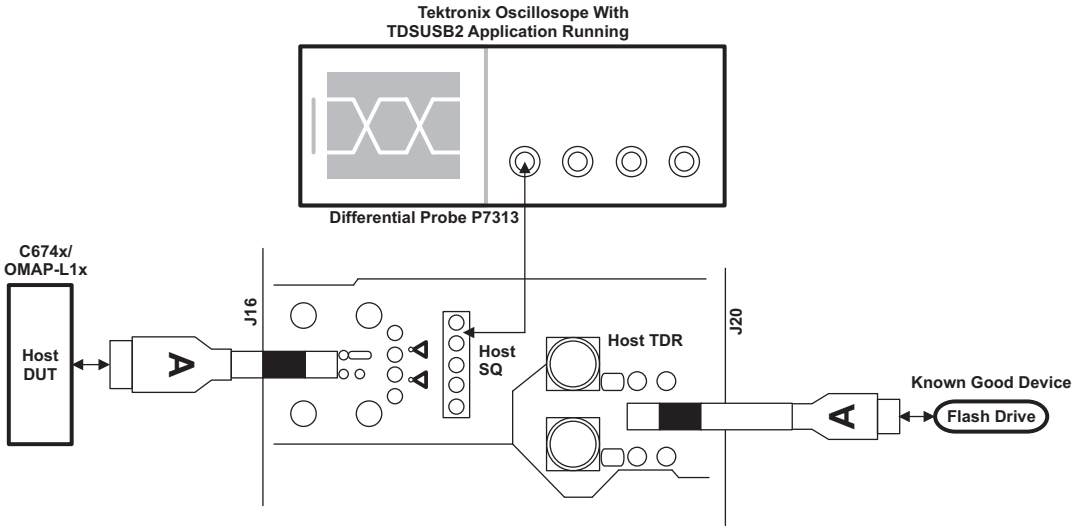

Figure 2. Equipment Setup for High-Speed Downstream Host Signal Quality Testing

4.2.1 EL_2: Signal Rate

A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ± 0.05%.

4.2.2 EL_3: Signal Quality/Eye Diagram Test

An eye diagram provides an intuitive view of jitter. It is a composite view of all the bit periods of a captured waveform superimposed upon each other. The USB 2.0 downstream port on a device, without a captive cable, must meet template 1 transform waveform requirements measured at a test point close to the port.

4.2.3 EL_6: Rise and Fall Time

A USB 2.0 high-speed driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

4.2.4 EL_7: Monotonic Data Transitions

A USB 2.0 driver must have monotonic data transitions over the vertical openings specified in the appropriate EYE pattern template. These results were based on USB-IF/waiver limits.

Table 6. Overall Results of Signal Quality Test (1)

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Pop.	Status
Eye diagram test	-	-	-	-	-	-	-	Pass
Signal rate	466.8138 Mbps	491.4934 Mbps	479.9683 Mbps	0.0000 bps	3.617680 Mbps	479.8033 Mbps	512	Pass
EOP width	-	-	16.69989 ns	-	-	-	1	Pass
EOP width (bits)	-	-	8.015420	-	-	-	1	Pass
Falling Edge Rate	805.5946 V/µs	1.011578 kV/µs	896.8093 V/µs	205.9832 V/µs	43.64434 V/µs	897.8607 V/µs	107	Pass
Rising Edge Rate	814.0531 V/µs	995.6332 V/µs	906.6210 V/µs	181.5801 V/µs	43.34522 V/µs	907.6470 V/µs	108	Pass

(1) Additional Information:

- Consecutive jitter range: -86.47 ps to 63.38 ps RMS jitter 24.85 ps
- KJ paired jitter range: - 88.62 ps to 70.38 ps RMS jitter 25.57 ps
- JK paired jitter range: -48.34 ps to 76.55 ps RMS jitter 22.73 ps

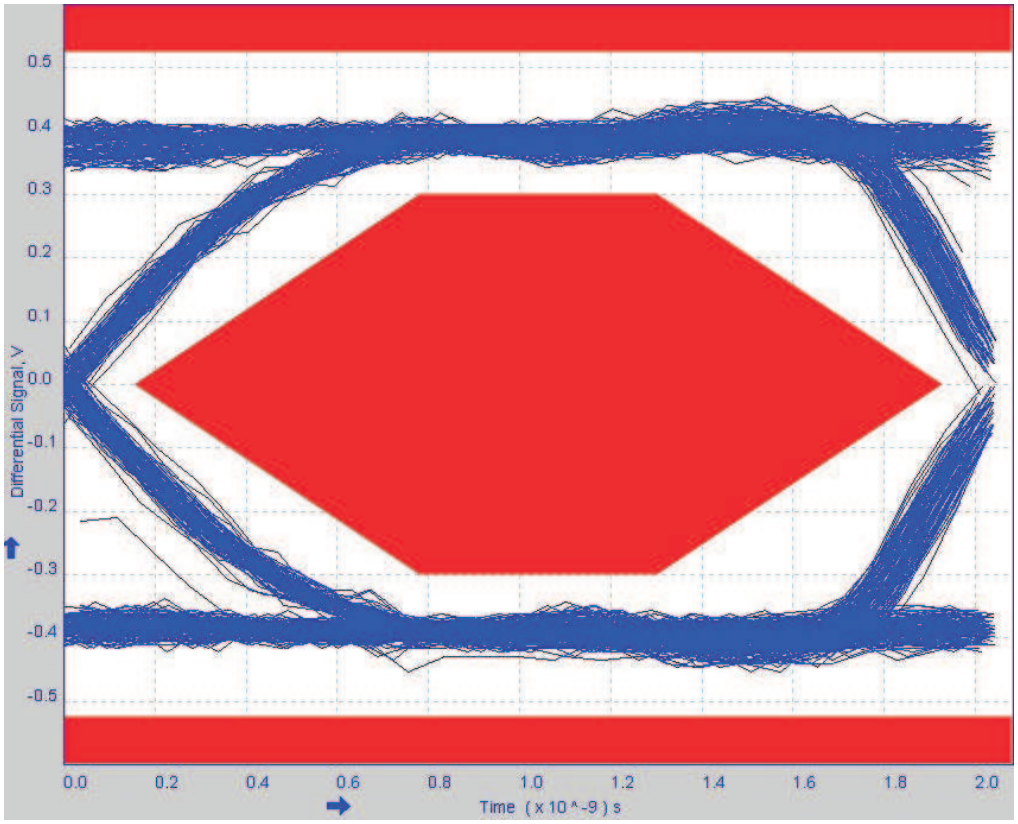

Figure 3. Downstream Eye Diagram

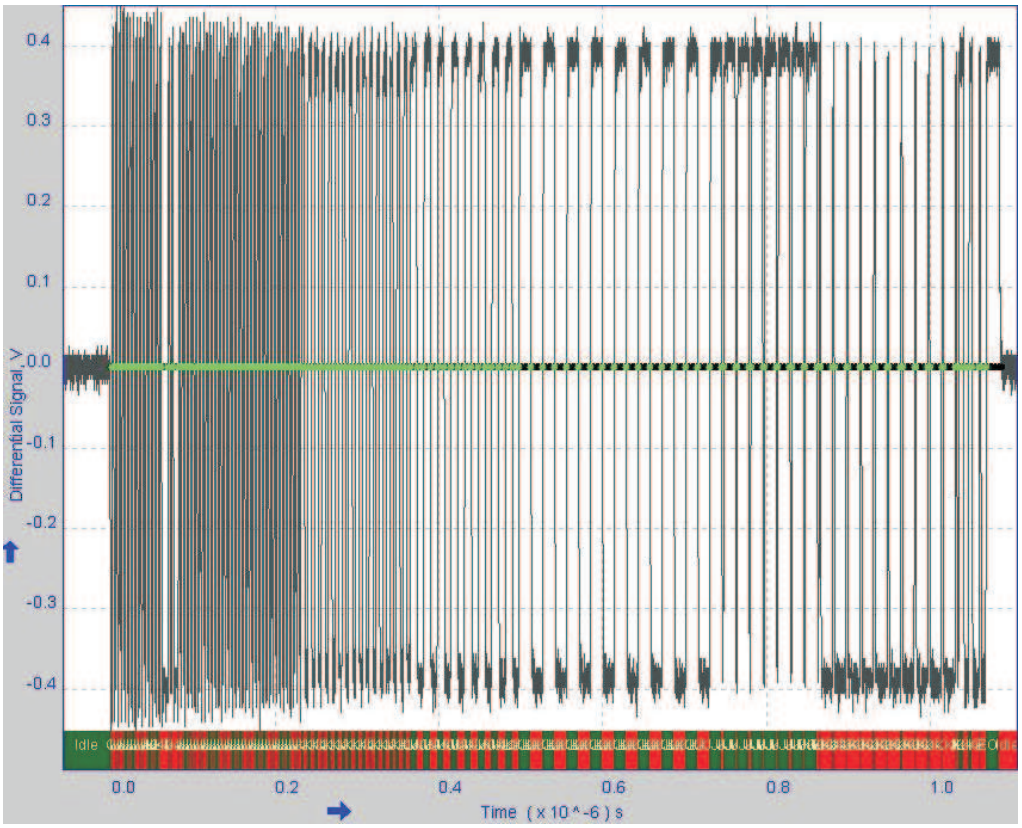

Figure 4. Downstream Waveform Plot

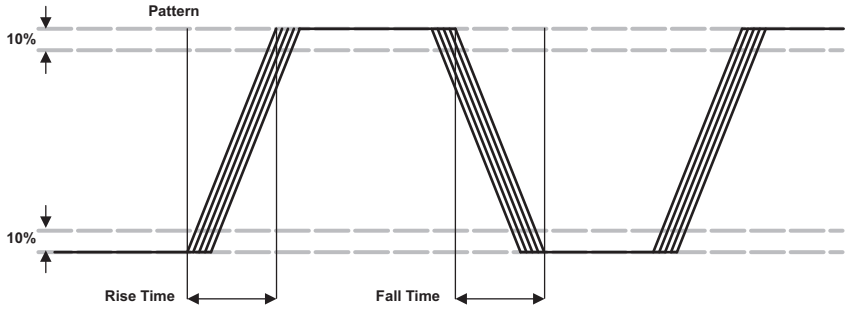

Figure 5. Rise and Fall Time Patterns

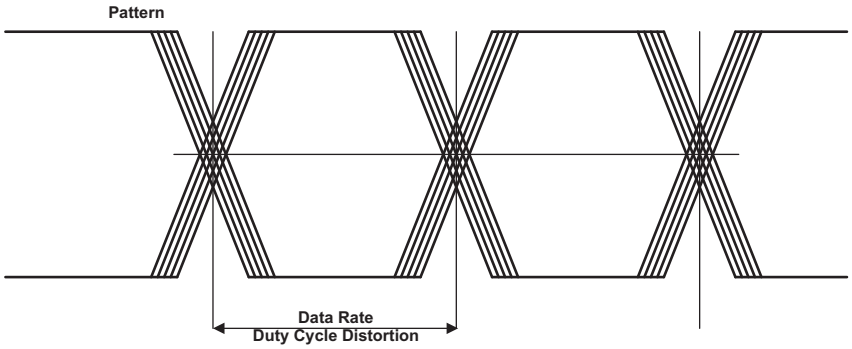

Figure 6. Duty Cycle Distortion (DCD)

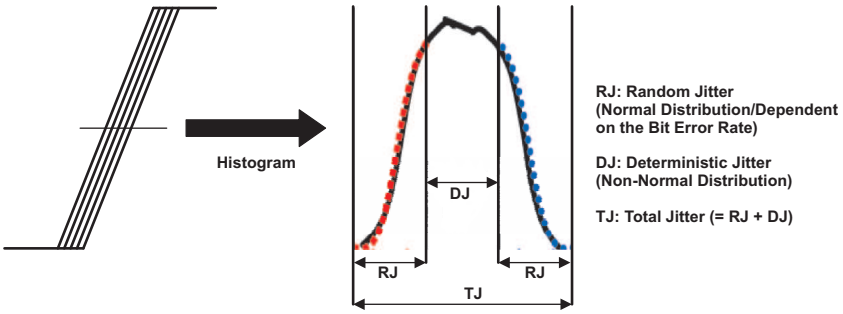

Figure 7. Random Jitter/Deterministic Jitter/Total Jitter

4.3 Host Packet Parameters

The Host packet parameter tests are comprised of a set of tests that pertains to the fields/elements of USB packets. Unlike the signal quality test, the Host controller does not need to enter into a test mode. A single step GET DEVICE DESCRIPTOR control transfer is invoked from the C6747/45/43 and OMAP-L1x7 DUT Host by pausing in between transactions to an attached known good high-speed device (Flash drive was used on this setup). The downstream host high-speed packet parameter test requires the use of the three stages of the GET DEVICE DESCRIPTOR command: setup, data, and status. The C6747/45/43 and OMAP-L1x7 DUT Host invokes the setup stage of the transaction and pauses until it is told to continue. For a GET DEVICE DESCRIPTOR command, it would be good to measure the Host packet parameters tests from either the setup stage or the status stage of the transaction since both of these stages comprises of the token and data packets originating from the Host. The packet delimiter fields, SYNC, EOP fields, and inter-packet delay are measured from either the setup stage or the status stage of the transaction.

Figure 8 displays the equipment setup for the high-speed downstream Host packet parameter tests.

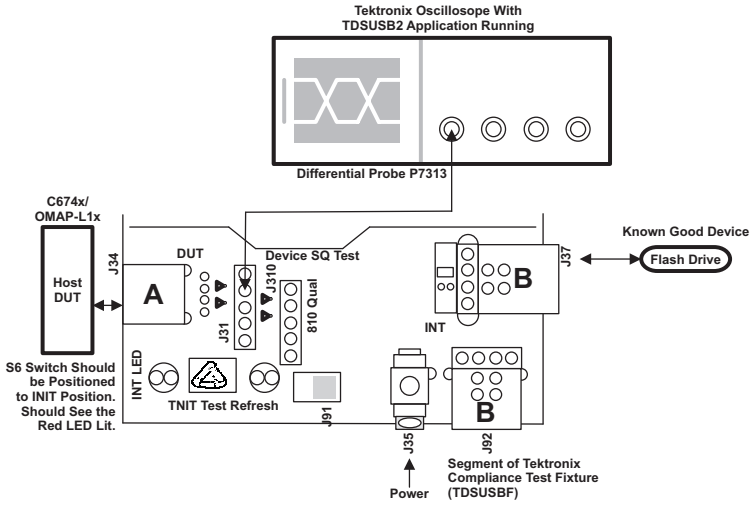

Figure 8. Equipment Setup for Downstream Host Packet Parameters Tests

4.3.1 EL_21: Synchronization (SYNC) Field

The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Figure 9 displays the status stage of the GET DESCRIPTOR command with the SYNC field of the token packet zoomed.

Handshake packet SYNC field: PASS

Note: Measured value: 66.0 ns => 66.0 ns x 480 Mbps = 31.68 bits.

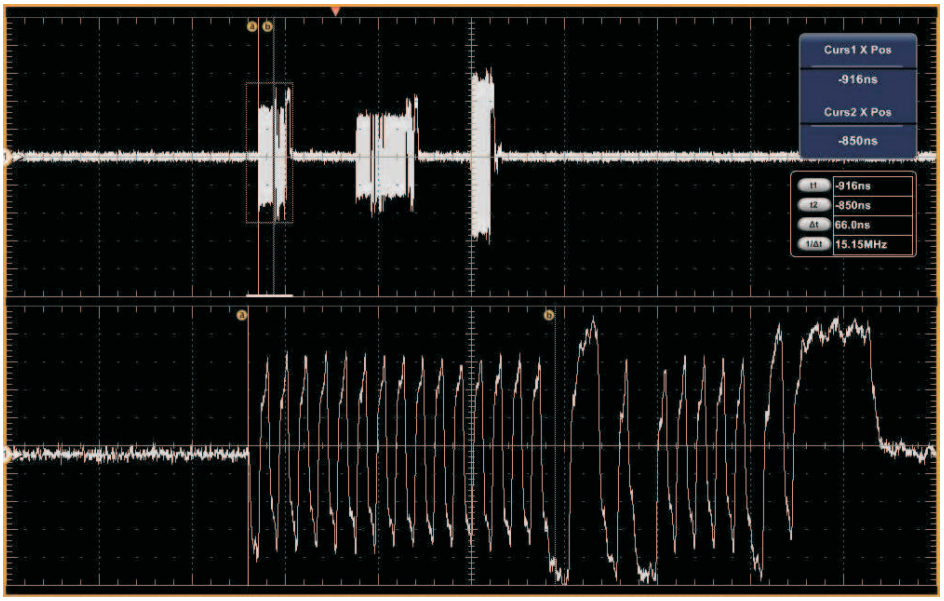

Figure 9. Status Stage of a GET DEVICE DESCRIPTOR Transaction SYNC Field of the Token Packet

4.3.2 EL_22: Inter-Packet-Gap Field of Device and Host Packets

When transmitting after receiving a packet, hosts and devices must provide an inter-packet-gap of at least 8-bit times and not more than 192-bit times.

To test this parameter, it is important to use a transaction that forces the C6747/45/43 and OMAP-L1x7 Host to source a packet in response to a reception of a packet from the known good device. The data stage of the GET DESCRIPTOR command is ideal transaction to measure the inter-packet-gap existing between the device responding with its descriptor data and the DUT Host acknowledging the reception by testing the gap time honored by the DUT Host C6747/45/43 and OMAP-L1x7 device.

Figure 10 displays the inter-packet-gap observed between the device and embedded Host packets.

Packet gap between device data packet and Host acknowledge packet: PASS

Note: Measured value: 227.2 ns => 227.2 ns x80 Mbps = 109.056 bits.

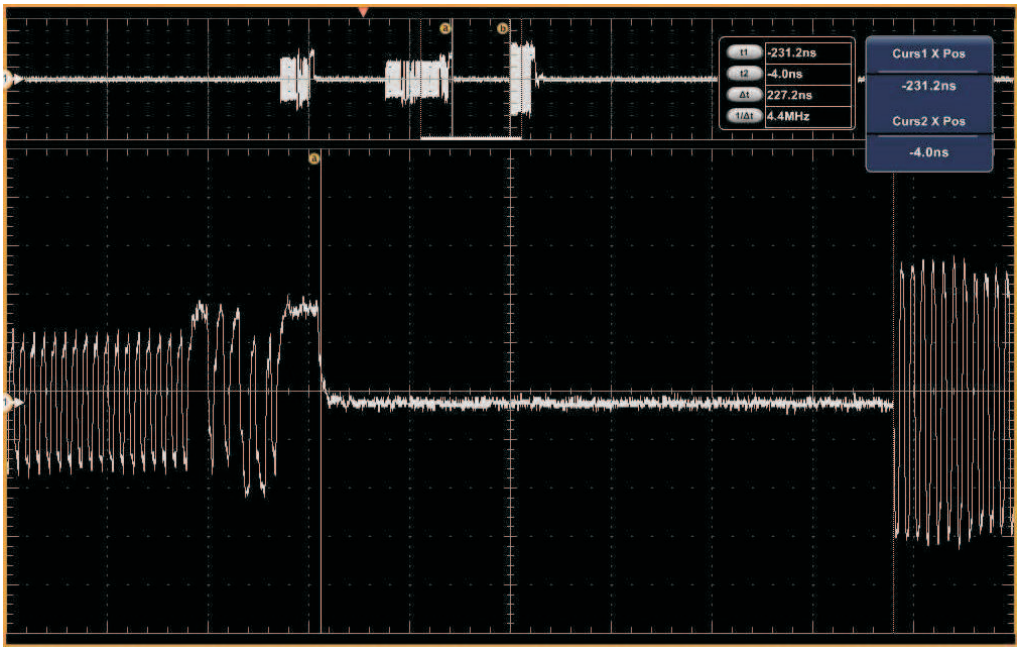

Figure 10. Inter-Packet-Gap Between the Data Packet of Device and Acknowledge Packet of the Embedded Host on the Data Stage of the GET DESCRIPTOR Command

4.3.3 EL_23: Inter-Packet-Gap Field of Back-to-Back Packets

The Host transmitting two packets in a row must have an inter-packet-gap of at least 8-bit times and not more than 192-bit times.

Figure 11 displays the inter-packet-gap between the token packet and the zero byte data packet of the status stage of a GET DESCRIPTOR command sourced from the DUT Host with the inter-packet-gap zoomed.

Packet gap between the Host token packet and the Host data packet: PASS

Note: Measured value: 281.6 ns => 281.6 ns x 480 Mbps = 135.168 bits.

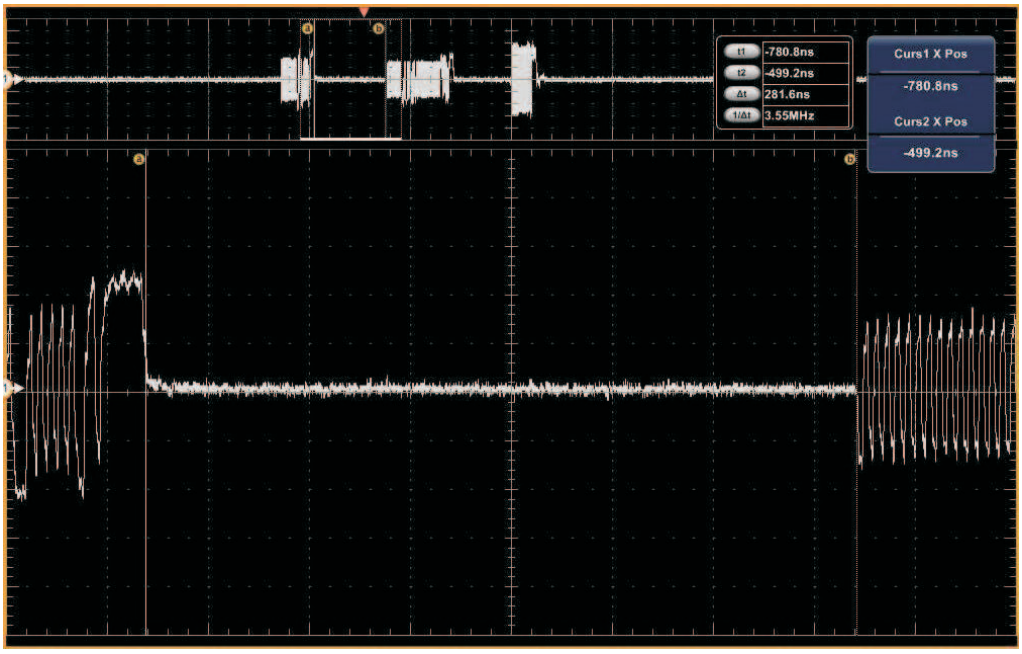

Figure 11. Inter-Packet-Gap Between the Token Packet and the Data Packet of the Status Stage of the GET DESCRIPTOR Transaction

4.3.4 EL_25: End-of-Packet (EOP) Field of Non-SOF Packets

The EOP for all transmitted packets (except SOF) must be an 8-bit NRZI byte of 01111111 without bit stuffing. Note, that a longer EOP is waiverable.

The EOP of the token packet or the data packet of the status stage can be used to verify this timing since both of these packets are sourced by the DUT C6747/45/43 and OMAP-L1x7 Host during the status stage of a GET DESCRIPTOR command. Figure 12 displays the EOP field of the data packet of the status stage of the GET DESCRIPTOR command.

Non-SOP EOP field: PASS.

Note: Measured value: 16.6 ns => 16.6 ns x 480 Mbps = 7.968 bits.

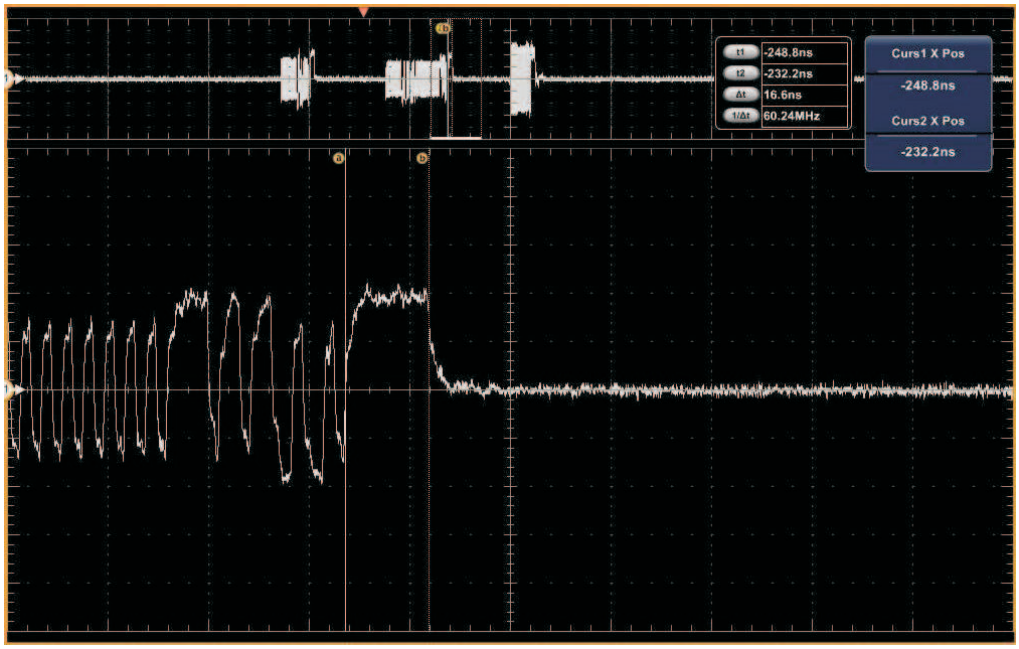

Figure 12. EOP Field of Non-SOP Packet of the Data Packet of the Status Stage of the GET DESCRIPTOR Command

4.3.5 EL_55: End-of-Packet (EOP) Field of SOF Packets

The Host transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol. Figure 13 displays the EOP field capture of a SOF packet.

SOF packet EOP Field: PASS.

Note: Measured value: 83.2 ns => 83.2 ns x 480 Mbps = 39.936 bits

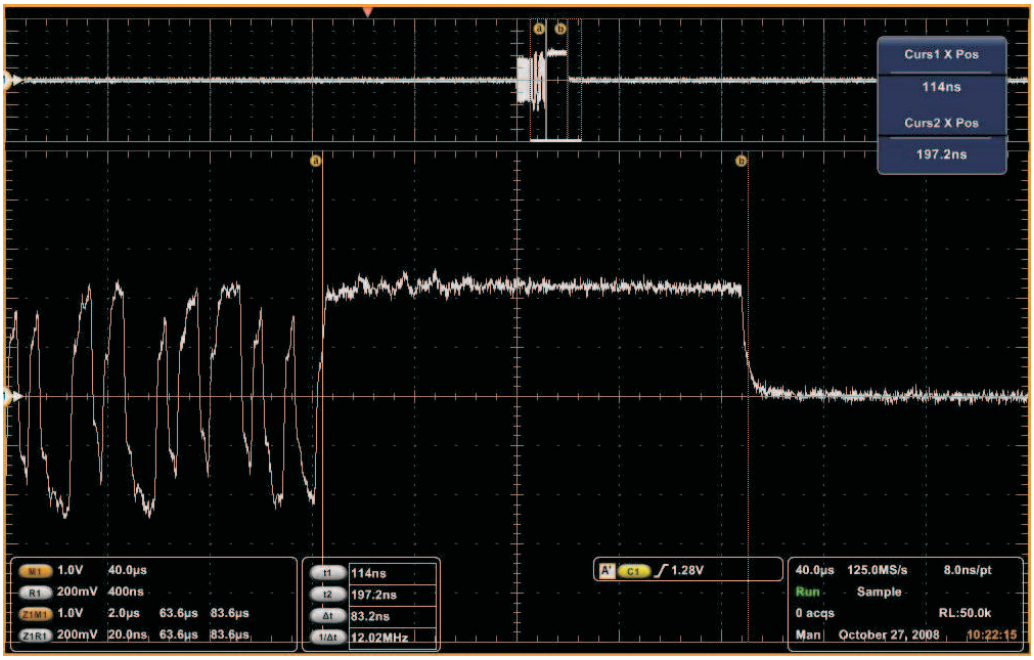

Figure 13. EOP Field of an SOP Packet

4.4 Device Chirp Timing

The Host chirp timing is used to validate high-speed detection handshake and happens during reset time. Some time after the Host resets a high-speed device, the device should indicate its high-speed capability by generating chirp-K signaling. A high-speed Host follows up by generating a minimum of three sets of chirp-KJ signaling at full-speed signaling environment. The device should disconnect its 1.5KΩ pull-up resistor and enable the 45 Ω termination resistors right after the last chirp J from the Host.

To invoke this test, a similar setup used for the device parameter testing, with two single ended FET probes replacing the differential probe, is used and shown on Figure 14.

There are several ways to perform this test. The method used here is to perform the test during an initial attachment. However, the embedded Host test software can be programmed to perform a RESET.

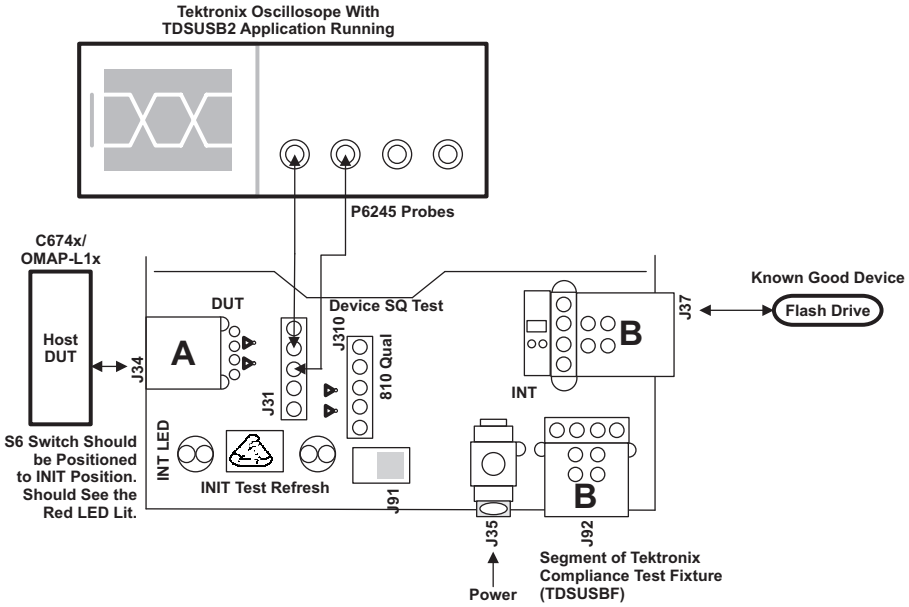

Figure 14. Equipment Setup for Downstream Host Chirp and Suspend and Resume Timings

4.4.1 EL_33: Chirp Response Timing

Downstream ports start sending and alternating a sequence of chirp K's and chirp J's within 100 µs after the device chirp K stops. Should be <= 100 µs.

The device chirp K stop time is usually detected when the signal level of the chirp K drops around = its high value.

Chirp response timing is the time between the device's de-assertion of chirp-K and the start of the alternate chirp-K and chirp-J sent by the Host.

Figure 15 displays the chirp response time measured for a downstream C6747/45/43 and OMAP-L1x7 Host device.

Chirp response time: PASS

Note: Measured value: 2.5 µs

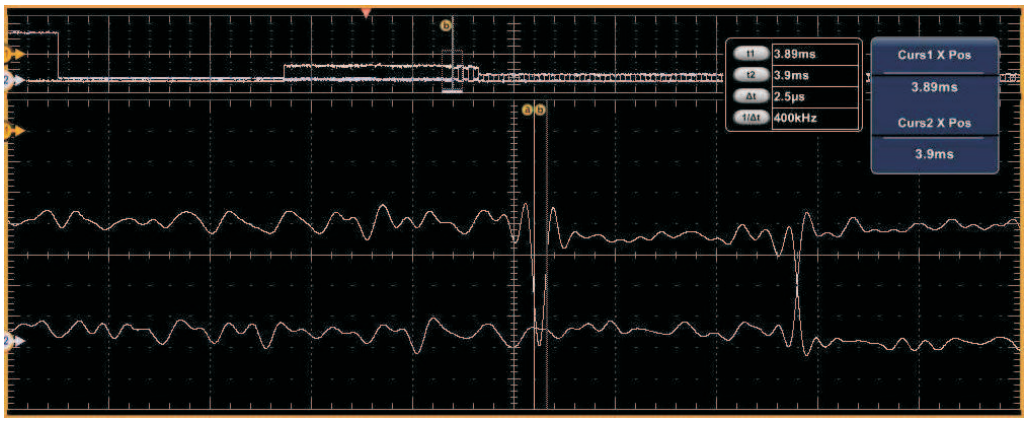

Figure 15. Downstream Chirp Response Time

4.4.2 EL_34: Chirp-K and Chirp-J Duration

Downstream ports start sending and alternating a sequence of chirp K's and chirp J's within 100 µs after the device chirp K stops.

Chirp-K and chirp-J duration must be between 40 µs and 60 µs.

Figure 16 displays chirp-K and chirp-J duration measured for the C6747/45/43 and OMAP-L1x7 Host DUT device.

Chirp-K and chirp-J duration: PASS.

Note: Measured value: 49.04631 µs and 50.98778 µs

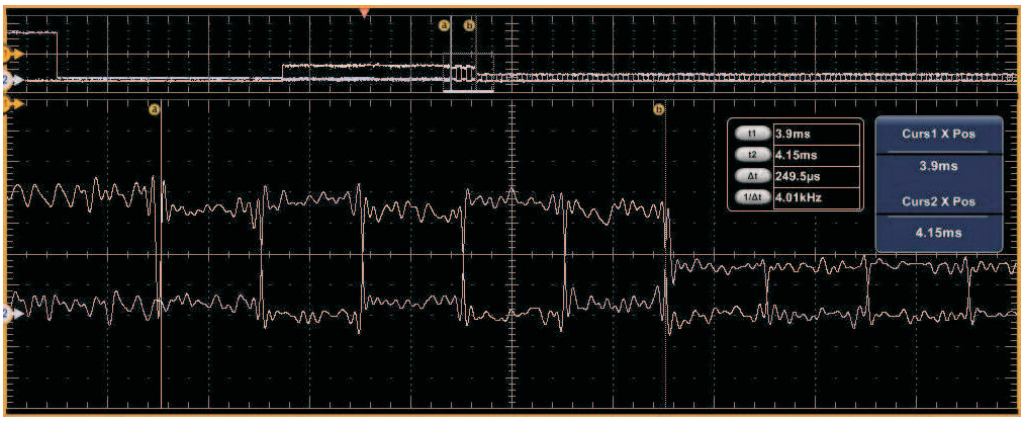

Figure 16. Chirp-K and Chirp-J Duration

4.4.3 EL_35: Time Between SOF and Last Chirp-(J or K)

The downstream C6747/45/43 and OMAP-L1x7 DUT Host should begin sending SOFs within 500 µs and not sooner than 100 µs from the transmission of the last chirp-(J or K).

Figure 17 displays the captured time for this event.

Time between SOF and the last chirp-(J or K): PASS

Note: Measured value: 100.06 µs.

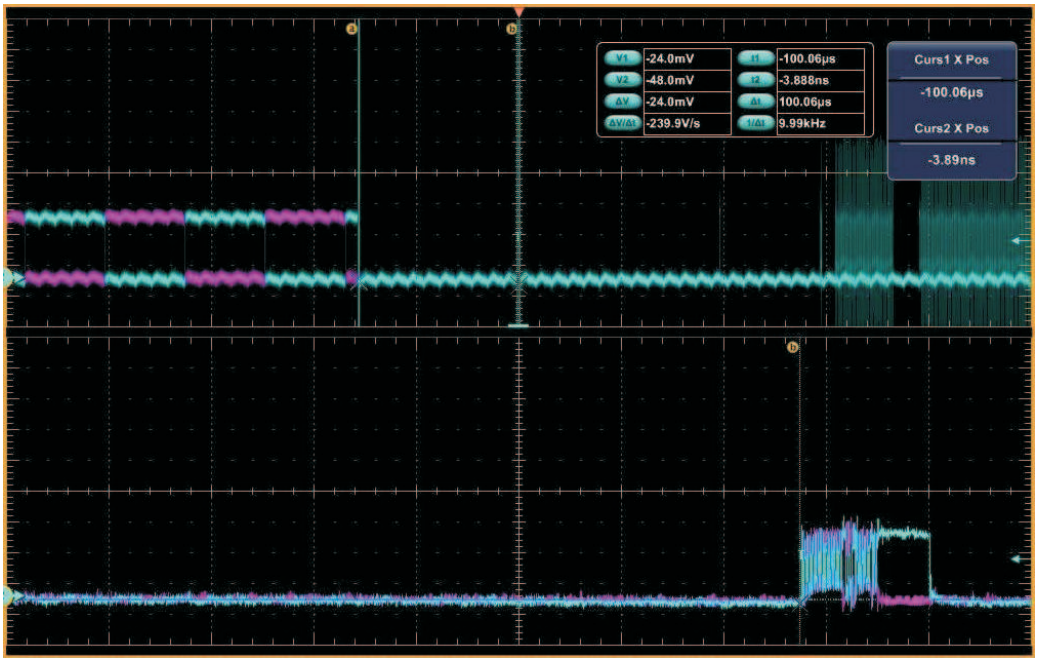

Figure 17. Time Between First SOF and Last Chirp-(J or K)

4.5 Host Suspend/Resume Timing

The embedded Host is attached to a known good high-speed device (Flash drive) and finishes up the enumeration process. The DUT Host does no transaction, but periodically generates a SOF packet to the attached high-speed device every 125 µs.

The Host DUT is forced to transition to suspend state via the firmware when needed. The results are that the C6747/45/43 and OMAP-L1x7 Host DUT stops generating SOF packets.

To exit suspend mode and start the resume process, the DUT Host firmware does the following:

1. Clears the suspend bit
2. Sets the resume bit
3. Leaves the resume bit set for around 20 ms
4. Clears the resume bit

This will end the resume state.

Figure 14 displays the equipment setup for the suspend and resume tests.

4.5.1 EL_39: Host Suspend Timing

This is the time interval from the end of the last SOF packet issued by the DUT host to when the device attached its full-speed pull-up resistor on D+ (transition to full-speed J-state). This time should be between 3.0 ms and 3.125 ms. No measurement is required as this sequence verifies that the Host supports the suspend state.

The embedded Host is attached to a known good high-speed device (Flash drive) and finishes up the enumeration process. The DUT Host does no transaction, but periodically generates a SOF packet to the attached high-speed device every 125 μs. The Host DUT is then forced to transition to suspend state via the Firmware. The results are that the C6747/45/43 and OMAP-L1x7 Host DUT stops generating SOF packets.

Figure 18 captures the signal capture of SOF from DUT Host vanishing when it enters into suspend mode along with the automatic result published by the TDSUSB2 software.

DUT Host support suspend capability: PASS

Note: Measured Value (by the TDSUSB2 S/W): 3.033085 ms.

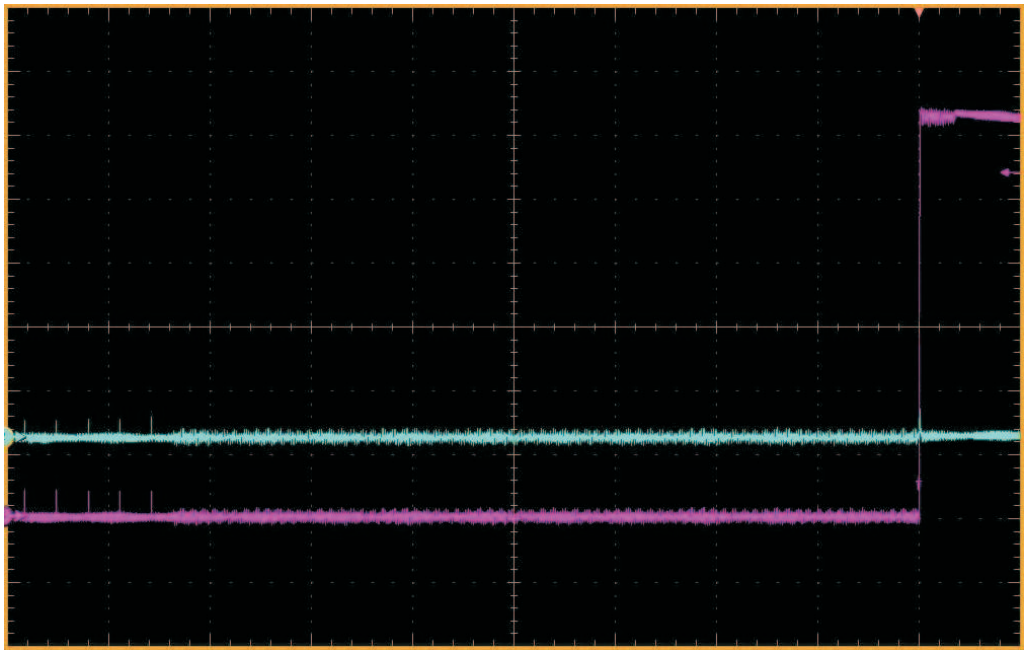

Figure 18. DUT Host Enters Suspend State

Measurement Name	Suspend Time	USB Limits	Status
Suspend Test	3.033085 ms	3.000000 ms to 3.125000 ms	Pass

4.5.2 EL_41: Host Resume Timing

After resuming a port, the Host must begin sending SOFs within 3 ms of the start of the idle state.

Figure 19 captures the resume signal capture alongside the automatic result generated by the TDSUSB2 software.

DUT Host support resume capability: PASS

Note: Measured Value: 101 µs

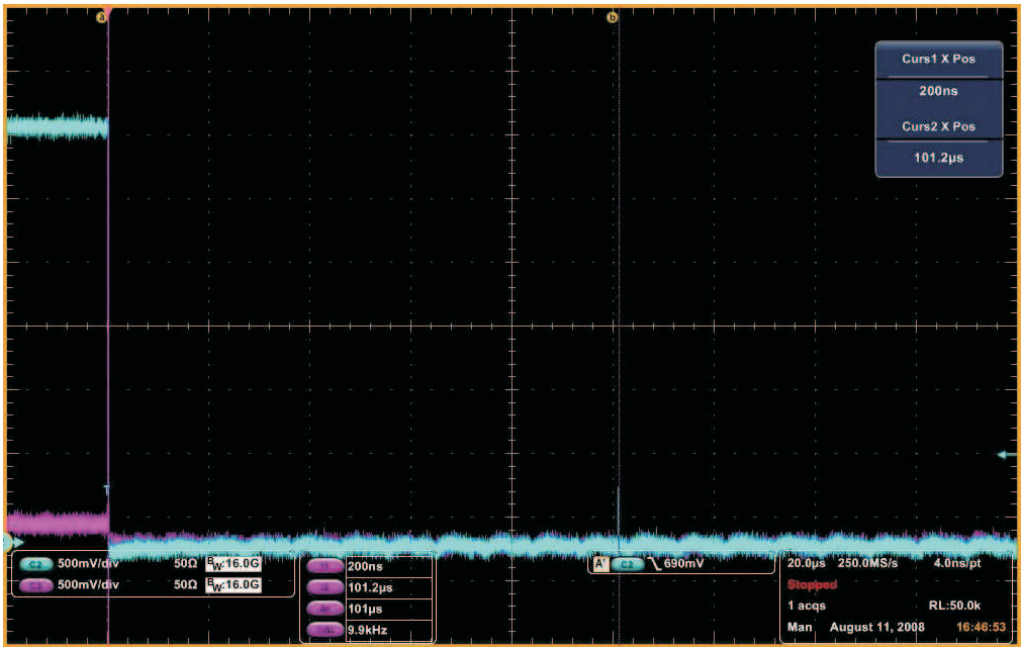

Figure 19. DUT Host Resumes

Measurement Name	Resume TIME	USB Limits	Status
Resume Test	101 µs	3.000000 ms	Pass

4.6 DUT Host Test_J/K, SE0

A USB 2.0 Specification compliant controller is required for the controller to support mandatory tests (where Test_SE0_NAK, Test_J, and Test_K are members of these tests). A digital multimeter is used to measure the DC voltage level of D+ and D- data lines after placing the controller in one of the test modes mentioned.

Test_SE0 places the controller in high-speed mode and keeps the controller from driving both D+ and D- data lines.

Figure 20 displays the equipment setup used for DUT Host Test_J, Test_K, and Test_SE0

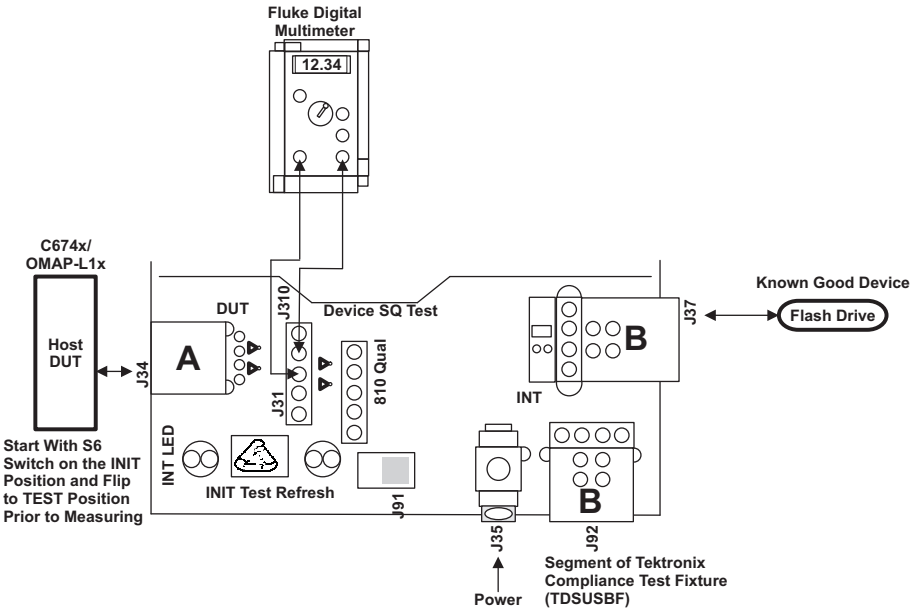

Figure 20. Equipment Setup for Downstream Test J/K, SEO_NAK

4.6.1 Test_J/ Test_K

4.6.1.1 Test_J

When the D+ is driven high, the output voltage must be 400 mV ± 10% when terminated with precision 45 Ω resistor.

D+ data line DC voltage level: PASS

Note: Measured value: 0.3964 V

D- data line DC voltage level: PASS

Note: Measured value: 0.00210 V

4.6.1.2 Test_K

When the D- is driven high, the output voltage must be 400mV ± 10% when terminated with precision 45 Ω resistor.

D- data line DC voltage level: PASS

Note: Measured value: 0.394 V

D+ data line DC voltage level: PASS

Note: Note: Measured value: 0.00162 V

4.6.2 EL_9: Test_SE0

When either D+ and D- are not being driven, the output voltage must be 0V ± 10% when terminated with precision 45 Ω resistors to ground.

D+ data line DC voltage level: PASS

Note: Measured value: 0.7 mV

D- data line DC voltage level: PASS

Note: Measured value: 0.7 mV

4.7 Legacy USB Compliance Testing

An eye diagram provides an intuitive view of jitter. It is a composite view of all the bit periods of a captured waveform superimposed upon each other. Full-speed and low-speed signal quality tests are good enough to determine that the embedded high-speed Host is capable of interacting with legacy devices that happen to be full- or low-speed in nature.

4.7.1 Full-Speed Downstream Signal Quality Test

For a full-speed downstream signal quality test, it is necessary to cascade four self-powered high-speed hubs and one self-powered full-speed hub with five meters of USB cables. The TDSUSB2F fixture is connected to the embedded Host with a known good five meter USB cable. The self-powered full-speed hub is directly attached (without using a short cable) to the TDSUSB2F fixture on the opposite side at the Tier 1 position. The remaining high-speed hubs are cascaded with five meter cables. A known good full-speed device, in this case a USB 1.1 Flash drive, is connected to the last high-speed hub via a five meter USB cable. Figure 21 displays the equipment setup for a full-speed downstream signal quality test.

To capture the signal quality test, it is necessary to enumerate the attached USB 1.1 device. Since the embedded Host is configured to operate at full-speed after the completion of the enumeration process, it will generate a start of frame packet at the start of every frame. This packet is good enough to perform the full-speed signal quality test.

Figure 21 displays the equipment setup for the full-speed downstream signal quality test.

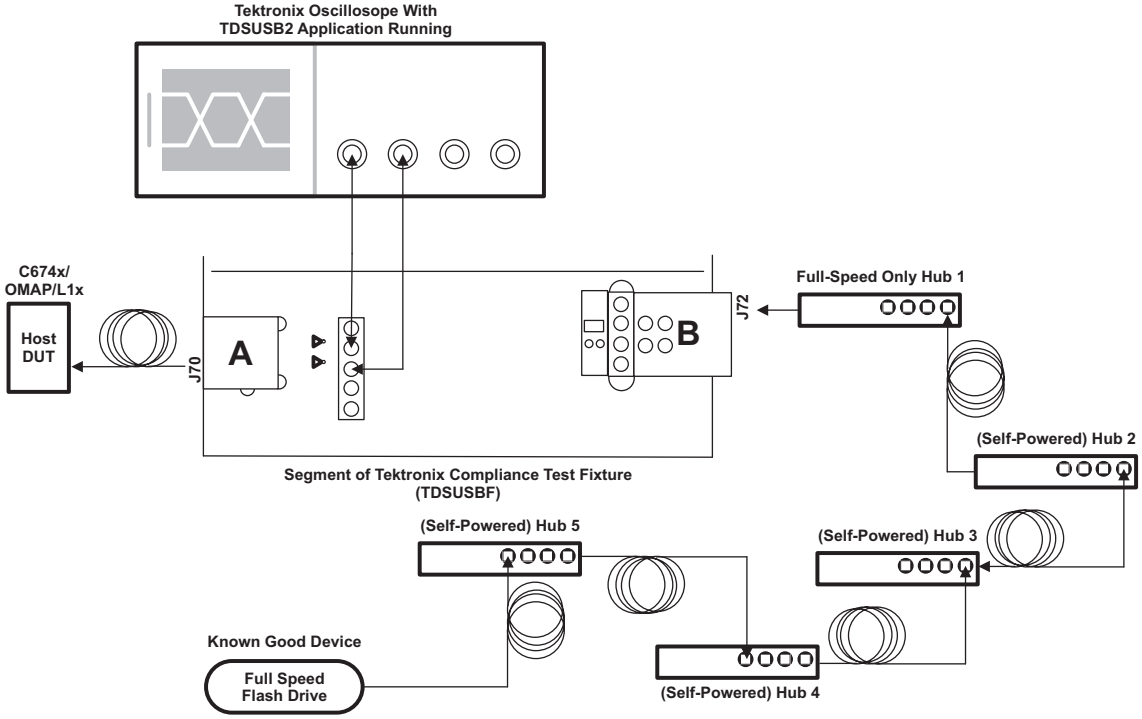

Figure 21. Equipment Setup for Full-Speed Downstream Host Signal Quality Testing

Figure 22 displays the full-speed waveform plot as it is captured by the TDSUSB2F software.

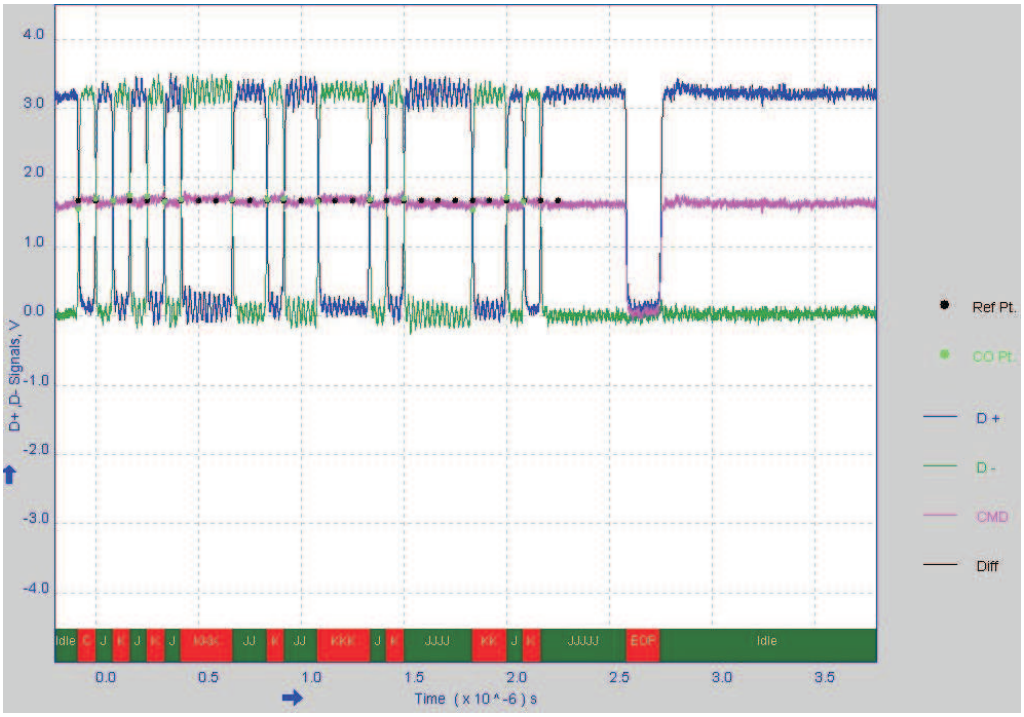

Figure 22. Waveform Plot

Figure 23 displays the eye diagram for the full-speed downstream Host.

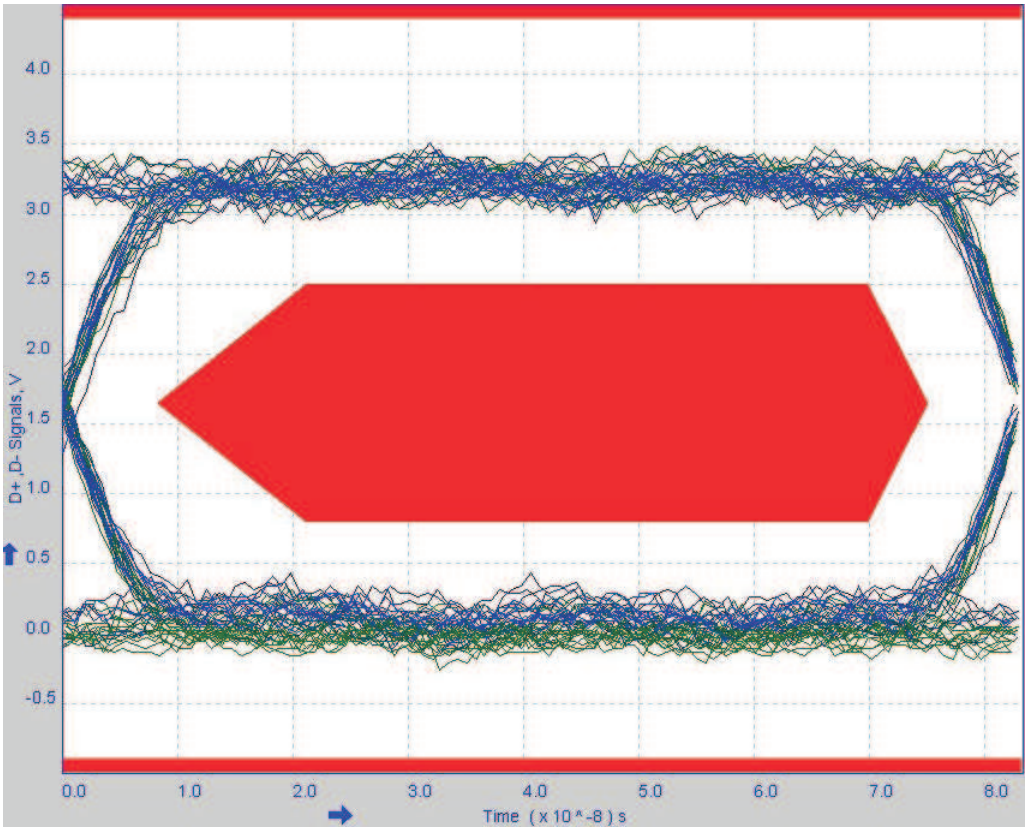

Figure 23. Full-Speed Eye Diagram

Table 7 displays the detailed result for the downstream full-speed signal quality testing.

Table 7. Result Summary for Full-Speed Downstream Host Signal Quality

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Pop.	Status (1)
Eye diagram test	-	-	-	-	-	-	-	Pass
Signal rate	11.93862 Mbps	12.07190 Mbps	12.00238 Mbps	0.0000 bps	37.58617 kbps	12.00126 Mbps	25	Pass
Crossover voltage	1.536364 V	1.737378 V	1.667468 V	201.0135 mV	56.03159 mV	1.668351 V	16	
EOP width	-	-	168.3717 ns	-	-	-	1	Pass
Consecutive jitter	-538.9500 ps	438.8717 ps	-4.371036 ps	977.8217 ps	323.1337 ps	312.2074 ps	15	Pass
Paired JK jitter	-979.7464 ps	871.7649 ps	-97.52604 ps	1.821511 ns	730.2702 ps	660.4143 ps	5	Pass
Paired KJ jitter	-829.9831 ps	359.9809 ps	-82.94101 ps	1.189964 ns	456.2189 ps	416.3986 ps	5	Pass

(1) Because the individual status of the measurements are Pass and performed on Tier 6 (as per USB-IF), the overall result for this test is PASS.

4.7.2 Low-Speed Downstream Signal Quality Test

The best method to capture and analyze low-speed downstream signal quality is to capture both a keep-alive (low-speed EOP) and a packet. The embedded Host is required to either generate a keep-alive or send low-speed traffic once per frame whenever a low-speed device is directly attached to achieve this LOOP GET DESCRIPTOR command is issued from the embedded Host; this is achieved by the Host issuing the GET DESCRIPTOR Command continually. The scope is configured to trigger on the packets transmitted by the Host. The triggering part is sometimes found to be hard depending upon the type of scope and its bandwidth. High bandwidth scopes are not ideal for USB compliance testing.

To achieve a stable trigger, it was necessary on our setup to modify the trigger hold off parameter. For a stable display of repetitive signals, trigger hold off allows you to match the trigger timing with pseudo-random bit streams. It was necessary to play with this setting in order to get a stable trigger for the TDSUSB2 software to measure the signal quality for low-speed downstream configuration. Even though values larger than 1 ms would also work, it is advisable to obtain a hold off value less than one ms that allows stable trigger on multiple packets within a frame.

Figure 24 displays the equipment setup for a low-speed downstream signal quality test.

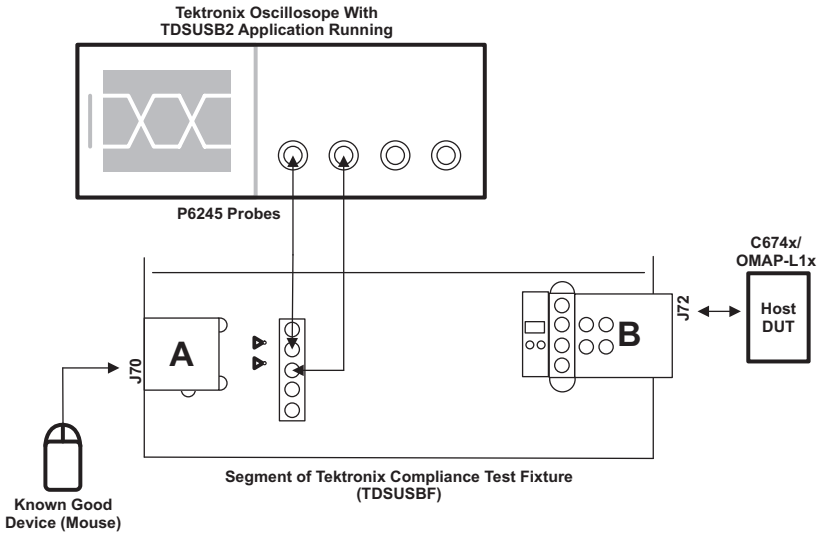

Figure 24. Equipment Setup for Low-Speed Downstream Host Signal Quality Testing

Figure 25 displays the low-speed waveform plot as it is captured by the TDSUSB2F software.

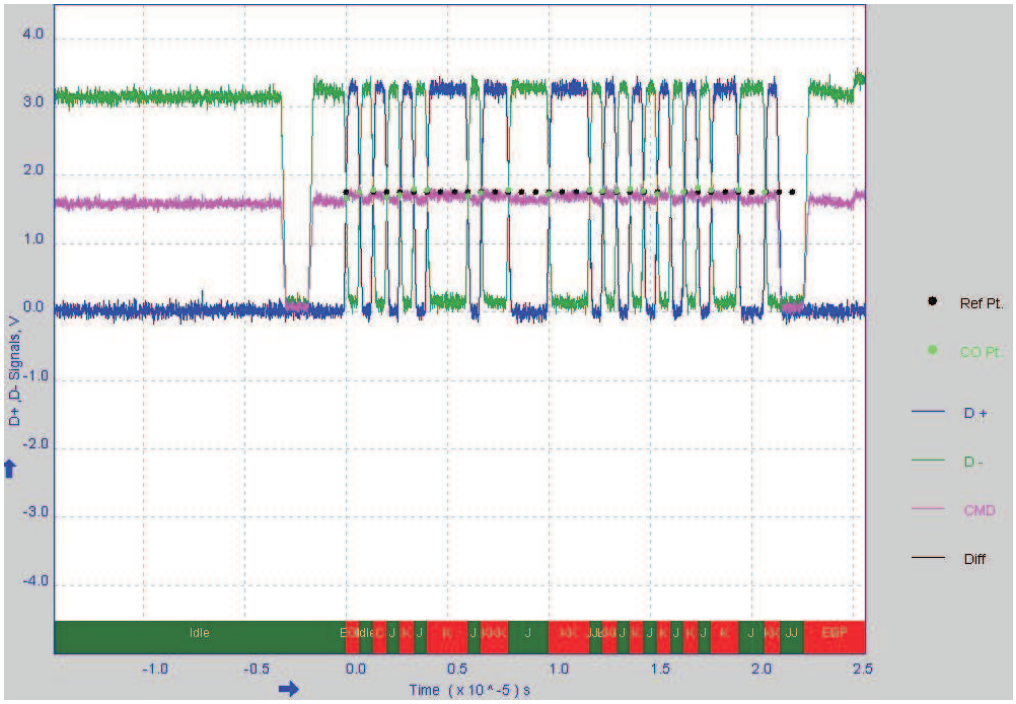

Figure 25. Low-Speed Waveform Plot

Figure 26 displays the eye diagram for low-speed downstream Host.

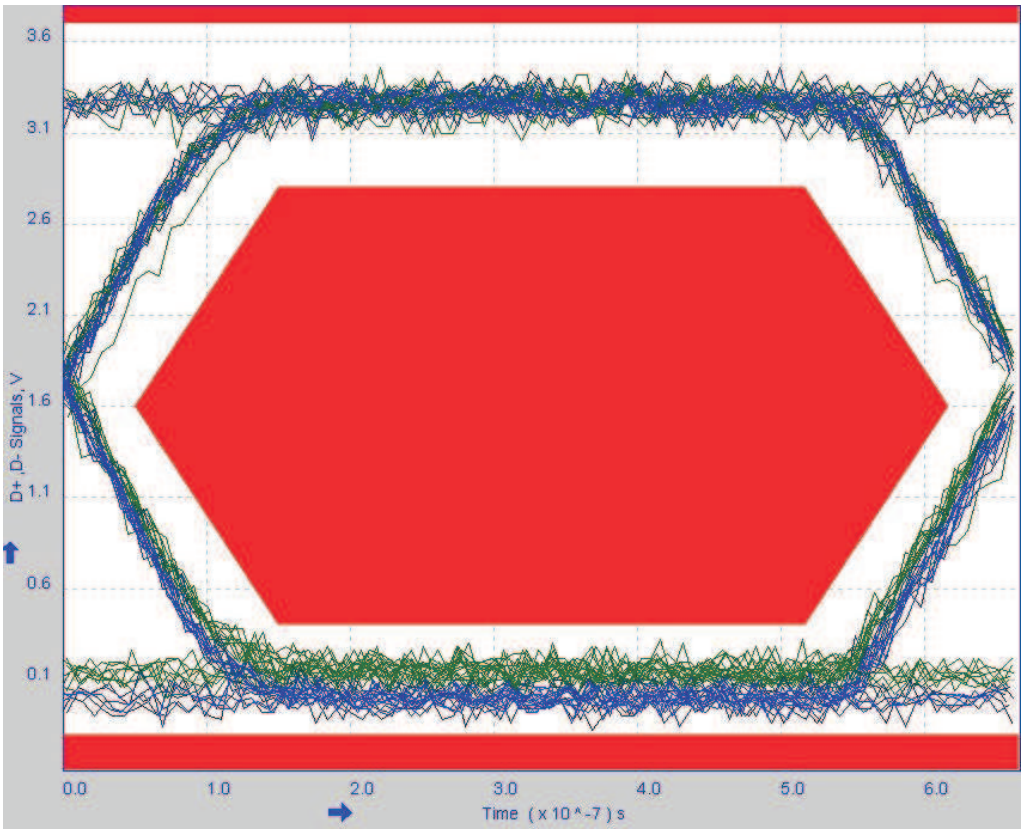

Figure 26. Low-Speed Eye Diagram

Table 8 displays the detailed result for the downstream low-speed signal quality testing.

Table 8. Result Summary for Low-Speed Downstream Host Signal Quality Test(1)

Measurement Name	Minimum	Maximum	Mean	pk-pk	Standard Deviation	RMS	Pop.	Status (2)
Eye diagram test	-	-	-	-	-	-	-	Pass
Signal rate	1.477700 Mbps	1.529572 Mbps	1.500047 Mbps	0.0000 bps	13.17851 kbps	1.499196 Mbps	30	Pass
Crossover voltage	1.671111 V	1.806667 V	1.754928 V	135.5556 mV	37.81959 mV	1.755318 v	23	
EOP width	-	-	1.356817 µs	-	-	-	1	Pass
Consecutive jitter	-6.497579 ns	8.496937 ns	100.5131 ps	14.99452 ns	3.798221 ns	3.712255 ns	22	Pass
Paired JK jitter	-4.813488 ns	6.847330 ns	852.8716 ps	11.66082 ns	3.865405 ns	3.764918 ns	10	Pass
Paired KJ jitter	-3.948052 ns	8.128139 ns	646.5801 ps	12.07619 ns	4.042096 ns	3.888799 ns	10	Pass
Falling edge rate	12.31343 V/µs	15.30612 V/µs	13.82698 V/µs	2.992690 V/µs	692.6314 mV/µs	13.84363 V/µs	25	Pass
Rising edge rate	11.81102 V/µs	15.58442 V/µs	13.93325 V/µs	3.773392 V/µs	880.3906 mV/µs	13.95988 V/µs	24	Pass

(1) Additional Information:
- Rising Edge Rate: 13.93325 V/µs (Equivalent rise time = 189.47 ns)
- Falling Edge Rate: 13.82698 V/µs (Equivalent fall time = 190.93 ns)

(2) Because the individual status of the measurements are Pass and performed on Tier 6 (as per USB-IF), the overall result for this test is PASS.

Note: The actual Tier level for the low-speed device used (mouse) was Tier 1, as is shown on the equipment setup diagram. During the time when the test was performed, the TDSUSB2 software has a bug that required the Tier number to be selected as Tier 6. Table 8 captures the test device position as such. This is a display error and does not comprise the integrity of the test.

5 References

- *Host High-Speed Electrical Test Procedure* documentation issued by the USB Implementers Forum (http://www.usb.org/home)

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