EVM User's Guide: AM261-SOM-EVM

AM261x controlSOM Evaluation Board

Description

AM261-SOM-EVM is an evaluation and development board for the Texas Instruments' Sitara™ AM261x series of microcontrollers (MCUs). The System-On-Module design with three 120-pin high-speed, high-density connectors is an excellent choice for initial evaluation and rapid prototyping. An XDS110ISO-EVM is required for evaluation using the AM261-SOM-EVM, and can be bundled with the AM261-SOM-EVM or purchased separately.

Get Started

1. Order the AM261 controlSOM Evaluation Board (EVM)
2. Order the XDS110 emulation board (XDS110ISO-EVM) and any optional adapter and base board hardware
   a. AM26x SOM to HSEC Adapter Board (HSEC180ADAPEVM-AM2)
   b. AM26x HSEC docking station (TMDSHSECDOCK-AM263)
3. Download the latest Code Composer Studio™ Integrated Development Environment (IDE) and the AM261x MCU PLUS Software Development Kit (SDK)
4. Read the Setup chapter in this User's Guide to get started

Features

- Multirail Power Management Integrated Circuit (PMIC) designed for safety-relevant applications
- 3x 120-pin controlSOM high-speed, high-density (HD) connectors
- Analog I/O, digital I/O and JTAG signals at board interface
- 3x push buttons:
  - PORz
  - User Interrupt
  - RESETz
- Power status LEDs
- User configurable LEDs
- Temperature sensor
- 2x current monitors
- On-board memory
  - 256Mb OSPI NOR Flash
  - 1Mb I2C EEPROM
- MIPI-60 header for TRACE debugging

1 Evaluation Module Overview

1.1 Introduction

The AM261-SOM-EVM evaluation module is a development platform that can be used to evaluate the performance of the AM261x device in automotive and industrial applications. The System-On-Module (SOM) architecture includes all the necessary power, reset, and clock logic to operate the AM261x device.

The 360-pin (3x 120-pin) controlSOM is intended to provide a well-filtered, robust design that is capable of working in most environments. This document provides the hardware details of the AM261x controlSOM and explains the functions of the on-board peripherals, locations of jumpers and connectors, and configurations of switches present on the PCB. Also included in this guide are instructions on how to start developing software applications on the controlSOM.

Preface: Read This First

1.1.1 Sitara MCU+ Academy

Texas Instruments offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.1.2 Important Usage Notes

Note

External power supply or power accessory requirements:

- Nominal output voltage: 5-VDC
- Max output current: 3000mA
- Efficiency Level V

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

1.2 Kit Contents

The AM261x controlSOM development kit contains the following items:

- AM261-SOM-EVM development board
- Quick Start Guide

The following items are not included:

- (Required) XDS110ISO-EVM debug probe needed to provide debug connectivity to the controlSOM
- (Optional) HSEC180ADAPEVM-AM2 adapter board which is used to interface the controlSOM to any hardware designed for the AM26x controlCARD standard
- (Optional) TMDSHSECDOCK-AM263 baseboard docking station which provides header pin access to key signals on the controlSOM

1.3 Specification

The AM261-SOM-EVM is designed to explore the functionality of AM261x microcontrollers. The controlSOM can be treated as a good reference design and is not intended to be a complete customer design. Full compliance to safety, EMI or EMC, and other regulations are left to the designer of the AM261x system.

1.3.1 Component Identification

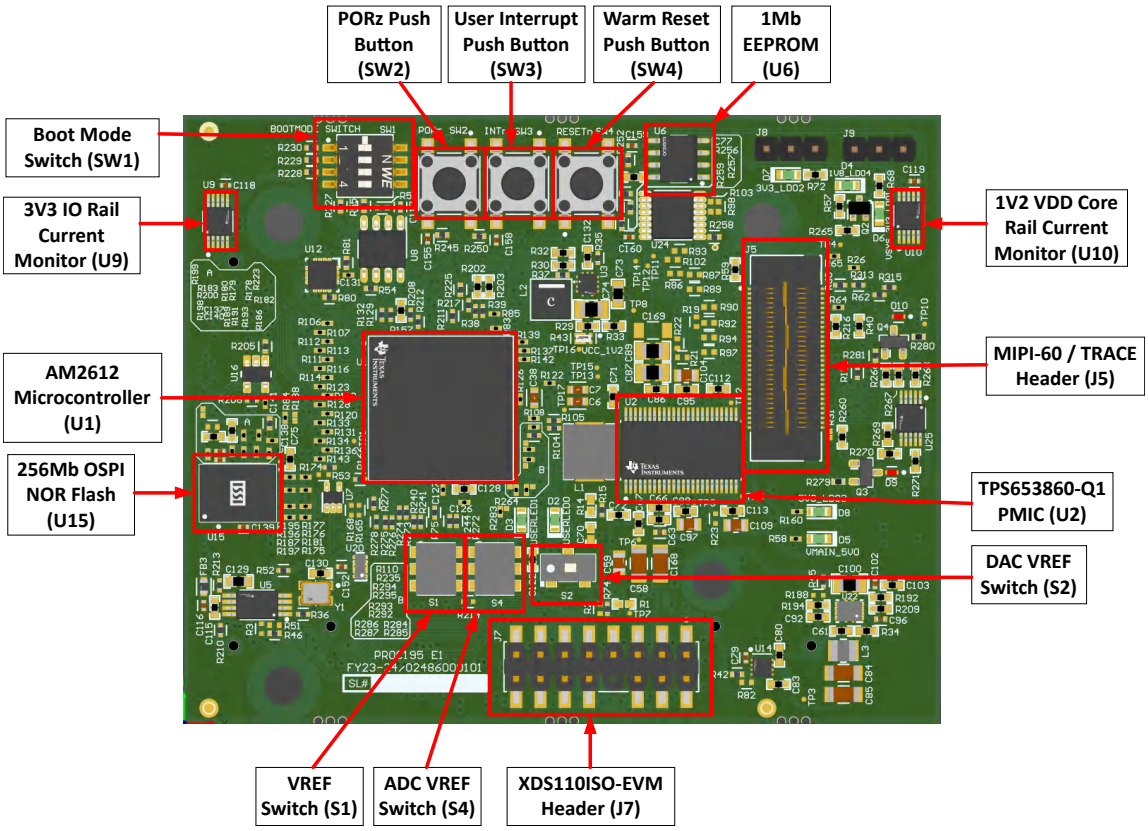

Figure 1-1. AM261-SOM-EVM (Top View)

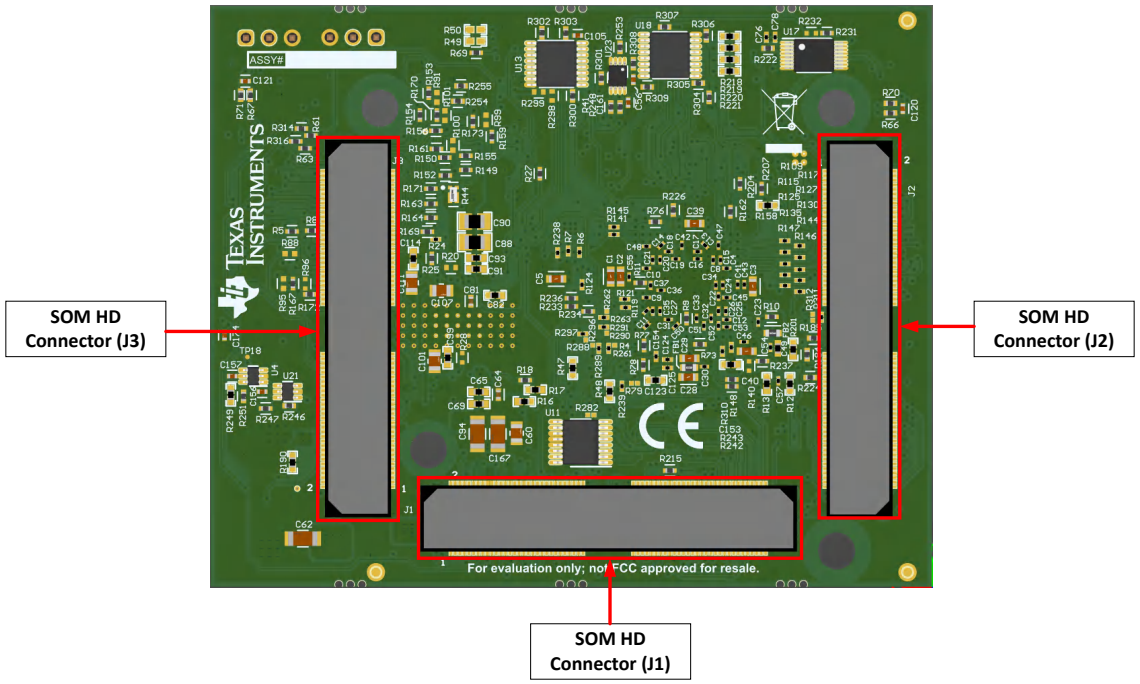

Figure 1-2. AM261-SOM-EVM (Bottom View)

1.3.2 Functional Block Diagram

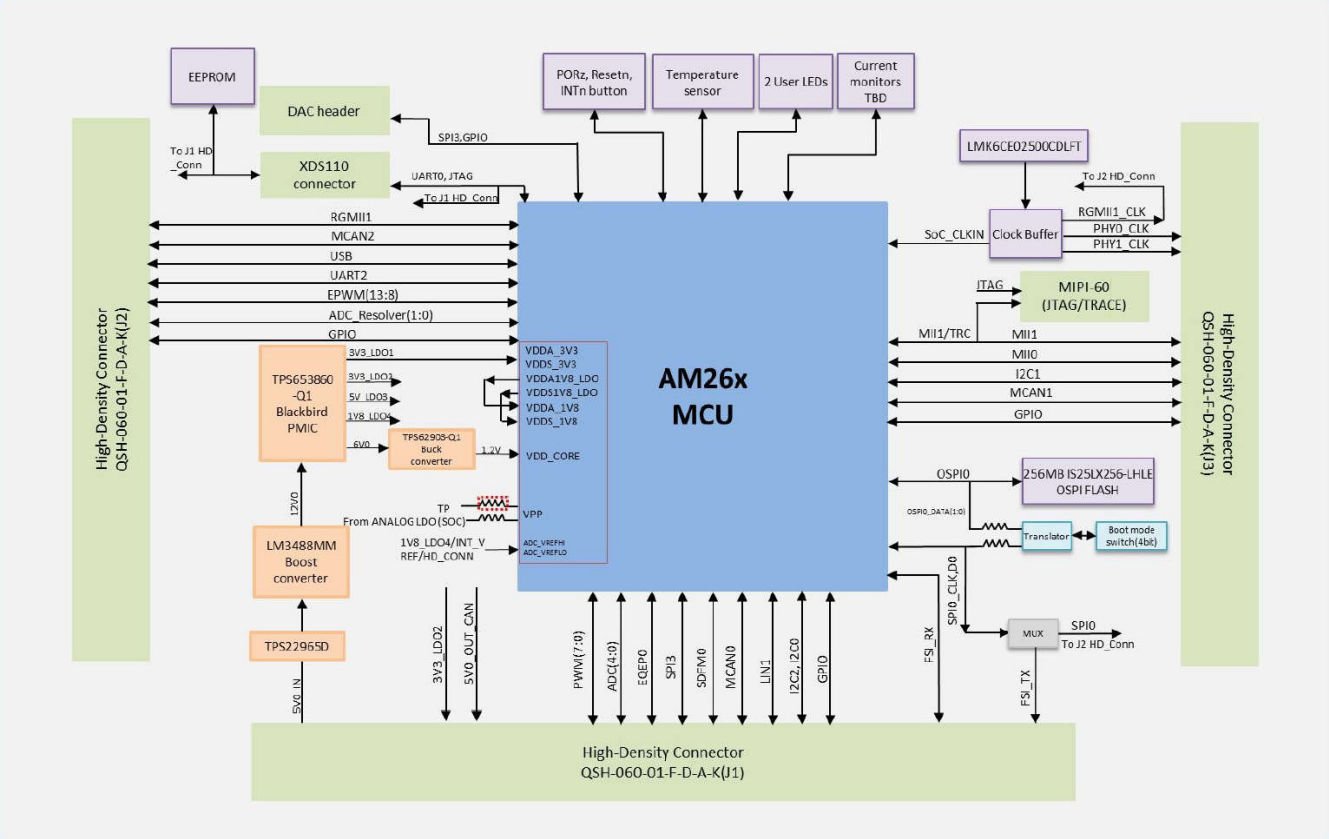

Figure 1-3. AM261-SOM-EVM Functional Block Diagram

1.4 Device Information

The AM261x Sitara Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm® Cortex®-R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by Hardware Security Manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared Tightly Coupled Memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

2 Hardware

2.1 Setup

The AM261x controlSOM supports three different configurations. Each configuration enables a different evaluation setup.

Note

When the controlSOM is used in a high-voltage setup, the user is responsible to confirm that the voltages and isolation requirements are identified and understood prior to energizing the board or simulation. When energized, the controlSOM or components connected to the controlSOM cannot be touched.

2.1.1 Configuration 1: Standalone Configuration

The standalone configuration can be used for most software development use cases that do not require the controlSOM to interface to other hardware. An XDS110 debug probe (XDS110ISO-EVM) is required for this configuration. Power is provided to the controlSOM through XDS110 debug-probe. The XDS110 debug probe is sold separately.

In this configuration, Code Composer Studio™ connects to the controlSOM by JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU by UART.

Follow these steps to enable this configuration:

1. Collect the required equipment:
   a. AM261x controlSOM (AM261-SOM-EVM)
   b. XDS110 isolated debug probe (XDS110ISO-EVM)
   c. USB Type-C® cable
2. Verify that the switch settings are correct on each EVM.
   a. AM261-SOM-EVM:
      i. Use SW1 to select the desired boot mode (Section 2.7).
      ii. Use S1, S2, S4 to select the desired ADC voltage reference mode (if applicable for the application) (Section 2.9.7).
   b. XDS110ISO-EVM: No switch configuration is necessary.
3. Connect the XDS110ISO-EVM to connector J1 of the controlSOM.
4. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe and the controlSOM are powered on.
5. Verify the power status LEDs (D5, D6, D7) on the controlSOM are turned on
6. The controlSOM is ready for use. Follow the steps in Section 3 to get started on developing software.

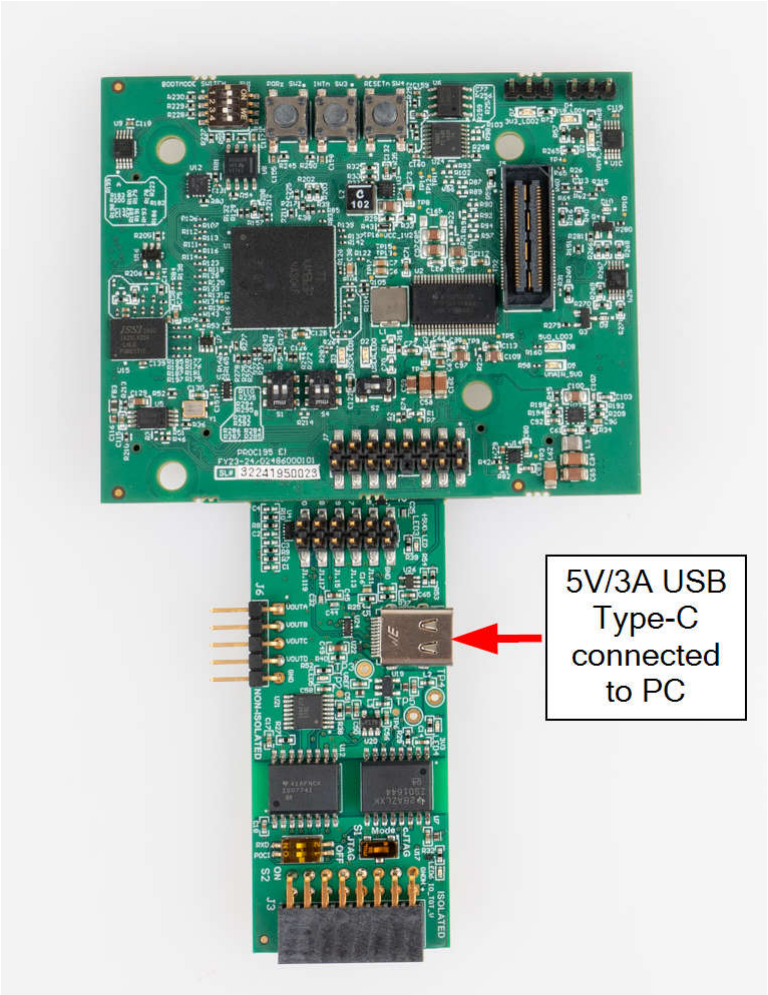

Figure 2-1. AM261-SOM-EVM Standalone Configuration with XDS110ISO-EVM

In the standalone configuration, the 12-pin prototype header (J2) on the XDS110ISO-EVM provides access to a few ADC and GPIO pins on the AM261x device. Table 2-1 lists the ADC and GPIO pins which can be accessed on this prototype header.

Table 2-1. XDS110ISO-EVM Prototype Header (J2) Pinout

MCU Signal	SOM Standard	Pin	Pin	SOM Standard	MCU Signal
GND	GND	12	11	GND	GND
EPWM2_B, GPIO48	J1.5	10	9	J1.11	EPWM1_A, GPIO45
EPWM2_A / GPIO47	J1.7	8	7	J1.13	EPWM0_B, GPIO44
EPWM1_B, GPIO46	J1.9	6	5	J1.15	EPWM0_A, GPIO43
ADC0_AIN3	J1.118	4	3	J1.117	ADC0_AIN1
ADC0_AIN2	J1.120	2	1	J1.119	ADC0_AIN0, DAC_OUT

2.1.2 Configuration 2: AM26x controlCARD Backward Compatibility Configuration

The backward compatibility configuration is used for cases which require the controlSOM to interface to a AM26x controlCARD compatible baseboard or docking station. An HSEC adapter board (HSEC180ADAPEVM-AM2) is required for this configuration. Power is provided to the controlSOM through the HSEC Dock (TMDSHSECDOCK-AM263 or TMDSHSECDOCK). An emulation debug-probe such as the XDS110ISO-EVM is required to provide debug connectivity to the MCU. The HSEC adapter board, XDS110 debug probe, and HSEC dock are sold separately.

TMDSHSECDOCK-AM263 and TMDSHSECDOCK are baseboards that enable rapid prototyping and enhances the development capability of the AM261x controlSOM. The TMDSHSECDOCK-AM263 contains hardware to enable AM26x MCU-specific features that allow various peripherals not enabled onboard the controlSOM to be interfaced with. The TMDSHSECDOCK only enables access to the IOs pinned out to the SOM HD connectors. Table 2-2 compares the features of each docking station.

Table 2-2. AM26x controlCARD HSEC Dock Comparison

Feature	TMDSHSECDOCK	TMDSHSECDOCK-AM263
USB Type-C power input	✓	✓
GPIO breakout headers	✓	✓
Breadboard area for customizable routing and prototyping	✓	
2-channel MCAN Transceiver		✓
2-channel LIN Transceiver		✓
MIPI-60 debug header		✓
14-pin JTAG header	✓	✓
ADC input signal conditioning		✓

In this configuration, Code Composer Studio connects to the controlSOM by JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU by UART.

Follow these steps to enable this configuration:

1. The following equipment is required:
   a. AM261x controlSOM (AM261-SOM-EVM)
   b. AM261x HSEC180 adapter board (HSEC180ADAPEVM-AM2)
   c. AM26x controlCARD compatible baseboard/HSEC180 docking station (TMDSHSECDOCK-AM263 or TMDSHSECDOCK)
   d. XDS110 isolated debug probe (XDS110ISO-EVM)
   e. Two USB Type-C cables
   f. (Optional) DC 5V power supply if using TMDSHSECDOCK
2. Verify the switch settings are correct on each EVM.
   a. AM261-SOM-EVM:
      i. Use SW1 to select the desired boot mode (Section 2.7).
      ii. Use S1, S2, S4 to select the desired ADC voltage reference mode (if applicable for the application) (Section 2.9.7).
   b. XDS110ISO-EVM:
      i. S1 selects JTAG mode – set to JTAG mode.
      ii. S2 enables UART, SPI connection – set to ON mode.
3. Attach the controlSOM to the HSEC180 adapter board.
4. Make sure the controlSOM is correctly oriented. The J1 header on the controlSOM connects with the J1 header on the HSEC180 adapter board.
5. Insert the HSEC180 adapter board into the HSEC docking station.
6. Connect the XDS110ISO-EVM into the connector J4 of the HSEC-180 adapter board (Figure 2-2) or J7 (Figure 2-3) of the controlSOM.
7. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe is powered on.
8. Connect a USB cable into the connector on the HSEC docking station.
9. HSEC Dock Power.
   a. If using TMDSHSECDOCK-AM263, then flip SW3 to the ON position.
   b. If using TMDSHSECDOCK, then flip S1 to the USB-ON position.
10. Verify the power status LEDs (D5, D6, D7) on the controlSOM are turned on.

11. The controlSOM is ready for use. Follow the steps in Section 3 to get started on developing software.

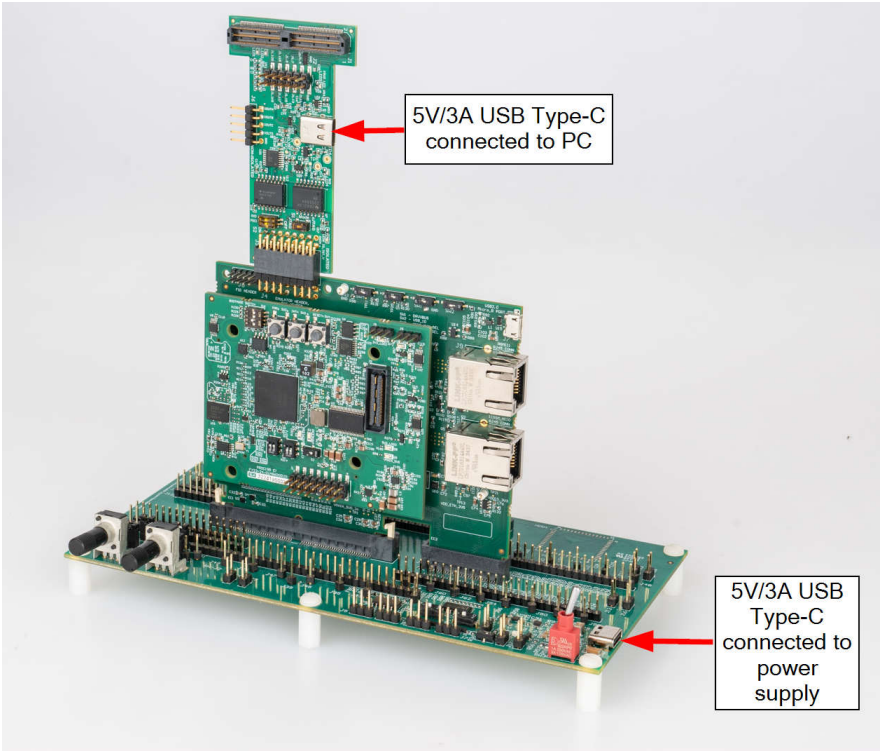

Figure 2-2. AM26x controlCARD Backward Compatibility Configuration - XDS110ISO Connected to HSEC180ADAPEVM-AM2 J4

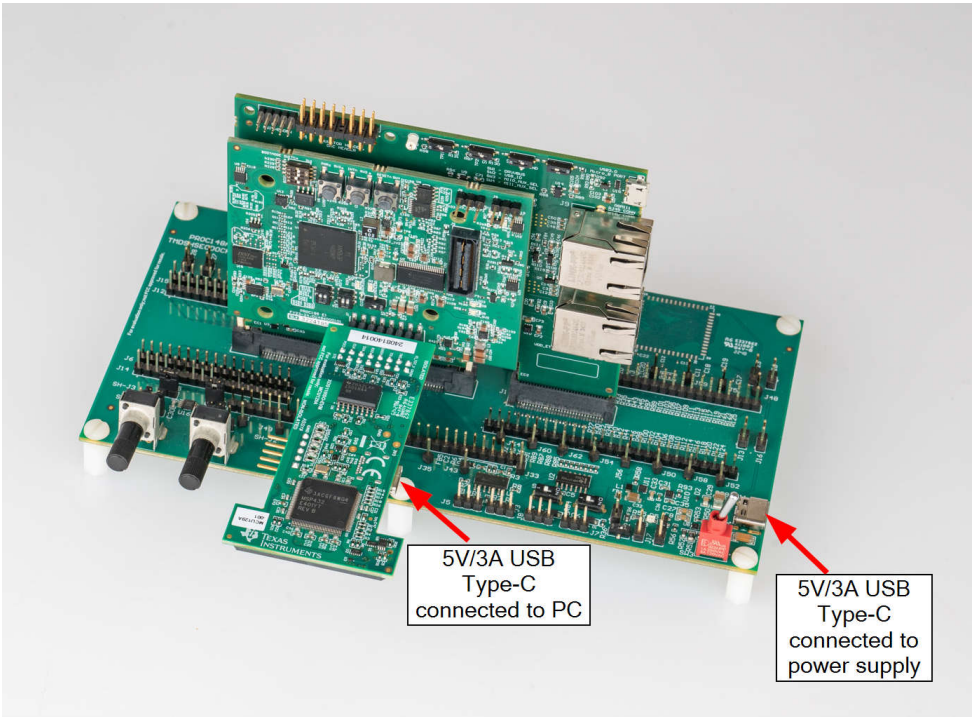

Figure 2-3. AM26x controlCARD Backward Compatibility Configuration - XDS110ISO connected to controlSOM J7

2.1.3 Configuration 3: Baseboard Configuration

The baseboard configuration is used for to interface the controlSOM directly to a compatible baseboard or docking station. Power is provided to the controlSOM through the baseboard. An emulation debug-probe such as the XDS110ISO-EVM is required to provide debug connectivity to the MCU. The XDS110 debug-probe and baseboard are sold separately.

In this configuration, Code Composer Studio Theia connects to the controlSOM via JTAG and enables software development. The XDS110 debug-probe also enumerates a virtual COM port (VCP) for communication with the MCU via UART.

Follow the steps in the baseboard user's guide to enable this configuration.

1. The following equipment is required:
   a. AM261x controlSOM (AM261-SOM-EVM)
   b. C2000, Sitara controlSOM compatible base board
   c. XDS110 isolated debug probe (XDS110ISO-EVM)
   d. One USB Type-C cable
2. Verify the switch settings are correct on each EVM.
   a. AM261-SOM-EVM:
      i. Use SW1 to select the desired boot mode (Section 2.7).
      ii. Use S1, S2, S4 to select the desired ADC voltage reference mode (if applicable for the application) (Section 2.9.7).
   b. XDS110ISO-EVM:
      i. S1 selects JTAG mode; set to JTAG mode.
      ii. S2 enables UART, SPI connection; set to ON mode
3. Set up the base board as per the user's guide instructions.
4. Attach the AM261x ControlSOM to the baseboard.
5. Make sure the controlSOM is correctly oriented. The J1 header on the controlSOM connects with the J1 header on the baseboard.
6. Connect the XDS110ISO-EVM into the XDS Debug Header (J4) of the controlSOM.
7. Connect the USB cable into connector J5 on the XDS110 isolated debug probe. The XDS110 isolated probe and the controlSOM are powered on
8. Provide power to the base board as per the user's guide instructions.
9. Verify the power status LEDs (D5, D6, D7) on the controlSOM are turned on.
10. The controlSOM is ready for use. Follow the steps in Section 3 to get started on developing software.

2.2 Power Requirements

The controlSOM receives power from the 5V input on the high-density connectors. This 5V input is boosted to 12V , which serves as the input to the TPS653860-Q1 PMIC. The PMIC and downstream buck converter on the board generate all the voltage rails required on the controlSOM. All power supply sequencing and voltage monitoring is handled by the PMIC. Figure 2-4 details the power tree of the AM261x controlSOM. Figure 2-5 details the power sequencing of the AM261x controlSOM.

2.2.1 Power Tree

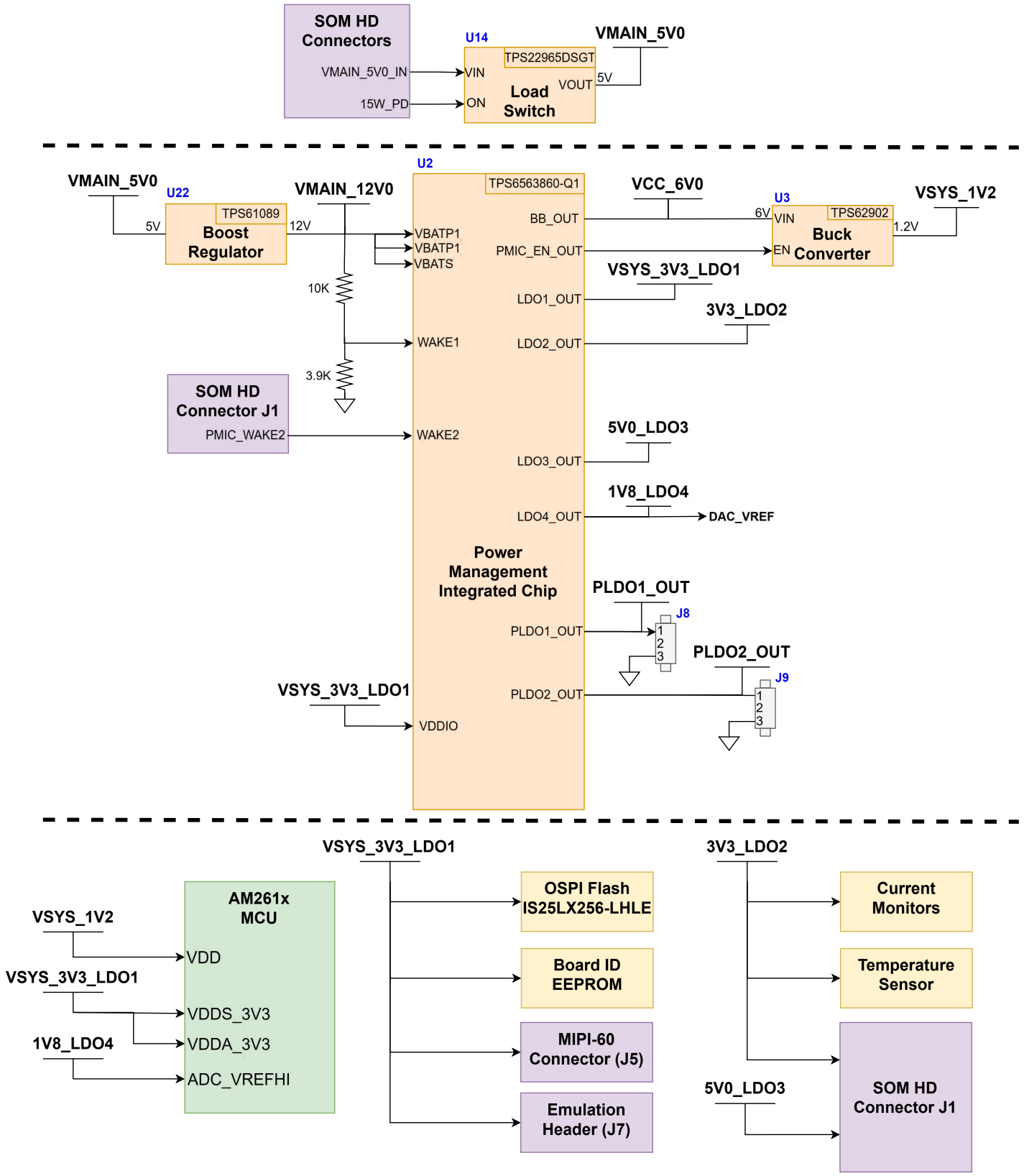

Figure 2-4. AM261-SOM-EVM Power Tree

2.2.2 Power Sequence

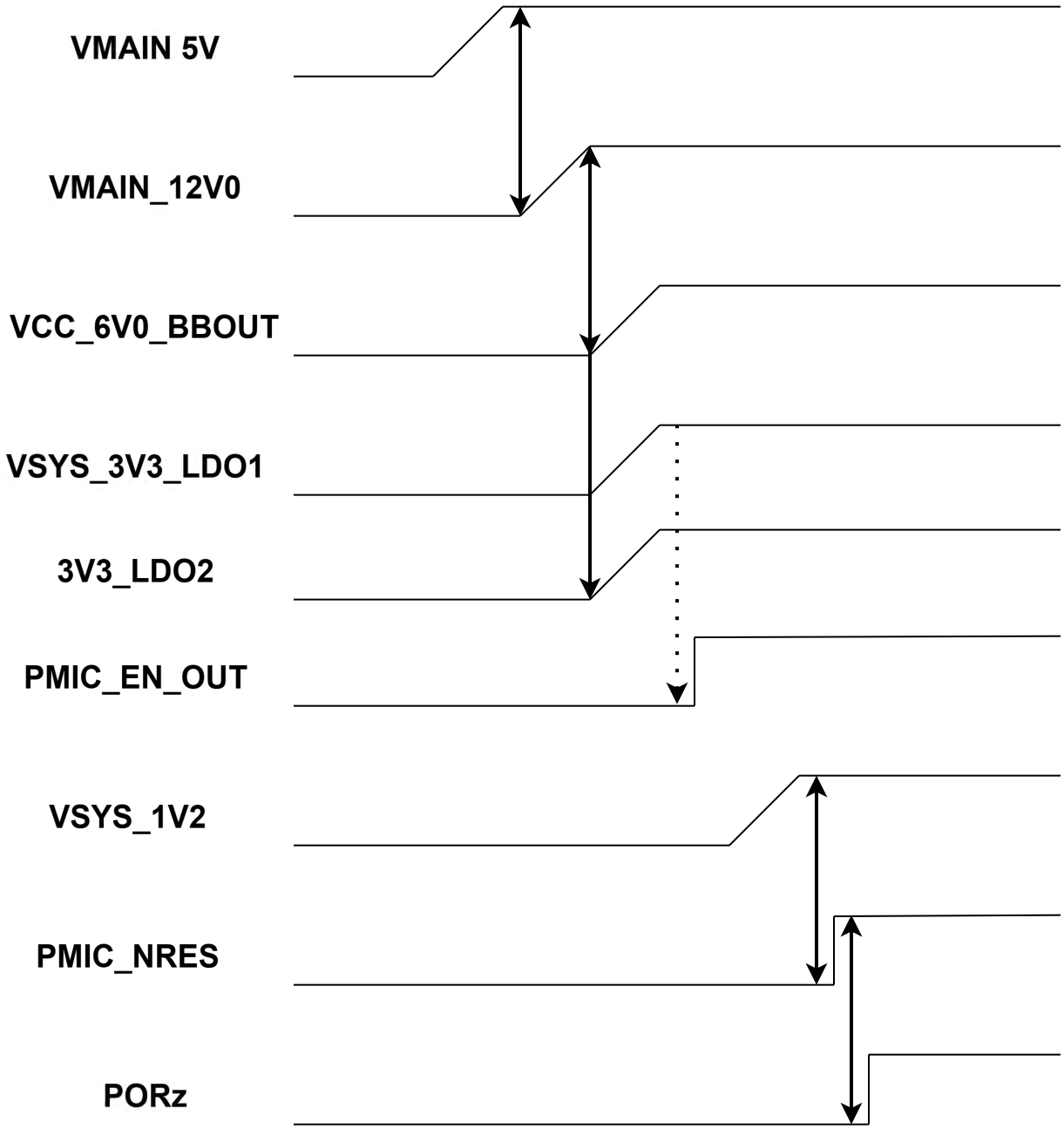

Figure 2-5. Power Sequence

2.2.3 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in the table below.

Table 2-3. Power Status LEDs

Name	Default Status	Operation	Function
D2	OFF	USER_LED0	User Programmable Red LED
D3	OFF	USER_LED1	User Programmable Green LED
D4	OFF	1V8_LDO4	Power indicator for PMIC LDO 1.8V supply
D5	ON	VMAIN_5V0	Power indicator for system 5V input supply
D6	ON	VSYS_3V3_LDO1	Power indicator for primary PMIC LDO 3.3V supply
D7	ON	3V3_LDO2	Power indicator for secondary PMIC LDO 3.3V supply
D8	OFF	5V0_LDO3	Power indicator for PMIC LDO 5.0V supply
D9	OFF	SAFETY_ERROR	Safety error output status pin from AM261x
D10	OFF	PMIC_SAFE_OUT2	Safety Error indicator output from PMIC

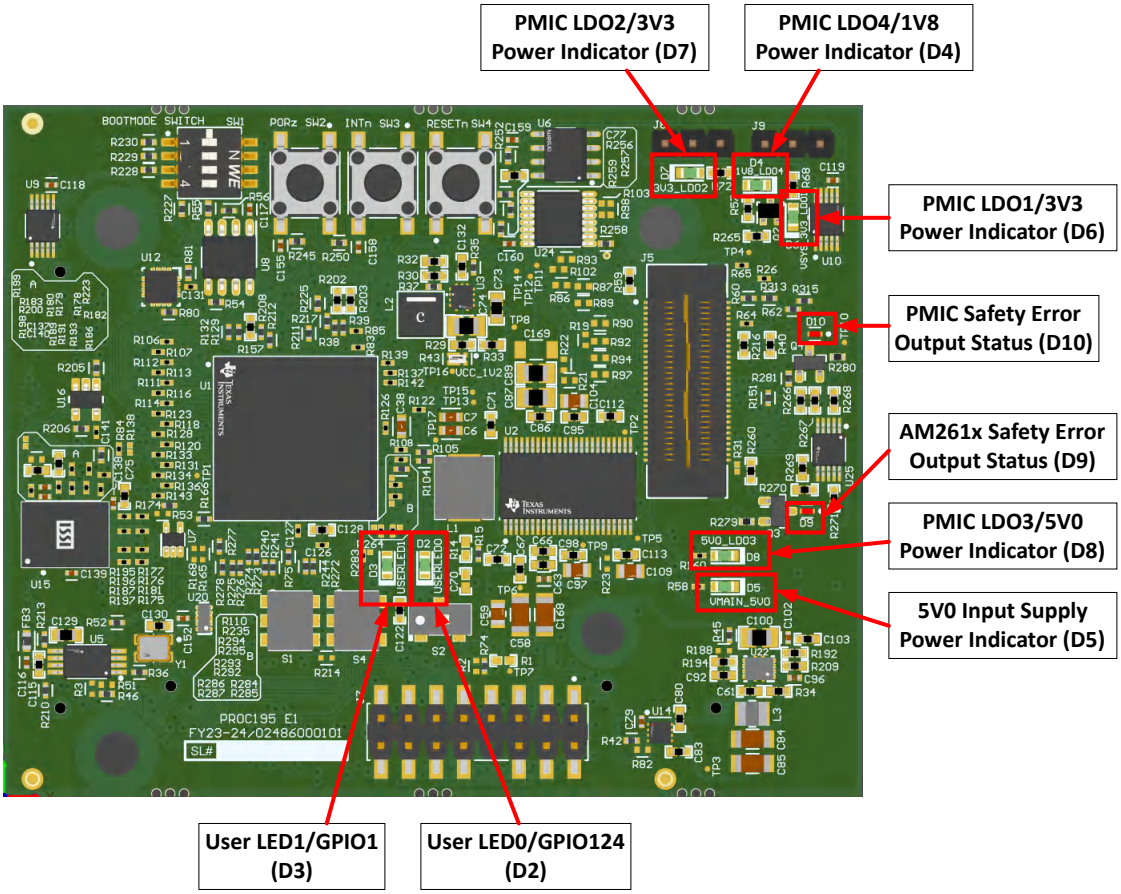

Figure 2-6. Power Status LEDs

2.2.4 PMIC

The AM261x controlSOM makes use of a multirail power supply for microcontrollers in safety-relevant applications (TPS6563860-Q1). The PMIC integrates multiple supply rails to power the MCU and other onboard peripherals.

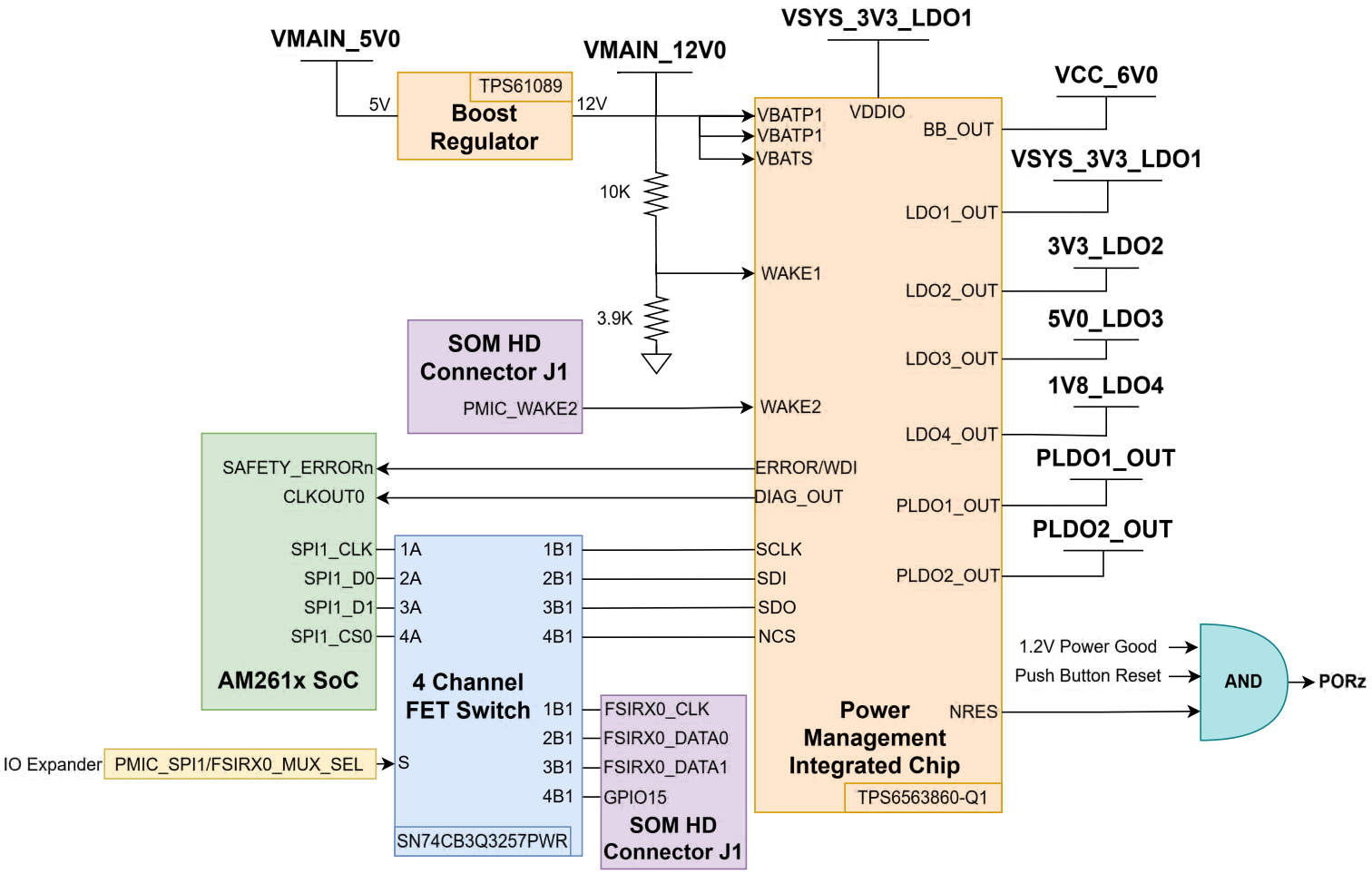

Figure 2-7. PMIC

Note

BB_OUT, LDO1_OUT, and LDO2_OUT are powered on by default. LDO[3:4]_OUT and PLDO[1:2]_OUT are not powered on by default at system start-up and require a SPI write from the AM261x to enable these supply rails.

An independent voltage monitoring unit inside the PMIC monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the supply. All supplies are protected with current limiting and overtemperature warning and shutdown.

2.3 Header Information

The AM261-SOM-EVM can be interfaced to a compatible baseboard through three 120-pin high-density connectors. These connectors provide access to a number of pins on the AM261x device and other signals found on the controlSOM board. For a complete pinout of these connectors, refer to the *PROC195E1(001)_SOM_pinout.pdf* file included in the AM261-SOM-EVM design file package. The design file package download link can be found in Section 4.

2.3.1 Baseboard Headers (J1, J2, J3)

The AM261-SOM-EVM conforms to the C2000, Sitara MCU controlSOM standard. Three baseboard headers (J1, J2, and J3) are supported for interfacing to compatible baseboards. Refer to the *PROC195E1(001)_SOM_pinout.pdf* document in the AM261-SOM-EVM design files for a complete pinout of these headers.

J1, J2, J3 header information:

- Part number: QSH-060-01-L-D-A
- Manufacturer: Samtec
- Maximum insertion cycles: 100

2.3.2 XDS Debug Header (J4)

The XDS debug header (J4) provides debug access to the AM261-SOM-EVM. This header is used when the controlSOM is used in SOM Configuration 2 or Configuration 3. The XDS debug header is compatible with the XDS110ISO-EVM. Table 2-4 provides a pinout of the J4 header.

CAUTION

The XDS debug header (J4) is only compatible with the XDS110ISO-EVM. Do not plug in any other debug probe directly into this header.

Table 2-4. XDS Debug Header (J4) Pinout

EVM Connection	Function	Pin	Pin	Function	EVM Connection
VSYS_3V3_LDO1	IO_TGT_V	1	2	GND	GND
TMS	MCU_TMS	3	4	MCU_TCK	TCK
TDI	MCU_TDI	5	6	MCU_TDO	TDO
GND	GND	7	8	KEY	NC
UART0_RXD	MCU_SCI_RX	9	10	MCU_SCI_TX	UART0_TXD
I2C0_SDA	EE_I2CSDA	11	12	EE_I2CSCL	I2C0_SCL
SPI3_CLK	DAC_SPI_SCLK	13	14	DAC_SPI_PICO	SPI3_D0
SPI3_D1	DAC_SPI_POCI	15	16	DAC_SPI_PTE	SPI3_CS0

2.3.3 MIPI-60 Header (J5)

The AM261x controlSOM includes a MIPI-60 (J5) connector to support external JTAG emulation and Trace debug capabilities. When an external emulator is connected, the signals are routed from the MIPI-60 connector to the AM261x SoC.

Note

To enable 16-bit Trace functionality on this EVM, there are several resistor modifications that are required on the EVM. See Section 2.9.6 for details on resistor modifications.

The pinout of the MIPI-60 connector is shown in Table 2-5

Table 2-5. MIPI-60 Header (J5) Pinout

EVM Connection	Function	Pin	Pin	Function	EVM Connection
VSYS_3V3_LDO1 via 100-ohm resistor	VREF_DEBUG	1	31	TRC_DATA[0][7]	TRC_DATA6
TMS	TMS/TMSC	2	32	TRC_DATA[0][27] or TRC_DATA[1][7]	
TCK	TCK	3	33	TRC_DATA[0][8]	TRC_DATA7

Table 2-5. MIPI-60 Header (J5) Pinout (continued)

EVM Connection	Function	Pin	Pin	Function	EVM Connection
TDO	TDO	4	34	TRC_DATA[0][28] or TRC_DATA[1][8]	
TDI	TDI	5	35	TRC_DATA[0][9]	TRC_DATA8
JTAG_RESETn	nRESET	6	36	TRC_DATA[0][29] or TRC_DATA[1][9]	
TCK	RTCK/EXTC	7	37	TRC_DATA[0][10] or TRC_DATA[3][0]	TRC_DATA9
	nTRST_PD	8	38	TRC_DATA[0][30] or TRC_DATA[1][10] or TRC_DATA[2][0]	
	nTRST/EXTD	9	39	TRC_DATA[0][11] or TRC_DATA[3][1]	TRC_DATA10
	EXTE/TRIGIN	10	40	TRC_DATA[0][31] or TRC_DATA[1][11] or TRC_DATA[2][1]	
	EXTF/TRIGOUT	11	41	TRC_DATA[0][12] or TRC_DATA[3][2]	TRC_DATA11
VSYS_3V3_LDO1 via 100-ohm resistor	VREF_TRACE	12	42	TRC_DATA[0][32] or TRC_DATA[1][12] or TRC_DATA[2][2]	
TRC_CLK	TRC_CLK[0]	13	43	TRC_DATA[0][13] or TRC_DATA[3][3]	TRC_DATA12
	TRC_CLK[1]	14	44	TRC_DATA[0][33] or TRC_DATA[1][13] or TRC_DATA[2][3]	
GND via 0- ohm resistor	Target Presence Detect	15	45	TRC_DATA[0][14] or TRC_DATA[3][4]	TRC_DATA13
GND	GND	16	46	TRC_DATA[0][34] or TRC_DATA[1][14] or TRC_DATA[2][4]	
TRC_CTL	TRC_DATA[0][0]	17	47	TRC_DATA[0][15] or TRC_DATA[3][5]	TRC_DATA14
	TRC_DATA[1][0] or TRC_DATA[0][20]	18	48	TRC_DATA[0][35] or TRC_DATA[1][15] or TRC_DATA[2][5]	
TRC_DATA0	TRC_DATA[0][1]	19	49	TRC_DATA[0][16] or TRC_DATA[3][6]	TRC_DATA15
	TRC_DATA[1][1] or TRC_DATA[0][21]	20	50	TRC_DATA[0][36] or TRC_DATA[1][16] or TRC_DATA[2][6]	
TRC_DATA1	TRC_DATA[0][2]	21	51	TRC_DATA[0][17] or TRC_DATA[3][7]	
	TRC_DATA[1][2] or TRC_DATA[0][22	22	52	TRC_DATA[0][37] or TRC_DATA[1][17] or TRC_DATA[2][7]	
TRC_DATA2	TRC_DATA[0][3]	23	53	TRC_DATA[0][18] or TRC_DATA[3][8]	

Table 2-5. MIPI-60 Header (J5) Pinout (continued)

EVM Connection	Function	Pin	Pin	Function	EVM Connection
	TRC_DATA[1][3] or TRC_DATA[0][23]	24	54	TRC_DATA[0][38] or TRC_DATA[1][18] or TRC_DATA[2][8]	
TRC_DATA3	TRC_DATA[0][4]	25	55	TRC_DATA[0][19] or TRC_DATA[3][9]	
	TRC_DATA[1][4] or TRC_DATA[0][24]	26	56	TRC_DATA[0][39] or TRC_DATA[1][19] or TRC_DATA[2][9]	
TRC_DATA4	TRC_DATA[0][5]	27	57	GND	GND
	TRC_DATA[1][5] or TRC_DATA[0][25]	28	58	GND	MIPI_DETECT - pulled to VSYS_3V3_LDO1 via 4.7k-ohm resistor
	TRC_DATA[0][6]	29	59	TRC_CLK[3]	
TRC_DATA5	TRC_DATA[1][6] or TRC_DATA[0][26]	30	60	TRC_CLK[2]	

Further information on the MIPI-60 emulation and trace header can be found in the Emulation and Trace Headers Technical Reference Manual.

2.4 Push Buttons

The AM261x controlSOM has three push buttons that provide reset inputs and user interrupts to the AM261x device.

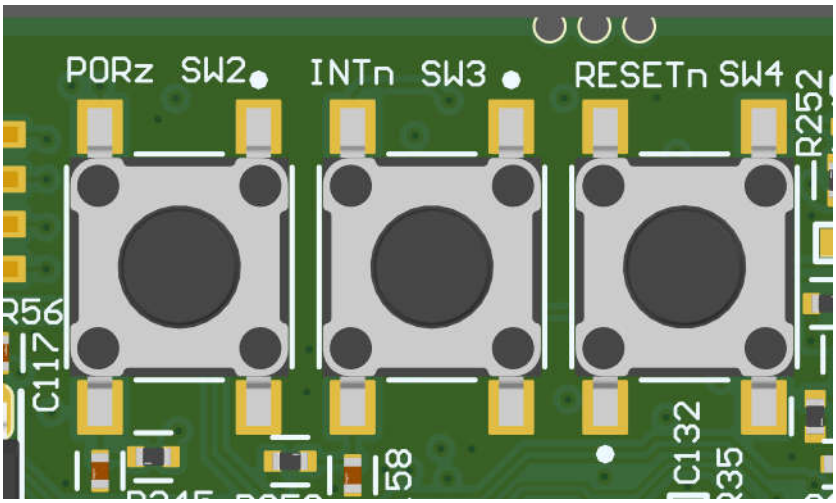

Figure 2-8. AM261x controlSOM Push Buttons

Table 2-6 lists the push buttons on the top side of the AM261x controlSOM.

Table 2-6. AM261x controlSOM Push Buttons

Designator	Signal	Function
SW2	PORz	AM261x Power-On-Reset input
SW3	INTn	User interrupt signal, connected to AM261x GPIO128
SW4	RESETn	AM261x warm reset input

2.5 Reset

Figure 2-9 shows the reset architecture of the AM261x controlSOM.

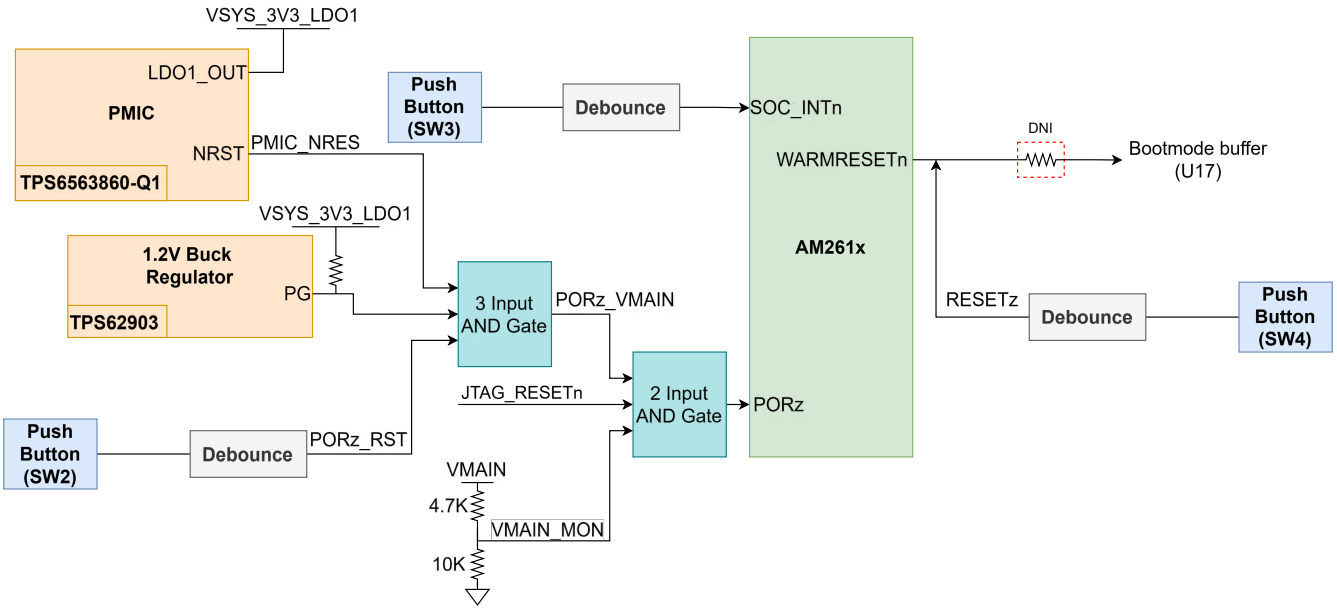

Figure 2-9. Reset Architecture

The AM261x SoC has the following resets:

- PORz is the Power-On-Reset for the MAIN Domain.
- WARMRESETn is the Warm Reset to MAIN Domain.

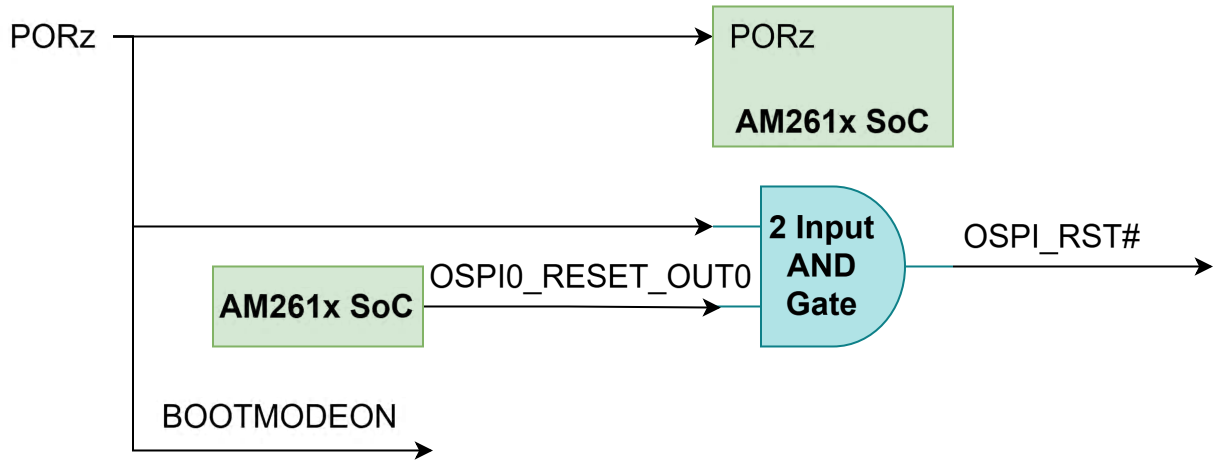

Figure 2-10. PORz Reset Signal Tree

The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The PMIC drives the NRES, MCU Reset output signal low.
- The 1.2V buck regulator outputs a low signal for the power good signal.
- The user push button (SW2) is pressed.

The PORz signal is tied to:

- AM261x SoC PORz input
- OSPI Flash Reset
- BOOTMODE buffer output enable
- SOM HD Connector J1

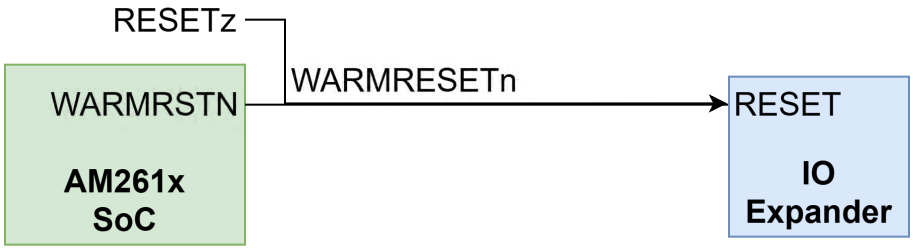

Figure 2-11. WARMRESETn Reset Signal Tree

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW4) is pressed.

The WARMRESETn signal is tied to:

- AM261x SoC WARMRESETN output
- RESETz signal created from push button + PMOS logic
- IO Expander reset

The AM263Px Control Card also has an external interrupt to the SoC, INTn, that occurs when:

- The user push button (SW3) is pressed.

2.6 Clock

The AM261x SoC requires a 25MHz clock input for XTAL_XI. All reference clocks required for the SoC and up to three off-board Ethernet PHYs (on SOM to HSEC adapter board or other base board) are generated from a single four output clock buffer (LMK1C1103PWR), which is sourced from a single 25MHz LVCMOS Oscillator. A clock buffer is used for level translation from 3.3V to 1.8V.

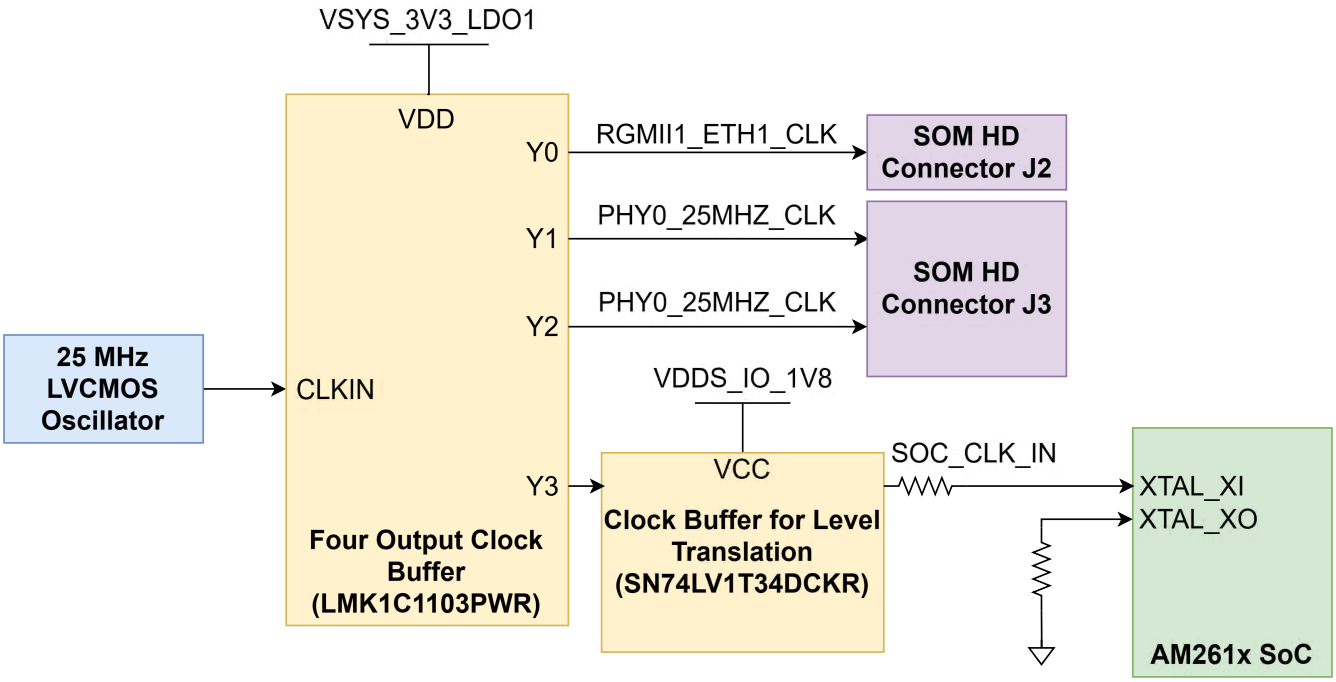

Figure 2-12. Oscillator Clock Tree

2.7 Boot Mode Selection

The bootmode for the AM261x is selected by a DIP switch (SW1). The supported boot modes are as shown in Table 2-7.

Table 2-7. Supported Boot Modes

Boot Mode or Peripheral	Boot Media or Host	Notes
OSPI-OSPI (4S), 50MHz, SDR, 0x6B	Flash Memory	ROM configures OSPI controller in QSPI 4S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
UART, XMODEM, 115200bps	External Host	ROM configures UART0 with baud rate of 115200bps and downloads image from external PC terminal using x-modem protocol.
OSPI-OSPI (1S), 50MHz, SDR, 0x0B	Flash Memory	ROM configures OSPI controller in QSPI 1S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
OSPI (8S), SDR, 33MHz, 0x8B	Flash Memory	ROM configures OSPI controller in 8S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
xSPI (1S->8D) , 25MHz, SFDP	QSPI Flash, External Host	ROM configures OSPI controller in xSPI 8D mode ,Reads SFDP table for read command and downloads image from external flash, Flashes with SFDP are of JEDEC standard Rev D only supported.
USB DFU	External Host	ROM configures USB controller to work in device mode and download the image into L2 memory to process. In case of any failure, ROM falls back to UART boot mode. Supports USB 2.0 device mode at High-Speed (HS, 480Mbps)
DevBoot	N/A	No SBL. Used for development purposes only.

Table 2-8. Boot-Mode Selection Table

Boot Mode	SW1.4, SOP3 SPI0_D0_pad	SW1.3, SOP2 SPI0_CLK_pad	SW1.2, SOP1 OSPI_D1	SW1.1, SOP0 OSPI_D0
OSPI-OSPI (4S), 50MHz, SDR, 0x6B	0	0	0	0
UART, XMODEM, 115200bps	0	0	0	1
OSPI-OSPI (1S), 50MHz, SDR, 0x0B	0	0	1	0
OSPI (8S), SDR, 33MHz, 0x8B	0	0	1	1
xSPI (1S->8D) , 25MHz, SFDP	1	1	0	0
USB DFU	1	1	1	0
DevBoot	1	0	1	1
Unsupported boot mode	All other combinations not defined above.			

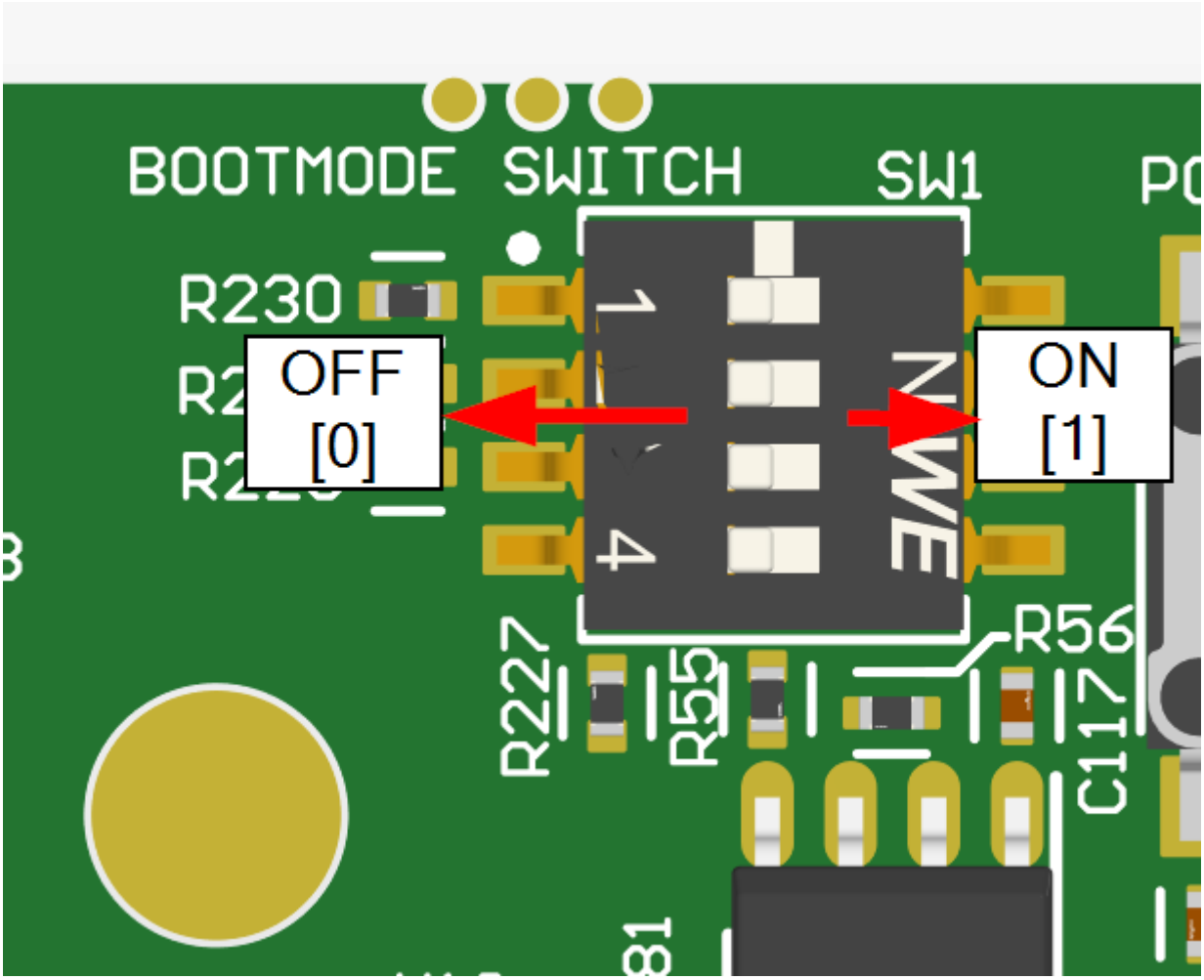

Figure 2-13. AM261-SOM-EVM Bootmode Switches

2.8 GPIO Mapping

Table 2-9. GPIO Mapping Table - Rev E1

GPIO	GPIO Description	Pin Name	Functionality	Net Name	Active Status	SOM HD Connect or Pin	Baseboard or Adapter Board Usage
GPIO66	Reset to OSPI flash device	GPIO66	Reset	OSPI0_RESET_OUTn	LOW		
GPIO138	Resistor option between GPIO and PMIC_DIAG_OUT	CLKOUT0	GPIO	MCU_GPIO138	PREFERABLE	J1-74	Default PMIC_DIAG_OUT. Remove R84 and populate R138 to use as GPIO.
GPIO65	Error signal from OSPI flash device	GPIO65	Error Signal	OSPI0_ECS	LOW		
GPIO1	USER_LED1	OSPI0_CSn1	GPIO	MCU_GPIO1	PREFERABLE	J1-52	Default USER_LED_OUT. Remove R140 and populate R237 to use as GPIO.
GPIO82	Select line for I2C1/ MCAN1 Mux, terminated to SOM HD Connector	MMC0_D3	Mux Select	MCU_GPIO82	PREFERABLE	J1-48	GPIO. Left floating on HSEC180ADAPEVM-AM2
GPIO73	Terminated to SOM HD Connector	PR1_PRU1_GPIO2	GPIO	MCU_GPIO73	PREFERABLE	J1-75	Interrupt signal for MII0 on HSEC180ADAPEVM-AM2
GPIO119	Terminated to SOM HD Connector	PR0_PRU1_GPIO19	GPIO	MCU_GPIO119	PREFERABLE	J3-66	Interrupt signal for MII1 on HSEC180ADAPEVM-AM2
GPIO128	SoC interrupt signal from push button SW3	SDFM0_CLK3	Interrupt	MCU_INTn	LOW		
GPIO126	Terminated to SOM HD Connector	SDFM0_CLK2	GPIO	MCU_GPIO126	PREFERABLE	J1-73	GPIO
GPIO71	Terminated to SOM HD Connector	PR1_PRU1_GPIO0	interrupt	RGMII1_INTn	LOW	J2-7	Interrupt signal for RGMII1 on HSEC180ADAPEVM-AM2
GPIO37	Terminated to SOM HD Connector	RGMII1_TD0	GPIO	RGMII1_TD0	PREFERABLE	J2-8	RGMII1 Transmit Data 0 on HSEC180ADAPEVM-AM2
GPIO121	Resistor option between SOM HD Connector and PMIC_INTn	EXT_REFCLK0	GPIO	MCU_GPIO121	PREFERABLE	J1-70	Default PMIC_INTn. Remove R311 and populate R312 to use as GPIO.
GPIO124	Resistor option between USER_LED0 and SOM HD Connector	SDFM0_CLK1	GPIO	MCU_GPIO124	PREFERABLE	J1-72	Default USER_LED0. Remove R215 and populate R214 to use as GPIO.
GPIO74	Terminated to SOM HD Connector	PR1_PRU1_GPIO9	GPIO	MCU_GPIO74	PREFERABLE	J2-25	MDIO & MDC MUX select line on HSEC180ADAPEVM-AM2
GPIO21	Connection for USB_DRVVBUS	LIN2_RXD	GPIO	AM26x_UART2_RXD	PREFERABLE	J2-26	USB_DRVVBUS
GPIO22	Connection for USB0_VBUS_OC	LIN2_TXD	GPIO	AM26x_UART2_TXD	LOW	J2-28	USB0_VBUS_OC
IO Expander							

Table 2-9. GPIO Mapping Table - Rev E1 (continued)

GPIO	GPIO Description	Pin Name	Functionality	Net Name	Active Status	SOM HD Connect or Pin	Baseboard or Adapter Board Usage
	Select line for PMIC SPI MUX/DEMUX (U24)	P0	Mux Select	PMIC_SPI1/ FSIRX0_MUX_ SEL	PREFERABLE		
	Select line for ADC0_AIN0/DAC_OUT MUX (U20)	P1	Mux Select	ADC0_AIN0/ DAC_OUT_MU X_SEL	PREFERABLE		
	MII Reset	P2	Reset	MII_RST#	LOW	J3-101	Reset signal for MII0 and MII1 on HSEC180ADAPEV M-AM2
	RGMII1 Reset	P3	Reset	RGMII1_RST	LOW	J2-11	Reset signal for RGMII1 on HSEC180ADAPEV M-AM2
	Select line for SPI0-FSI MUX/DEMUX (U13)	P4	Mux Select	SPI0/ FSITX0_MUX_ SEL	PREFERABLE		
	Select line for SPI3 MUX/ DEMUX (U18)	P5	Mux Select	SPI3_MUX_SE L	PREFERABLE		
	Select line for HSEC180ADAPEVM-AM2 MII0 Mux	P6	Mux Select	IOEXP_OUT_P 6	PREFERABLE	J2-5	MII0 Mux select line on HSEC180ADAPEV M-AM2
	Select line for HSEC180ADAPEVM-AM2 MII1 Mux	P7	Mux Select	IOEXP_OUT_P 7	PREFERABLE	J2-9	MII1 Mux select line on HSEC180ADAPEV M-AM2

2.9 Interfaces

2.9.1 Memory Interface

2.9.1.1 OSPI

The AM261x controlSOM has a 256Mbit OSPI NOR flash memory device (IS25LX256-LHLE), which is connected to the OSPI0 interface of the AM261x SoC. The OSPI Flash is powered by the 3.3V IO supply (VSYS_3V3_LDO1).

The OSPI0_D0 and OSPI0_D1 signals are used for BOOTMODE control logic. There are 10kΩ resistors used to isolate the BOOTMODE control logic after the value is latched.

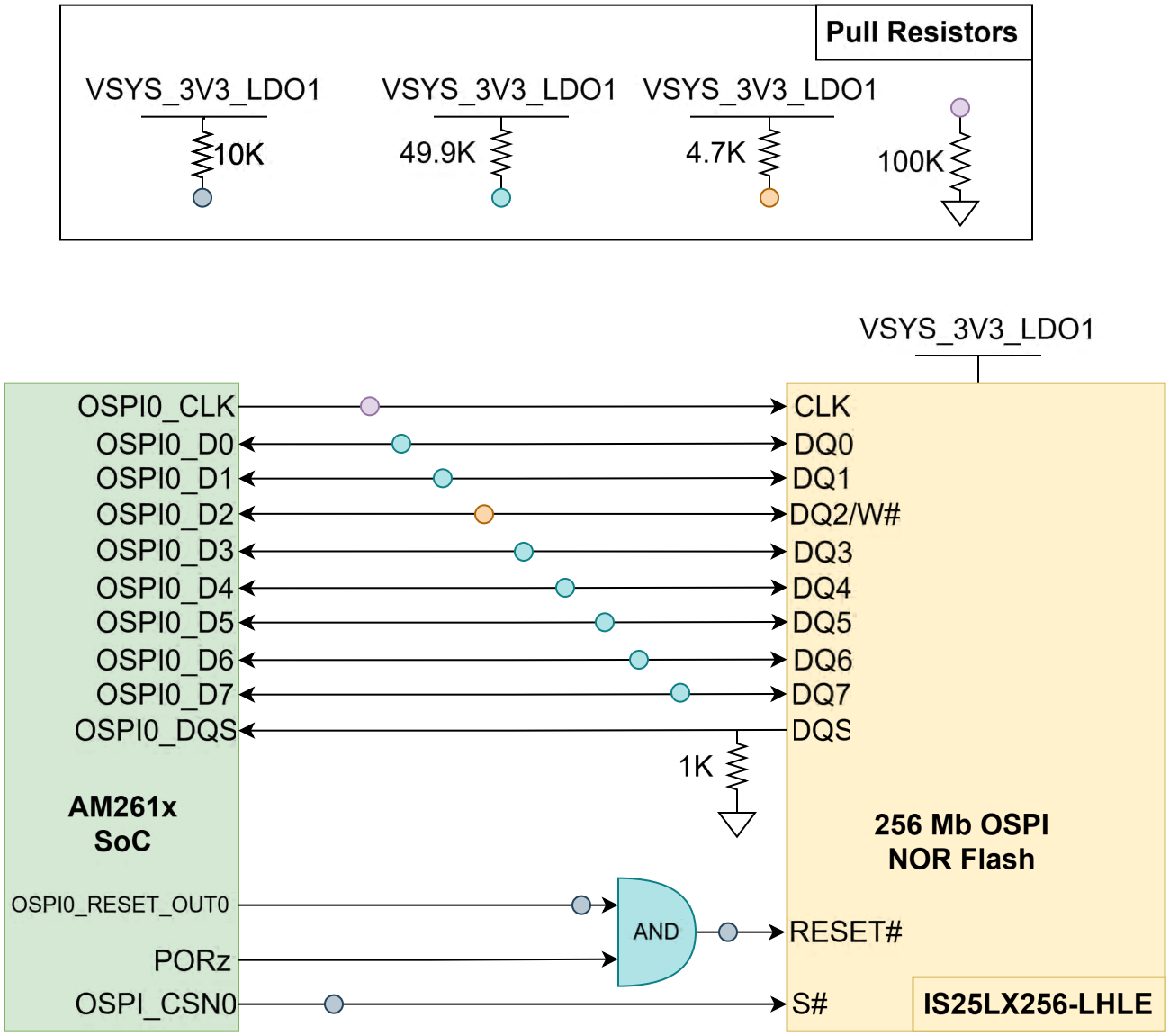

Figure 2-14. OSPI

2.9.1.2 Board ID EEPROM

The AM261x controlSOM has an I2C based 1Mbit EEPROM (CAT23M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C0 interface of the AM261x. The default I2C address of the EEPROM is set to 0x50 by pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is pulled down to ground and Write Protect is disabled.

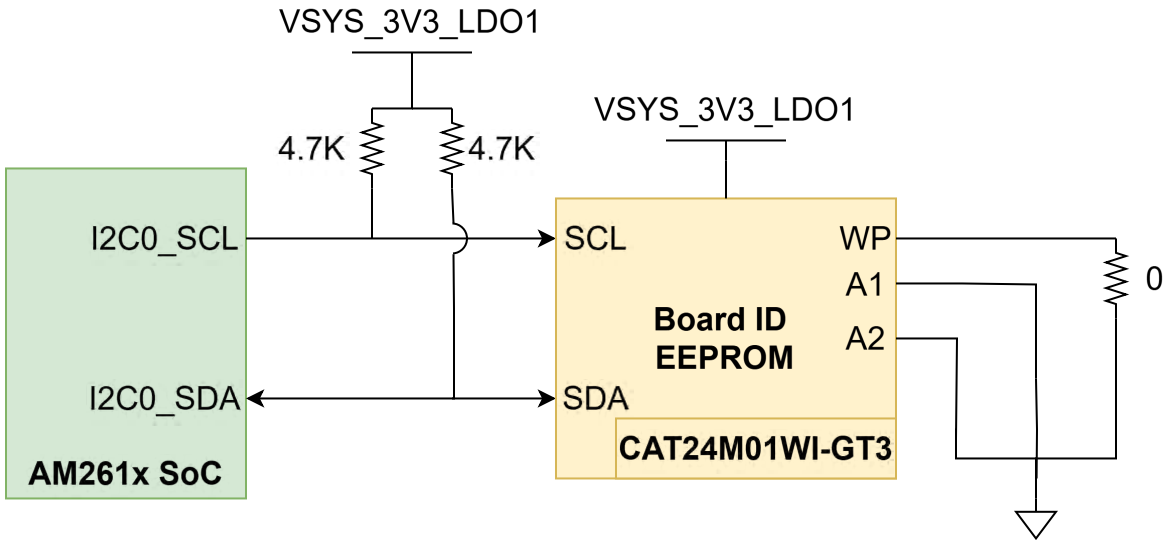

Figure 2-15. Board ID EEPROM

2.9.2 I2C

The AM261x controlSOM uses three SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. All I2C data and clock lines are pulled up to the 3.3V IO voltage supply.

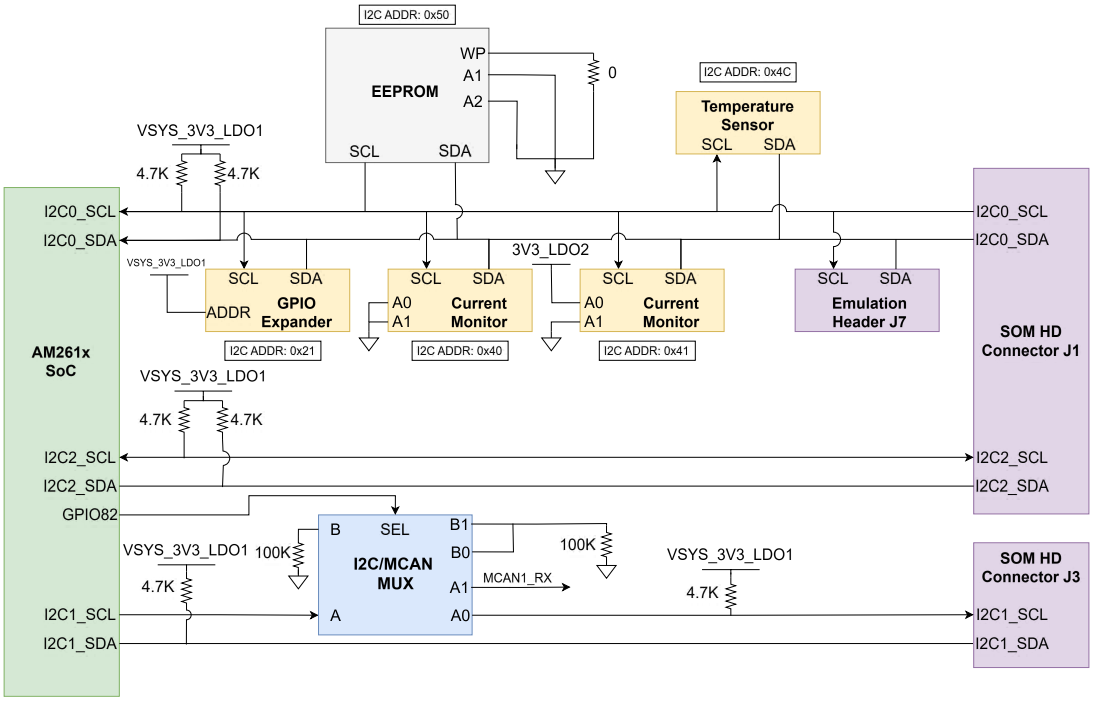

Figure 2-16. I2C Tree

Table 2-10. I2C Addressing

Target	I2C Instance	I2C Address Bit Description	Device Configuration	CC Config.	I2C Address
Board ID EEPROM	I2C0	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1/A2 are connected to ground	0b1010000	0x50
GPIO Expander	I2C0	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected to 3V3	0b0100001	0x21
Current Monitor	I2C0	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device Data Sheet*.	0b1000000	0x40
Current Monitor	I2C0	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device Data Sheet*.	0b1000001	0x41
Temperature Sensor	I2C0	Fixed value of 1001100 for part number TMP411Ax	N/A	0b1001100	0x4C
Emulation Header J7	I2C0	Allows XDS110 device on XDS110ISO-EVM to read Board ID EEPROM			
SOM HD Connector J1	I2C0	Target dependent			
	I2C2	Target dependent			
SOM HD Connector J3	I2C1	Target dependent			

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

2.9.3 SPI

The AM261x controlSOM maps three SPI instances (SPI0, SPI1, SPI3) from the AM261x SoC to the SOM HD Connectors. Series termination resistors are placed near the SoC for each SPI clock signal. Each SPI instance is routed through a 4-channel FET switch that routes between the SOM HD connector and a specific peripheral or alternative header. Table 2-11 details the Muxing scheme on the SPI instances:

Table 2-11. AM261x controlSOM SPI Routing

SPI Instance	B1	B2	Default
SPI0	SPI0 → SOM HD Connector J2	FSITX0 → SOM HD Connector J1	B1
SPI1	SPI1 → PMIC	FSIRX0 → SOM HD Connector J1	B1
SPI3	SPI3 → SOM HD Connector J1	DAC_SPI3 → Emulation Header J7	B2

SPI0 is routed to the SOM HD connector J2 at the SPI standard location. The 4-channel FET switch can route the same AM261x device pins to the FSITX standard location on SOM HD connector J1 to be used as FSI signals.

SPI1 is routed to either the on-board PMIC (default selection) or as FSI signals to the FSIRX standard location on SOM HD connector J1.

SPI3 is routed to the standard SPI location on SOM HD connector J1 or to the Emulation Header (J7) to communicate with the DAC IC on the XDS110ISO-EVM (default selection).

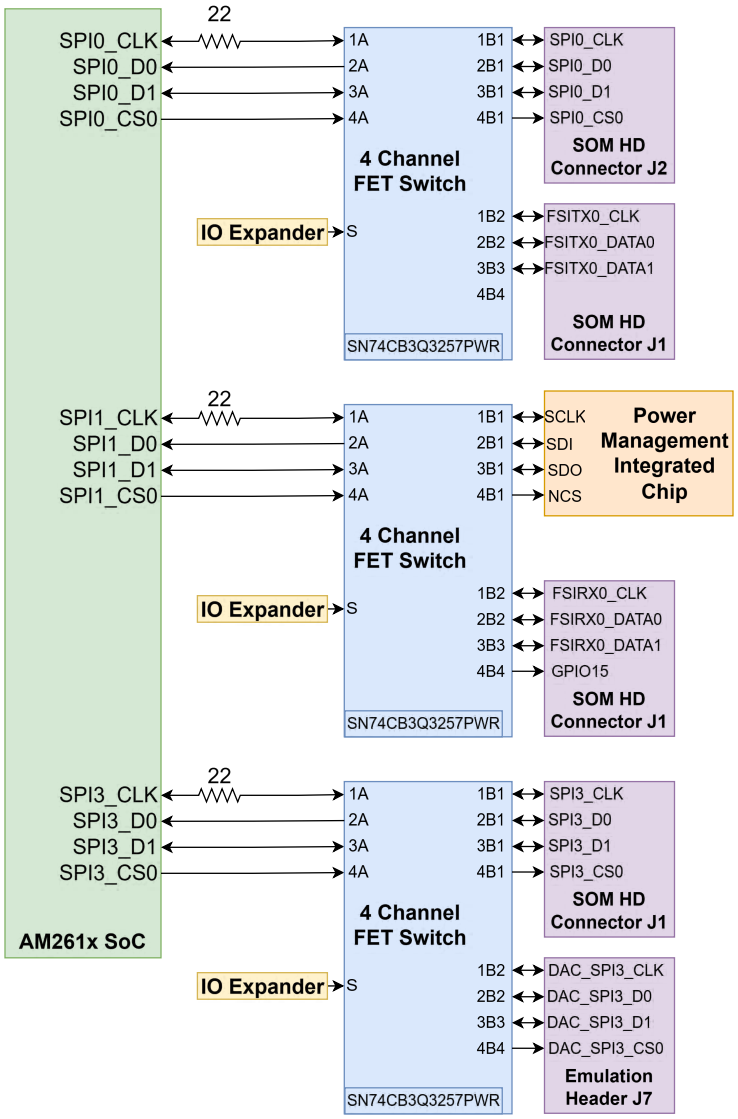

Figure 2-17. SPI

2.9.4 UART

The AM261x controlSOM connects to the XDS110ISO-EVM which uses the onboard XDS110 emulator as a USB2.0 to UART bridge for terminal access. The UART0 transmit and receive signals of the AM261x SoC are mapped to SOM HD Connector J1 to connect to the XDS110ISO-EVM in non-isolation mode, and to the Emulation Header (J7) for use in isolation mode.

The AM261x controlSOM supports an additional UART2 instance that has the transmit and receive signals mapped from the AM261x SoC to the SOM HD Connector J2.

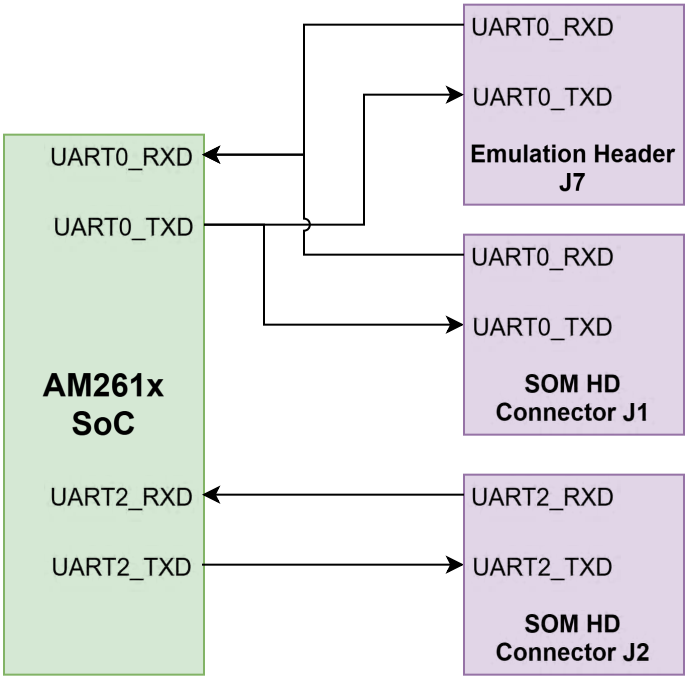

Figure 2-18. UART

2.9.5 JTAG

The AM261x controlSOM maps the JTAG signals from the AM261x SoC to the SOM HD Connector J1, MIPI-60 Connector J5, and to the Emulation Header J7.

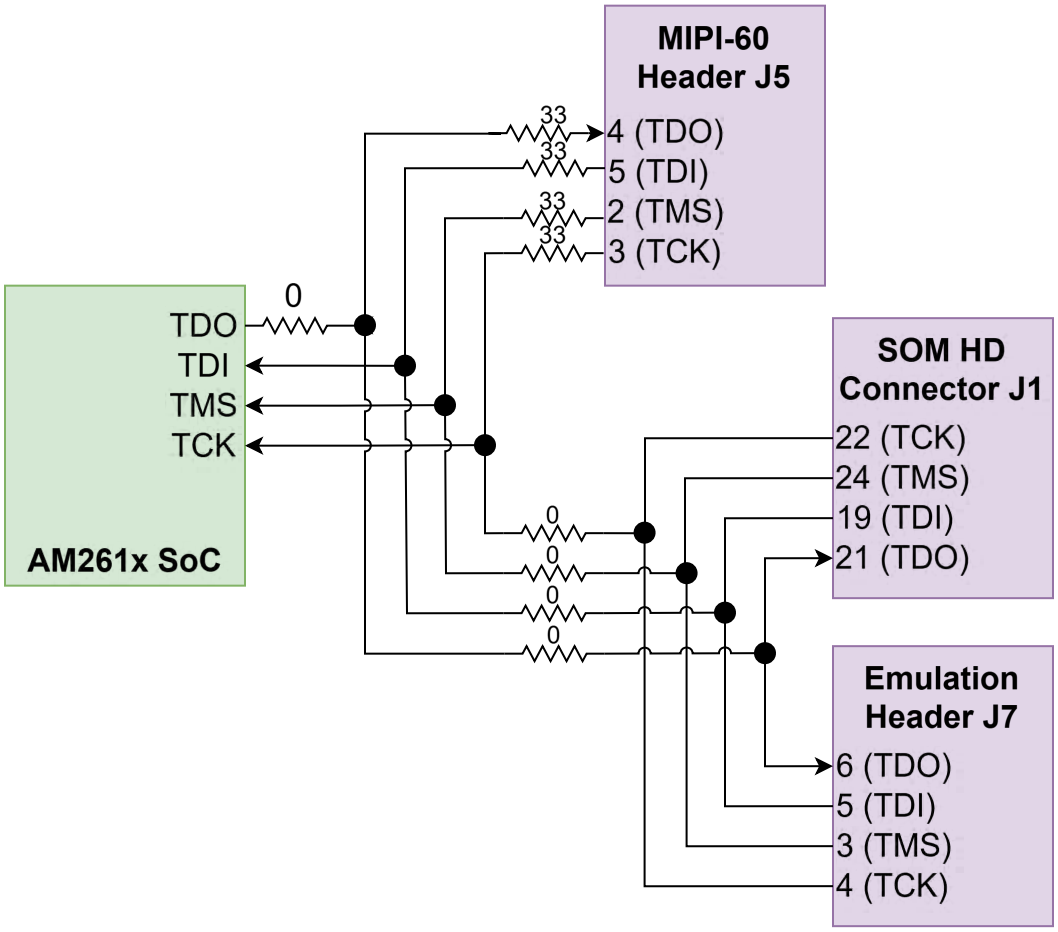

Figure 2-19. JTAG

2.9.6 TRACE

The AM261x controlSOM has up to 16-bit TRACE debug capability. To enable TRACE on the MIPI-60 header (J5), the following resistor modifications must be made. Table 2-12 details what resistors must be removed and populated to enable the correct paths on the EVM.

Table 2-12. AM261-SOM-EVM Resistor Modifications for Trace Debug

Designator	Value (Ω)	Action	AM261x Signal Disabled	Trace Signal Enabled
R149	0	REMOVE	PR0_PRU1_GPIO0	
R150	0	REMOVE	PR0_PRU1_GPIO1	
R151	0	REMOVE	PR0_PRU1_GPIO2	
R152	0	REMOVE	PR0_PRU1_GPIO3	
R153	0	REMOVE	PR0_PRU1_GPIO4	
R154	0	REMOVE	PR0_PRU1_GPIO5	
R155	0	REMOVE	PR0_PRU1_GPIO6	
R156	0	REMOVE	PR0_PRU1_GPIO8	
R159	0	REMOVE	PR0_PRU1_GPIO9	
R161	0	REMOVE	PR0_PRU1_GPIO10	
R163	0	REMOVE	PR0_PRU1_GPIO11	
R164	0	REMOVE	PR0_PRU1_GPIO12	
R167	0	REMOVE	PR0_PRU1_GPIO13	
R169	0	REMOVE	PR0_PRU1_GPIO14	
R170	0	REMOVE	PR0_PRU1_GPIO15	
R171	0	REMOVE	PR0_PRU1_GPIO16	
R172	0	REMOVE	GPIO120	
R173	0	REMOVE	GPIO119	
R86	10	POPULATE		TRC_DATA6
R87	10	POPULATE		TRC_DATA7
R88	10	POPULATE		TRC_DATA8
R89	10	POPULATE		TRC_DATA9
R90	10	POPULATE		TRC_DATA10
R91	10	POPULATE		TRC_DATA11
R92	10	POPULATE		TRC_DATA12
R93	10	POPULATE		TRC_CLK
R94	10	POPULATE		TRC_DATA13
R95	10	POPULATE		TRC_DATA14
R96	0	POPULATE		TRC_CTL
R97	10	POPULATE		TRC_DATA15
R98	10	POPULATE		TRC_DATA0
R99	10	POPULATE		TRC_DATA1
R100	10	POPULATE		TRC_DATA2
R101	10	POPULATE		TRC_DATA3
R102	10	POPULATE		TRC_DATA4
R103	10	POPULATE		TRC_DATA5

Figure 2-20 shows the resistors that are to be removed. Figure 2-21 shows the resistors to populate.

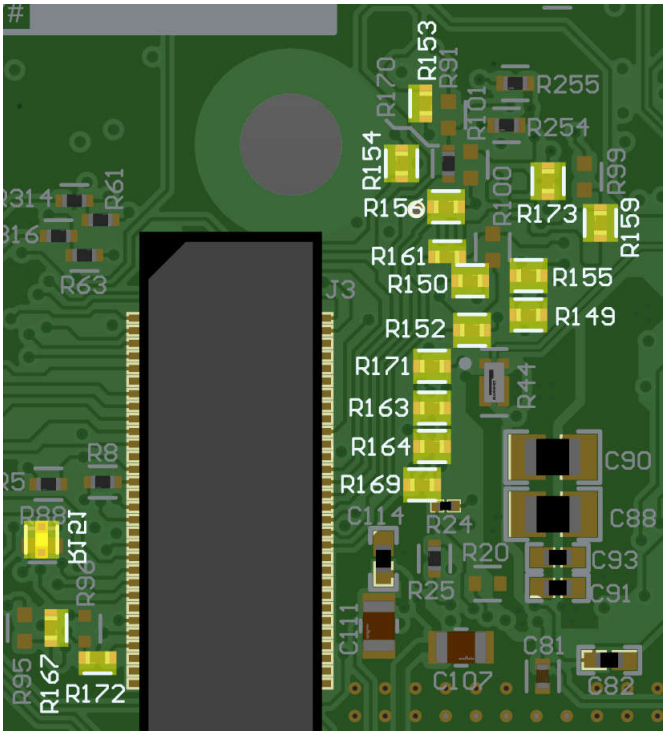

Figure 2-20. Resistors to Remove to enable TRACE

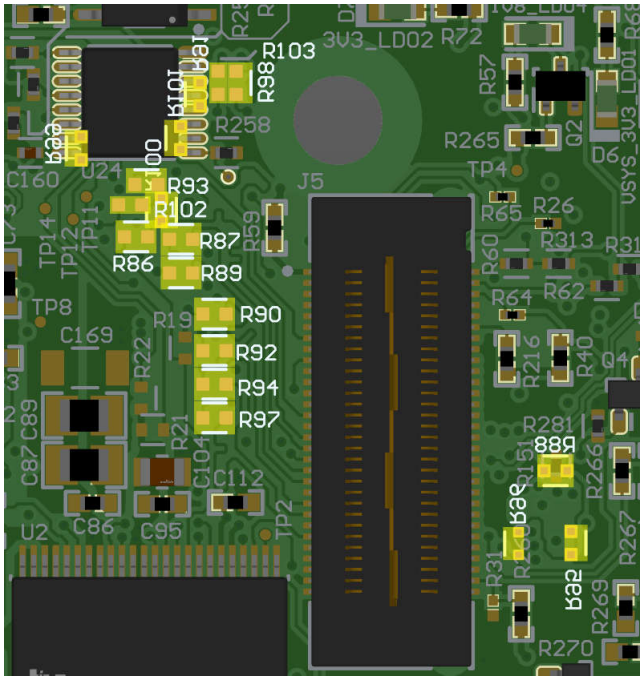

Figure 2-21. Resistors to Populate to enable TRACE

2.9.7 ADC and DAC

The AM261x controlSOM supports 18 ADC signal channels that are mapped from the AM261x SoC and terminated to the SOM HD Connector J1.

The signals with the _P and _N suffix are routed as differential pairs. For ADC0, the pairs are AIN2/AIN3 and AIN4/AIN5. For ADC1 and ADC2, the pairs are AIN0/1 and AIN2/3.

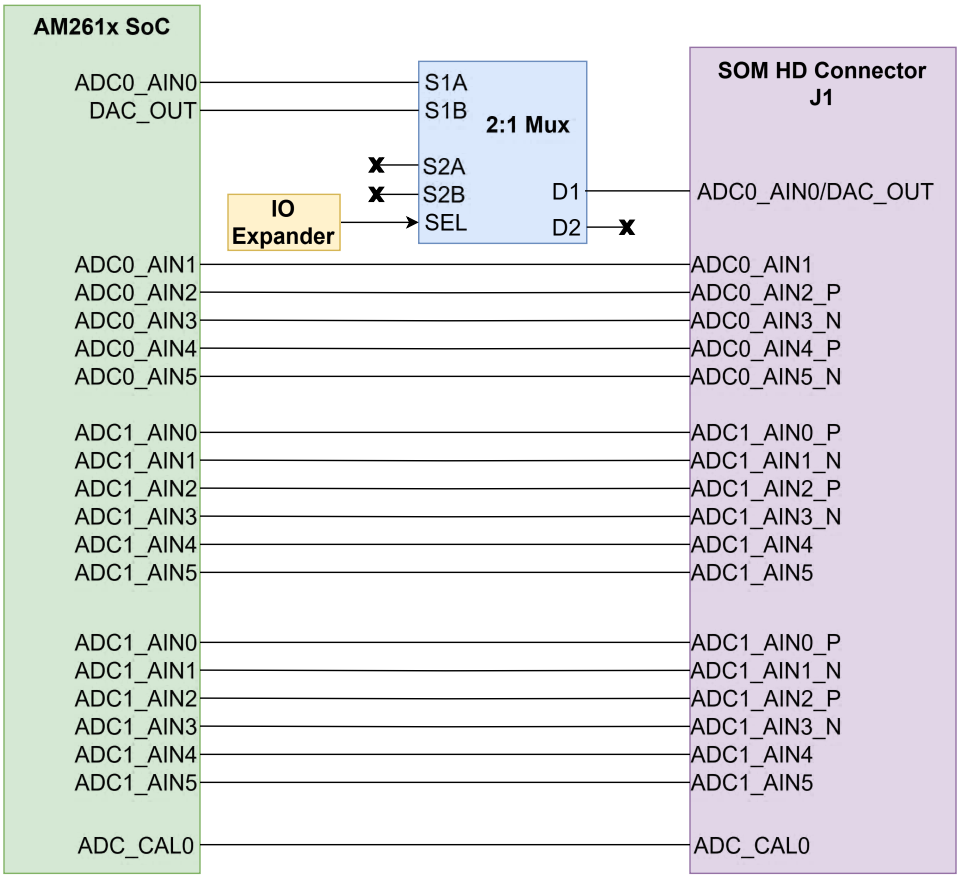

Figure 2-22. ADC SOM Connections

There is one mux (TMUX1136DQAR) that determines the routing of ADC signals to and from the SOM HD Connector.

Table 2-13. ADC MUX Select Logic

MUX Select Signal	Condition	Function	Description
ADC0_AIN0/ DAC_OUT_MUX_SEL	SEL Signal HIGH	S1A → D1	ADC0_AIN0 selected
	SEL Signal LOW	S1B → D1	DAC_OUT selected

ADC Switches

There are three switches that are used to configure the reference voltages for the ADC and DAC. Refer to Figure 2-24 for the on-board switch configuration.

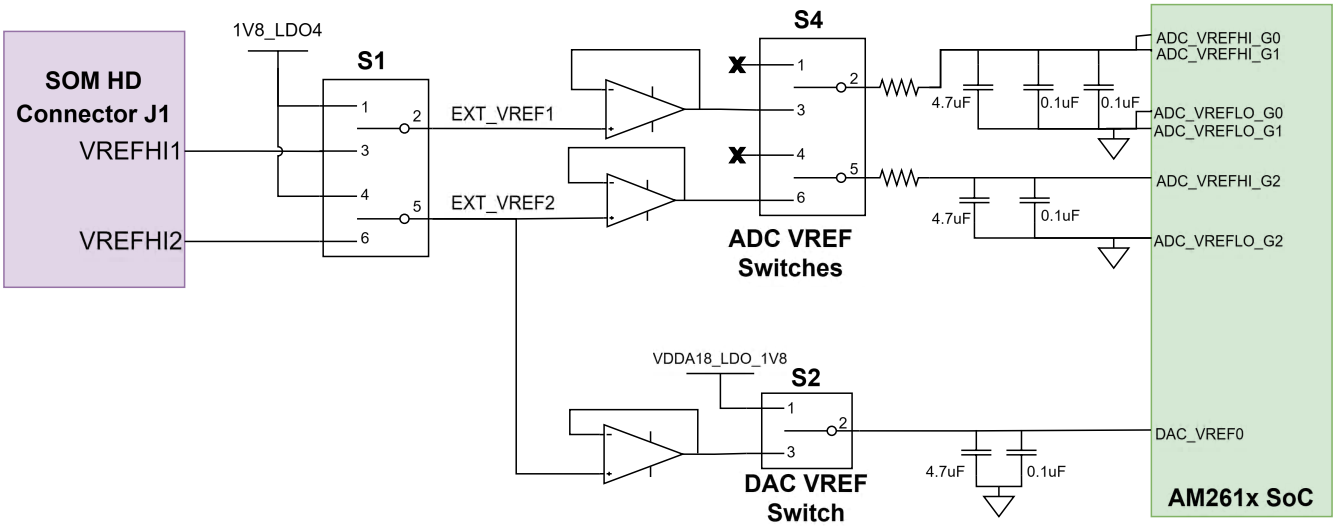

Figure 2-23. ADC Switch Routing

- The VREF Switch (S1) is a single pole double throw switch that controls which 1.8V reference is used for ADC and DAC.

Table 2-14. VREF Switch

VREF Switch Position	Reference Selection
Pin 1-2 (LEFT switch UP)	EXT_VREF1 = PMIC LDO4 1.8V Reference (1V8_LDO4)
Pin 2-3 (LEFT switch DOWN)	EXT_VREF1 = SOM HD Connector VREF
Pin 4-5 (RIGHT switch UP)	EXT_VREF2 = PMIC_LDO4 1.8V Reference (1V8_LDO4)
Pin 5-6 (RIGHT switch DOWN)	EXT_VREF2 = SOM HD Connector VREF

- The DAC VREF Switch (S2) is a single pole double throw switch that controls the input for the DAC VREF inputs of the AM261x SoC.

Table 2-15. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2 (LEFT)	AM261x on-die LDO
Pin 2-3 (RIGHT)	Output of VREF Switch (EXT_VREF2)

- The ADC VREF Switch (S4) contains two single pole double throw switches that control the input for the ADC VREF inputs of the AM263Px SoC.

Note

S4.1 must be in the Pin 1-2 position and S4.2 must be in the pin 4-5 position for AM261x MCU+ SDK ADC Examples to function properly.

Table 2-16. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2 (LEFT switch UP)	OPEN - Allow for reference to be AM261x on-die LDO reference
Pin 2-3 (LEFT switch DOWN)	Output of VREF Switch (EXT_VREF1)
Pin 4-5 (RIGHT switch UP)	OPEN - Allow for reference to be AM261x on-die LDO reference
Pin 5-6 (RIGHT switch DOWN)3	Output of VREF Switch (EXT_VREF2)

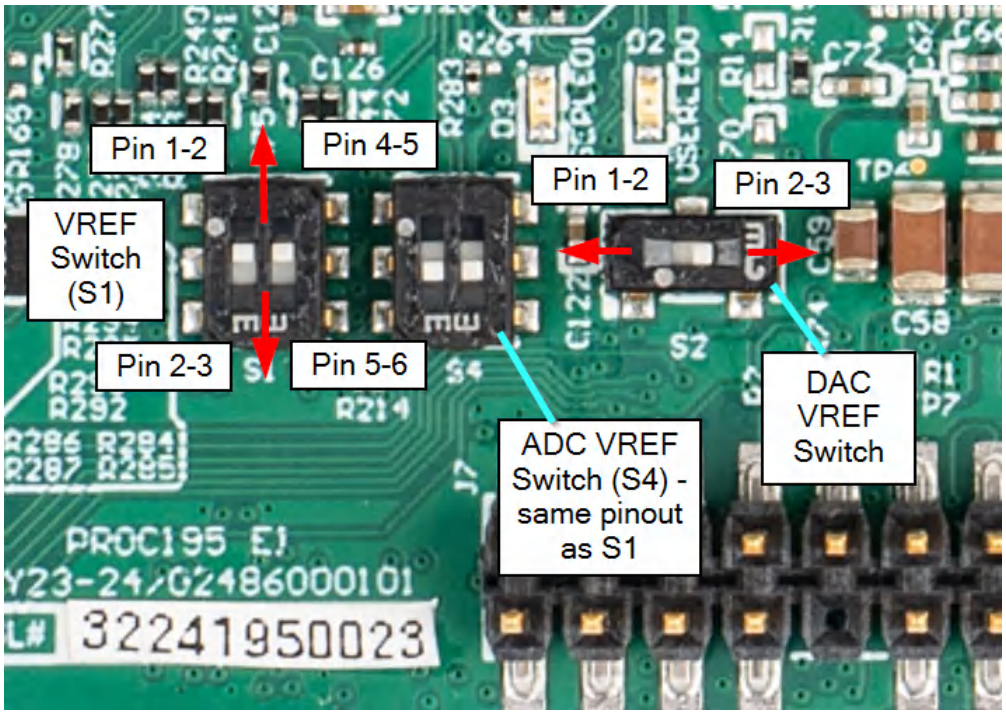

Figure 2-24. ADC, DAC VREF Switch Configuration

2.9.8 Off-SOM Peripherals

There are several AM261x peripherals that cannot be interfaced without additional EVM hardware. This section details each peripheral and specifies the hardware required to connect to the SOM.

2.9.8.1 MCAN

The AM261x controlSOM does not have any onboard MCAN transceiver. To interface with the AM261x MCAN peripheral, the AM261x controlSOM must be connected to the HSEC180ADAPEVM-AM2 and plugged into the TMDSHSECDOCK-AM263. The TMDSHSECDOCK-AM263 has an onboard 2-channel MCAN transceiver.

Two instances of MCAN are MCAN0 and MCAN1, which are routed to the SOM HD Connectors for interfacing using the HSEC180ADAPEVM-AM2 and TMDSHSECDOCK-AM263 or compatible base board. Both MCAN peripherals can be accessed through the 2-channel MCAN transceiver on the TMDSHSECDOCK-AM263.

There is a single 1:2 Mux that controls the routing of the MCAN1_RX signal, which is muxed with I2C1_SCL. Figure 2-25 shows the MCAN peripheral routing on the AM261x controlSOM.

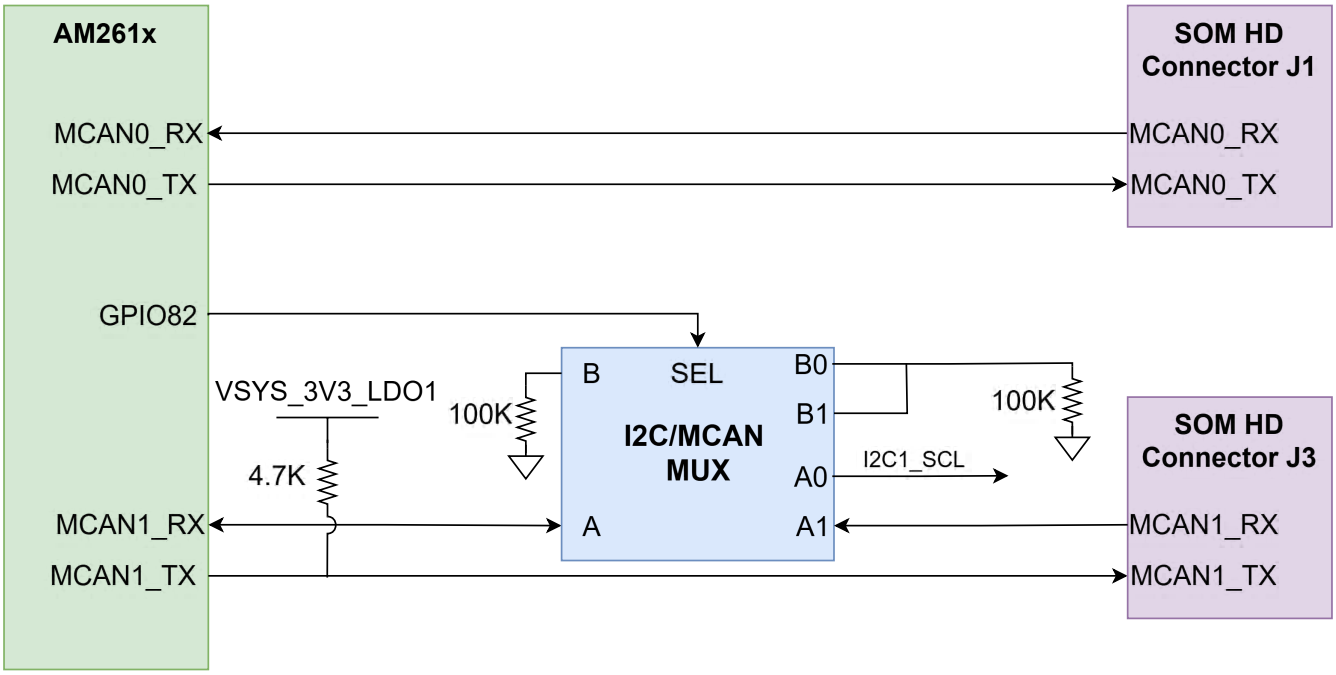

Figure 2-25. MCAN

2.9.8.2 LIN

The AM261x controlSOM does not have an onboard LIN transceiver. To interface with the AM261x LIN peripheral, the AM261x controlSOM must be connected to the HSEC180ADAPEVM-AM2 and plugged into the TMDSHSECDOCK-AM263. The TMDSHSECDOCK-AM263 has an onboard 2-channel LIN transceiver.

One instance of LIN is that LIN1 is routed to the SOM HD Connectors for interfacing using the HSEC180ADAPEVM-AM2 and TMDSHSECDOCK-AM263 or a compatible baseboard. The LIN1 peripheral can be accessed through one channel of the 2-channel LIN transceiver on the TMDSHSECDOCK-AM263.

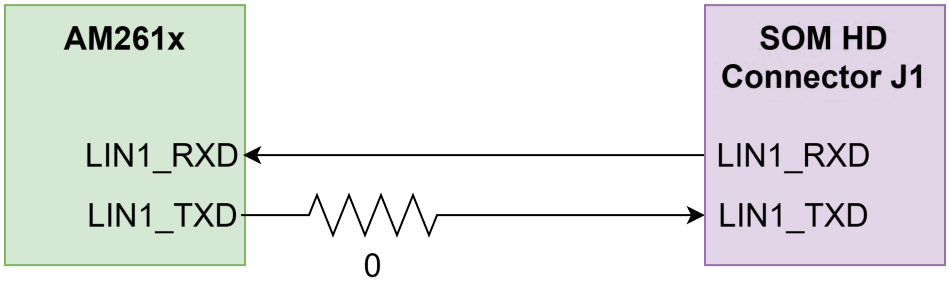

Figure 2-26. LIN

2.9.8.3 FSI

The AM261x controlSOM supports a fast serial interface by terminating the SoC signals SOM HD Connector J1. The HSEC180ADAPEVM-AM2 has a 10 pin header for interfacing with the FSI peripheral.

The interface has two lines of data and a clock line for both the receive and transmit signals.

The FSI TX signals go through a 4-bit 1:2 signal routing mux. There is a pull-down resistor on the select line of the mux, which does not route FSI as the default selection. To use FSI, the SPI0/FSITX0_MUX_SEL GPIO from the IO expander must be configured as a logic high output. In addition, the FSI RX signals go through a separate 4-bit 1:2 signal routing mux. There is a pull-down resistor on the select line of the mux, which does not route FSI as the default selection. To use FSI, the PMIC_SPI1/FSIRX0_MUX_SEL GPIO from the IO expander must also be configured as a logic high output.

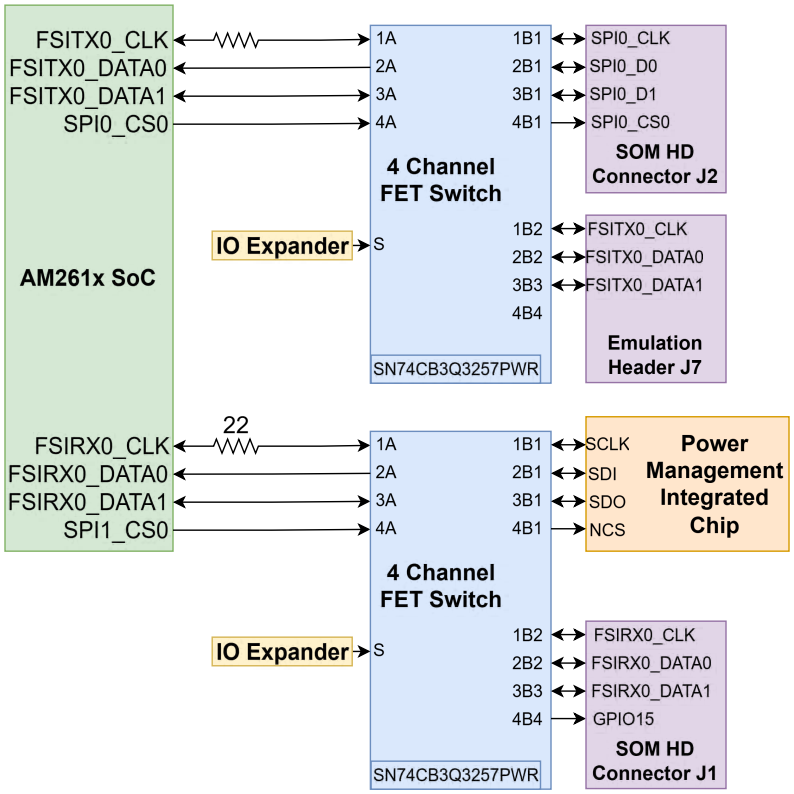

Figure 2-27. FSI

2.9.8.4 USB

The AM261x SoC has one USB 2.0 peripheral that is routed to SOM HD Connector J2. To access the USB peripheral, the HSEC180ADAPEVM-AM2 must be connected to the AM261x controlSOM. The HSEC180ADAPEVM-AM2 has an on-board USB interface for interfacing in host mode or peripheral mode.

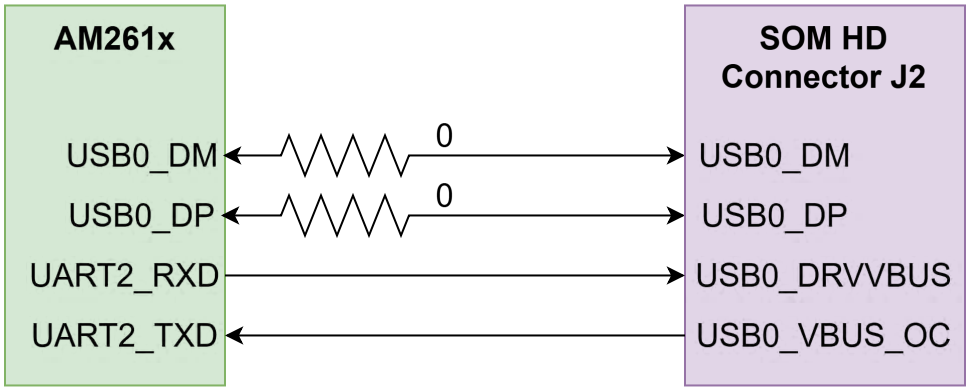

Figure 2-28. USB

2.9.8.5 Ethernet

The AM261x SoC has the necessary signals pinned out to the SOM HD Connectors to support up to 3 external Ethernet ports. The Ethernet interfaces can be accessed using the HSEC180ADAPEVM-AM2 SOM to HSEC adapter board. See the HSEC180ADAPEVM-AM2 User's Guide for more details.

2.9.8.5.1 RGMII

The AM261x controlSOM uses one port of RGMII signals to be connected to SOM HD Connector J2. When using the AM261x controlSOM with the HSEC180ADAPEVM-AM2, the RGMII signals are connected to a 48-pin Ethernet PHY (DP83869), which is configured to advertise 1Gb operation. See the HSEC180ADAPEVM-AM2 User's Guide for more information.

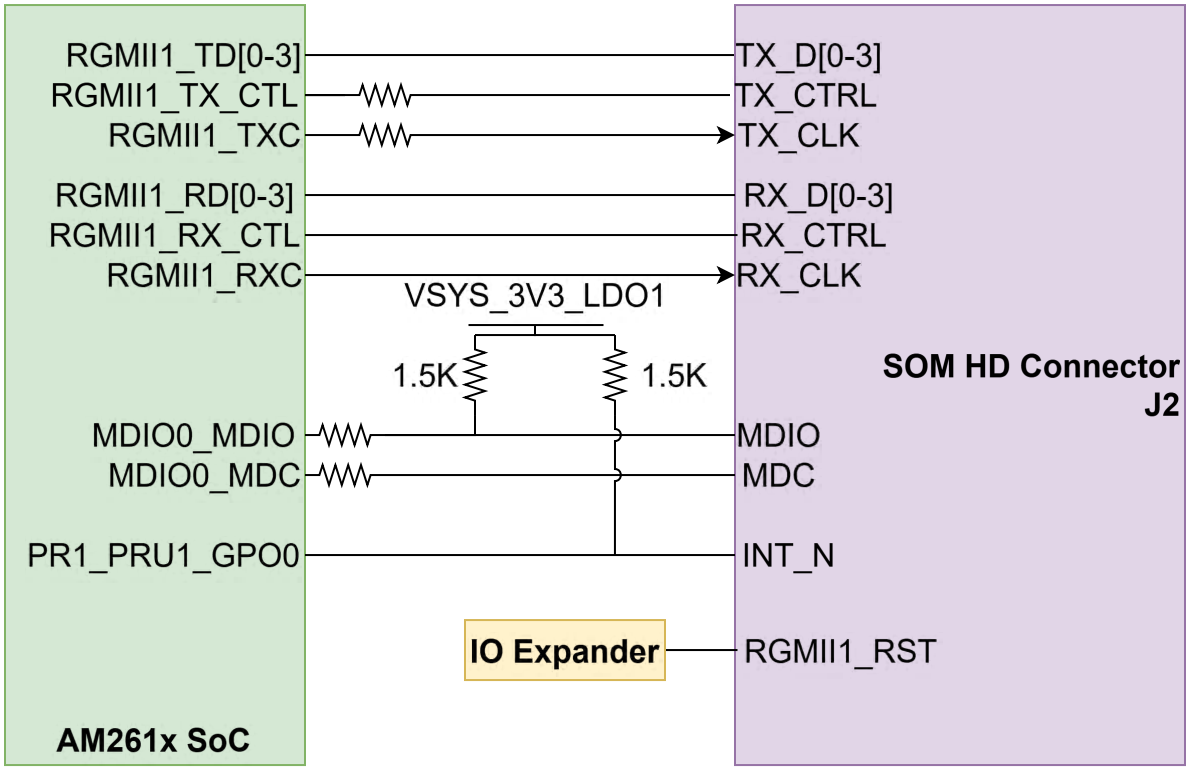

Figure 2-29. RGMII

2.9.8.5.2 PRU-ICSS

The AM261x controlSOM makes use of two (out of the four) on-die programmable real-time unit and industrial communication subsystems (PRU-ICSS) of the AM261x SoC to interface with up to two Ethernet® ports. When using the AM261x controlSOM with the HSEC180ADAPEVM-AM2, the PR0_PRU0 signals are connected to a Gigabit Ethernet PHY transceiver (DP83869), and the PR0_PRU1 signals are connected to a 48-pin Ethernet Add-on Board Connector. The Ethernet Add-on Board connector allows Ethernet PHY PCBs from the TI Ethernet Add-on Board Ecosystem to be connected to the HSEC180ADAPEVM-AM2 and interfaced with using the AM261x controlSOM. For more information, see the AM261x SOM to HSEC Adapter Board User's Guide.

Signals from the PRU-ICSS PR0 core are connected to SOM HD Connector J3.

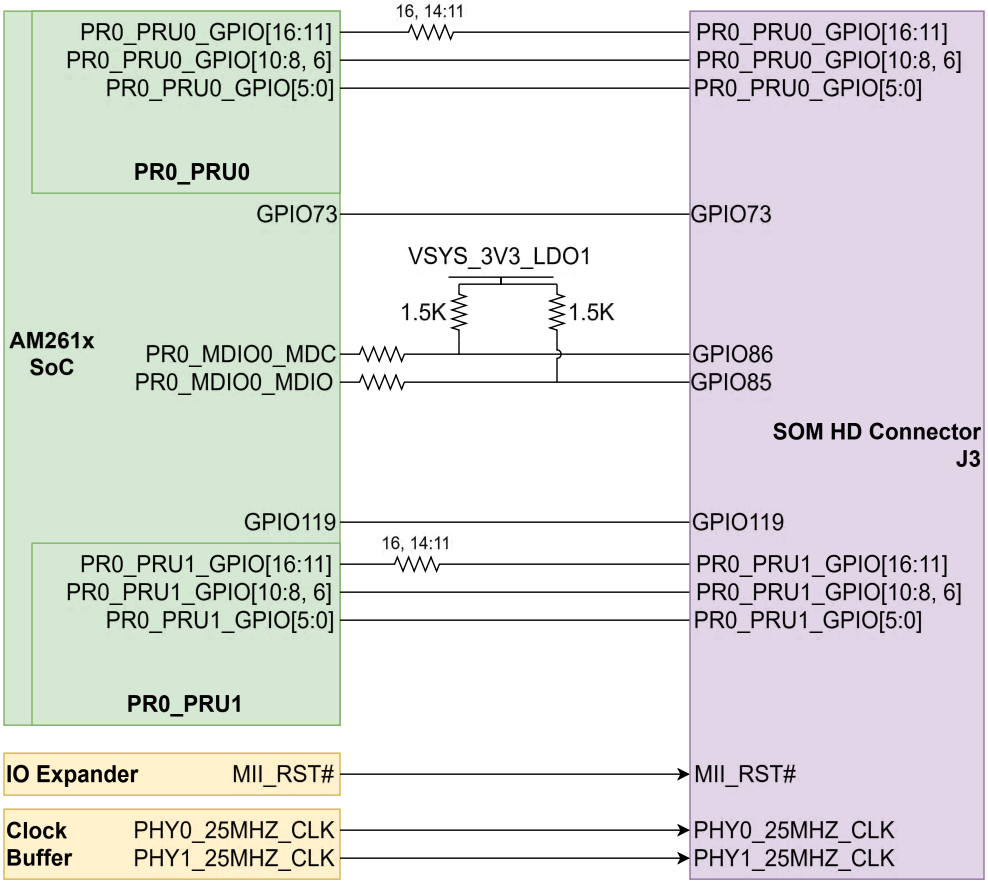

Figure 2-30. PRU-ICSS

Note

The PRU-ICSS and AM261x GPIO signal mapping to MII Ethernet is given in Table 2-17 below. See the HSEC180ADAPEVM-AM2 User's Guide for more information and implementation details.

Table 2-17. AM261x controlSOM PRU-ICSS to MII Signal Mapping

MII Port	AM261x controlSOM Signal	MII Ethernet Mapping
MII0	PR0_PRU0_GPIO0	RXD0
	PR0_PRU0_GPIO1	RXD1
	PR0_PRU0_GPIO2	RXD2
	PR0_PRU0_GPIO3	RXD3
	PR0_PRU0_GPIO4	RX_DV
	PR0_PRU0_GPIO5	RX_ER
	PR0_PRU0_GPIO6	RX_CLK
	PR0_PRU0_GPIO8	RX_LINK
	PR0_PRU0_GPIO9	COL
	PR0_PRU0_GPIO10	CRS
	PR0_PRU0_GPIO11	TXD0
	PR0_PRU0_GPIO12	TXD1
	PR0_PRU0_GPIO13	TXD2
	PR0_PRU0_GPIO14	TXD3
	PR0_PRU0_GPIO15	TX_EN
	PR0_PRU0_GPIO16	TX_CLK
	GPIO73	INTn
MII0/MII1	GPIO85	MDIO0_MDIO
	GPIO86	MDIO0_MDC
	MII_RST# (IO Expander)	RESET
MII1	PR0_PRU1_GPIO0	RXD0
	PR0_PRU1_GPIO1	RXD1
	PR0_PRU1_GPIO2	RXD2
	PR0_PRU1_GPIO3	RXD3
	PR0_PRU1_GPIO4	RX_DV
	PR0_PRU1_GPIO5	RX_ER
	PR0_PRU1_GPIO6	RX_CLK
	PR0_PRU1_GPIO8	RX_LINK
	PR0_PRU1_GPIO9	COL
	PR0_PRU1_GPIO10	CRS
	PR0_PRU1_GPIO11	TXD0
	PR0_PRU1_GPIO12	TXD1
	PR0_PRU1_GPIO13	TXD2
	PR0_PRU1_GPIO14	TXD3
	PR0_PRU1_GPIO15	TX_EN
	PR0_PRU1_GPIO16	TX_CLK
	GPIO119	INTn

2.10 Test Points

The AM261x controlSOM includes multiple test points to aid in hardware debug. Table 2-18 includes a list of the test points available on the controlSOM.

Table 2-18. AM261-SOM-EVM Test Points

Test Point Designator	Test Point Net Name	Description
TP1	VPP_1V8	AM261x VPP supply from VDDA18_LDO_1V8 (internally generated analog 1.8V)
TP2	COMP2_OUT	PMIC comparator 2 output
TP3	VMAIN_5V0	SOM system 5V input
TP4	1V8_LDO4	PMIC LDO4 1.8V output
TP5	COMP1_OUT	PMIC comparator 1 output
TP6	VMAIN_12V0	U22 boost converter 12V output
TP7	3V3_LDO2	PMIC LDO2 3.3V output. Secondary 3.3V I/O system voltage
TP8	VCC_6V0	PMIC buck-boost 6V output. Input to 1.2V core voltage regulator (U3)
TP9	5V0_LDO3	PMIC LDO3 5V output
TP10	VSYS_3V3_LDO1	PMIC LDO1 3.3V output. Primary 3.3V I/O system voltage.
TP11	PMIC_SPI1_CLK	PMIC SPI clock
TP12	PMIC_SPI1_D0	PMIC SPI Data 0
TP13	VREG_1P8_OUT	PMIC 1.8V internal analog/digital supply
TP14	PMIC_SPI1_CS0	PMIC SPI chip select
TP15	VREG_OUT	PMIC gate-drive supply for the buck-boost regulator
TP16	VCC_1V2	1.2V AM261x core voltage supply
TP17	VDD_IO_3V3	3.3V AM261x I/O voltage supply
TP18	MCU_PORz	AM261x power-on-reset
TP19	VDDA18_LDO_1V8	AM261x internal analog LDO 1.8V output
TP20	VDDS18_LDO_1V8	AM261x internal digital LDO 1.8V output
TP21	GND	GND
TP22	+1V2	U3 buck converter 1.2V output
TP23	MCU_RESETn	AM261x warm reset

2.11 Best Practices

Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to electrostatic discharge (ESD). TI recommends this product be used in ESD controlled environment. This includes a temperature or humidity controlled environment to limit the buildup of ESD. TI recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

Assumed Operating Conditions

This kit is assumed to run at standard room conditions. Standard ambient temperature and pressure (SATP) with moderate-to-low humidity is assumed.

3 Software

The AM261x MCU+ Software Development Kit (MCU-PLUS-SDK-AM261X) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations. This software accelerates application development schedules by eliminating creating basic system software functions from scratch.

The AM261x MCU+ Academy provides a Getting Started Guide for first-time software development using the AM261-SOM-EVM. Follow the steps in this guide to begin development.

4 Hardware Design Files

The AM261-SOM-EVM hardware design files can be downloaded from the EVM Tool Page, or by clicking this link.

5 Additional Information

5.1 Trademarks

Sitara™ and Code Composer Studio™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
USB Type-C® is a registered trademark of USB Implementers Forum.
Ethernet® is a registered trademark of Xerox Corporation .
All trademarks are the property of their respective owners.

6 References

In addition to this document, the following references are available at TI.com.

- Texas Instruments, AM2612 Microcontroller, webpage
- Texas Instruments, AM261x Sitara™ Microcontrollers, data sheet
- Texas Instruments, AM261x Technical Reference Manual
- Texas Instruments, AM261x Register Addendum, technical reference manual
- Texas Instruments, XDS110ISO-EVM, webpage
- Texas Instruments, TMDSHSECDOCK, webpage
- Texas Instruments, TMDSHSECDOCK-AM263, webpage

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265