EVM User's Guide: TPSM65630SEVM

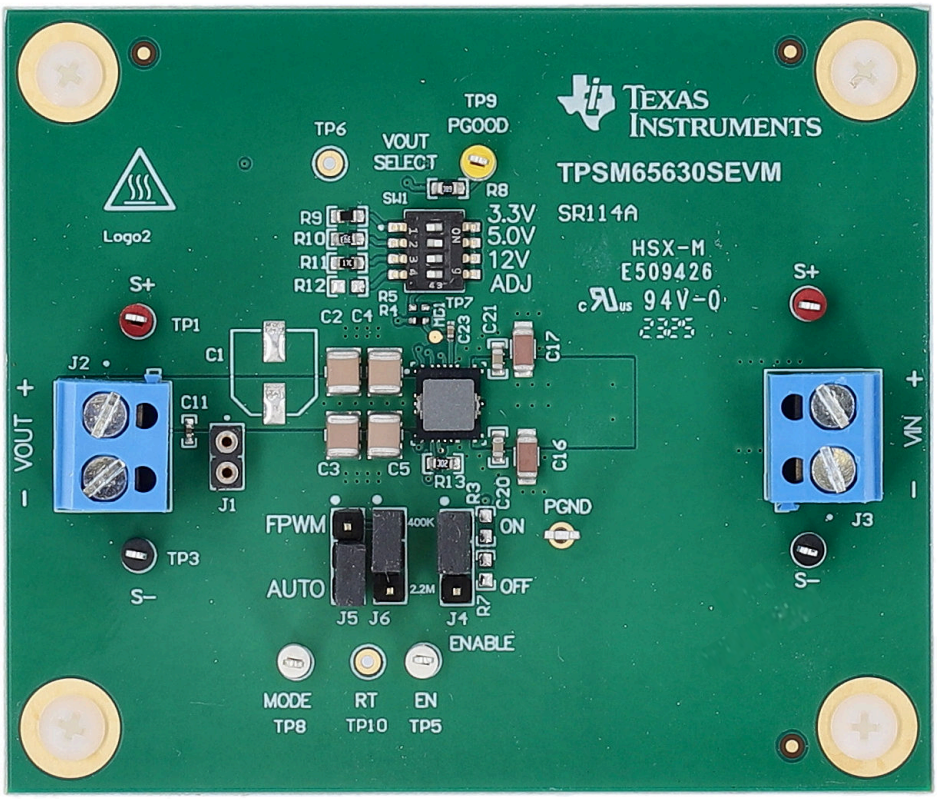
TPSM65630SEVM Evaluation Module

Description

The Texas Instruments TPSM65630SEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPSM65630 family of wide input voltage buck modules. The TPSM65630 family are easy to use, synchronous, step-down modules capable of supplying up to 1A, 2A, or 3A of load current from an input voltage as high as 65V.

Features

- 3V to 65V wide input voltage range
- Fixed 3.3V, 5V, and adjustable output voltage options
- Up to 3A output current
- 300kHz to 2.2MHz switching frequency
- Minimized switch node ringing to reduce Electromagnetic Interference (EMI)
- Input transient capability up to 70V



TPSM65630SEVM

1 Evaluation Module Overview

1.1 Introduction

The TPSM65630SEVM is configured to deliver optional 3.3V, 5V, 12V, or 24V output to a load up to 3A. The TPSM65630SEVM can be used in many different configurations by substituting other versions of the TPSM656x5 and re-configuring the board components. See Section 1.4 for more details.

1.2 Kit Contents

This kit includes one TPSM65630SEVM.

1.3 Specification

Performance characteristics for the TPSM65630SEVM are found in Section 3.2.

Unless otherwise stated: V_{IN} = 24V, V_{OUT} = 5V, T_A = 25ºC.

1.4 Device Information

The default EVM features the TPSM65630. Table 1-1 provides a list of additional devices that can be used with the TPSM65630SEVM. Appropriate passive component changes must be made to use these devices in the EVM.

Table 1-1. TPSM65630SEVM Device Options

Device OPN	Output Current	Spread Spectrum
TPSM65630SVCGR	3A	Y
TPSM65630VCGR	3A	N
TPSM65620SVCGR	2A	Y
TPSM65610SVCGR	1A	Y

General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within the recommended electrical rated voltage and power limits. Always use electrical safety precautions to verify that your personal safety and those working around you. For further information, contact TI's Product Information Center http://ti.com/customer support.

Save all warnings and instructions for future reference.

WARNING
Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, then immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, a good engineering practice is to assume that the entire EVM can have fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

   WARNING
   While the EVM is energized, never touch the EVM or the electrical circuits, as the EVM or the electrical circuits can be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment, for example, latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

2 Hardware

2.1 Additional Images

Figure 2-1 and Figure 2-2 show the front and back of the TPSM65630SEVM respectively.

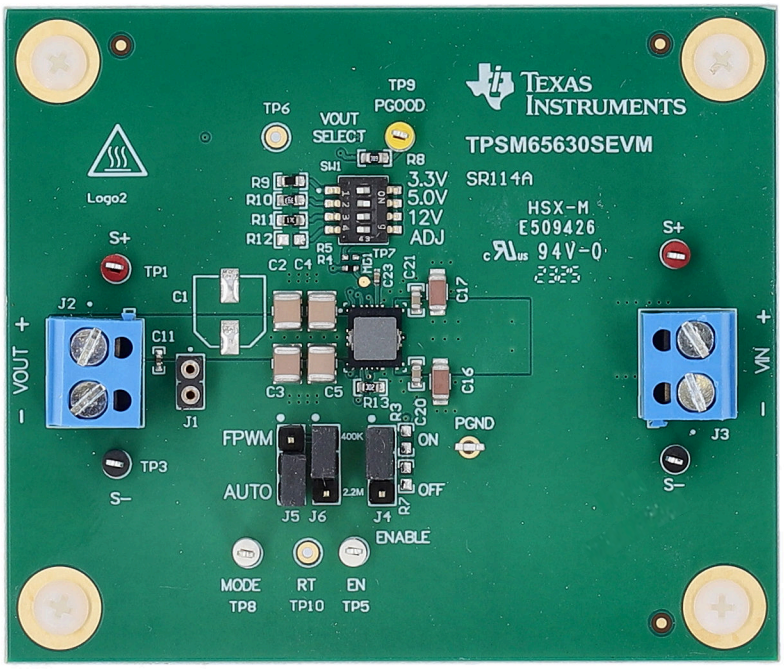


Figure 2-1. TPSM65630SEVM Top Side

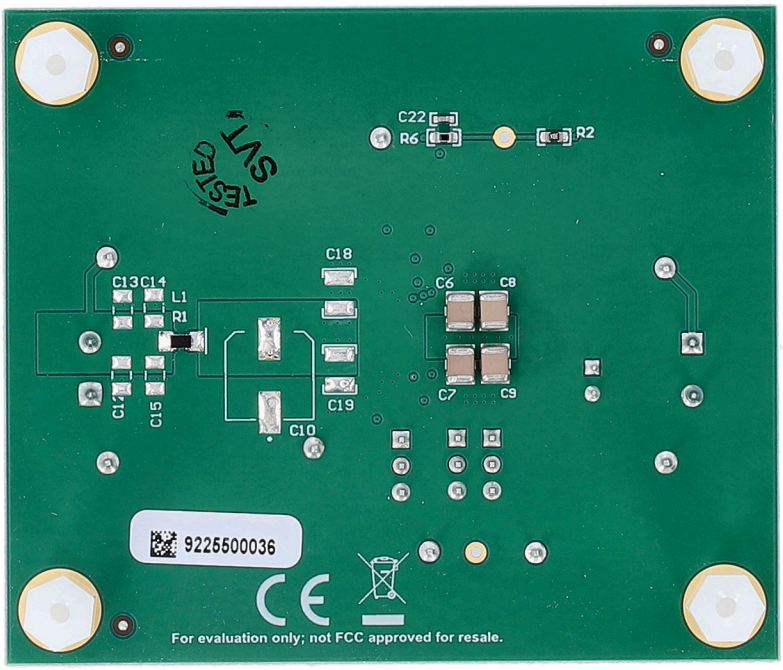


Figure 2-2. TPSM65630SEVM Bottom Side

2.2 Power Requirements

Any power source in the range of 6V to 65V, and capable of delivering 3A, can be used to evaluate the TPSM65630SEVM, under normal conditions.

2.3 Setup and Operation

This section describes the connectors, test points, and jumpers on the EVM and how to properly connect, set up, and use the TPSM65630SEVM. See Figure 2-3 for location of connectors and jumpers and typical setup. See Figure 2-4 for bode plot connections.

Note that the EMI filter is not populated on this EVM. To evaluate the EMI filter, components L1, C6 must be populated, while R2 must be removed. Typical values for these components are given in Table 4-1.

Signal	Connector and Test Points	Description
VIN	J3, TP2, TP4	The terminal block J3 is used as the input of the module. Apply input voltage to this module. TP2 (S+) is used as the positive DMM connection for input voltage sense. TP4 (S–) is used as the negative DMM connection for input voltage sense.
VOUT	J2, TP1, TP3	The terminal block J2 is used as the output of the module. Connect the output load to this block. TP1 (S+) is used as the positive DMM connection for VIN sensing. TP3 (S–) is used as the negative DMM connection for VOUT sensing.
GND	TP11	Ground of the converter. TP111 can be used as any ground connector as needed.
EN	J4, TP5	The EN jumper (J5) is used to enable or disable the EVM. To use the external UVLO feature, populate R3 and R7 and remove the EN jumper shunt. Note that for accurate shutdown quiescent current measurement, these resistors must be removed (if used) and the EN jumper shunt moved to OFF.
MODE	J5, TP8	The MODE jumper (J5) is used to select the operating mode . With MODE in the AUTO position, the device operates in automatic PFM/FPWM mode depending on load current. With the MODE in the FPWM position, the device operates at fixed frequency under all load conditions. The MODE pin is also the frequency synchronization input. To synchronize the device to an external clock, remove the MODE jumper shunt and apply the clock to the MODE test point (TP8) or J5_pin_2.
RT	J6, TP10	The RT jumper (J6) is used to select the switching frequency. The default setting on the EVM is designed for 400kHz. To adjust the switching frequency, remove the RT jumper shunt and populate R11 with the desired value. See the data sheet for frequency vs RT resistor value.
PGOOD	TP9	The PGOOD test point (TP9) is used to monitor the power-good indicator. This flag indicates whether the output voltage has reached the regulation level. PGOOD is an open-drain output that is tied to VOUT through a 49.9kΩ resistor (R8) on the EVM.
FB Connections	SW1	The Dip Switch (SW1) is used to choose the EVM output voltage setting. In the factory default configuration, the EVM takes an external adjustable setting for 5V output. To switch to a different output voltage like 3.3V, 12V or 24V, set the corresponding SW1 switch to ON, and all other channels must be OFF. To change the onboard adjustable output voltage setting to a different value not among the preset voltage lis, suggest to use the ADJ channel switch of SW1, and replace R12 by referring to the TPSM656x0 data sheet feedback resistor selection equation. To set the EVM for fixed 5V output, put all switche channels of SW1 to OFF, depoluate R6, but populate R5. To set the EVM for fixed 3.3V output, suggest to use ADJ channel by putting the switch to ON, and all other channels of SW OFF. Then depoluate R5, R6, but replace R12 with a 0 Ohm resistor.
BIAS	TP7	The BIAS pin (TP7) acts as an auxiliary input to the internal LDO regulator. C23 helps bypassing the switching noise. In the EVM factory default configuration, BIAS is connected to VCC through R4. To change the LDO input to an available external supply from 3.3V to 30V, depopulate R4, and connect this pin to the external supply directly. If configure for fixed 3.3V or 5V output, R4 should be installed to close the control loop. See the TPSM65630 datasheet for details.
Loop response plot	TP1, TP3, TP6	When using the adjustable output voltage mode, a Bode plot measurement can be taken using the connection shown in Figure 2-4. R2 must be populated for this test, and probes must have a ground connection to TP3. In the fixed 3.3V or 5V output voltage configuration, a Bode plot measurment can not be taken. It is suggested to run a step load response to evaluate the loop stability.

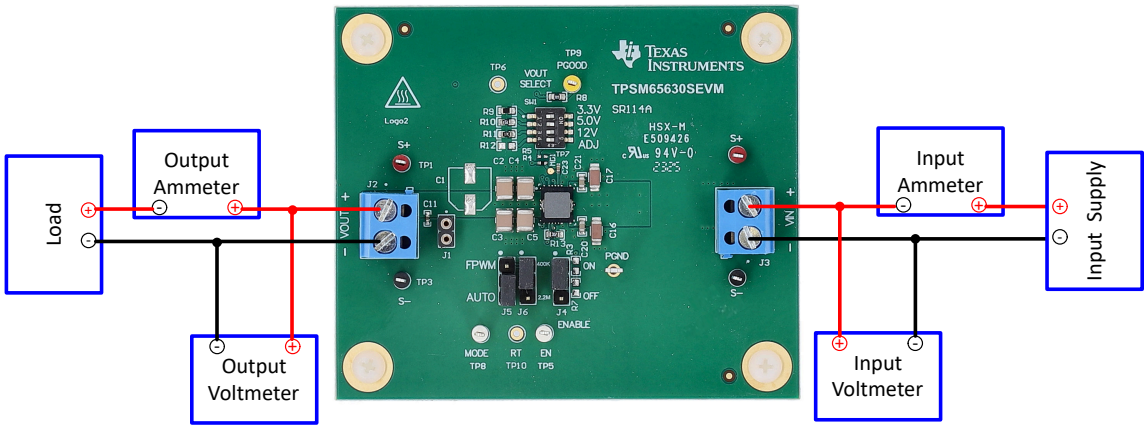


Figure 2-3. TPSM65630SEVM Setup

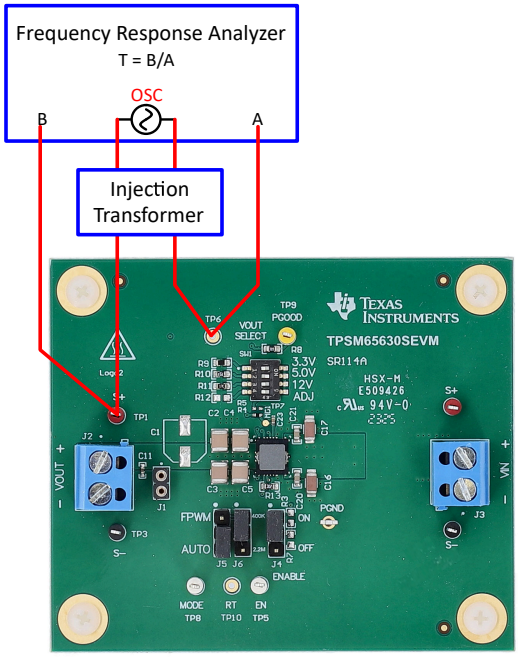


Figure 2-4. TPSM65630SEVM Bode Connections

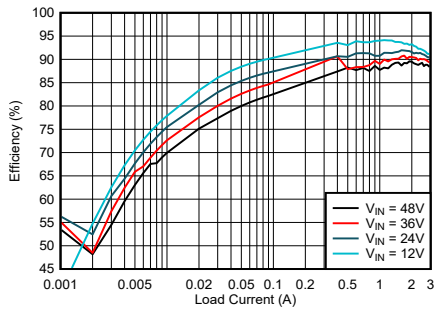
3 Implementation Results

3.1 Evaluation Setup

The LM65645VM was used to take the following data with the setup shown in Figure 2-3.

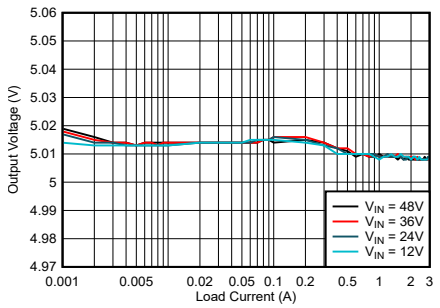
3.2 Performance Data and Results

Unless otherwise specified the following condition apply: T_A = 25ºC, V_{IN} = 24V, 400kHz.



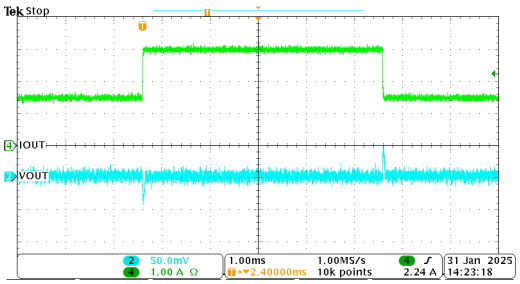
V_{OUT} = 5V 400kHz, AUTO

Figure 3-1. Efficiency



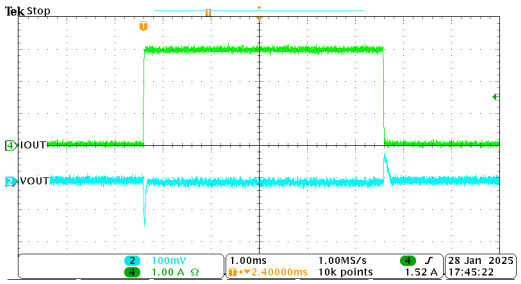
V_{OUT} = 5V 400kHz, AUTO

Figure 3-2. Line and Load Regulation



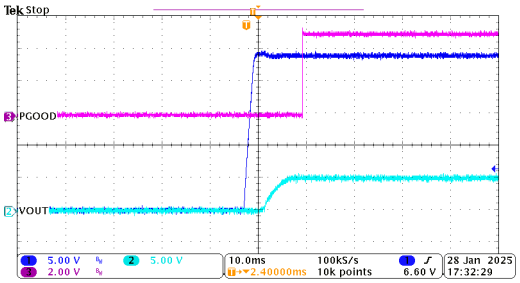
I_{OUT} = 0A to 3A V_{IN} = 24V AUTO V_{OUT} = 5V

Figure 3-3. Load Transient (50% to 100%)



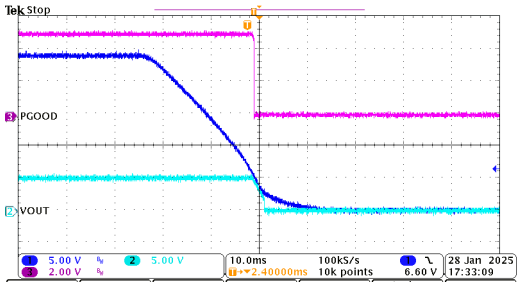
I_{OUT} = 40mA to 3A V_{IN} = 24V AUTO V_{OUT} = 5V

Figure 3-4. Load Transient (0% to 100%)



I_{OUT} = 3A V_{IN} = 24V AUTO V_{OUT} = 5V

Figure 3-5. Start-Up



I_{OUT} = 3A V_{IN} = 24V AUTO V_{OUT} = 5V

Figure 3-6. Shutdown

4 Hardware Design Files

4.1 Schematics

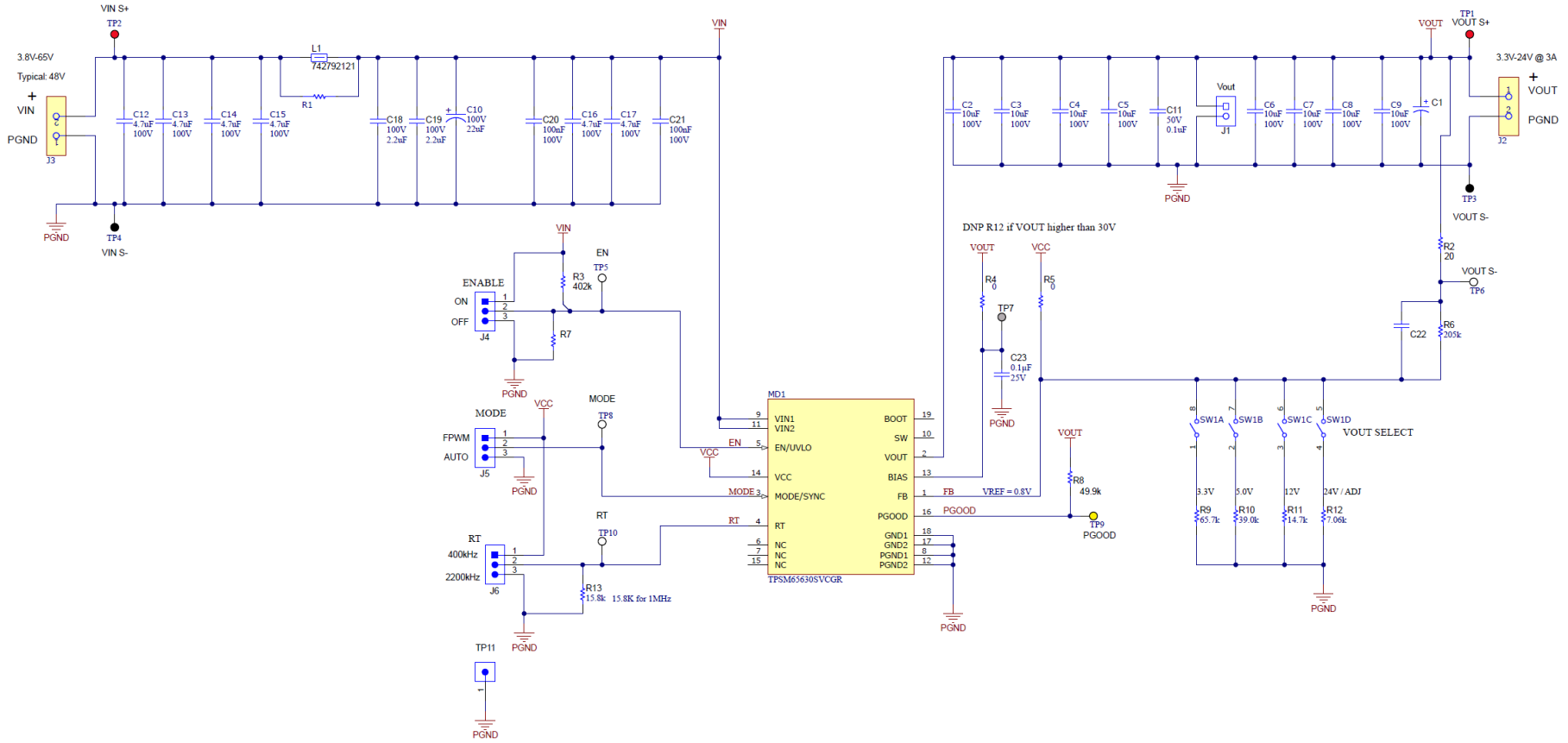


Figure 4-1. TPSM65630SEVM Schematic

4.2 PCB Layouts

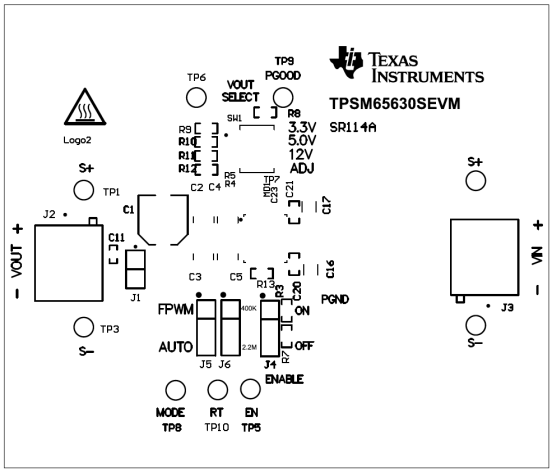


Figure 4-2. PCB Top Silkcreen

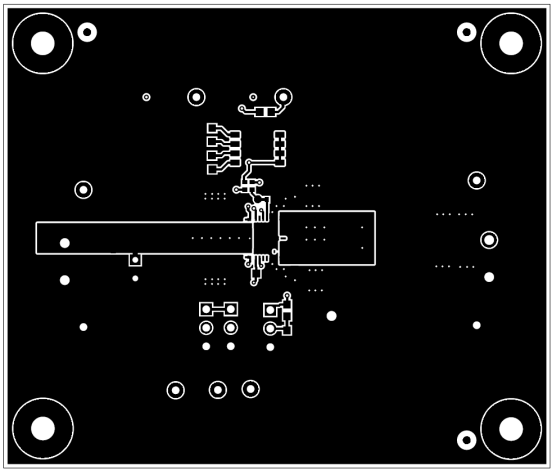


Figure 4-3. PCB Top Layer

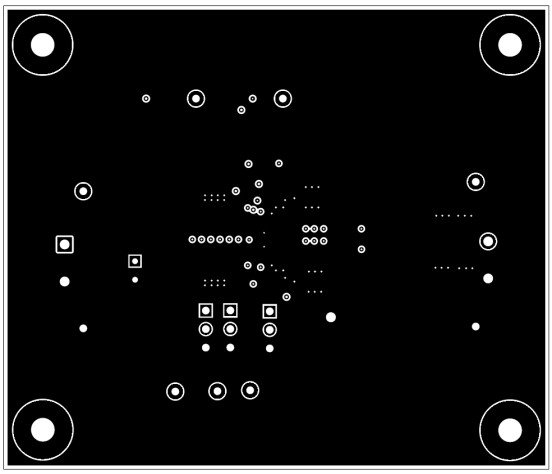


Figure 4-4. PCB Signal Layer 1

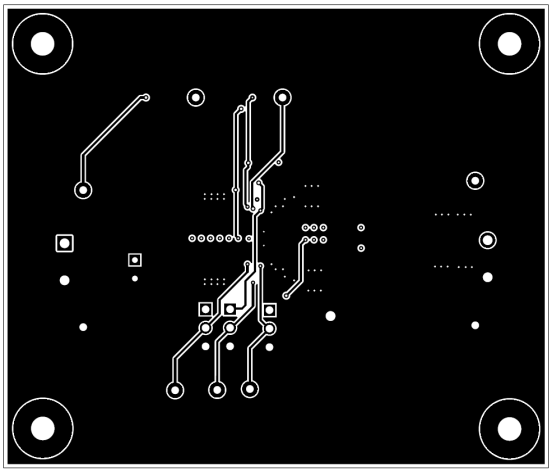


Figure 4-5. PCB Signal Layer 2

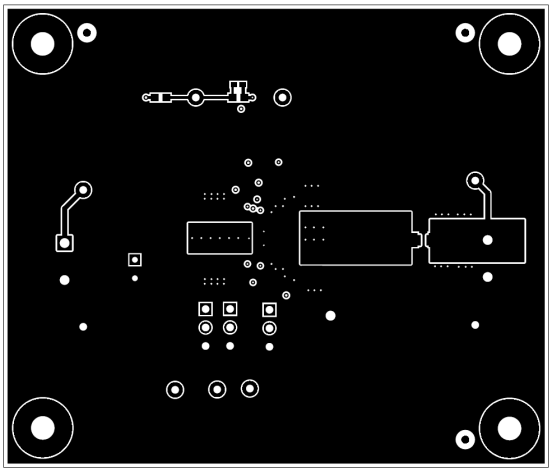


Figure 4-6. PCB Bottom Layer

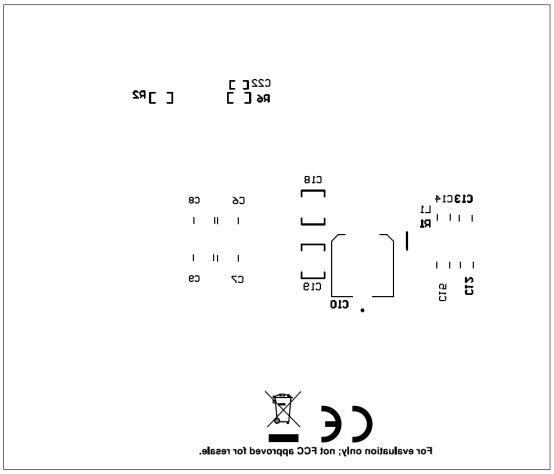


Figure 4-7. PCB Bottom Silkcreen

4.3 Bill of Materials (BOM)

Table 4-1. TPSM65630SEVM BOM (With Options)

REF DES	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C2, C3, C4, C5, C6, C7, C8, C9	8	10µF	10µF ±10% 100V Ceramic Capacitor X7R 1210 (3225 Metric)	GMC32X7R106K100NT	Cal-Chip Electronics
C11	1	0.1µF	CAP, CERM, 0.1µF, 50V, ±10%, X7R, 0402	C1005X7R1H104K050BB	TDK
C16, C17	2	4.7µF	4.7µF ±10% 100V Ceramic Capacitor X7S 1206 (3216 Metric)	C3216X7R2A475K160AC	TDK
C20, C21	2	0.1µF	CAP, CERM, 0.1µF, 100V, ±10%, X7R, AEC-Q200 Grade 1, 0603	HMK107B7104KAHT	Taiyo Yuden
C22	1	47pF	CAP, CERM, 47pF, 50V, ±5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H470J050BA	TDK
C23	1	0.1µF	CAP, CERM, 0.1µF, 25V, ±10%, X8L, AEC-Q200 Grade 0, 0402	GCM155L81E104KE02D	MuRata
J1	1		Socket Strip, 2x1, 100mil, Black, Tin, TH	310-43-102-41-001000	Mill-Max
J2, J3	2		2 Position Wire to Board Terminal Block Horizontal with Board 0.200" (5.08mm) Through Hole	OSTTA024163	On Shore Technology
J4, J5, J6	3		Header, 100mil, 3x1, Tin, TH	PEC03SAAN	Sullins Connector Solutions
MD1	1		High-Density, 3V to 65V Input, 0.8V to 24V Output, 3A Synchronous Buck DC/DC Power Module With Enhanced HotRod™ QFN Package	TPSM65630SVCGR	Texas Instruments
R1	1	0	0 Ohms Jumper 0.245W Chip Resistor 0805 (2012 Metric) - Metal Element	JR0805X35E	Ohmite
R2	1	20	RES, 20, 5%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060320R0JNEA	Vishay-Dale
R4	1	0	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America
R6	1	205k	RES, 205k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603205KFKEA	Vishay-Dale
R8	1	49.9k	RES, 49.9k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060349K9FKEA	Vishay-Dale
R9	1	65.7k	RES, 65.7k, 0.5%, 0.1 W, 0603	RT0603DRE0765K7L	Yageo America
R10	1	39.0k	RES, 39.0k, 1%, 0.1W, 0603	RC0603FR-0739KL	Yageo
R11	1	14.7k	RES, 14.7k, 1%, 0.1W, 0603	RC0603FR-0714K7L	Yageo
R13	1	15.8k	RES, 15.8k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW060315K8FKEA	Vishay-Dale
SW1	1		Dip Switch SPST 4 Position Surface Mount Slide (Standard) Actuator 25mA 24VDC	97C04ST	Samtec
TP1, TP2	2		Test Point, Miniature, Red, TH	5000	Keystone Electronics
TP3, TP4	2		Test Point, Miniature, Black, TH	5001	Keystone Electronics
TP5, TP8	2		Test Point, Miniature, White, TH	5002	Keystone Electronics
TP9	1		Test Point, Miniature, Yellow, TH	5004	Keystone
TP11	1		TEST POINT SLOTTED .118", TH	1040	Keystone Electronics
C1	0	47µF	CAP, AL, 47µF, 50V, ±20%, 0.68ohm, AEC-Q200 Grade 2, SMD	EEEFT1H470AP	Panasonic
C10	0	22µF	Cap Aluminum 22µF 100V ±20% (8 X 10.2mm) SMD 1.3 Ohm 70mA 2000h 125 C T/R	EEE-TG2A220UP	Panasonic Electronic Components
C12, C13, C14, C15	0	4.7µF	100V 4.7µF X7R ±20% 1206 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	CGA1206X7R475M101NT	HRE
C18, C19	0	2.2µF	CAP, CERM, 2.2µF, 100 V, ±10%, X7R, 1210	C1210C225K1RAC7800	Kemet
L1	0	300 ohm	Ferrite Bead, 300 ohm @ 100 MHz, 3 A, 1206	742792121	Wurth Elektronik
R3	0	402k	RES, 402k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW0603402KFKEA	Vishay-Dale
R5	0	0	RES, 0, 5%, 0.063W, 0402	RC0402JR-070RL	Yageo America
R7	0	133k	RES, 133k, 1%, 0.1W, AEC-Q200 Grade 0, 0603	CRCW0603133KFKEA	Vishay-Dale
R12	0	7.06k	RES, 7.06k, 0.5%, 0.1W, 0603	RT0603DRE077K06L	Yageo America
TP6, TP10	0		Test Point, Miniature, White, TH	5002	Keystone Electronics

5 Additional Information

5.1 Trademarks

All trademarks are the property of their respective owners.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (December 2025)	Page
• Updated board pictures	1
• Updated board images	4
• Added connector and test point names to the table and updated some descriptions	5
• Updated board pictures with the final ones	5
• Added note regarding the EMI filter	5
• Updated the cross-reference from Figure 2-4 to Figure 2-3	7
• Updated EVM schematic	8
• Added silkscreen images	9
• Updated the BOM and added manufacturing info	11

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Last updated 10/2025