User's Guide

LM5157EVM-BST Evaluation Module

ABSTRACT

The LM5157EVM-BST evaluation module showcases the features and performance of the LM5157 device as wide input voltage, non-synchronous boost converter with dual random spread spectrum. The standard configuration is designed to provide a regulated output of 12 V at 1.6 A from an input of 3 V to 9 V (load derated for input voltages below 6 V), switching at a frequency of 2.1 MHz.

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1 Features and Electrical Performance

The LM5157EVM-BST supports the following features and performance capabilities:

- Tightly regulated output voltage of 12 V with 1% accurate reference voltage
- High conversion efficiency of > 92% at full load
- Constant cycle-by-cycle peak inductor current limit over input voltage range
- Programmable hiccup mode for output overcurrent protection
- User-adjustable soft-start time using C_{SS}
- Output overvoltage protection
- Multiple BIAS pin and VCC pin connections to test multiple configurations
  - BIAS connect to VCC
  - BIAS supplied with external power supply
  - BIAS supplied by output voltage
- Power-good (PGOOD) indicator with selectable pullup source
- 2.1-MHz switching frequency
- External clock synchronization
- Programmable dual random spread spectrum reduces the EMI

1.1 Electrical Parameters

Table 1-1. Electrical Performance Standard Configuration

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage range V_{IN}	Operation	3	6	9	V
OUTPUT CHARACTERISTICS					
Output Voltage V_{OUT}			12		V
Maximum output current I_{OUT}	VIN = 6 V~9 V		1.6		A
	VIN = 4 V~6 V		0.8		
Output Over-voltage V_{OUT_OV}			13.6		V
SYSTEM CHARACTERISTICS					
Switching frequency			2.1		MHz
External clock synchronization		1.8		2.4	kHz
Full load efficiency	V_{IN} = 6 V, I_{OUT} = 1.6 A		92.2		%
Junction temperature, T_J		-40		150	C

1.2 Configuration Points

Table 1-2 indicates the available test points and configuration jumpers. These points offer flexibility in configuring the evaluation module and include but not limited to:

- BIAS pin to be connected to the following:
  - External supply (VAUX)
  - Input voltage (VIN)
  - Regulated output voltage (VOUT)
  - VCC pin
- PGOOD pin to be supplied by either VCC or VAUX
- External clock synchronization
- Shut-down signal by pulling the SD pin high
- Four different operation modes to enable and disable the spread spectrum and hiccup mode

Table 1-2. Jumper Description

JUMPER	PIN	DESCRIPTION
TP1	VIN+	Positive input voltage sense connection
TP2	SW	Probe point for the switch node of the LM5157 boost circuit
TP3	VOUT+	Positive output voltage sense connection
TP4	GND	Negative input voltage sense connection
TP5	GND	Negative output voltage sense connection
TP6	SYNC	Input for external clock signal. To implement the external clock synchronization, remove the jumper resistor R10 and tie the external signal to the TP6 (SYNC).
TP7	VAUX	Supply the BIAS pin from an external supply (if J9 is connected).
TP8	VOUT+	Loop response positive injection point (bottom side)
TP9	UVLO	Middle point of UVLO resistor divider
TP10	VOUT–	Loop response negative injection point (bottom side)
TP11	SD	High signal pulls the UVLO pin to ground entering shutdown mode
TP12	AGND	Negative input of external signals
J6	Pin 1 to pin 2	Connect VOUT to the BIAS pin of the LM5157 through D2 (only set one jumper to J6, J7, J8, or J9).
	Pin 2 to pin 3	Directly connect VOUT to the BIAS pin of the LM5157 (only set one jumper to J6, J7, J8, or J9).
J7	Pin 1 to pin 2	Connect VIN to the BIAS pin of the LM5157 through D3 (only set one jumper to J6, J7, J8, or J9).
	Pin 2 to pin 3	Directly connect VIN to BIAS pin of the LM5157 (only set one jumper to J6, J7, J8, or J9).
J8	Pin 1 to pin 2	Directly connect VCC to the BIAS pin (only set one jumper to J6, J7, J8 or J9).
J9	Pin 1 to pin 2	Directly connect VAUX to the BIAS pin (only set one jumper to J6, J7, J8, or J9).
J10	SS (Pin 1)	Monitor the SS pin.
	COMP (Pin 2)	Monitor the COMP pin.
	AGND (Pin 3)	Connection to AGND plane
	SYNC (Pin 4)	Monitor the EN/UVLO/SYNC pin.
	PGOOD (Pin 5)	Monitor the PGOOD pin.
	BIAS-IC (Pin 6)	Monitor the BIAS pin.
	VCC (Pin 7)	Monitor the VCC pin.
J11 (only use one jumper on J11)	Pin 1 to pin 2 (NN)	Hiccup mode disabled, spread spectrum disabled
	Pin 3 to pin 4 (HS)	Hiccup mode enabled, spread spectrum enabled
	Pin 5 to pin 6 (HN)	Hiccup mode enabled, spread spectrum disabled
	Pin 7 to pin 8 (NS)	Hiccup mode disabled, spread spectrum enabled

2 Application Schematic

The LM5157EVM-BST is capable of multiple configurations. Figure 2-1 shows the standard configuration of the LM5157EVM-BST for which the parameters in Table 1-1 are valid. Section 4.2 describes the correct jumper settings and measurement locations to recreate the data presented in Section 5.

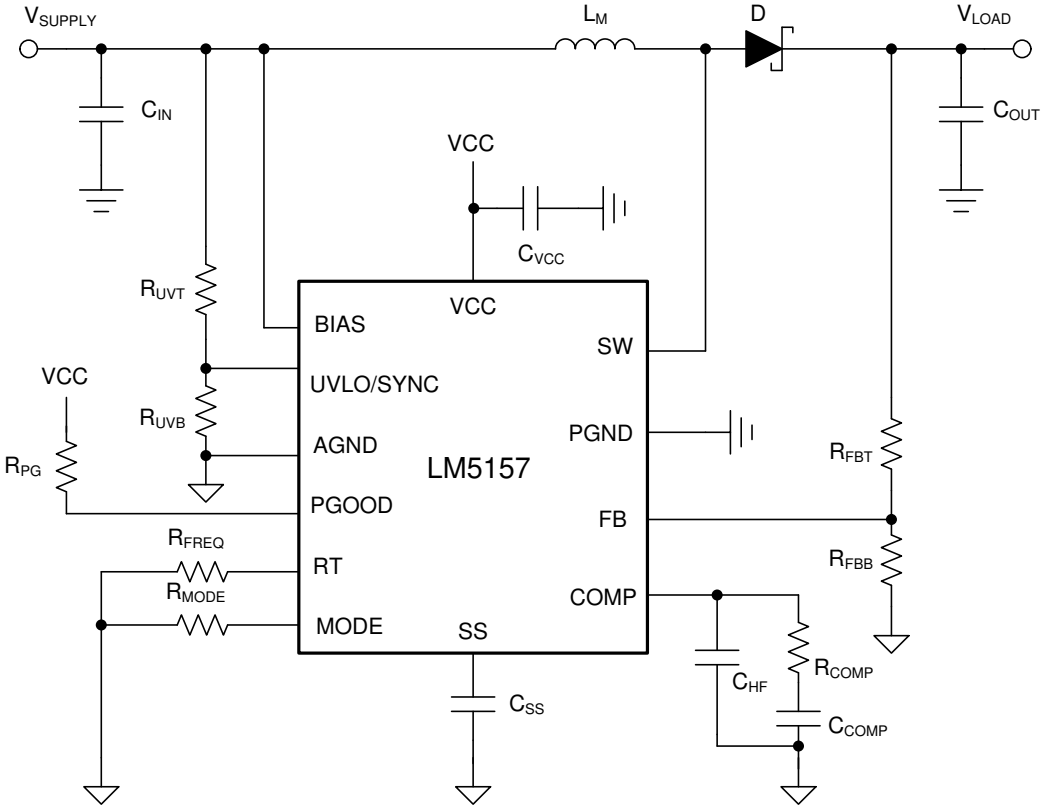

Figure 2-1. Application Circuit

3 EVM Picture

Figure 3-1 shows the 3D-rendered picture of the LM5157EVM-BST. The actual board color can differ.

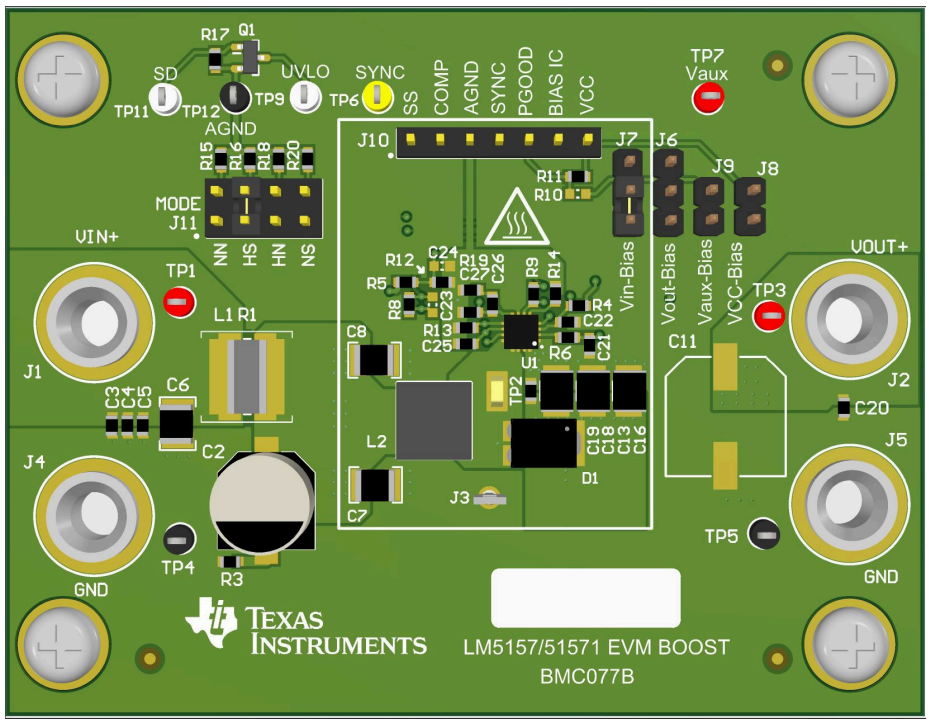

Figure 3-1. EVM Picture

4 Test Setup and Procedure

4.1 Test Setup

Figure 4-1 shows the correct jumper positions to configure the evaluation module for the typical application, as shown in Figure 2-1. The correct equipment connections and measurement points are shown in Table 4-1.

Table 4-1. Standard Configuration Jumper Connections

JUMPER	POSITION
J7	Jumper from pin 2 to pin 3 (VIN to BIAS)
J11	Jumper from pin 3 to pin 4 (HS)

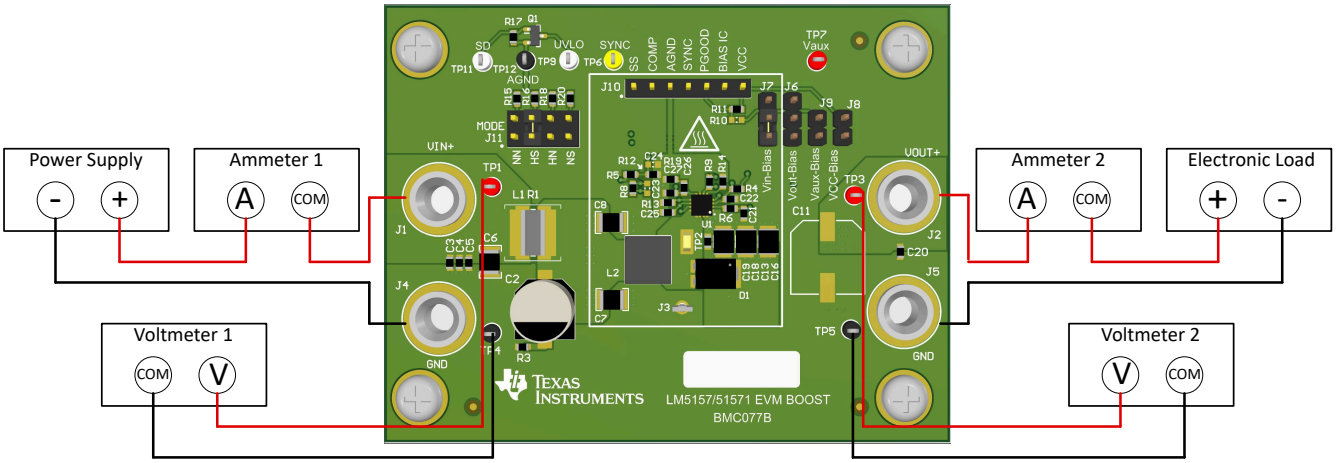

Figure 4-1. Test Setup

4.2 Test Equipment

Power Supply: The input voltage source (VIN) should be a variable supply capable of 0 V to 10 V and source at least 10 A.

Multi-meters:

- Voltmeter 1: Input voltage, connect from VIN+ to GND.
- Voltmeter 2: Output voltage, connect from VOUT+ to GND.
- Ammeter 1: Input current, must be able to handle 10 A. Shunt resistor can be used as needed.
- Ammeter 2: Output current, must be able to handle 2 A. Shunt resistor can be used as needed.

Electronic Load: The load should be constant resistance (CR) or constant current (CC) capable. It should safely handle 2 A at 12 V.

Oscilloscope: 20-MHz bandwidth and AC coupling. Measure the output voltage ripple directly across an output capacitor with a short ground lead. It is not recommended to use a long-leaded ground connection due to the possibility of noise being coupled into the signal. To measure other waveforms, adjust the oscilloscope as needed.

5 Test Results

Figure 5-1 through Figure 5-17 present the typical performance of the LM5157EVM-BST according to the BOM and the configuration described in Section 4. Based on measurement techniques and environmental variables, measurements can differ slightly than the data presented.

5.1 Efficiency Curve

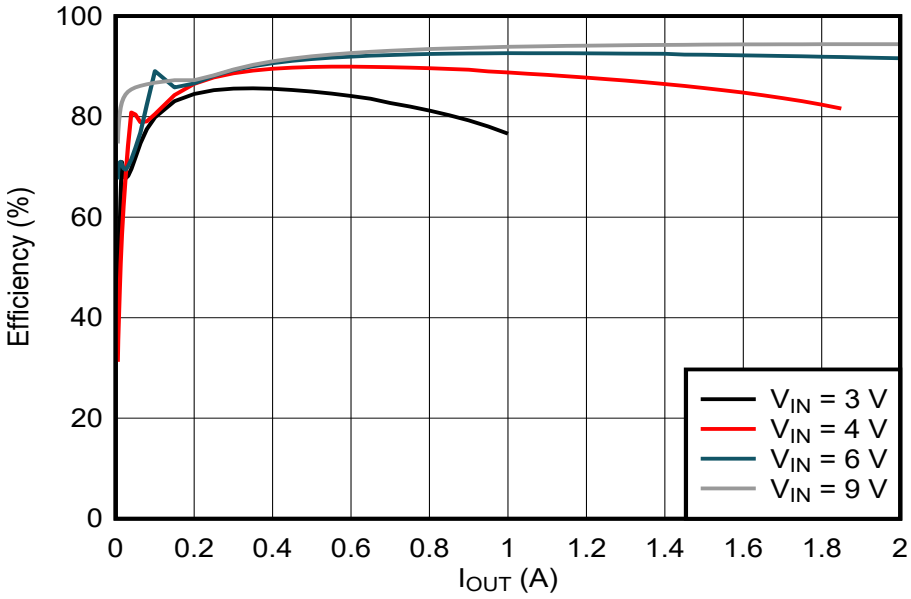

Figure 5-1. Efficiency vs Load

5.2 Load Regulation Curve

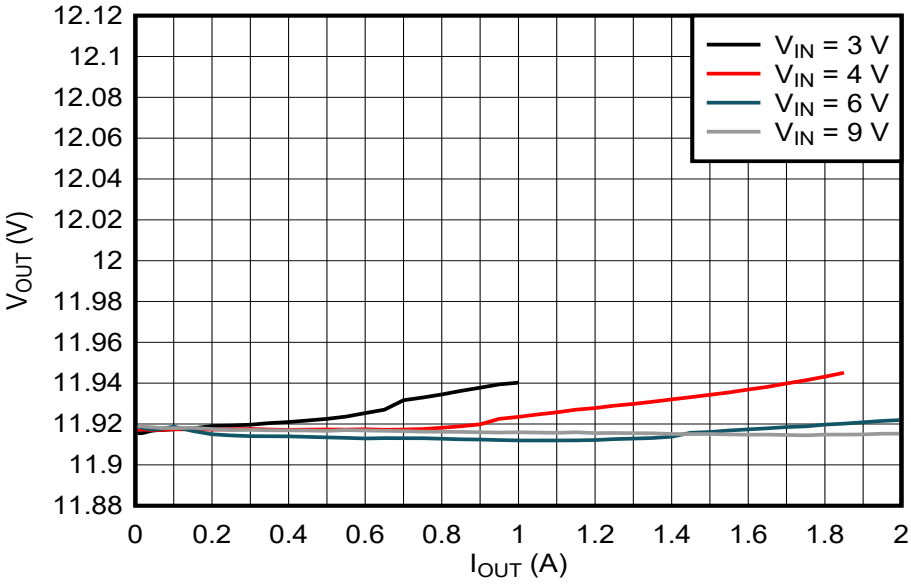

Figure 5-2. Load Regulation

5.3 Thermal Performance

Figure 5-3 shows the thermal image.

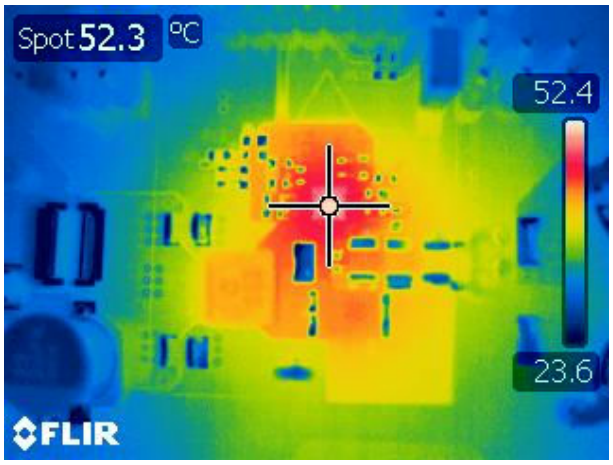

Figure 5-3. Thermal Image V_{IN} = 3 V I_{OUT} = 0.6 A, V_{BIAS} = V_{IN}, no Forced Air Cooling

Figure 5-4. Thermal Image V_{IN} = 3 V I_{OUT} = 0.6 A, V_{BIAS} = 12 V, no Forced Air Cooling

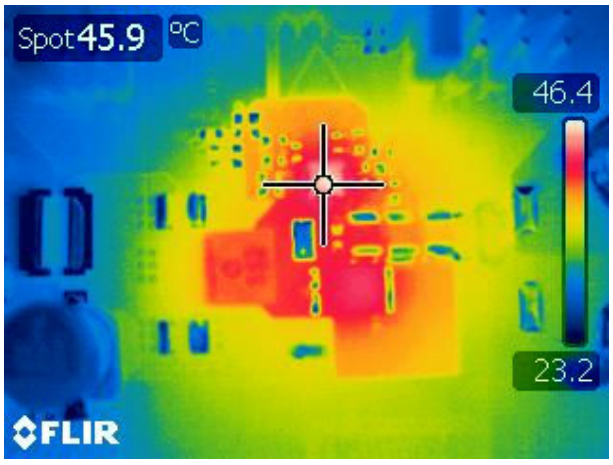

Figure 5-5. Thermal Image V_{IN} = 6 V I_{OUT} = 1.6 A, V_{BIAS} = V_{IN}, no Forced Air Cooling

Figure 5-6. Thermal Image V_{IN} = 9 V I_{OUT} = 1.6 A, V_{BIAS} = V_{IN}, no Forced Air Cooling

5.4 Steady State Waveforms

The output voltage ripple is measured directly next to C16.

Figure 5-7. Steady State, V_{IN} = 3 V, I_{OUT} = 0.6 A

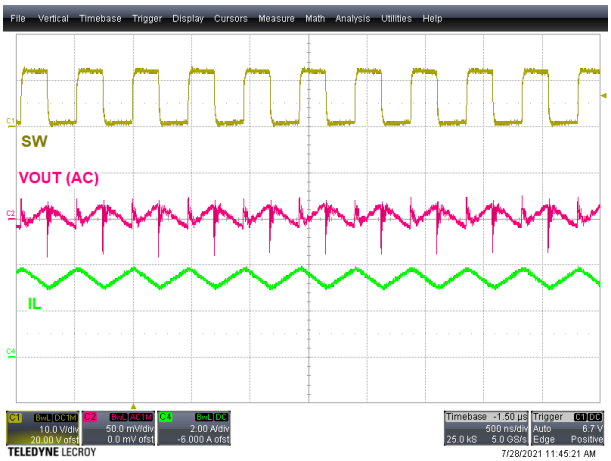

Figure 5-8. Steady State, V_{IN} = 6 V, I_{OUT} = 1.6 A

Figure 5-9. Steady State, V_{IN} = 9 V, I_{OUT} = 1.6 A

5.5 Start-Up Waveforms

Figure 5-10. Start-Up, V_{IN} = 3 V, I_{OUT} = 0.6 A (20 Ω)

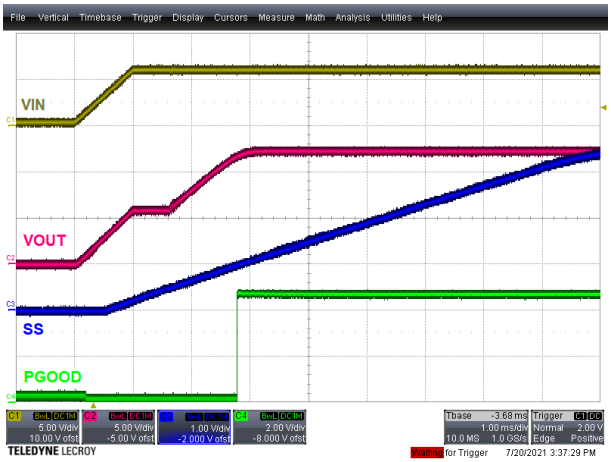

Figure 5-11. Start-Up, V_{IN} = 6 V, I_{OUT} = 1.6 A (7.5 Ω)

Figure 5-12. Start-Up, V_{IN} = 9 V, I_{OUT} = 1.6 A (7.5 Ω)

5.6 Load Transient Waveforms

The load transients are measured with J11 set to NN.

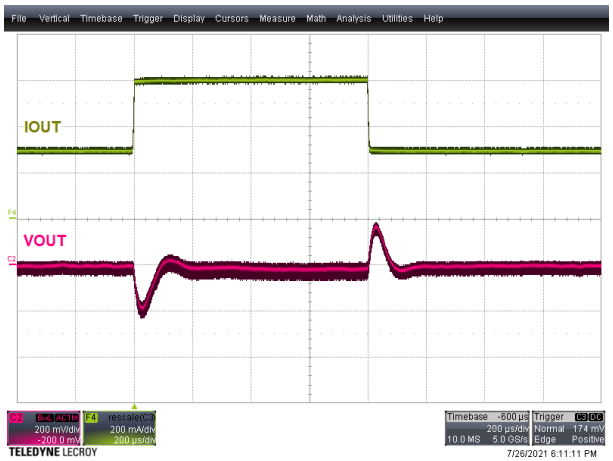

Figure 5-13. Load Transient, V_{IN} = 3 V, I_{OUT} = 0.3 A to 0.6 A

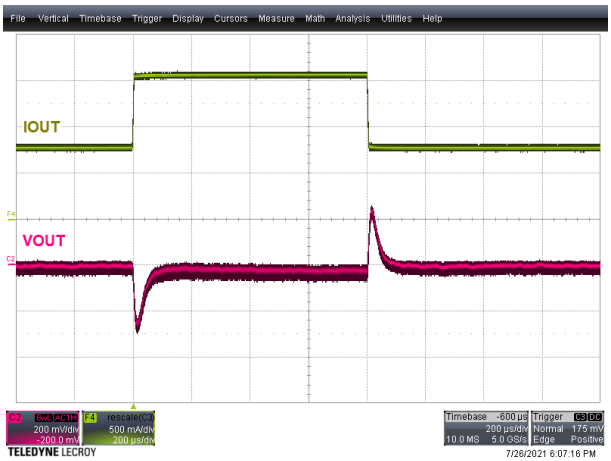

Figure 5-14. Load Transient, V_{IN} = 6 V, I_{OUT} = 0.8 A to 1.6 A

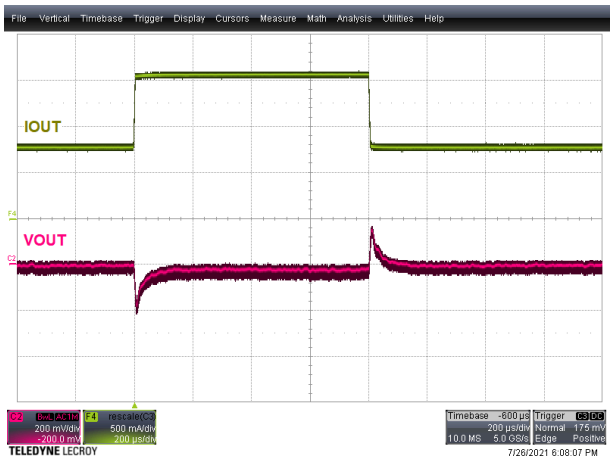

Figure 5-15. Load Transient, V_{IN} = 9 V, I_{OUT} = 0.8 A to 1.6 A

5.7 AC Loop Response Curves

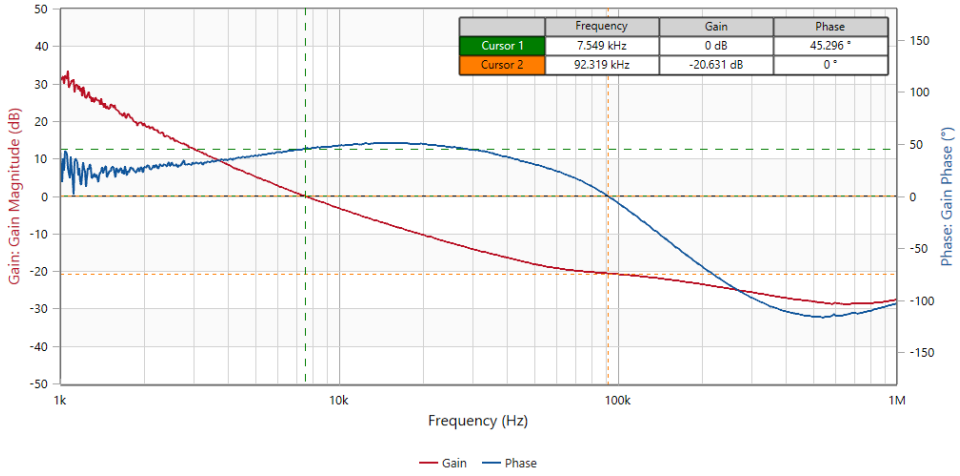

Figure 5-16. Control Loop Response, V_{IN} = 3 V, I_{OUT} = 0.6 A

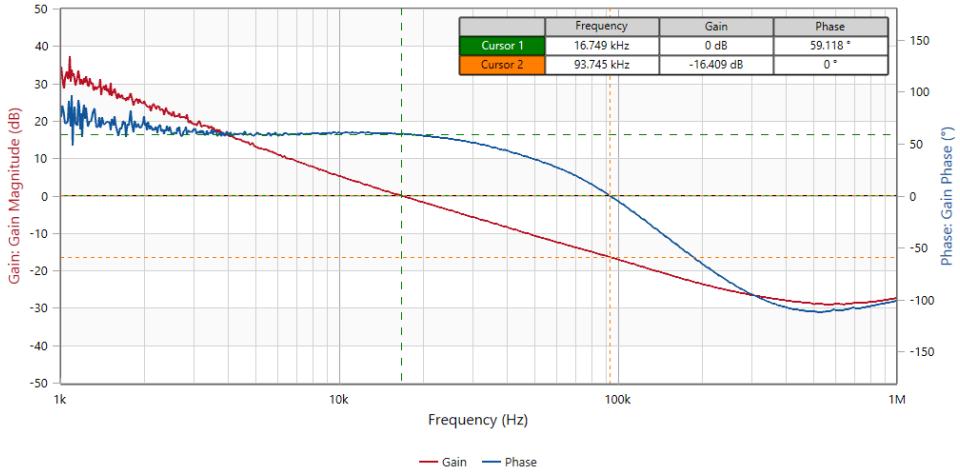

Figure 5-17. Control Loop Response, V_{IN} = 6 V, I_{OUT} = 1.6A

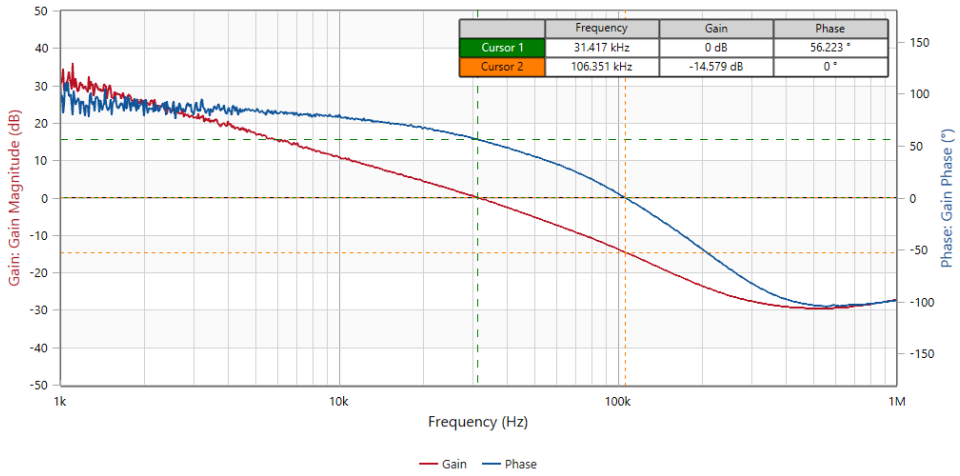

Figure 5-18. Control Loop Response, V_{IN} = 9 V, I_{OUT} = 1.6 A

6 Design Files

Figure 6-1 through Figure 6-6 illustrate the EVM PCB layout images.

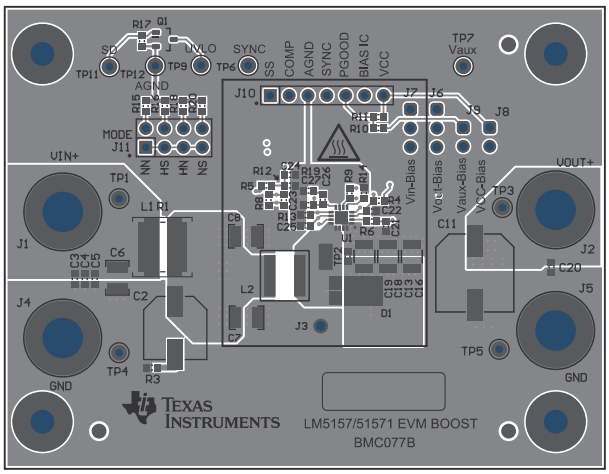

Figure 6-1. Top Layer and Silkscreen

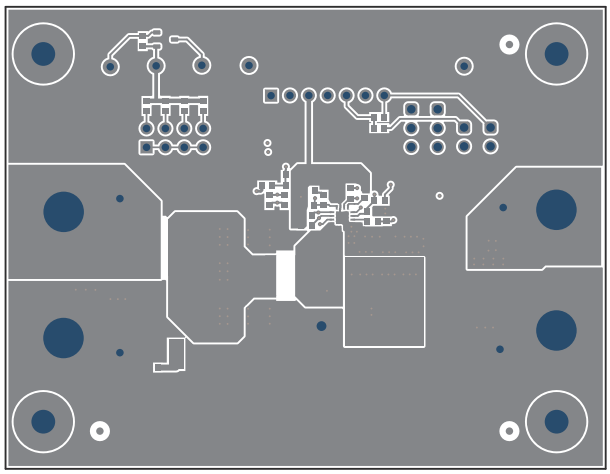

Figure 6-2. Top Layer

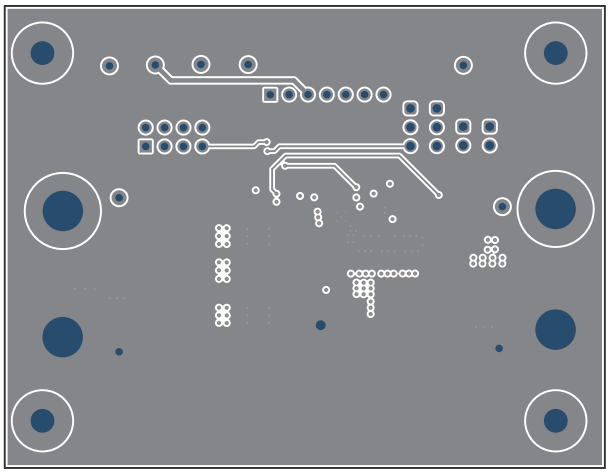

Figure 6-3. Signal Layer 1

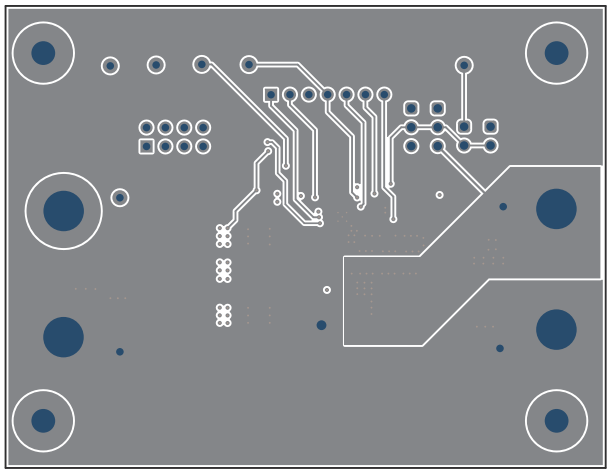

Figure 6-4. Signal Layer 2

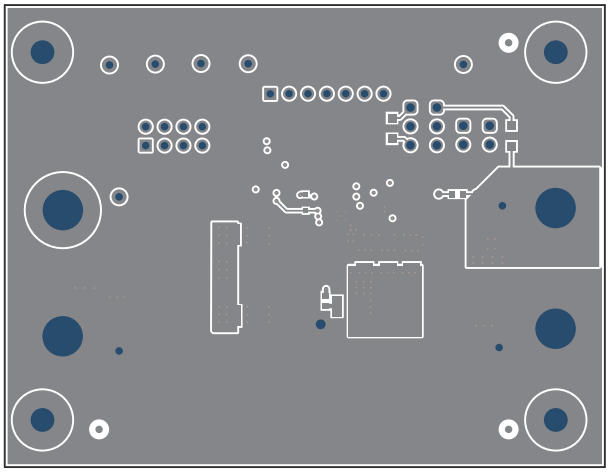

Figure 6-5. Bottom Layer

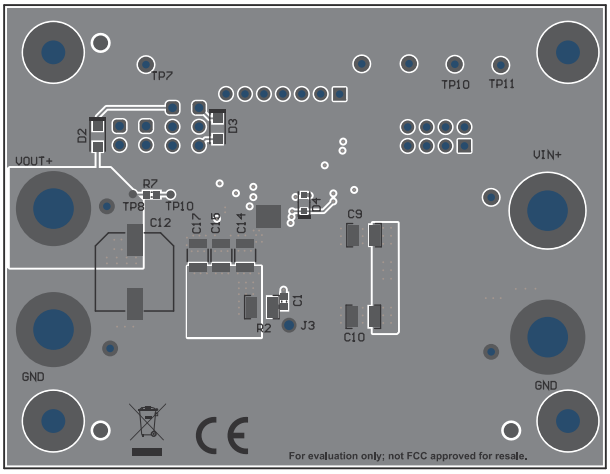

Figure 6-6. Bottom Layer and Silkscreen (mirrored)

6.1 Schematic

Figure 6-7 shows the EVM schematic.

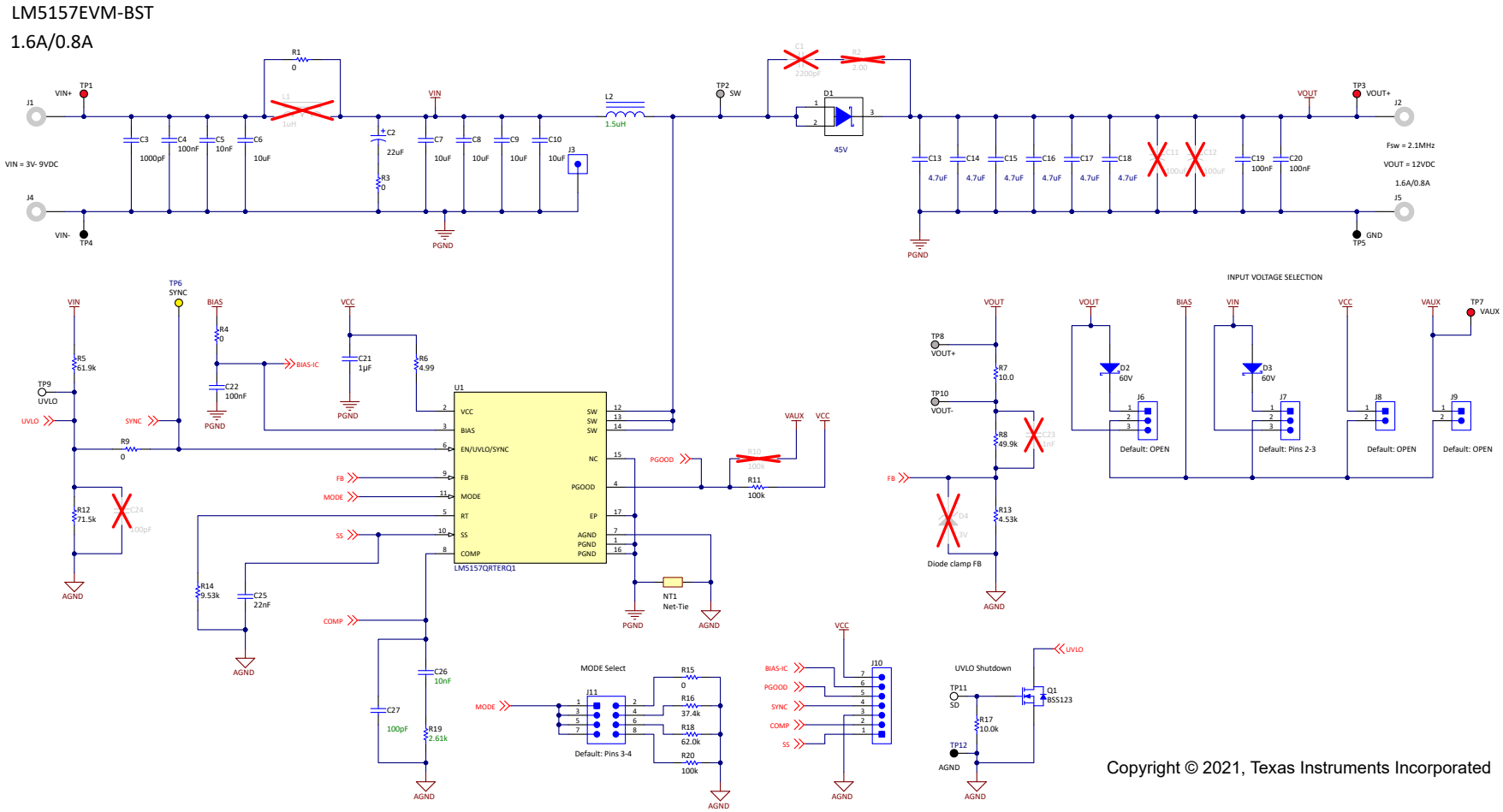

Figure 6-7. LM5157EVM-BST Schematic

6.2 Bill of Materials

Table 6-1 lists the EVM bill of materials.

Table 6-1. LM5157EVM-BST Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C2	1	22 µF	CAP, AL, 22 µF, 100 V, ±20%, 1.3 Ω, AEC-Q200 Grade 2, SMD	SMT Radial F	EEE-FK2A220P	Panasonic
C3	1	1000 pF	CAP, CERM, 1000 pF, 50 V, ±10%, X7R, 0603	603	C0603X102K5RACTU	Kemet
C4, C19, C20	3	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	603	C0603C104K5RACAUTO	Kemet
C5, C26	2	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ±10%, X7R, 0603	603	C0603X103K5RACTU	Kemet
C6, C7, C8, C9, C10	5	10 µF	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	1210	GRM32ER71H106KA12L	MuRata
C13, C14, C15, C16, C17, C18	6	4.7 µF	CAP, CERM, 4.7 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 1210	1210	CGA6P3X7R1H475K250AB	TDK
C21	1	1 µF	CAP, CERM, 1 µF, 16 V,±10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E1X7R1C105K080AC	TDK
C22	1	0.1 µF	CAP, CERM, 0.1 µF, 100 V,±10%, X7R, AEC-Q200 Grade 1, 0603	603	GCJ188R72A104KA01D	MuRata
C25	1	0.022 µF	CAP, CERM, 0.022 µF, 50 V, ±10%, X7R, 0603	603	C0603X223K5RACTU	Kemet
C27	1	100 pF	CAP, CERM, 100 pF, 50 V, ±5%, C0G/NP0, AEC-Q200 Grade 0, 0603	603	CGA3E2NP01H101J080AA	TDK
D1	1	45 V	Diode, Schottky, 45 V, 10 A, AEC-Q101, CFP15	CFP15	PMEG045V100EPDAZ	Nexperia
D2, D3	2	60 V	Diode, Schottky, 60 V, 1 A, SOD-123F	SOD-123F	PMEG6010CEH,115	Nexperia
L2	1	1.5 µH	Inductor, Shielded, Composite, 1.5 µH, 14 A, 0.01052 Ω, AEC-Q200 Grade 1, SMD		XEL6030-152MEB	Coilcraft
Q1	1	100 V	MOSFET, N-CH, 100 V, 0.17 A, SOT-23	SOT-23	BSS123	Fairchild Semiconductor
R1	1	0	RES, 0, 5%, 2 W, 2512 WIDE	2512 WIDE	RCL12250000Z0EG	Vishay Draloric
R3, R4, R9, R15	4	0	RES, 0, 5%, 0.1 W, 0603	603	RC0603JR-070RL	Yageo
R5	1	61.9 k	RES, 61.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0761K9L	Yageo
R6	1	4.99	RES, 4.99, 1%, 0.1 W, 0603	603	RC0603FR-074R99L	Yageo
R7	1	10	RES, 10.0, 1%, 0.1 W, 0603	603	RC0603FR-0710RL	Yageo
R8	1	49.9 k	RES, 49.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0749K9L	Yageo

Table 6-1. LM5157EVM-BST Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R11, R20	2	100 k	RES, 100 k, 1%, 0.1 W, 0603	603	RC0603FR-07100KL	Yageo
R12	1	71.5 k	RES, 71.5 k, 1%, 0.1 W, 0603	603	RC0603FR-0771K5L	Yageo
R13	1	4.53 k	RES, 4.53 k, 1%, 0.1 W, 0603	603	RC0603FR-074K53L	Yageo
R14	1	9.53 k	RES, 9.53 k, 1%, 0.1 W, 0603	603	RC0603FR-079K53L	Yageo
R16	1	37.4 k	RES, 37.4 k, 1%, 0.1 W, 0603	603	RC0603FR-0737K4L	Yageo
R17	1	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo
R18	1	62.0 k	RES, 62.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0762KL	Yageo
R19	1	2.61 k	RES, 2.61 k, 1%, 0.1 W, 0603	603	RC0603FR-072K61L	Yageo
U1	1		2.2-MHz Wide VIN Boost/Sepic/ Flyback Converter with Dual Random Spread Spectrum, RTE0016K (WQFN-16)	RTE0016K	LM5157QRTERQ1	Texas Instruments

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (August 2021)	Page
• Updated all measurements	1
• Added resistor in series to the VCC capacitor	1
• Updated Figure 6-7	15
• Updated Table 6-1	16

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