

# **LM5140-Q1 High Density EVM**

## **User's Guide**



Literature Number: SNVU521  
July 2016

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## Introduction

The LM5140-Q1 High Density evaluation module helps designers to evaluate the operation and performance of the LM5140-Q1 synchronous buck controller. The EVM operates over the input voltage range of 3.8 V to 42 V. The EVM provides two independent outputs, a 3.3-V output with a maximum load current of 5 A, and a 5-V output with a maximum load current of 5 A. The device offers configurability and can be setup to switch at 440 kHz or 2.2 MHz.

### 1.1 Features and Performance

The EVM supports the following features and performance capabilities:

- The LM5140-Q1 is qualified to AEC-Q100 grade 1 (-40°C to +125°C operating junction temperature)
- VIN 3.8 V to 42 V (EVM)
- Two outputs:
  - VOUT1 fixed 3.3 V, 5 V, or adjustable from 1.5 V to 15 V
  - VOUT2 fixed 5 V, 8 V, or adjustable from 1.5 V to 15 V
- Shutdown Mode IQ: 9 µA
- Low IQ Standby: 35 µA typical (1-channel in regulation, no load)
- The outputs can be synchronized to an external clock
- A SYNC output
- A fixed 2.2 MHz, or 440-kHz oscillator frequency
- EN1 enables Output 1
- EN2 enables Output 2
- Hiccup Mode for sustained overload
- Independent power good (PG1 and PG2) signals
- Gate drive with slew rate control for reduced EMI
- Diode Emulation or forced pulse-width modulation (FPWM)

Table 1-1 contains the electrical performance data for this EVM.

**Table 1-1. Electrical Performance**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>					
Input Voltage	3.3-V Output	3.8	42		V
	5-V Output	5.5	42		
<b>OUTPUT CHARACTERISTICS</b>					
Output Voltage 1	$I_{LOAD} = 5 \text{ A}$	3.267	3.3	3.333	V
Output Current				5	A
Output Voltage 2	$I_{LOAD} = 5 \text{ A}$	4.95	5.0	5.05	V
Output Current				5	A
<b>SYSTEM CHARACTERISTICS</b>					
Switching Frequency		2	2.2	2.4	MHz
Full Load Efficiency	VIN = 12 V, VOUT1 = 3.3 V at 5 A, VOUT2 = 5 V at 5 A		84%		

## Setup

This section describes the input and output connections to the LM5140-Q1 HD EVM and other functional settings.

[Table 2-1](#) lists the jumpers and test point descriptions.

**Table 2-1. Jumpers and Test Points**

PIN NAME	DESCRIPTION	COMMENTS
J1-1	The + (positive) VIN power for the EVM.	
J1-2	The - (negative) VIN power for the EVM.	
J5-1	EN1- Enable VOUT1	
J5-2		
J5-3	EN1 Disable VOUT1	Factory default setting
J6-1	EN2-Enable VOUT2	
J6-2		
J6-3	EN2-Disable VOUT2	Factory default setting
J7-1	FPWM	
J7-3	DEMB	Factory default setting
TP1	Output 1 regulated output voltage.	
TP2	Output 1 ground (GND) connection.	
TP3	PG1 an open collector output which goes low if VOUT1 is outside of the regulation window.	Monitor for PG1
TP6	SYNC_OUT a TTL level output signal 180° out of phase of HO1.	
TP8	PG2 an open collector output which goes low if Vout1is outside of the regulation window	Monitor for PG2
TP9	Output 2 regulated output voltage for the converter.	
TP10	Output 2 ground (GND) connection.	

## ***Setup Input and Loads***

### **3.1 Input and Output**

The input voltage range for the EVM is 3.8 V to 42 V. The EVM output 1 is configured for 3.3V and is rated for 5-A continuous, output 2 is 5 V, and is rated for 5-A continuous.

### **3.2 Enabling the Outputs**

To enable VOUT1 place a header from J5-1 to J5-2, to enable VOUT2 place header from J6-1 to J6-2. The EVM outputs can be enabled before or after VIN has been applied.

## ***Test Equipment***

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### **4.1 Power Supply**

The power supply should be capable of 50 V / 10 A.

### **4.2 Electronic Loads**

The electronic load should be capable of 10 V / 10 A used in Constant Current Mode.

### **4.3 Meters**

A current meter is required to measure the input current accurately. The maximum current rating of the meter should be carefully considered. The input current can be as high as 7.5 A with both outputs at full load at the minimum input voltage. The output voltage should be monitored with a voltage meter capable of monitoring up to 10 V.

### **4.4 Oscilloscope**

A oscilloscope and 10x probe with at least 20-MHz bandwidth is required.

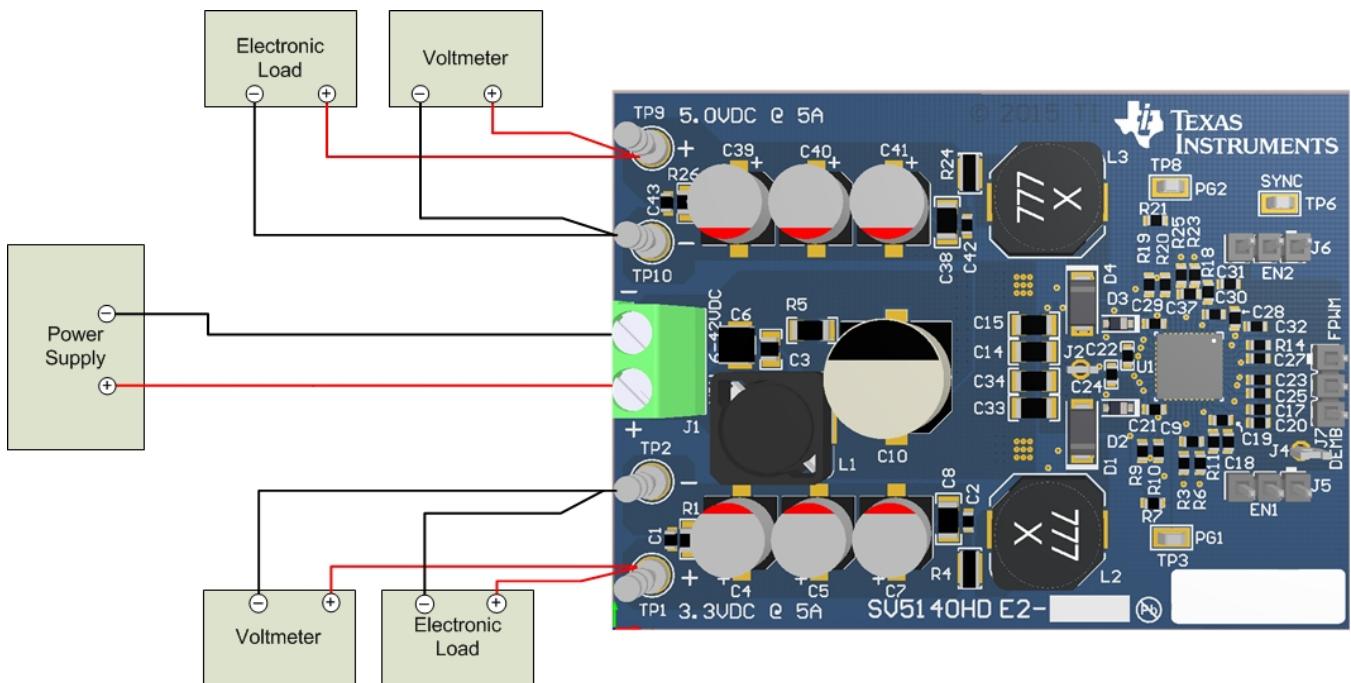
### **4.5 Airflow**

Full rated power should never be attempted without providing the specified 200 CFM of air flow over the evaluation board. This can be provided by a stand-alone fan.

## ***Test Setup and Procedure***

Please read the LM5140-Q1 data sheet ([SNVSA02](#)) before using the EVM. A typical LM5140-Q1 test bench setup is shown in [Figure 5-1](#). The power supply and loads should be capable of handling the input and output voltage and current rating of the board. Prior to applying power to the EVM, make sure that jumpers J5, J6, and J7 are set to the correct positions, refer to [Table 2-1](#).

1. Connect the power and ground connections VIN (J1-1) and GND (J1-2) to the power supply.
2. Connect an ammeter in series with the positive input, if needed.
3. Connect a DVM from TP1 (+) to TP2 (-).
4. Connect a DVM from TP9 (+) to TP10 (-).
5. Connect a resistive load or an electronic load across terminals (VOUT1) TP1 (+) and GND (TP2).
6. Connect a resistive load or an electronic load across terminals (VOUT2) TP9 (+) and GND (TP10-).
7. An ammeter can be inserted in series with the loads to observe the load current.
8. Refer to Table 2 for the jumper setting to enable VOUT1 and VOUT2.
9. With the load initially set to no load, set the power supply to 12 V and turn on the power supply. Check for VOUT1 3.3 V and VOUT2 5 V at the output.
10. Once the output is at the expected target (12 V), increase the load gradually within the operating range.



**Figure 5-1. EVM Connections**

## ***Test Data Performance and Curves***

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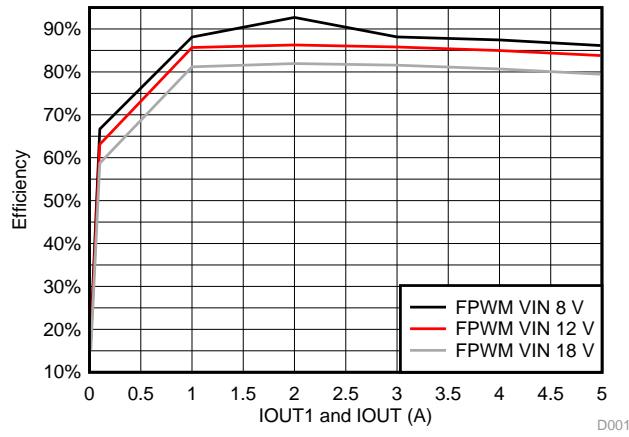


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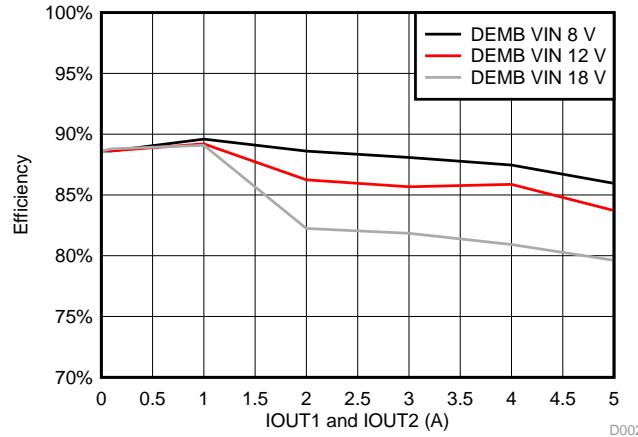
The following curves are presented for reference. Actual field data may differ for the curves. Actual performance data can be affected by measurement technique, equipment settings, and environmental conditions.

### **6.1 Efficiency**

The efficiency measurements ([Figure 6-1](#) and [Figure 6-2](#)) were made with VOUT1 and VOUT2 enabled and with the same load current, operating at 2.2 MHz.

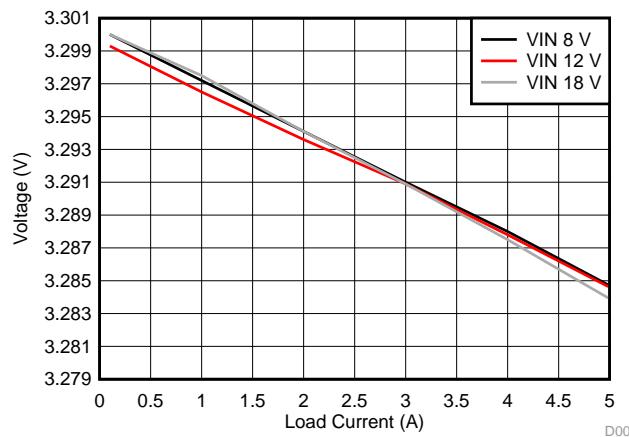


**Figure 6-1. Efficiency in FPWM, VIN 12 V**

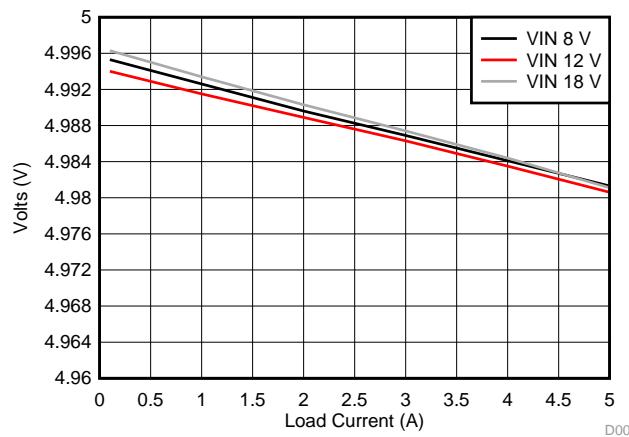


**Figure 6-2. Efficiency in DEMB, VIN 12 V**

## 6.2 Voltage Regulation



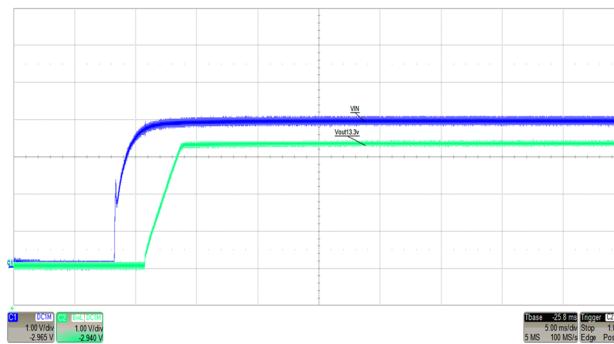
**Figure 6-3. Voltage Regulation 3.3-V Output**



**Figure 6-4. Voltage Regulation 5-V Output**

## 6.3 Low VIN Start-Up (3.8 V)

The Low VIN start-up test (Figure 6-5) run with VOUT 1 enabled (3.3 V) with a 4-A load, VOUT2 disabled.



**Figure 6-5. 3.8 V Start-Up**

## 6.4 CISPR 25 Class 5

Figure 6-6 and Figure 6-7 illustrate CISPR Class 5 limits with 12-V input, 5 A at 3.3-V and 5 A at 5-V outputs, 2.2 MHz, resistive loads, CISPR 25 CE setup.

Input 12V, Output 6A@3.3V, 5A@5V, 2.2MHz, resistive loads, CISPR 25 CE setup

**Red Line:** Class 5 Limit (Peak Detection)

**Yellow:** Peak detection result

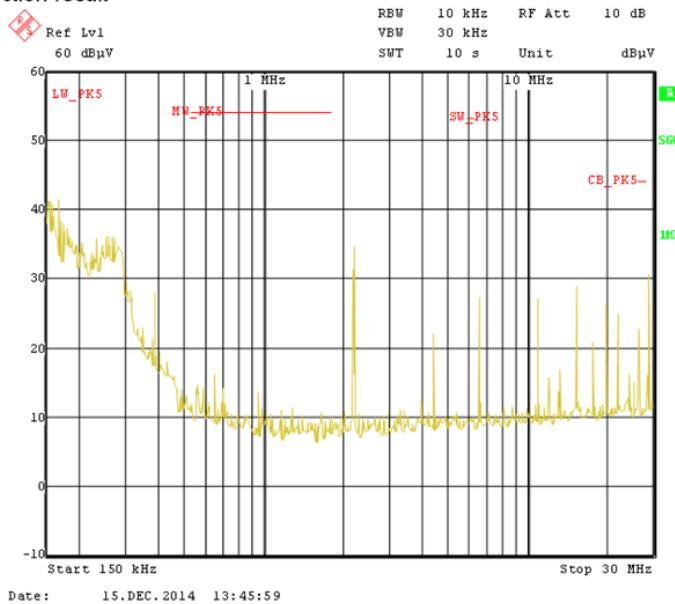


Figure 6-6. CISPR 25 Class 5 Peak Detection 150 kHz to 30 MHz

Input 12V, Output 6A@3.3V, 5A@5V, 2.2MHz, resistive loads, CISPR 25 CE setup

**Red Line:** Class 5 Limit (Average Detection)

**Blue:** Average detection result

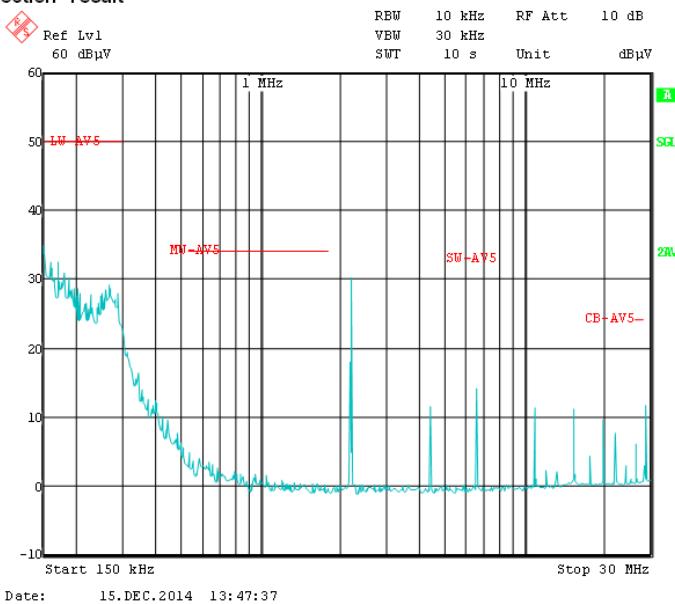
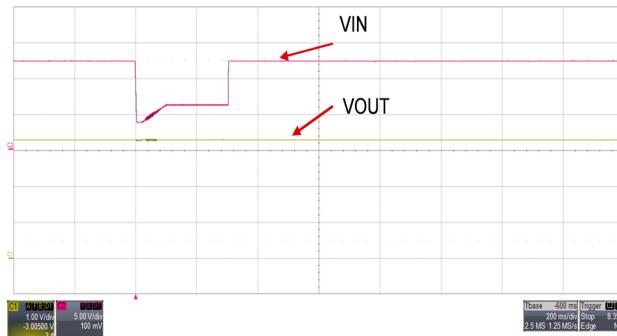


Figure 6-7. CISPR 5 Average Detection 150 kHz to 30 MHz

## 6.5 Cold Crank

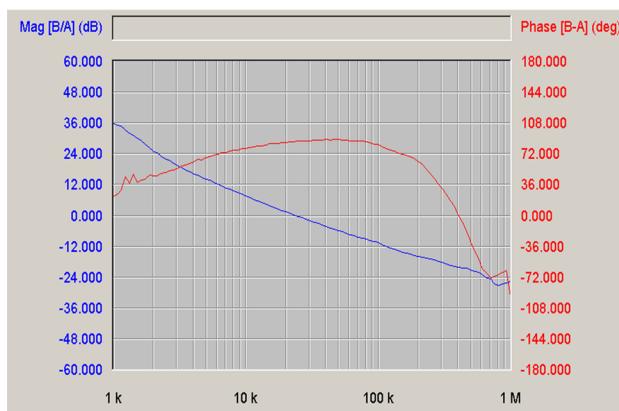
Cold Crank Start-Up, Vout1 enabled (3.3 V) with a 4-A load, VOUT2 (5 V) disabled.



**Figure 6-8. Cold Crank Start-Up**

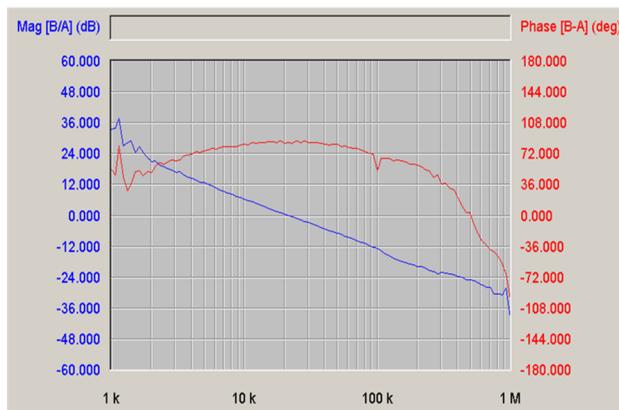
## 6.6 Bode Plot

The Bode Plot (Figure 6-9) VIN 12 V, VOUT1 (3.3 V) with a 5-A load, VOUT2 was disabled. The phase margin is 90 degrees and the gain margin is –20 dB.



**Figure 6-9. Bode Plot 3.3-V Output, 5-A Load**

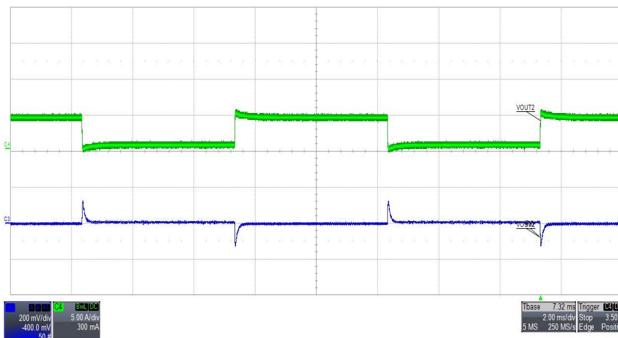
The Bode Plot (Figure 6-10) VIN 12 V, VOUT (5 V) with 5-A load, VOUT1 was disabled. The phase margin is 90 degrees and the gain margin is –24 dB.



**Figure 6-10. Bode Plot 5-V Output, 5-A Load**

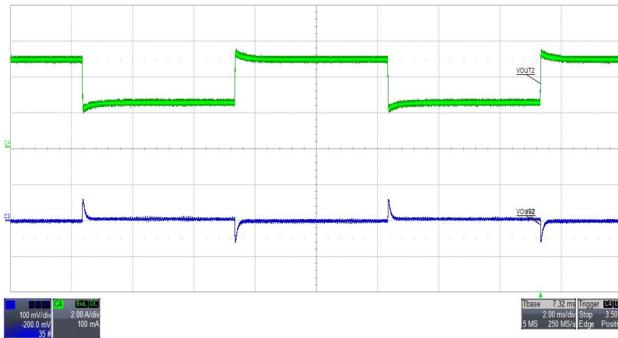
## 6.7 Transient Response

The transient response test, Figure 6-11, VOUT1 enabled, operating at 2.2 MHz, and VOUT2 disabled. The load step from 0.6 A to 5 A, the output undershoot and overshoot 100 mV.



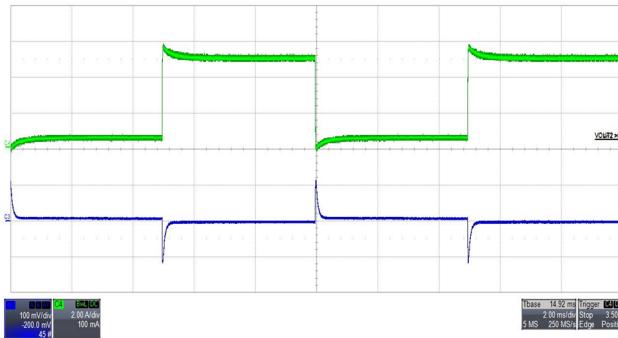
**Figure 6-11. 3.3-V Output Transient Response 0.6 A to 5 A**

The transient response test, Figure 6-12, VOUT1 enabled, operating at 2.2 MHz, and VOUT2 disabled. The load was step from 3 A to 5 A, the output overshoot and undershoot 50 mV.



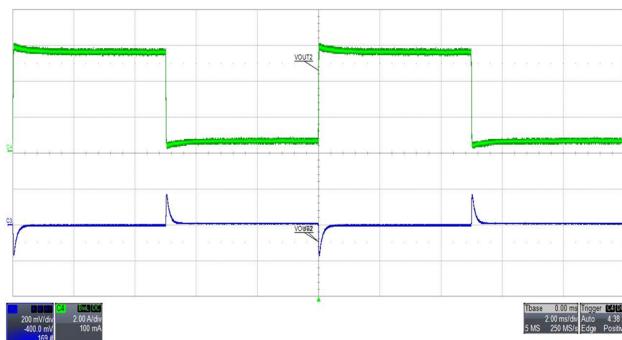
**Figure 6-12. 3.3-V Output Transient Response 3 A to 5 A**

The transient response test, Figure 6-13, VOUT2 enabled, operating at 2.2 MHz, and VOUT1 disabled. The load was step from 0.6 A to 5 A, the output overshoot and undershoot 120 mV.



**Figure 6-13. 5-V Output Transient Response 0.6-A to 5-A Load**

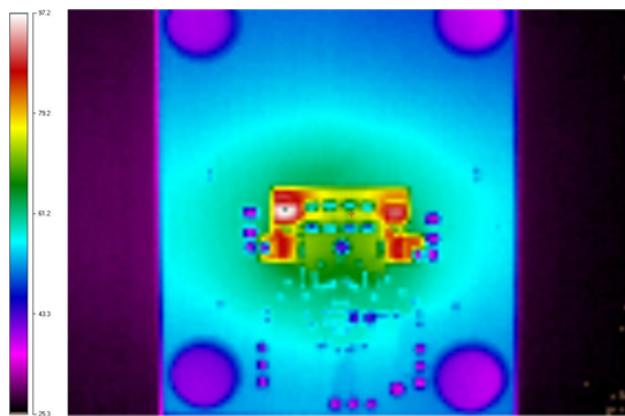
The transient response test, Figure 6-14, VOUT2 enabled, operating at 2.2 MHz, and VOUT1 disabled. The load was step from 3 A to 5 A, the output undershoot and overshoot 180 mV.



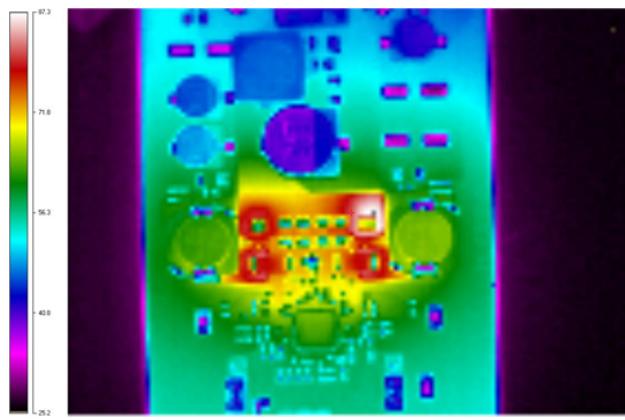
**Figure 6-14. 5-V Output Transient Response 3-A to 5-A Load**

## 6.8 PWB Board Temperature

VIN 12 V, 3.3 V at 5 A, 5 V at 5 A



**Figure 6-15. Thermal Image PWB Bottom Side**



**Figure 6-16. Thermal Image PWB Top Side**

## Design Files

### 7.1 Schematics

To download the schematics for each board, see the design files at <http://www.ti.com/tool>.

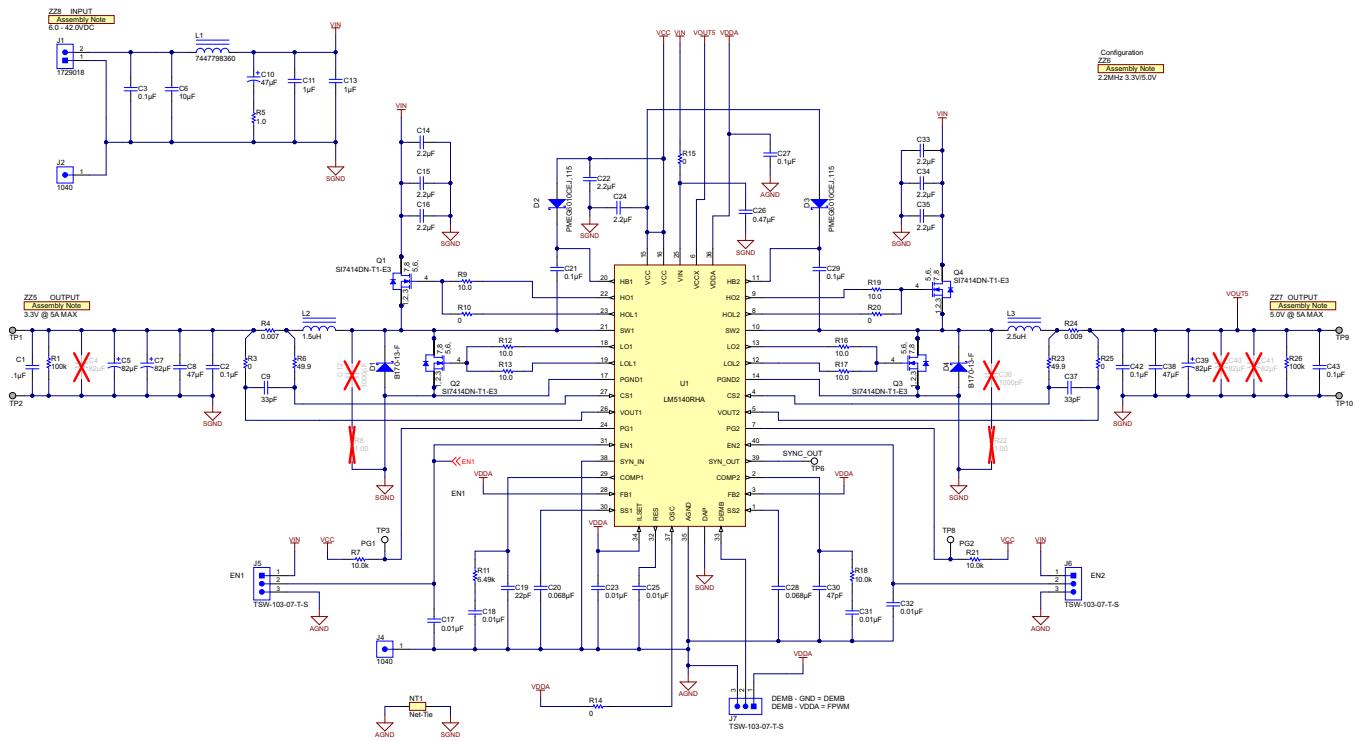


Figure 7-1. Schematic LM5140HD EVM

## 7.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at <http://www.ti.com/tool>.

**Table 7-1. BOM LM5140HD EVM**

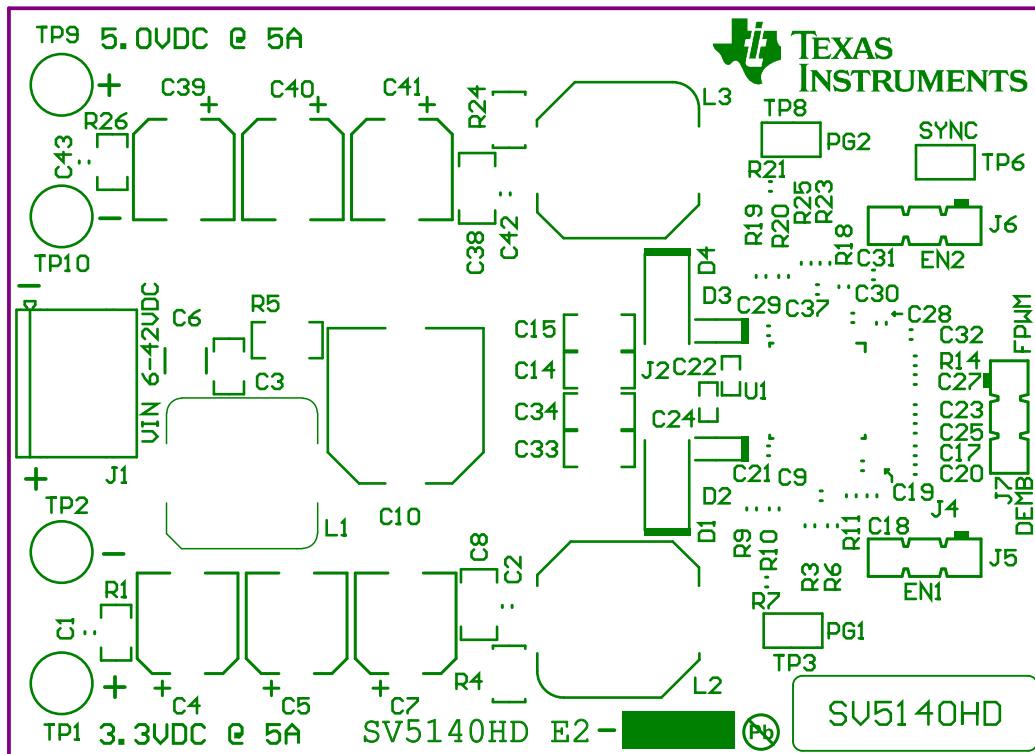
ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	PCB FOOTPRINT
1	1	SVA	—	Printed Circuit Board	Any	SV5140HD	—
2	1	C1, C2, C21, C29, C42, C43	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 100V, $\pm 10\%$ , X7R, 0603	MuRata	GRM188R72A104 KA35D	0603
3	6	C3	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 100 V, $\pm 10\%$ , X7R, 0805	Kemet	C0805C104K1RA CTU	0805
4	1	C5, C7, C39	82 $\mu$ F	CAP, Aluminum Polymer, 82 $\mu$ F, 16 V, $\pm 20\%$ , 0.03 $\Omega$ , D6.3xL5.8mm SMD	Wurth Elektronik	875105344009	D6.3xL5.8mm
5	3	C6	10 $\mu$ F	CAP, CERM, 10 $\mu$ F, 63 V, $\pm 10\%$ , X7R, 1210	MuRata	GRM32ER71J106 KA12L	1210
6	1	C8, C38	47 $\mu$ F	CAP, CERM, 47 $\mu$ F, 16V, $\pm 15\%$ , X5R, 1206	TDK	C3216X5R1C476 M160AB	1206
7	2	C9, C37	33 PF	CAP, CERM, 33 pF, 100 V, $\pm 5\%$ , COG/NP0, 0603	AVX	06031A330JAT2A	0603
8	2	C10	47 $\mu$ F	CAP, AL, 47 $\mu$ F, 50 V, $\pm 20\%$ , 0.3 $\Omega$ , SMD	Panasonic	EEE-FC1H470P	SMT Radial G
9	1	C11, C13	1 $\mu$ F	CAP, CERM, 1 $\mu$ F, 100V, $\pm 20\%$ , X7R, 1206	TDK	C3216X7R2A105 M160AA	1206
10	2	C14, C15, C16, C33, C34, C35	2.2 $\mu$ F	CAP CER 2.2 $\mu$ F 100V 10% X7R 1206	Samsung	CL31B225KCHSN NE	1206 (3216 Metric)
11	6	C17, C18, C23, C25, C31, C32	0.01 $\mu$ F	CAP, CERM, 0.01 $\mu$ F, 100 V, $\pm 20\%$ , X7R, 0603	TDK	C1608X7R2A103 M	0603
12	6	C19	22 PF	CAP, CERM, 22 pF, 50 V, $\pm 5\%$ , COG/NP0, 0603	Kemet	C0603C220J5GA CTU	0603
13	1	C20, C28	0.068 $\mu$ F	CAP, CERM, 0.068 $\mu$ F, 25 V, $\pm 10\%$ , X7R, 0603	MuRata	GRM188R71E683 KA01D	0603
14	2	C22, C24	2.2 $\mu$ F	CAP, CERM, 2.2 $\mu$ F, 10 V, $\pm 20\%$ , X5R, 0603	Kemet	C0603C225M8PA CTU	0603
15	2	C26	0.47 $\mu$ F	CAP, CERM, 0.47 $\mu$ F, 100V, $\pm 10\%$ , X7R, 0805	MuRata	GRM21BR72A474 KA73L	0805
16	1	C27	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, $\pm 10\%$ , X7R, 0603	MuRata	GRM188R71H104 KA93D	0603
17	1	C30	47 pF	CAP, CERM, 47 pF, 50 V, $\pm 5\%$ , COG/NP0, 0603	Kemet	C0603C470J5GA CTU	0603
18	1	D1, D4	70 V	Diode, Schottky, 70 V, 1A, SMA	Diodes Inc.	B170-13-F	SMA
19	2	D2, D3	60 V	Diode, Schottky, 60 V, 1 A, SOD-323F	NXP Semiconductor	PMEG6010CEJ,11 5	SOD-323F
20	2	H1, H2, H3, H4	—	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	Transparent Bumpon
21	4	J1	—	TERM BLOCK 2POS 5mm, TH	Phoenix Contact	1729018	10x10x8.1 mm
22	1	J2, J4	—	TEST POINT SLOTTED .118", TH	Keystone	1040	Test point, TH Slot Test point
23	2	J5, J6, J7	—	Header, 2.54 mm, 3x1, Tin, TH	Samtec	TSW-103-07-T-S	Header, 2.54 mm, 3x1, TH
24	3	L1	3.6 $\mu$ H	Inductor, Shielded, Metal Composite, 3.6 $\mu$ H, 8.6 A, 0.00525 $\Omega$ , SMD	Wurth Elektronik	7447798360	10.2 x 6.4 x 10.2mm
25	1	L2	1.5 $\mu$ H	Inductor, Shielded Drum Core, Ferrite, 1.5 $\mu$ H, 7.85 A, 0.01 $\Omega$ , SMD	Coilcraft	MSS1038-152NLB	MSS1038
26	1	L3	2.5 $\mu$ H	Inductor, Shielded Drum Core, Ferrite, 2.5 $\mu$ H, 6.65 A, 0.01 $\Omega$ , SMD	Coilcraft	MSS1038-252NLB	MSS1038
27	1	Q1, Q2, Q3, Q4	60 V	MOSFET, N-CH, 60 V, 5.6 A, PowerPAK 1212	Vishay-Siliconix	SI7414DN-T1-E3	PowerPAK 1212
28	4	R1, R26	100 k	RES, 100 k, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805100KF KEA	0805

**Table 7-1. BOM LM5140HD EVM (continued)**

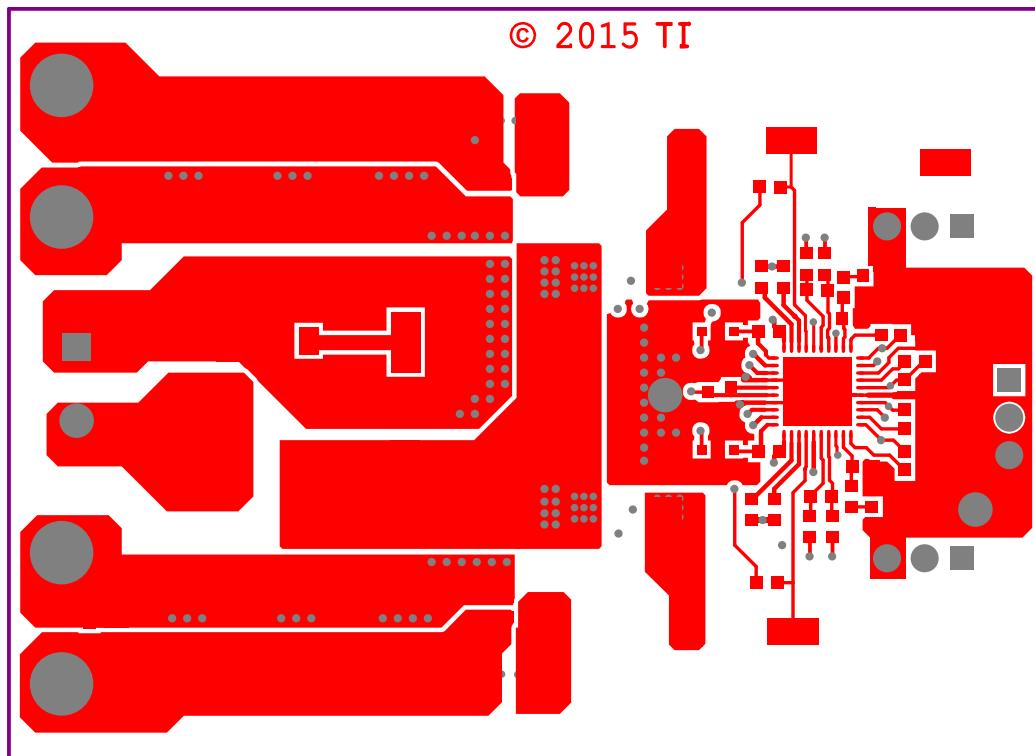
ITEM	QTY	REFERENCE	VALUE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER	PCB FOOTPRINT
29	2	R3, R10, R15, R20, R25	0	RES, 0, 5%, 0.1 W, 0603	Yageo America	RC0603JR-070RL	0603
30	5	R4	0.007	RES, 0.007, 1%, 1 W, 0612	Susumu Co Ltd	PRL1632-R007-F-T1	0612
31	1	R5	1	RES, 1.0 Ω, 5%, 0.25W, 1206	Vishay-Dale	CRCW12061R00J NEA	1206
32	1	R6, R23	49.9	RES, 49.9, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349R9F KEA	0603
33	2	R7, R21	10 k	RES, 10.0 kΩ, 1%, 0.1W, 0603	Yageo America	RC0603FR-0710KL	0603
34	2	R9, R12, R13, R16, R17, R19	10	RES, 10.0, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0710RL	0603
35	6	R11	6.49 k	RES, 6.49 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06036K49F KEA	0603
36	1	R14	0	RES, 0 Ω, 5%, 0.1W, 0603	Yageo America	RC0603JR-070RL	0603
37	1	R18	10 k	RES, 10.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0710KL	0603
38	1	R24	0.009	RES, 0.009, 1%, 1 W, 0612	Susumu Co Ltd	PRL1632-R009-F-T1	0612
39	1	SV5140HD		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	PCB Label 0.650" W x 0.200" H
40	1	TP1, TP2, TP9, TP10	Triple	Terminal, Turret, TH, Triple	Keystone	1598-2	Keystone1598-2
41	4	TP3, TP6, TP8	SMT	Test Point, Miniature, SMT	Keystone	5015	Testpoint_Keysto ne_Miniature
42	3	U1		Wide Input Range Dual Synchronous Buck Controller, RHA0040C	Texas Instruments	LM5140RHA	RHA0040C
43	1	C4, C40, C41	82 µF	CAP, Aluminum Polymer, 82 µF, 16 V, ±20%, 0.03 Ω, D6.3xL5.8mm SMD	Wurth Elektronik	875105344009	D6.3xL5.8mm
44	0	C12, C36	1000 pF	CAP, CERM, 1000 pF, 100 V, ±5%, C0G/NP0, 0805	TDK	C2012C0G2A102J	0805
45	0	R8, R22	1	RES, 1.00, 1%, 0.5 W, 1206	Stackpole Electronics Inc.	CSR1206FK1R00	1206

## 7.3 Layout Prints

To download the layout prints for each board, see the design files at <http://www.ti.com/tool>.



**Figure 7-2. EVM Top Layer Silkscreen**



**Figure 7-3. EVM Top Copper Layer**

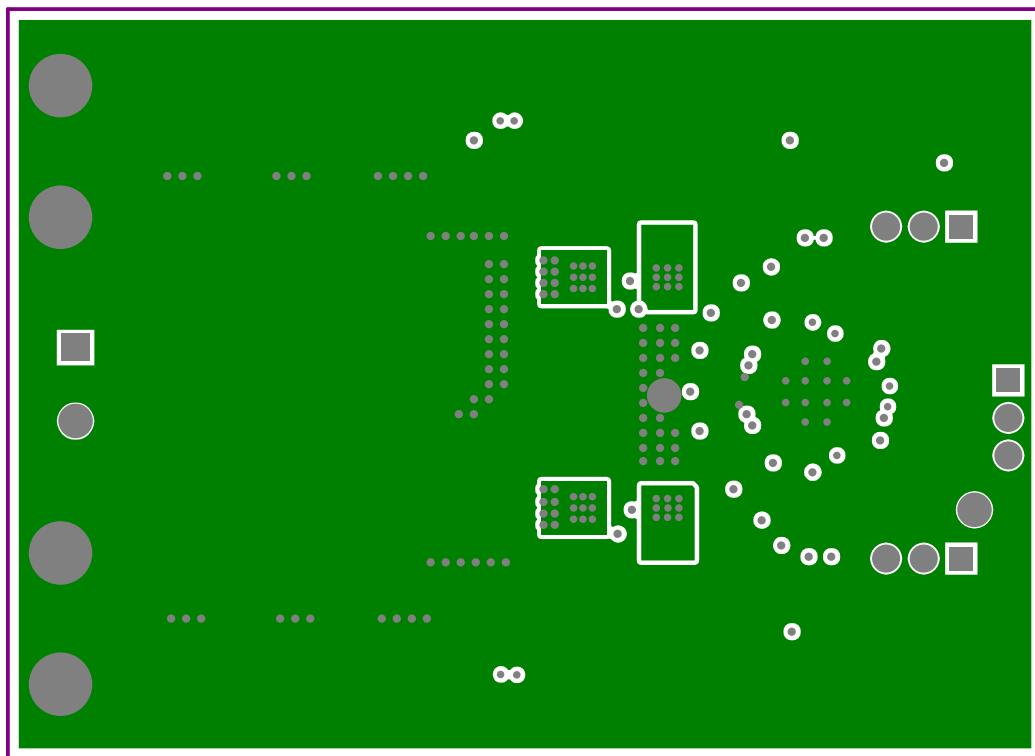


Figure 7-4. EVM Middle Layer 1

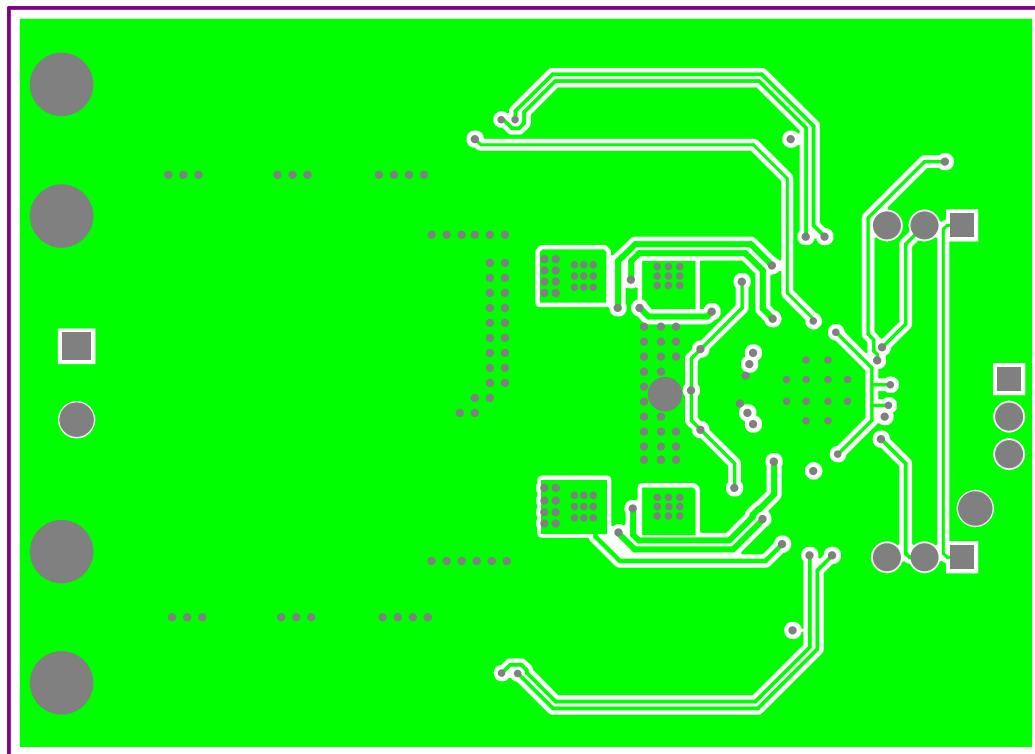


Figure 7-5. EVM Middle Layer 2

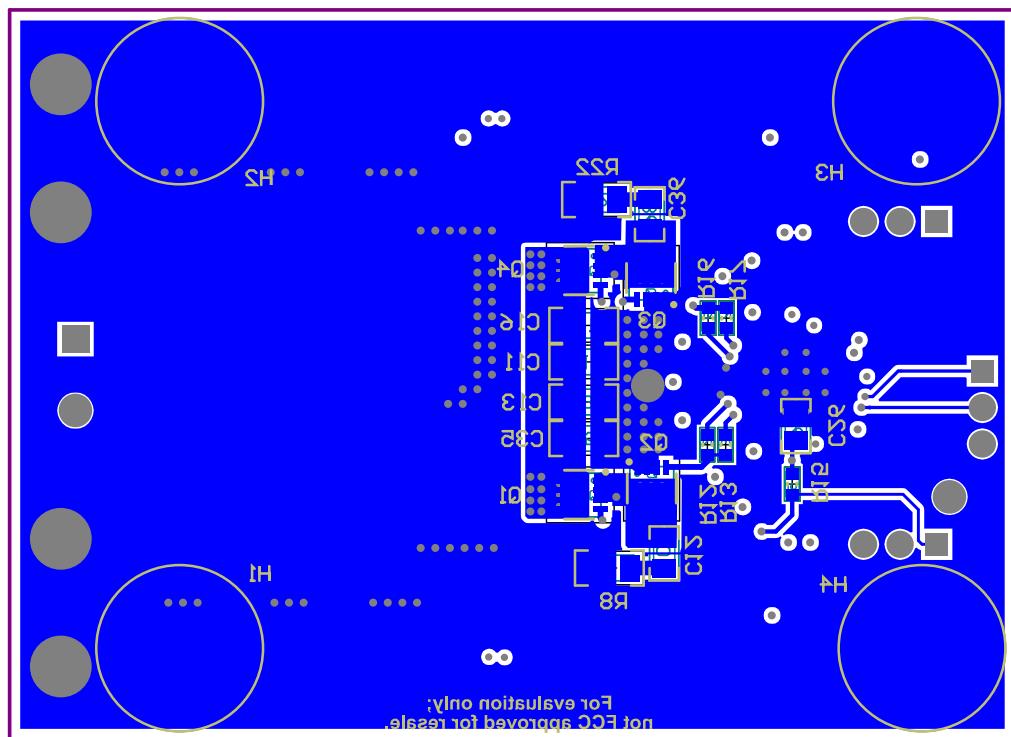


Figure 7-6. Bottom Layer Silkscreen

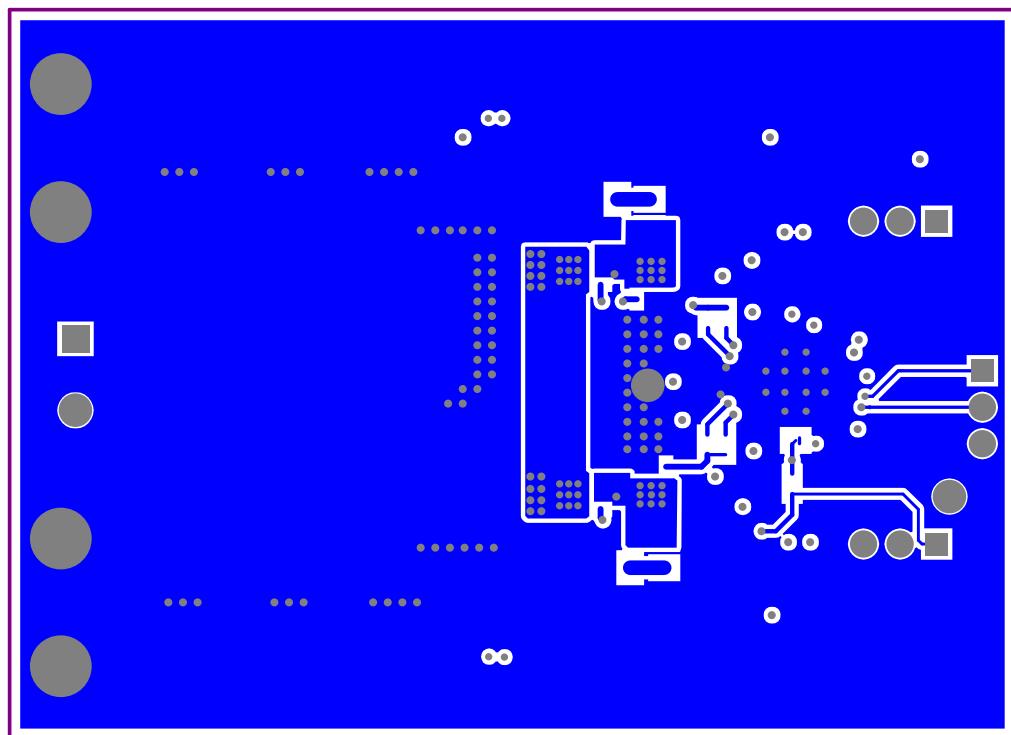


Figure 7-7. EVM Bottom Copper Layer

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