Creating a Sequencing Voltage Supervisor (Reset IC) Using TPS386000 and LM3880

Introduction

This Texas Instruments TechNote explains how to create a 3-channel voltage supervisor with programmable power-up and power-down sequencing, optional manual reset, as well as a watchdog timer monitoring feature. In an application with multiple voltage rails such as a FPGA or processor, this circuit can be used to detect under-voltage conditions, ensure all voltage rails are above their respective voltage thresholds before implementing a power up sequence, and protect the data being written into memory by implementing a power down sequence in case of a power loss.

Circuit Configuration

The circuit consists of a multi-channel voltage supervisor, TPS386000, which monitors 3 supply voltage rails, a watchdog timer and a manual reset. The manual reset ($\overline{MR}$) pin from the TPS386000 connects to the enable (EN) pin of a 3-channel sequencer. This allows the voltage supervisor to control when the sequencer should power up and power down. The power-up and power-down timing delays and sequence are dependent on the version of LM3880. For this example, we are using LM3880MF-**1AA**. The **1** represents the power-up sequence order 1-2-3 and power-down sequence order 3-2-1. The **AA** represents 10ms enable and the sequence start and between each rail. Other sequence and delay options are available and if you want a programmable time delay for each rail, then use LM3881. The LM3880 voltage sequencer's outputs (EN_1 through EN_3) are pulled up via pull-up resistors to the 3 supply rails and the outputs are used to power an application, such as a FPGA or Microprocessor.

Power-Up Sequence

The TPS386000 voltage supervisor monitors all 3 supply rails via sense inputs SENSE2, SENSE3 and SENSE4. SENSE1 is monitoring the VCC input of the supervisor itself. The outputs ($\overline{RESET1}$ through $\overline{RESET4}$) are tied together and pulled up to VCC via pull-up resistors (required for an open-drain type supervisor). Also the Manual Reset ($\overline{MR}$) pin controls the state of $\overline{RESET1}$. Only when the voltage rails tied to SENSE1 through SENSE4 are above their respective voltage thresholds and $\overline{MR}$ is logic high, $\overline{RESET1}$ through $\overline{RESET4}$ will release and get pulled up to VCC. As the output pin of TPS386000 is tied to the ENABLE pin of the LM3880, this enables the LM3880 to start its power-up sequence only when the supply voltage are good. If any one of the $\overline{RESET}$ pins on the TPS386000 is low, as they are all tied together, then the total supervisor output will keep $\overline{RESET1}$ low (regardless if SENSE1 is good) and LM3880 won't enable the power-up sequence. This ensures all 3 monitored supply rails, as well as VCC, have to be above their respective voltage thresholds before the solution can begin sequencing.

When LM3880MF-1AA becomes enabled, it waits 10ms, and then releases EN_1 connected to FLAG1 so it gets pulled high to enable SUPPLY_1. After another 10ms, the power-up sequence continues and the sequencer releases EN_2 connected to FLAG2 so it gets pulled high to enable SUPPLY_2. After a final 10ms, the power-up sequence concludes and the sequencer releases EN_3 connected to FLAG3 so it gets pulled high to enable SUPPLY_3. This completes the power-up sequence.

Power-Down Sequence

The power-down sequence initiates if any of the supplies connected to SENSE1 through SENSE4 exhibit an under-voltage condition. As $\overline{RESET1}$ through $\overline{RESET4}$ are all tied together, any $\overline{RESET}$ getting pulled low will automatically pull the other $\overline{RESET}$ pins low. This forces the ENABLE on the LM3880 to get pulled low which triggers the LM3880 to enter a power-down sequence.

Also featured is a MASTER RESET pin connected to an external push button. By pressing the push button, the $\overline{MR}$ pin on the TPS386000 gets pulled low (regardless of the state of SENSE1), which will force ENABLE on the LM3880 low. This will disable the LM3880 and cause it to enter a power-down sequence.

When LM3880MF-1AA becomes disabled, it waits 10ms, and then EN_3 connected to FLAG3 will get pulled low. Then after another 10ms, EN_2 connected to FLAG2 gets pulled low. After a final 10ms, EN_3 connected to FLAG3 gets pulled low. This completes the power-down sequence.

Table 1. Alternative Device Recommendations

Device	Optimized Parameters	Performance Trade-Off
LM3881	Programmable Sequence Delay	size

Appendix A Schematics

A.1 Typical Application

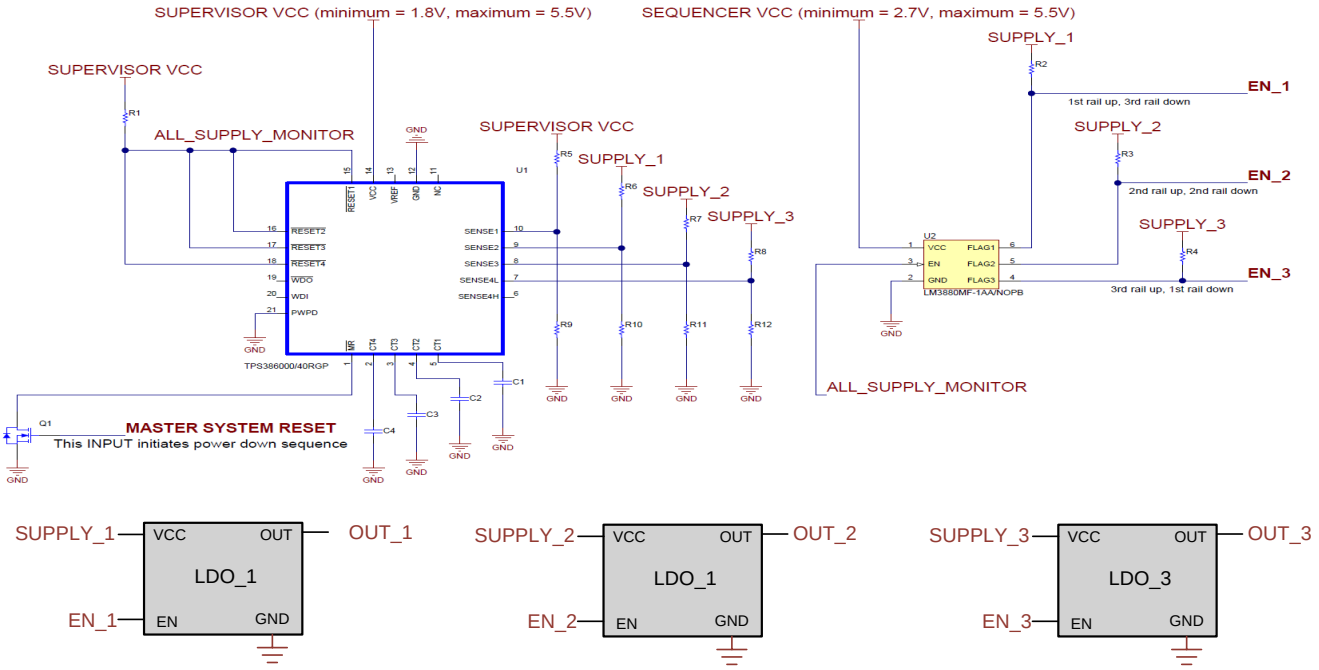

Figure 1. Sequencing Supervisor Schematic

NOTE: The voltage regulators (LDO_1, LDO_2, and LDO_3) can be replaced with pass PFETs and the EN_1, EN_2, and EN_3 signals coming from the LM3880 can be used to control the gates of the pass PFETs if no voltage regulation is required.

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