

LP8860-Q1 Electrical Overstress Analysis and Recommendation

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ABSTRACT

The LP8860-Q1 is an automotive high-efficiency LED driver that has boost controller and four high-precision current sinks. Clean silicon is expected to perform as specified by the [LP8860-Q1 data sheet](#) when operated under normal operation. There are several root causes that could potentially be associated to electrical overstress (EOS) damage inherent to integrated circuits. This application report discusses some details about models, examples, solutions, and best practices associated to EOS damage induced by external applications and procedures using LP8860-Q1.

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1 Overview of Common EOS Failure Models: An Applications and Procedure Perspective

1.1 The Electric Short Circuit (ESC) Model

The ESC model captures well several EOS cases attributed to external applications and procedures that can induce EOS-related damage to LP8860-Q1. This ESC model is based on the system behavior to the unit step response with fast transient response, overshoot, and oscillation, similar to that observed on the unit step response for a standard second-order system in underdamped cases. When such step response is triggered by a given node (aggressor) that has a high enough voltage level, high levels of energy can be transferred to other nodes (victims) that may ultimately exhibit fast rising time and voltage peak levels that can damage internal ESD protection structures.

The voltage level on the aggressor node and the RLC parasitic model along the aggressor-victim path defines characteristics such as the ringing pattern, overshoot voltage peak levels, and the settling time affecting the victim nodes. Figure 1 shows a typical ESC model circuit, and Figure 2 is the simulation result of the V2 node in Figure 1 for different a V1 voltage level from 20 V to 50 V with 10-V voltage increment. The SW switch is closed when an accidental short happens. The peak voltage of the ringing at the V2 node after short accident can be 80% higher than the DC voltage at the V1 node.

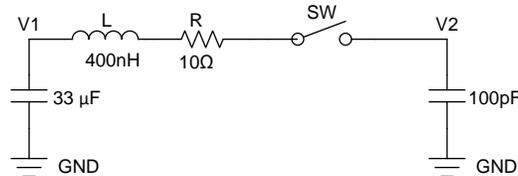


Figure 1. ESC Model Circuit

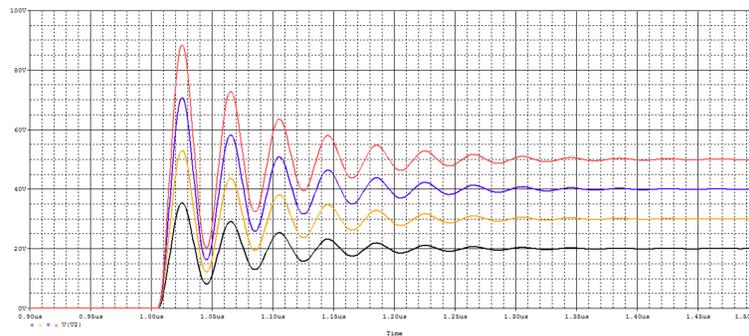


Figure 2. Simulation Results Using ESC Model

Figure 3 gives simulation result for different inductance value at V1 = 40 V. The green line shows a 400-nH inductance value, and the red line shows an 800-nH inductance value. Large inductance results large peak voltage of the ring and longer damping period.

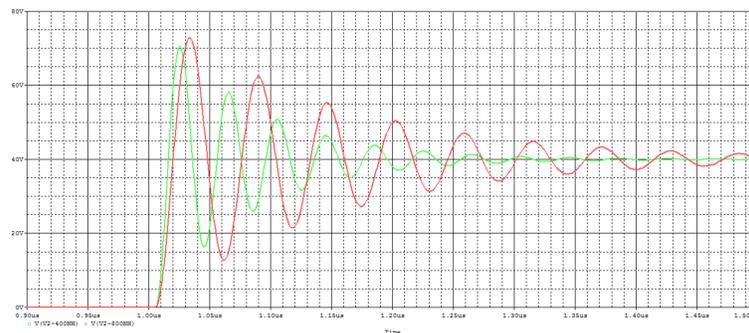


Figure 3. Parasitic Dependency on ESC Model

2 Examples of Implementation of ESC Model via Applications / Procedures That Can Lead to EOS Damage

2.1 Cabling/De-Cabling Procedures

Certain cabling/de-cabling procedures in conjunction with the discharge dynamic of the boost capacitors (C_{OUT}) of LP8860-Q1 can potentially lead to EOS damage if C_{OUT} is still charged and the aggressor node (C_{OUT}) is shorted with other victim pins such as output pins (OUTx).

2.1.1 Plugging LED Display/Load Board

One possible scenario would be during cabling procedures between the main board with LP8860-Q1 and the LED display / load board. For example, If the main board has previously been powered up when no display board is connected to LP8860-Q1, the boost output capacitor (C_{OUT}) would initially get highly charged (approximately 50-V open led string fault detection) before connecting the display board to the main board. Under these conditions, accidental electric shorts between the approximately 50-V C_{OUT} node and other pins can happen if there is any misalignment when plugging the display board to the main board. Flat flex cables are especially conducive for misalignment during its plugging/unplugging.

A further consideration is the slow discharge of C_{OUT} . Because of the slow boost discharge dynamic, even if the main board has been powered down there is still some risk for inducing a short when the main board is plugged back in (for example, for further testing on a different station), and the C_{OUT} has not been previously discharged.

2.1.2 Unplugging LED Display/Load Board

Similarly, another possible scenario is that the display board is disconnected from the main board without being previously powered down. Again, this would raise C_{OUT} voltage to approximate 50 V, and misalignment during the unplugging of the display board can lead to a short with high voltage levels of C_{OUT} .

Figure 4 shows a typical connector between main board and display/LED board.

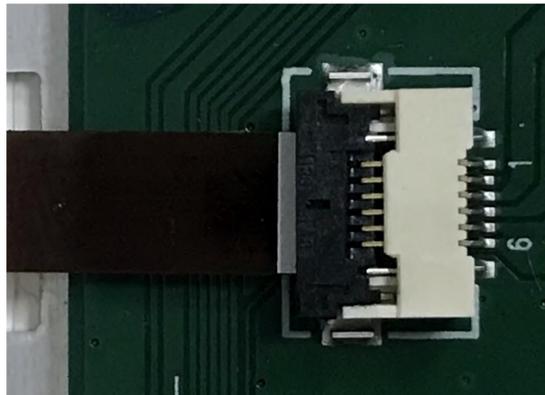


Figure 4. Typical Connector Between Main Board and LED Load

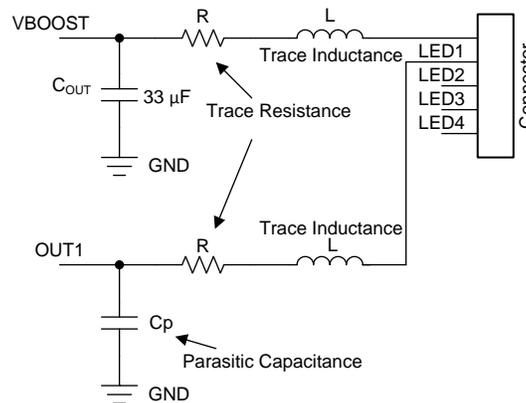


Figure 5. Typical ESC Model for Cabling and De-cabling LED Load From Main Board

As Figure 5 illustrates, the trace inductance, resistance, and the parasitic capacitance are main components building an unexpected RLC network. Normally the value of the parasitic capacitance, C_p is about few to tens pF range depending on the layout. The trace inductance and resistance can be accurately calculated through Equation 1 and Equation 2:

$$R = 1.7 \times 10^{-6} \times \frac{l}{w \times t}$$

where

- w = width of the PCB trace in cm
- l = length of the PCB trace in cm
- t = thickness of the PCB trace in cm
- R is the trace resistance in Ω

(1)

$$L = 2 \times 10^{-3} \times l \times \left[\ln \left(\frac{2 \times l}{w + t} \right) + 0.5 + 0.2235 \times \frac{w \times t}{l} \right]$$

where

- w = width of the PCB trace in cm
- l = length of the PCB trace in cm
- t = thickness of the PCB trace in cm
- L is the trace inductance in μH

(2)

Figure 6 is the simulation result for an accidental short between full charged C_{OUT} and one of OUT pin based on the ESC model as Figure 5 for $L = 140 \text{ nH}$, $R = 191 \text{ m}\Omega$, $C_p = 10 \text{ pF}$ and $V_{BOOST} = 20 \text{ V}$ to 50 V with 10-V increments.

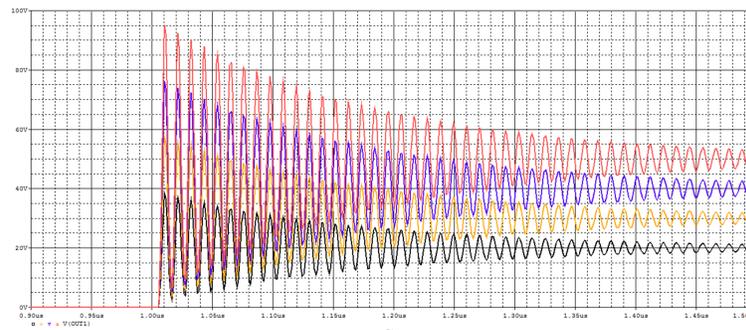


Figure 6. Simulation Result for Cabling and De-cabling ESC Model

2.2 Feedback Divider Without The Appropriated Overvoltage Protection

LP8860-Q1 has the ability to accommodate and provide control for a resistor divider configuration connected to the FB pin in order to increase the output voltage. However, that implementation requires the appropriated overvoltage protection on each one of the active output pins. Failing to do so can lead to reproduction of the ESC model, therefore potentially inducing that one or several output pins can be permanently damaged (for example, shorted to ground).

A consideration is that projections for voltage levels on the output of the boost must not be less than 30% higher than maximum LED string voltage.

3 Preventive Strategies to Minimize EOS Failures Due to ESC Model

3.1 Recommended Power-Up Sequence

- Connect the LED display or any load before powering up LP8860-Q1.
- Power down the main board before disconnecting it from the LED display or any load.

3.2 C_{OUT} Discharge and Pulldown Resistor

Discharge C_{OUT} before plugging/unplugging main board from the display LED board. If fast discharge is required, a resistor can be placed between VBOOST (after C_{OUT} node) and GND. The discharge time depends on the resistor value, C_{OUT} , and discharge voltage limits.

4 Solutions to Minimize EOS Failures Due to ESC Model

4.1 RC Circuit

The RC circuit helps with the ringing reduction and damping of the overshoot voltage. As Figure 7 shows a resistor in serial of LED string and a capacitor on each OUT pin to VBOOST constitutes an RC circuit to prevent the large voltage ringing on each of OUT pins.

Alternatively, the capacitor can be connected to GND instead of VBOOST if required. In that case, at very low brightness dimming ratio can be relatively less optimum.

4.1.1 Recommended Resistor and Capacitor Values

- R = 5.9 Ω
- C = 4.7 nF

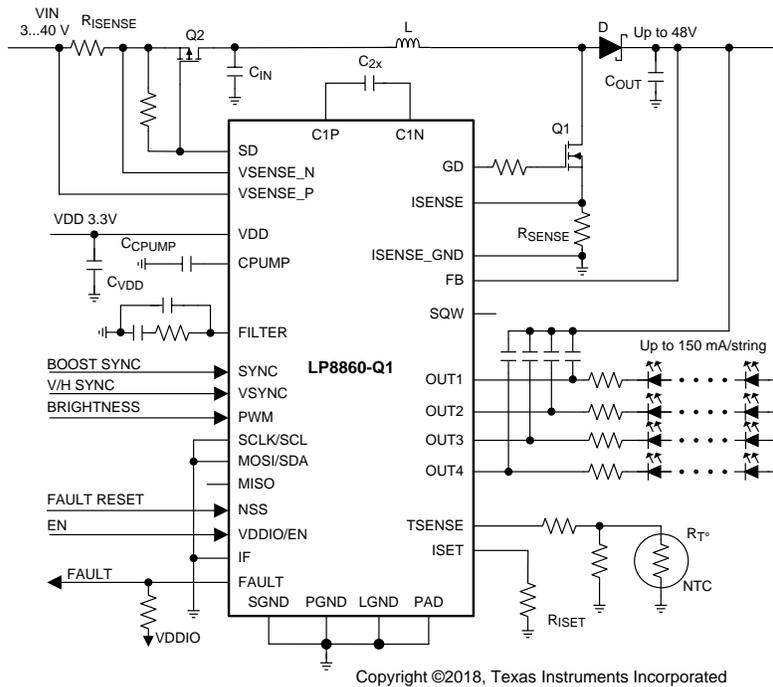


Figure 7. Typical Application Schematic with RC Circuit

4.1.2 Simulation Result

As simulation result in Figure 8, under conditions of 40-V VBOOST, the peak transient voltage with RC implemented in green line is significantly reduced than peak voltage in red line by approximate 30 V, which prevents the OUT pin from EOS damage.

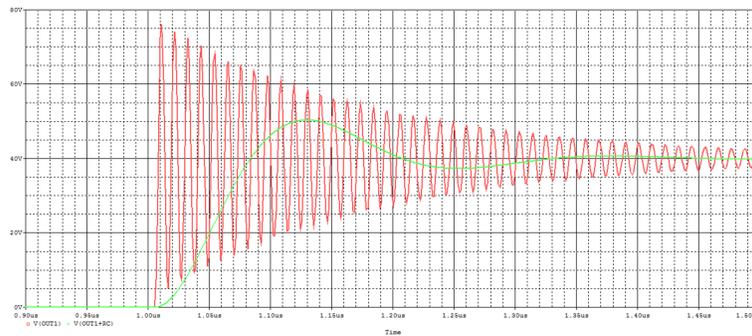


Figure 8. Simulation Result for RC Circuit

4.2 RC Circuit + Diodes

The additional diode connected between each OUT pin and VBOOST builds a voltage discharge path when the ring voltage on OUT pin is higher than the boost output as Figure 9 shows. Also, the value of R can be reduced from 5.9 Ω to 2 Ω to reduce additional power dissipation on the resistors.

Alternatively C_{OUT} can be connected to GND instead of VBOOST if required. In that case, At very low brightness dimming ratio can be relatively less optimum.

4.2.1 Recommended Resistor and Capacitor Values

- R = 2 Ω
- C = 2.2 nF

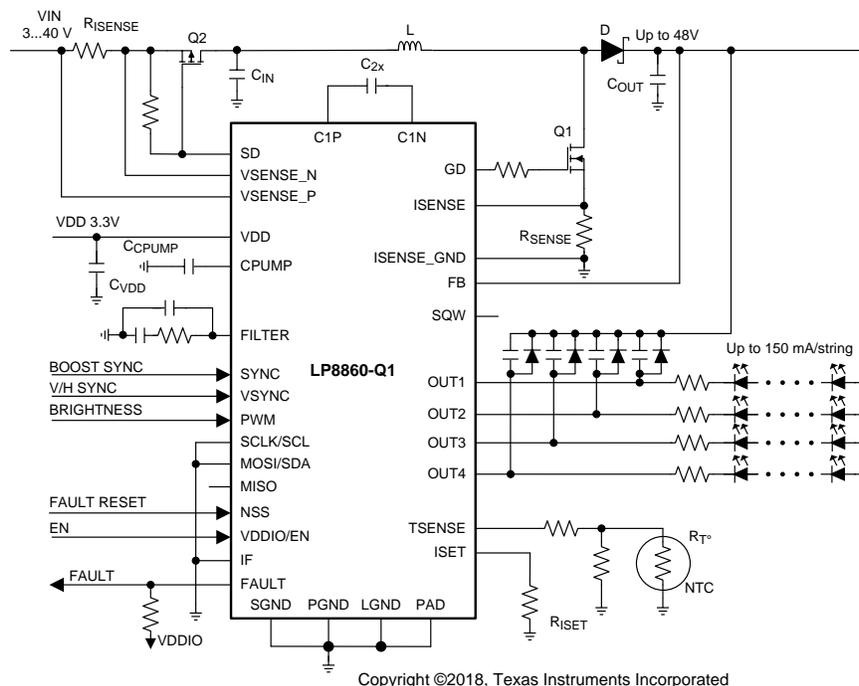


Figure 9. Typical Application Schematic with RC Circuit Plus Diodes

4.2.2 Simulation Result

As the simulation result in [Figure 10](#) shows, under conditions of 40-V VBOOST the peak transient voltage with RC circuit plus diode (green line) is significantly reduced from the peak voltage for RC circuit (red line) by approximate 10 V, which further prevents the OUT pin from damage.

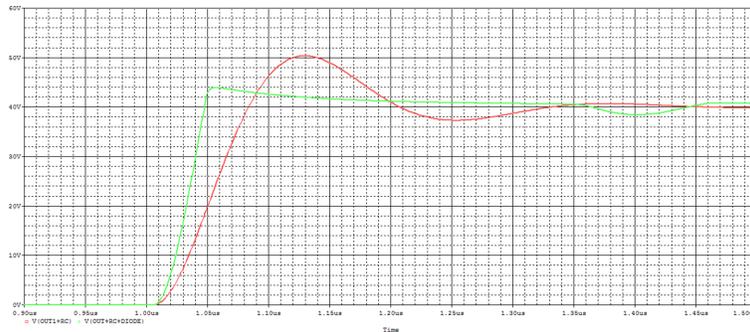


Figure 10. Simulation Result for RC circuit Plus Diodes

4.3 RC Circuit + TVS

Besides the RC and diodes combination, RC and TVS combination is another alternative option to suppress the spike voltage. As [Figure 11](#) illustrates, the cathode of TVS is connected to the end of LED string, and the anode of TVS is connected to the GND. Select the clamping voltage of the chosen TVS to be below the maximum rating of the output pins (OUTx) and slightly above the typical outputs boost voltage. Also, the power rating of the TVS must be able to handle the power dissipation requirements during the transient short or overvoltage events. The TVS can be implemented in the LED load board instead of the main board. Normally the single display/load board is reused to test large volume of the main boards in production line. Implementing the TVS components to each display/load board does not increase the extra component cost and PCB area for the main board.

4.3.1 Recommended Resistor and Capacitor Values

- R = 5.9 Ω
- C = 2.2 nF

5 Best Practice

5.1 EEPROM Programming Sequence

The EEPROM programming sequence should be implemented as provided by the data sheet (*Programming* section), which includes the following provision: PWM outputs and PLL must be disabled when writing to EEPROM registers or burning EEPROM (DISP_CL1_BRT[15:0]=0000h, CL2_BRT[12:0]=0000h, CL3_BRT[12:0]=0000h, CL4_BRT[12:0]=0000h, EN_PLL=0). Therefore, programming register values or burning is not a recommended practice when, for example, the device is already turned on and brightness is set above 0%. Otherwise, register values or burning may not be captured/retained as expected and therefore, target performance could be impacted.

5.2 Cabling to Display / Load board and Power Up/Down Sequence

Refer to [Section 2](#) and [Section 3](#) of the this application note.

5.3 EOS Troubleshooting: List of Questions

The following listed items can help narrow down the possible root-causes for EOS damage.

Table 1. Table with Questions (EOS Troubleshooting)

NO.	ITEM	COMMENTS
1	ATE/x-Ray/Backside Laser Imaging	Provided by Quality
2	PCB layout	Please provide PCB layout including traces going from LP8860-Q1 to the connector
3	Pin arrangement on connector to display/LED board	Please provide the pin arrangement/order on the PCB to display/LED board
4	Schematics involved on the project (not only prototype) and type of load and its voltage drop	Please provide schematics used not only on the prototype but also during production (functional testing) or during any other stage involving testing of LP8860-Q1 (regardless that units have been damaged or not). Schematics information should also show details about any overvoltage protection or clipping circuitry intended to protect OUTx pins of LP8860-Q1 (mounted on LP8860-Q1 PCB or on display unit), target V_{OUT} (# of LEDs and max LED Vf)
5	EEPROM and upload sequence	Please provide the EEPROM used and upload sequence used
6	Cabling/de-cabling	Please provide detail information about the cabling/de-cabling procedure (how and when). For example: Is LP8860-Q1 first powered up and then the LED unit is connected to the PCB (LP8860-Q1)? Or for example: Is LP8860-Q1 being tested in different stations/test-benches and once a given test is completed then LP8860-Q1 PCB is disconnected from LED unit and then connected to another station/test-bench?...
7	Power up sequence and C_{OUT} discharge procedures	Related to the above item but also, is C_{OUT} completely discharged before connecting/disconnecting LP8860-Q1 to any load or display unit?
8	Test that generated failing unit and when the failing unit was generated (during production, unit mounted on car...?)	This information can help to narrow down root-cause and focus on the right direction. Generally provided by quality.

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