Application Report
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How to Configure LMZ30604 Power Module With Ceramic Capacitors

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ABSTRACT

The Simple Switcher LMZ3 module is widely used in space-sensitive applications because of the highly integrated features. The total power solution requires as few as three external components. While some customers prefer to remove the output POSCAP to reduce cost and save space, removing POSCAP causes instability at low temperature. This application report, using the LMZ30604 device as the example, introduces an implementation in which two ceramic capacitors are added paralleled with the divided resistors to solve this issue.

First, this report describes the possible instability issue at low temperature for the LM30604 solution without POSCAP. Second, an accurate peak current mode (PCM) module was built and a forward capacitance compensation method was introduced. Finally, step-by-step calculations, as well as the simulation and test results, were provided to verify the theories. This approach also could be applied to other LMZ3 modules.

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1 Introduction

The LMZ30604 device is power module which combines a 4-A DC-DC converter with power MOSFETs, a shielded inductor, and passives into a low-profile QFN package. This device offers the flexibility and the feature set of a discrete point-of-load design and is ideal for powering performance DSPs and FPGAs.

This power module has been designed with input of 2.95 V to 6 V, and has a loading capability of up to 4 A output current. The few external components, up to 96% efficiency, adjustable frequency and slow-start, programmable under voltage lockout (UVLO), and overtemperature protection configuration benefit the customer design with more compact size, high flexibility, and reliability.

Figure1 indicates LMZ30604 simplified application. The required output capacitance must include at least one 47-µF ceramic capacitor. For applications where the ambient operating temperature is less than 0°C, TI recommends an additional 100-µF POSCAP. However, some customers wish to remove the POSCAP to reduce cost and save space. This action, however, causes instability at low temperature.

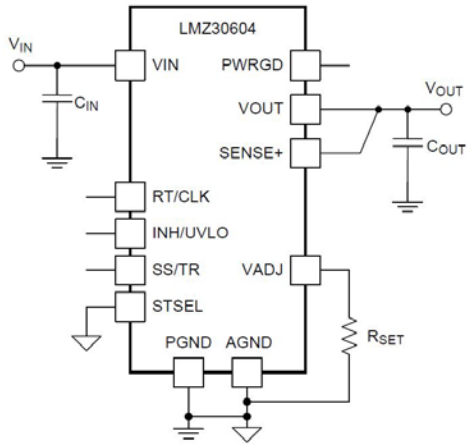
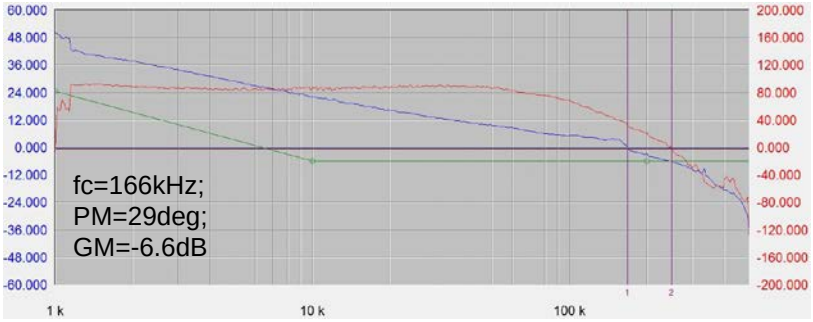
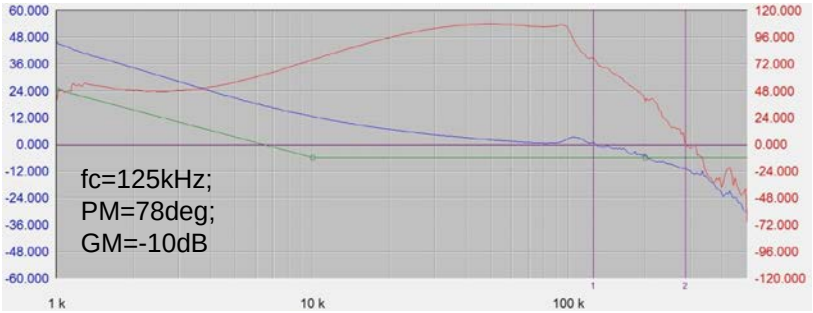


Figure 1. LMZ30604 Simplified Application

Figure 2 shows the Bode plot of LMZ30604 with and without POSCAP solution at low temperature. The test conditions are: V_{in} = 5 V, V_{out} = 1.8 V, Io = 4 A, f_s = 1 MHz, C_{cer} = 47 µF, C_{pos} = 100 µF, L_f = 1 µH. It could be observed that the phase margin of non-POSCAP solution is only 29 degrees and would easily cause an instability issue.



(a) C_{ou} = 47-µF ceramic



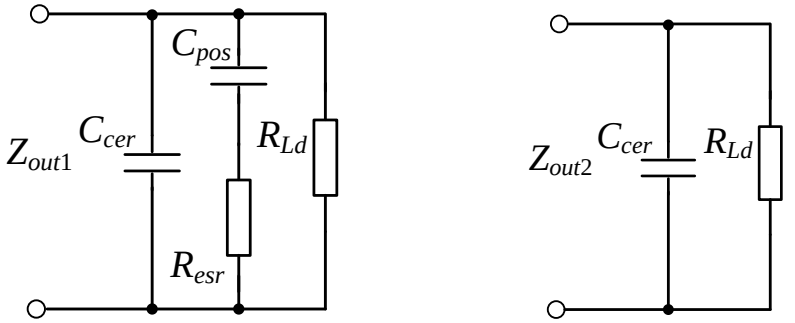
(b) C_{out} = 47-µF ceramic/100-µF POSCAP

Figure 2. Bode Plot Test Results (V_{IN} = 5 V and V_{OUT} = 1.8 V/4 A @ –35°C)

2 Analysis and Solution

2.1 Output Impedance Comparison of With or Without POSCAP Solution

Removing POSCAP changes the output impedance of the converter and influences the crossover frequency and phase margin. Figure 3 shows the two kinds of output impedance.



(a) With POSCAP (b) Without POSCAP

Figure 3. Output Impedance Comparison—With or Without POSCAP

The Z_{out1} and Z_{out2} could be derived as shown in Equations 1 and 2.

$$Z_{out1}(s) = \frac{1}{s \cdot C_{cer}} // \left(\frac{1}{s \cdot C_{pos}} + R_{esr} \right) // R_{Ld} = \frac{\left(C_{pos} \cdot R_{esr} + 1\right) R_{Ld}}{C_{cer} \cdot C_{pos} \cdot R_L \cdot R_{esr} \cdot s^2 + \left(C_{cer} + C_{pos}\right) R_{Ld} \cdot s + 1} \quad (1)$$

$$Z_{out2}(s) = \frac{1}{s \cdot C_{cer}} // R_{Ld} = \frac{R_{Ld}}{1 + R_{Ld} \cdot C_{cer} \cdot s} \quad (2)$$

Draw the Z_{out1} and Z_{out2} Bode plot as shown in Figure 4. It is obvious that when POSCAP is removed, the phase value is much smaller than the default value at approximately 100 kHz, which is the crossover frequency. That is why the phase margin of the solution without POSCAP in Figure 2(b) is not sufficient. Decreasing crossover frequency and thus raising the phase margin could solve this issue.

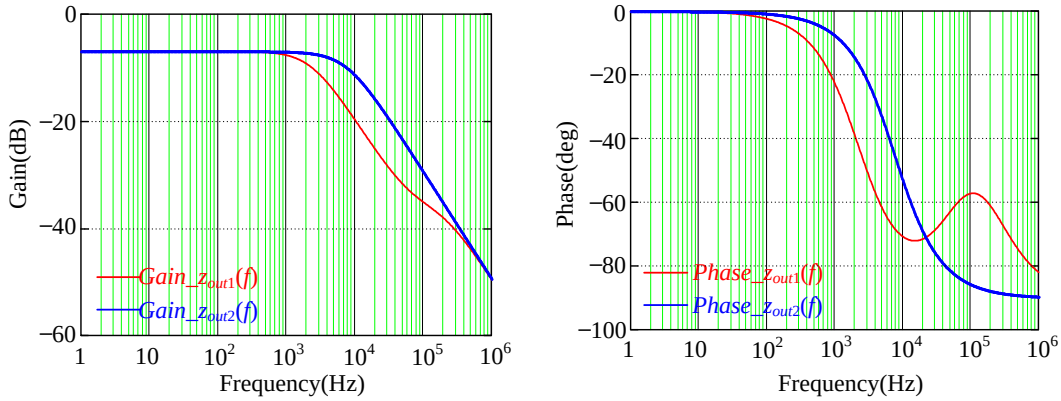


Figure 4. Output Impedance Bode Plot Comparison—With and Without POSCAP

2.2 Accurate PCM Modeling

Figure 5 is the LMZ30604 functional block diagram and Figure 6 is the peak current mode (PCM) overall control implementation. The i_L (inductor current) disturbance includes two parts: V_{in} and duty cycle, which is generated by the comparison of a current sampling ramp and output of the EA (Error Amplifier). Because the current waveform is in conjunction with external ramp, the modulator gain of the circuit F_m is shown in Equation 3:

$$F_m = \frac{1}{(S_n + S_e)T_s} \tag{3}$$

Where:

- T_s is the switching period.
- S_n is the on-time slope of the sensed-current waveform.
- S_e is the external ramp.

In Figure 6, $H_{vi}(s)$ is the input to i_L transfer function and $H_{di}(s)$ is the duty cycle to i_L transfer function. R_i is current sample resistor and $H_e(s)$ is the sample-and-hold system gain function. $G_{EA}(s)$ is the gain function of the error amplifier and $H_{div}(s)$ is the gain of the divided resistor network.

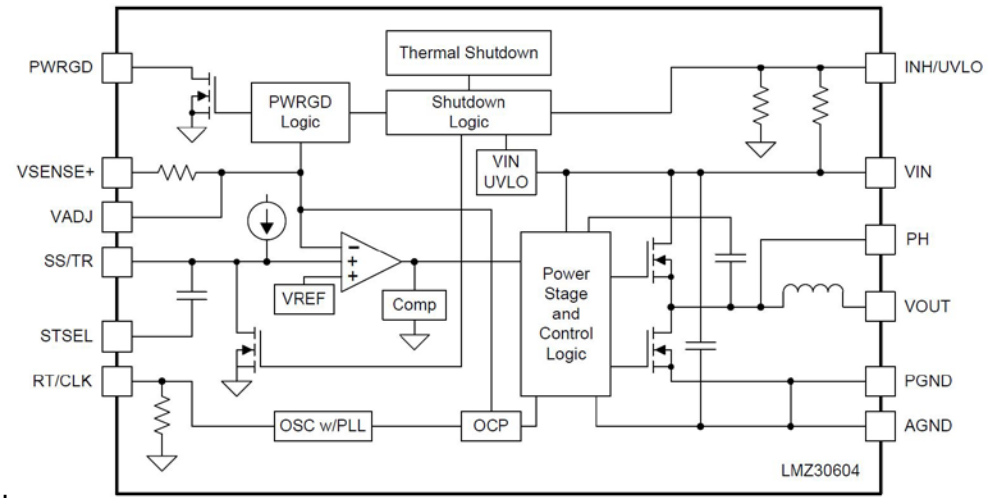


Figure 5. LMZ30604 Functional Block Diagram

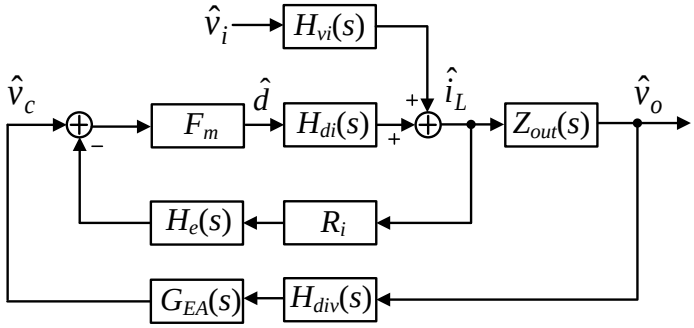


Figure 6. Overall Control Implementation

Figure 7 shows the average small-signal model of CCM buck converter. According to the KCL and KVL principle, Equation 4 and Equation 5 could be derived.

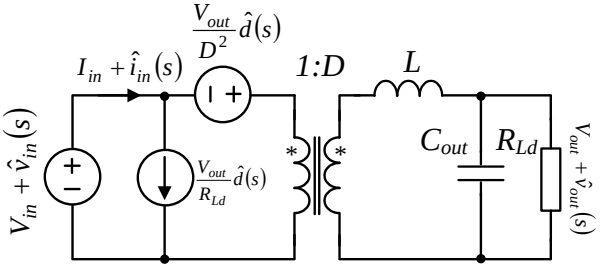


Figure 7. Small-Signal Model of CCM Buck Converter

$$\left[V_{in}+\hat{v}_{in}(s)+\frac{V_{out}}{D^2}\cdot\hat{d}(s)\right]\cdot D=\left[I_L+\hat{i}_L(s)\right]\cdot sL+V_{out}+\hat{v}_{out}(s) \quad (4)$$

$$I_{in} + \hat{i}_{in}(s) = \frac{V_{out}}{R_{Ld}} \hat{d}(s) + \left[I_L + \hat{i}_L(s) \right] \cdot D \tag{5}$$

To separate the small signal disturbance, the gain function from duty cycle to inductor current could be calculated as shown in Equation 6.

$$H_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{in} \cdot (1 + s \cdot R_{Ld} \cdot C_{out})}{R_{Ld} + sL + s^2 R_{Ld} L C_{out}} \tag{6}$$

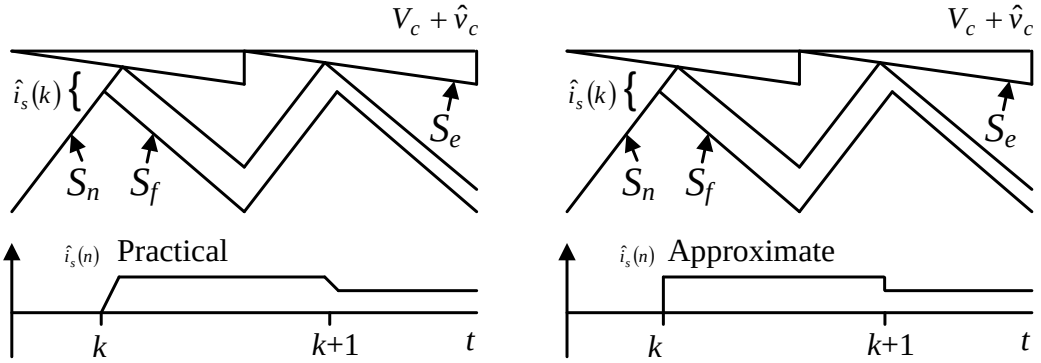
Considering the practical crossover frequency is much higher than the corner frequency with PCM control, simplify Equation 6 into Equation 7.

$$H_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} \approx \frac{V_{in}}{sL} \tag{7}$$

The gain function from V_{in} to inductor current could be calculated as shown in Equation 8.

$$H_{vi}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{D \cdot \left(sC_{out} + \frac{1}{R_{Ld}} \right)}{1 + s\frac{L}{R_{Ld}} + s^2 LC_{out}} \approx \frac{D}{sL} \tag{8}$$

Figure 8 shows the practical and approximated sampling-hold waveforms with the current and control distortion.



(a) Practical (b) Approximate

Figure 8. Sampling-Hold Waveform With Current and Control Distortion

The discrete equation could be derived to describe the sampling-hold behavior:

$$\hat{i}_L(k+1) = -\alpha \cdot \hat{i}_L(k) + \frac{1+\alpha}{R_i} \hat{v}_c(k+1) \tag{9}$$

Where S_f is the inductor current ramp down slope.

$$\alpha = \frac{S_f - S_e}{S_f + S_e} \tag{10}$$

Based on the discrete sampling model and Z(k+1) = Z(k) × k, |Z| domain translation results of Equation 9 should be:

$$H(Z)=\frac{I_L(Z)}{V_c(Z)}=\frac{1+\alpha}{R_i}\frac{Z}{Z+\alpha} \tag{11}$$

With substituting |Z| with $e^{Ts\cdot S}$ and considering zero order sampling-hold gain $(1-e^{-Ts\cdot S})$ / $(T_s\cdot S)$, the gain function could be calculated from Equation 12.

$$H(s)=\frac{1+\alpha}{R_i}\frac{e^{Ts\cdot S}}{e^{Ts\cdot S}+\alpha}\frac{1-e^{-Ts\cdot S}}{Ts\cdot S}=\frac{1+\alpha}{R_iT_sS}\frac{\left(e^{Ts\cdot S}-1\right)}{e^{Ts\cdot S}+\alpha} \tag{12}$$

Ignoring the disturbance of V_{in}, the control block for the current regulation loop can be taken from Figure 6 (see Figure 9).

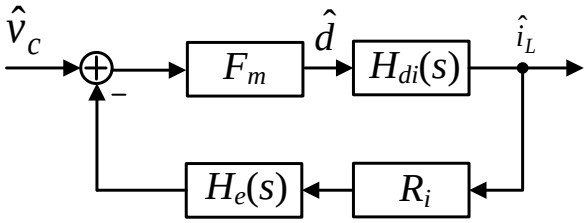


Figure 9. Control Block For Current Regulation Loop

Equation 13 shows the gain function from comp voltage to inductor current.

$$H(s)=\frac{\hat{i}_L(s)}{\hat{v}_c(s)}=\frac{F_m\cdot H_{di}(s)}{1+H_e(s)\cdot R_i\cdot F_m\cdot H_{di}(s)} \tag{13}$$

According to Equations 3, 6, 12, and 13, $H_e(s)$ could be calculated as follows:

$$H_e(s)=\frac{T_s\cdot S}{e^{Ts\cdot S}-1}\approx 1-\frac{S}{2/T_s}+\frac{S^2}{(\pi/T_s)^2} \tag{14}$$

As a result, the approximate gain from control to inductor current should be:

$$H_e(s)\approx\frac{1}{R_i}\frac{1}{1+s\cdot\left[\frac{T_sL_f\cdot(S_n+S_e)}{V_{in}\cdot R_i}-\frac{T_s}{2}\right]+s^2\frac{T_s^2}{\pi^2}} \tag{15}$$

To simulate this accurate PCM control model, the equivalent small-signal model is built (see Figure 10).

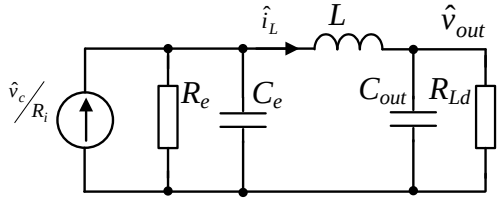


Figure 10. Equivalent Small-Signal Model

Because C_{out} is the approximate shorted circuit at crossover frequency, the gain function from control to inductor current could be calculated as shown in Equation 16.

$$\frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i} \cdot \frac{R_e // (1/sC_e)}{R_e // (1/sC_e) + sL} = \frac{1}{R_i} \frac{1}{1 + \frac{L}{R_e} s + L \cdot C_e \cdot s^2} \tag{16}$$

As a result, R_e and C_e could be calculated as shown in Equation 17.

$$C_e = \frac{T_s^2}{\pi^2 \cdot L}, R_e = \frac{2L}{T_s\left(\frac{2}{1+\alpha} - 1\right)} \tag{17}$$

2.3 Comparison of Simplified and Accurate PCM Modeling

Figure 11 shows a practical LMZ30604 schematic with a 5-V to 1.8-V design.

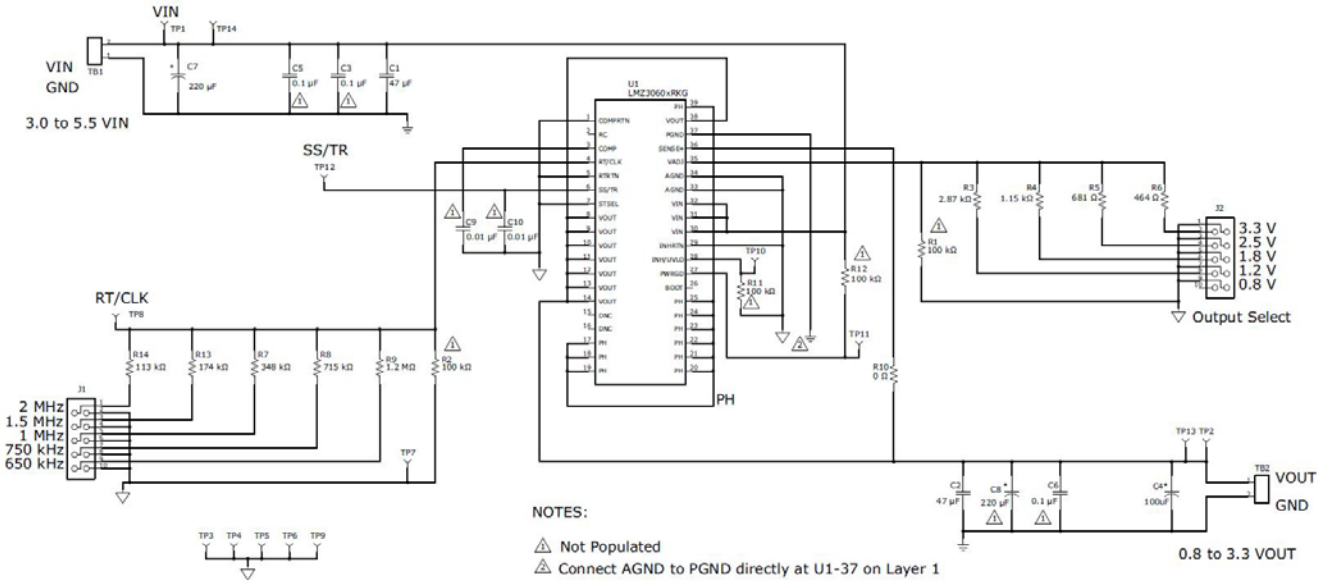


Figure 11. LMZ30604 EVM Schematic

Table 1 lists the relative parameters.

Table1. Modeling Parameters

Vin(V)	Vout(V)	Io(A)	fs(kHz)	L(µH)	RFBT(Ω)	RFBB(Ω)	Ccer(µF)
5	1.8	4	1000	1	1430	1150	47
Cpos(µF)	**Resr(mΩ)**	**Gm(A/V)**	**G_{EA}(µA/V)**	**Ri(mΩ)**	**Se(V/µS)**	**Sn(V/µS)**	**Sf(V/µS)**
100	25	13	218	32	0.18	0.10	0.06
Re(Ω)	**Ce(nF)**	**Rcomp(kΩ)**	**Ccomp(nF)**	**α**			
1.704	101	13	1.8	–0.08			

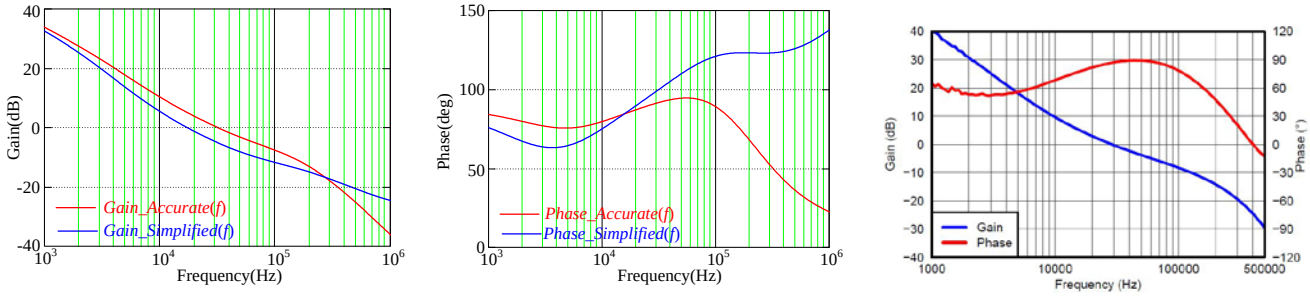
The gain function of loop response could be calculated as shown in Equation 18.

$$T_{Loop}(s) = \frac{R_{FBT}}{R_{FBT} + R_{FBB}} \cdot Z_{out}(s) \cdot G_{EA} \left(R_{comp} + \frac{1}{s \cdot C_{comp}} \right) \cdot H(s), \quad (18)$$

In a simplified PCM, H(s) is approximately equal to G_m. The gain function of a simplified PCM loop response should be:

$$T_{Loop}(s) = \frac{R_{FBT}}{R_{FBT} + R_{FBB}} \cdot Z_{out}(s) \cdot G_{EA} \left(R_{comp} + \frac{1}{s \cdot C_{comp}} \right) \cdot G_m, \quad (19)$$

Figure 12 shows the Bode plot of accurate PCM, simplified PCM, and the one presented in the LMZ30604 data sheet. It is obvious that accurate module more closely matches the data sheet, while the phase margin of the simplified module is higher than reality.



(a) Gain frequency (b) Phase frequency (c) Practical Bode plot

Figure 12. Calculated and Practical Bode Plot

Figure 13 indicates calculated frequency response with and without POSCAP at room temperature. Removing POSCAP enlarges crossover frequency and decreases phase margin, which closely matches test results in Figure 2. Removing POSCAP also causes instability at low temperature because R_{ds}(on) and G_{EA} would change substantially with temperature. One way to resolve the non-POSCAP instability issue is to reduce the crossover frequency.

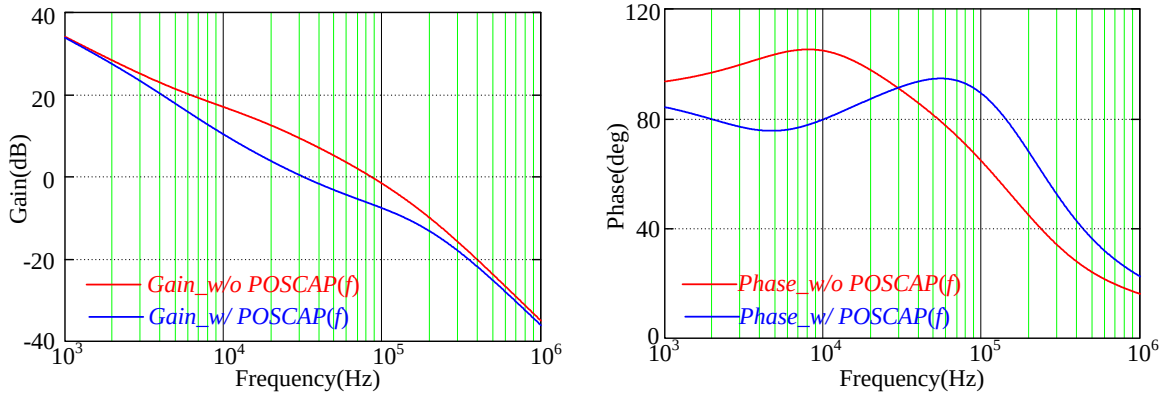
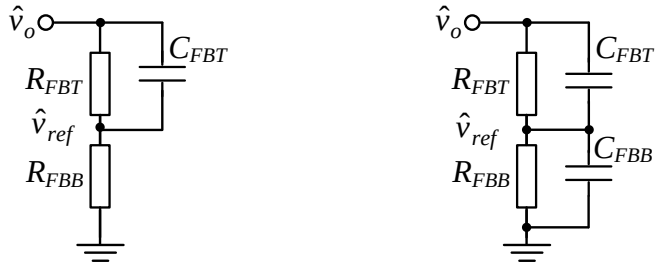


Figure 13. Calculated Bode Plot—With and Without POSCAP

2.4 Two Types of Forward Capacitance Compensation

As LMZ30604 compensation is integrated inside, the R_{comp} and C_{comp} could no longer be changed. Paralleling forward capacitance with divide resistors effectively adjusts loop response, which usually has two types, as shown in Figure 14.



(a) Single-capacitance compensation (b) Dual-capacitance compensation

Figure 14. Two Types of Forward Capacitance Compensation

The gain function of reference voltage to output voltage shown in Figure 14(a) is calculated in Equation 20, which adds a zero-pole to original function.

$$\frac{\hat{v}_{ref}(s)}{\hat{v}_o(s)} = \frac{Z_{FBB}(s)}{Z_{FBB}(s)+Z_{FBT}(s)} = \frac{R_{FBB}}{R_{FBB}+R_{FBT}} \frac{1+s\cdot R_{FBT}\cdot C_{FBT}}{1+s\cdot\left(R_{FBT}\,//\,R_{FBB}\right)\cdot C_{FBT}} \tag{20}$$

The zero and pole frequency can be calculated in Equation 21.

$$f_{z1} = \frac{1}{2\pi\cdot R_{FBT}\cdot C_{FBT}}, f_{p1} = \frac{1}{2\pi\cdot\left(R_{FBT}\,//\,R_{FBB}\right)\cdot C_{FBT}} \tag{21}$$

Figure 15(a) shows the simplified gain frequency of single-capacitance compensation. The dotted line is the original curve, and the solid line is the compensated curve. In this situation, A_{z1}, A_{p1}, f_{c1}, and f_{c2} match Equation 22.

$$\begin{cases} \dfrac{A_z - 0}{\log(f_z)-\log(f_{c1})} = -20 \\ A_p = A_z \\ \dfrac{A_p - 0}{\log(f_p)-\log(f_{c2})} = -20 \end{cases} \tag{22}$$

As a result:

$$\frac{f_{c12}}{f_{c11}} = \frac{f_{p1}}{f_{z1}} = \frac{R_{FBT}+R_{FBB}}{R_{FBB}} \tag{23}$$

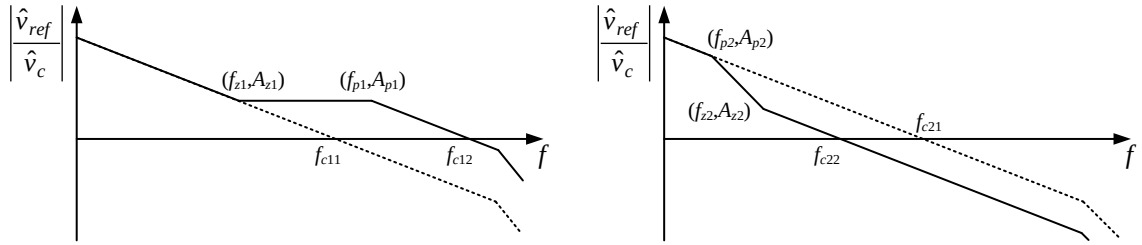
This means the single-capacitance compensation enlarges crossover frequency but could not increase the phase margin. With the same method in dual-capacitance compensation, Equations 24 through 26 could be calculated as follows:

$$\frac{\hat{v}_{ref}(s)}{\hat{v}_o(s)} = \frac{Z_{FBB}(s)}{Z_{FBB}(s)+Z_{FBT}(s)} = \frac{R_{FBB}}{R_{FBB}+R_{FBT}} \frac{1+s\cdot R_{FBT}\cdot C_{FBT}}{1+s\cdot(R_{FBT}\,//\,R_{FBB})\cdot(C_{FBT}+C_{FBB})} \quad (24)$$

$$f_{z2} = \frac{1}{2\pi\cdot R_{FBT}\cdot C_{FBT}}, f_{p2} = \frac{1}{2\pi\cdot(R_{FBT}\,//\,R_{FBB})\cdot(C_{FBT}+C_{FBB})} \quad (25)$$

$$\frac{f_{c22}}{f_{c21}} = \frac{f_{p2}}{f_{z2}} \quad (26)$$

Because f_{p2} and f_{z2} are relative to C_{FBT} and C_{FBB}, the fc22 could be located at any frequency to adjust the phase margin.



(a) Single-capacitance compensation (b) Dual-capacitance compensation

Figure 15. Two Types of Forward Capacitance Compensation Gain Frequency Response

3 Parameter Design and Verification

3.1 LMZ30604 Forward Capacitance Design Procedure

The following steps were used to verify the forward capacitance design for the LMZ30604.

1. Calculate the original crossover frequency with Mathcad, here f_{c2} = 95.4 kHz.
2. Set the compensated crossover frequency f_{c1} = 30 kHz, which is the same as the crossover frequency of non-POSCAP solution at room temperature.
3. Set zero frequency f_z = 3 kHz, to achieve the pole frequency, as in Equation 27.

$$f_p = \frac{f_{c1}}{f_{c2}}\cdot f_z = 895\text{Hz} \quad (27)$$

4. Calculate C_{FBT}:

$$C_{FBT} = \frac{1}{2\pi\cdot R_{FBT}\cdot f_z} = 37.1nF \quad (28)$$

Here choose C_{FBT} = 39 nF.

5. Calculate C_{FBB}:

$$C_{FBB} = \frac{1}{2\pi\cdot(R_{FBT}\,//\,R_{FBB})\cdot f_p} - C_{FBT} = 228.1nF \quad (29)$$

Here choose C_{FBB} = 220 nF.

3.2 Simulation and Experiment Verification

The overall small-signal modeling by TINA can be attained as shown in Figure 16. Figure 17(a) shows the AC simulation results, which revealed a crossover frequency of 36.6 kHz and a phase margin of 86.5 degrees. Figure 17(b) shows the test results, which revealed a crossover frequency of 30 kHz and a phase margin of 80 degrees. The matched results verified that the accurate PCM module built in Section 2 is correct.

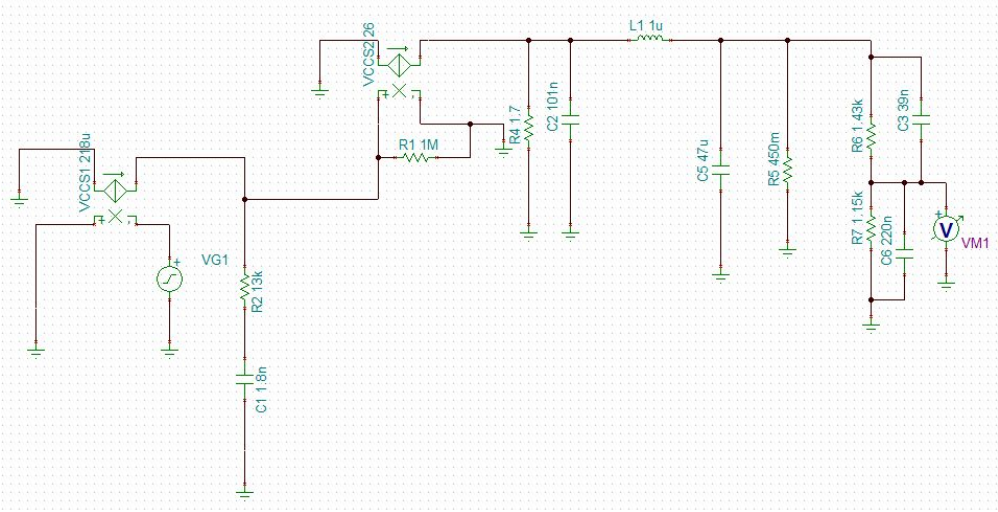
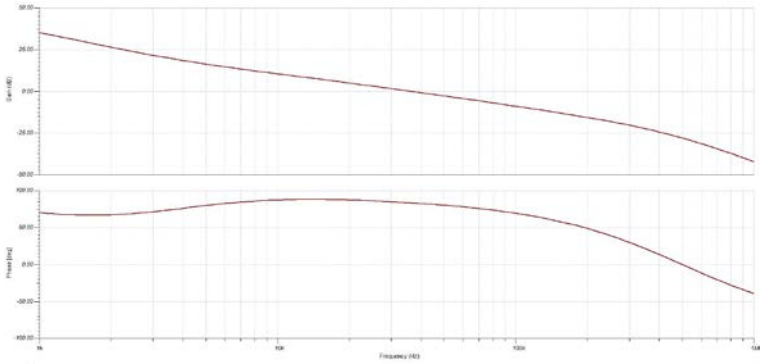
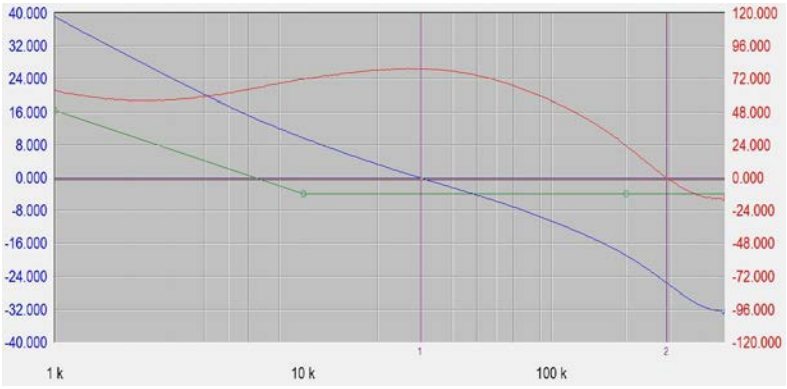


Figure 16. Overall Small-Signal Modeling for LMZ30604



(a) Simulation results



(b) Test results

Figure 17. Bode Plot Comparison of Simulation and Test Results

Figure 18 shows the compensated Bode plot at low temperature, which has a much higher phase margin than Figure 2(b). This means LMZ30604 could also work normally at low temperature even without POSCAP after compensation**.**

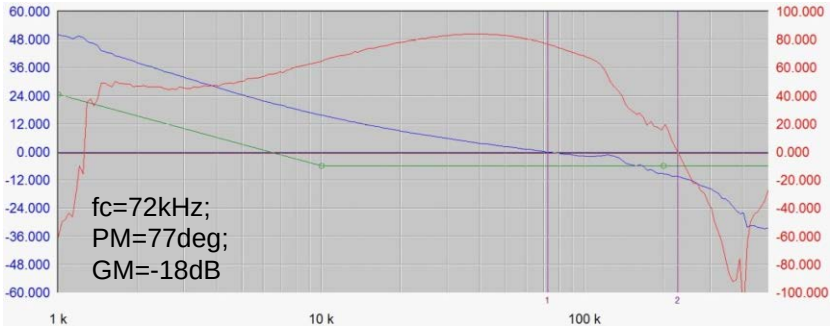
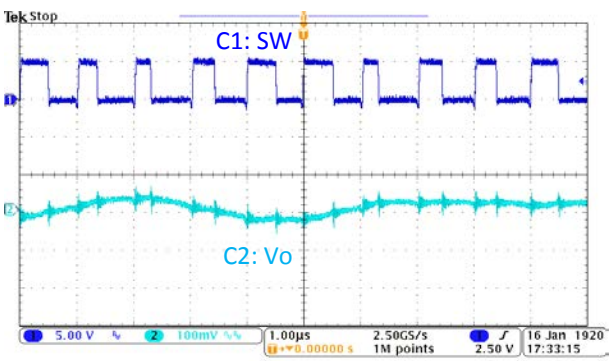
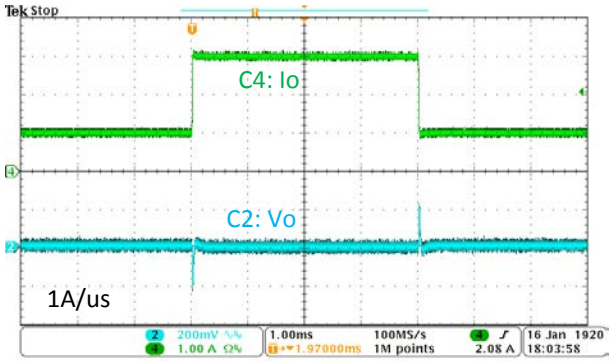


Figure 18. Bode Plot of Non-POSCAP Solution After Compensation @ –35°C

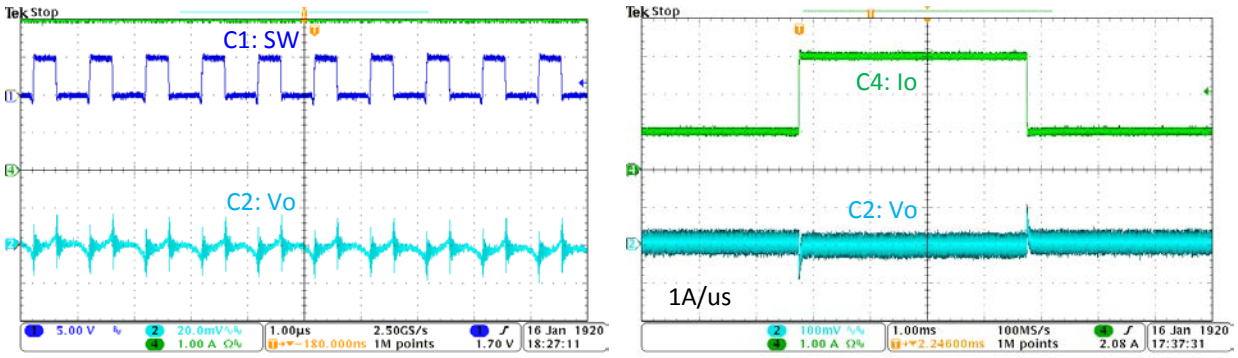
Figure 19 shows the steady-state and load transient performance with and without forward capacitance @ –35°C. Test conditions are: Vin = 5 V, Vout = 1.8 V; Io = 4 A (steady-state) or 1 A to 3 A with 1 A/µs slew rate (load transient). The LMZ30604 module would have a low-frequency ripple at output in no CFB situation; adding the forward capacitance would help improve this performance, and thus verify the frequency analysis well.



(a) Steady-state without C_{FB}



(b) Load transient without C_{FB}



(c) Steady-state with C_{FB} (d) Load transient with C_{FB}

Figure 19. Comparison of Steady-State and Transient Performance @ –35°C

4 Conclusion

Removing the output POSCAP would cause the LMZ30604 module to have an instability issue at low temperature. This application built an accurate PCM module, compared a simplified PCM module, and then determined the simplified solution, which would have a higher phase margin. Two types of forward capacitance compensated methods (single- and dual-capacitance) were compared. The dual-capacitor compensated method proved to solve this low-temperature instability issue. Mathcad calculation, TINA simulation, and test results are used to demonstrate this solution.

References

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2. TPS54418 data sheet, SLVS946C, Texas Instruments
3. Tony Huang*, TPS65270 Loop Compensation Design Consideration,* SLVA510*,* Texas Instruments
4. Jian Li, Fred C. Lee, *New Modeling Approach for Current-Mode Control,* 2009 IEEE

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