Application Report
SNVA009AI–September 1999–Revised December 2019

AN-1112 DSBGA Wafer Level Chip Scale Package

ABSTRACT

This application note provides information on handling, assembly, and usage of the die-sized ball grid array (DSBGA) wafer chip scale package (WCSP).

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Trademarks

PicoStar is a trademark of Texas Instruments.
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1 Introduction

This application note provides guidelines and recommendations for wafer chip scale packages (WCSP). WCSP is a package type that is completely processed in wafer form; and when singulated, the package is complete. In this document, the following references are included:

- Package descriptions
- Surface mount assembly considerations
- PCB layout

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- Thermal characterization

2 DSBGA Technology Description

Die-sized ball grid array (DSBGA) is the broader term for WCSP technologies with the following features:

- Package size equal to die size
- Smallest footprint per I/O count
- Interconnect layout available in 0.3-mm, 0.35-mm, 0.4-mm, or 0.5-mm pitch
- No interposer between the silicon IC and the printed circuit board
- TI DSBGA solutions include Standard WCSP, PicoStar™, and PowerWCSP
- TI DSBGA products are designed and tested to ensure excellent board-level thermal cycling reliability without the need for underfill in intended applications. If a customer chooses to underfill a DSBGA product, TI recommends following the guidelines below to maximize reliability.
- The underfill fillet should extend partially up the die edges. Underfill that ends at the bottom (ball side) of the die will degrade reliability.
- The underfill should have a CTE closely matched to the CTE of the solder interconnect.
- The underfill should have a Tg above the expected maximum exposure temperature.

Typical DSBGA products have solder bumps located on the active side of silicon IC. The DSBGA manufacturing process steps include the following:

- Standard wafer fabrication process
- Wafer re-passivation
- Deposition of solder bumps on I/O pads
- Backgrinding
- Application of protective encapsulation coating
- Testing using wafer sort platform
- Laser marketing
- Singulation
- Packing in tape and reel

The package is assembled on PCB using standard surface mount assembly techniques (SMT).

2.1 Standard WCSP

Packages are available in standard bump arrays ranging from 2 x 2 to 11 x 11. Standard pitch options are 0.3, 0.35, 0.4, and 0.5 mm with package heights ranging from 0.35 to 0.55 mm. Please contact a TI sales representative for available combinations.

The cross section drawings in Figure 1 show two types of standard WCSP bumping technologies.

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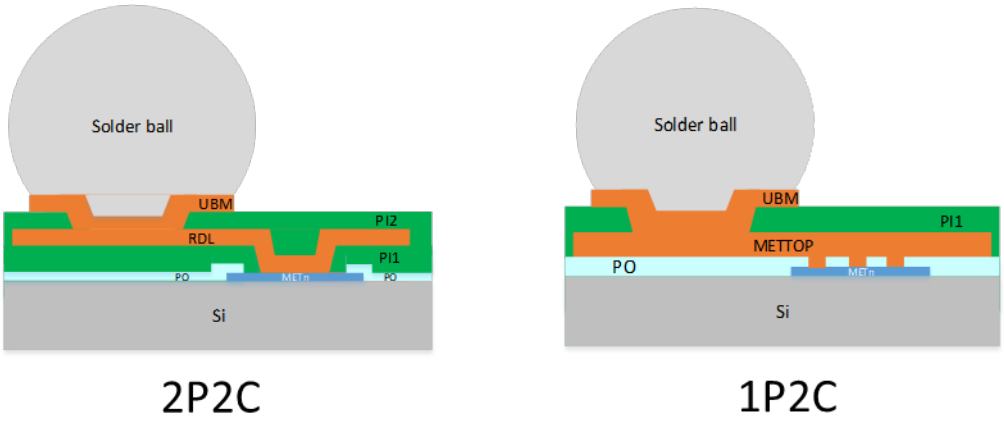

Figure 1. Standard WCSP Cross Sections

2.2 Power WCSP

PowerWCSP is an enhanced WCSP package capable of having low package profile (maximum 0.3-mm thickness). The unique bump structure depicted below improves thermal performance and current carrying density compared to standard WCSP packages.

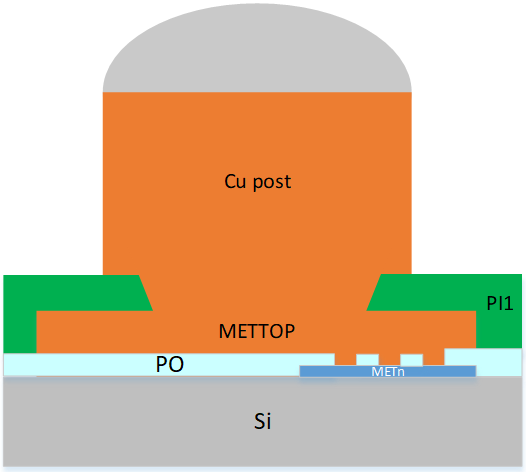

Figure 2. PowerWCSP Cross Section

2.3 PicoStar

PicoStar is another type of DSBGA solution TI provides, including embedded PicoStar and PicoStar SMT. Embedded PicoStar gives the customer the ability to insert it into a substrate. This increases the versatility of the package for various applications including embedded and system in package (SiP) solutions. PicoStar SMT provides the smallest possible package height, and is applicable to smaller packages. Please contact a TI sales representative for more information regarding.

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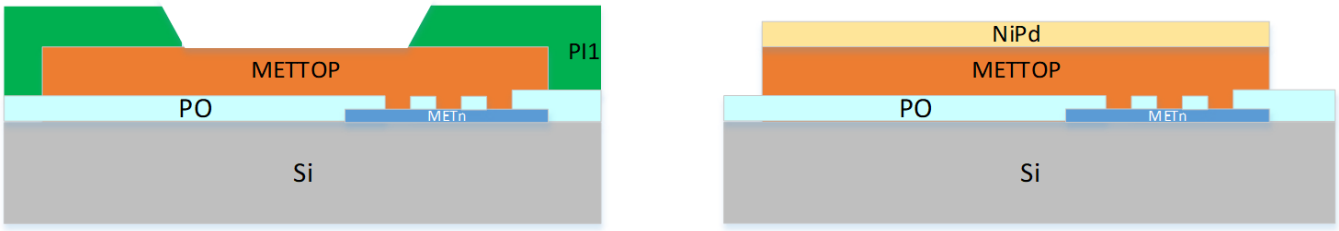

Figure 3. Embedded PicoStar (Left) and PicoStar SMT (Right) Cross Section

2.4 Attributes Applicable for All Technologies

2.4.1 MSL/Storage

The Moisture Sensitivity Level (MSL) indicates the floor life of the component kept at or below conditions of 30°C and 60% RH. All DSBGA packages are ranked as level 1. Refer to JEDEC for conditions.

Table 1. MSL Classifications

LEVEL	FLOOR LIFE
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Time on label

2.4.2 Tape and Reel Information

DSBGA units are contained within Tape and Reel (T and R) configurations, which are intended to protect devices from damage during transportation and storage. Figure 4 is an example of T and R dimensions provided in the data sheet of each device.

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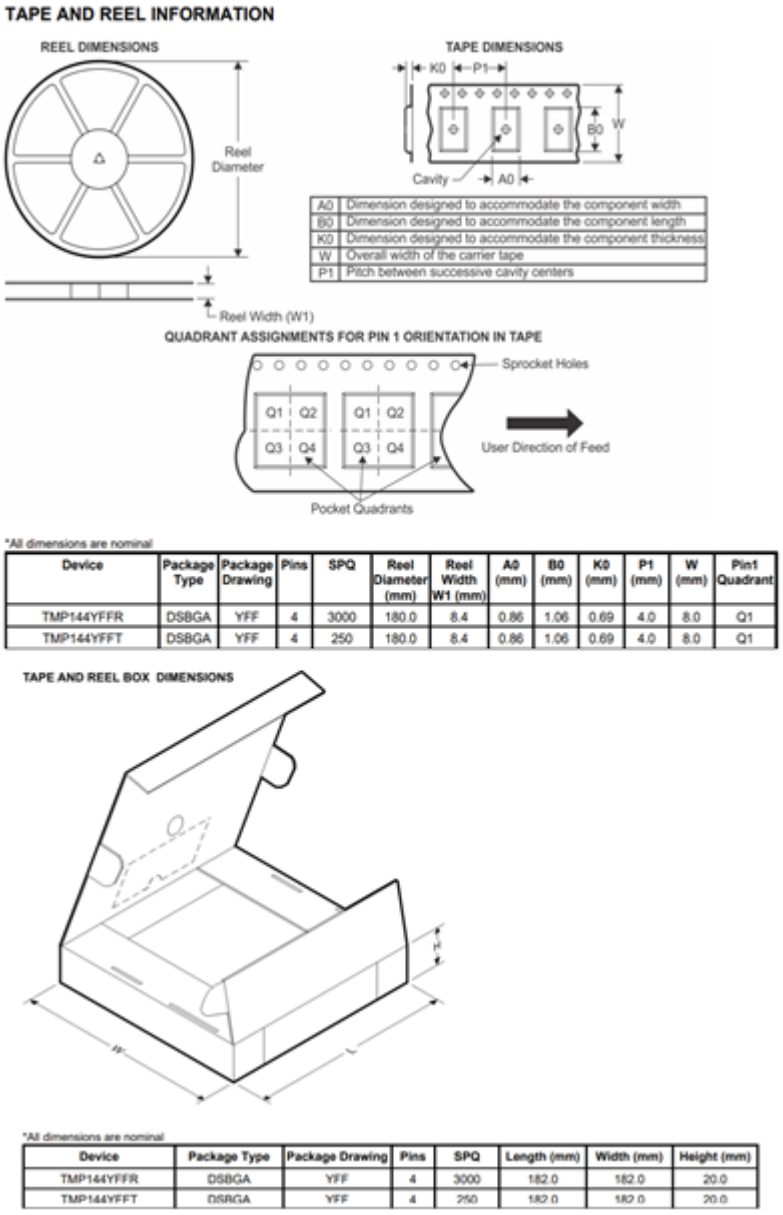

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP144YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.86	1.06	0.69	4.0	8.0	Q1
TMP144YFFT	DSBGA	YFF	4	250	180.0	8.4	0.86	1.06	0.69	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP144YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TMP144YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0

Figure 4. Tape and Reel Information (Example)

2.4.3 ePOD

Figure 5 illustrates an example of an enhanced package outline drawing (ePOD). Refer to the TI data sheet for device specific information.

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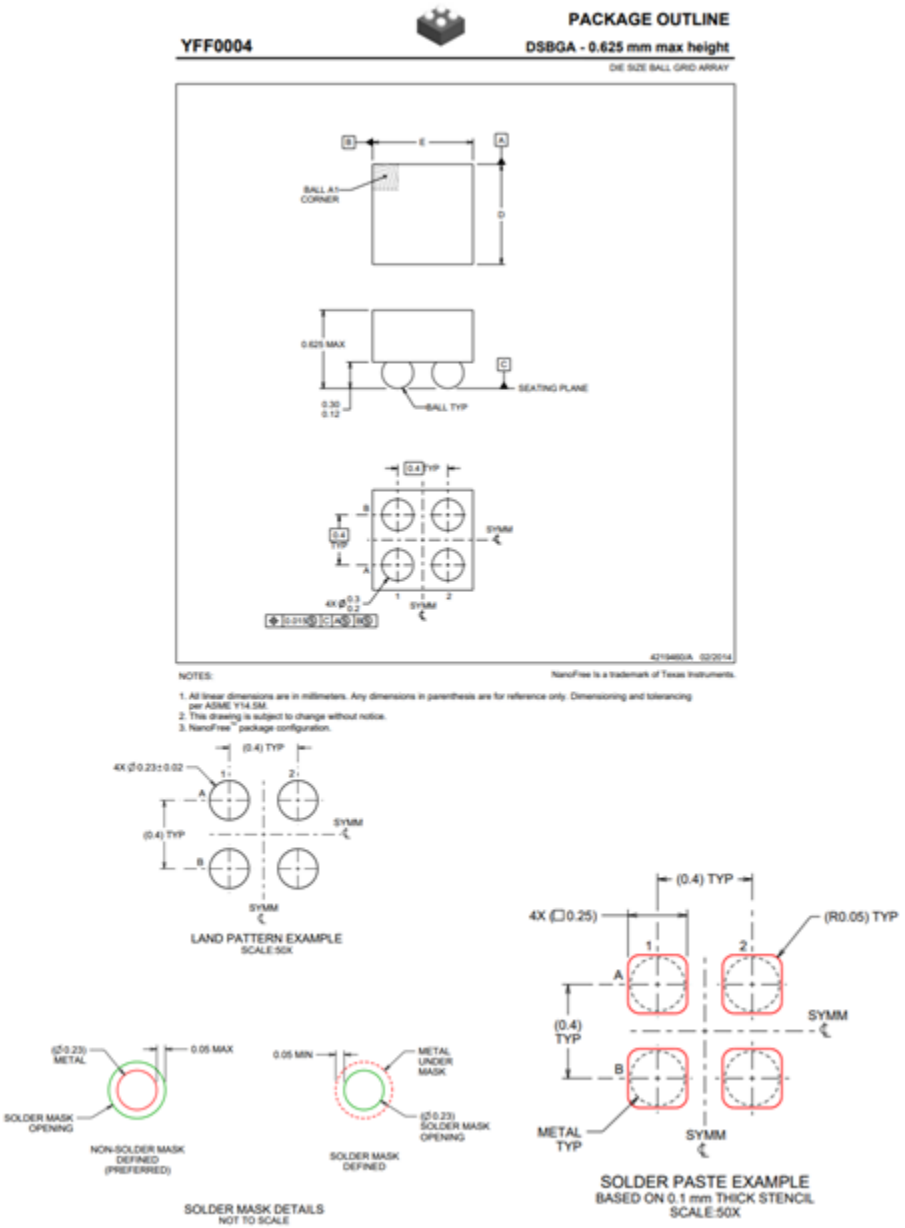

Figure 5. WCSP ePOD Example

2.4.4 Laser Marking Decoder

Laser marking provides traceability information of where the device is manufactured. Please note all information may not be included in the markings, depending on die size. Standard laser marking may contain, but is not limited to:

- Pin 1 identification
- Commercial product name
- Codes for traceability, wafer fabs, testing, and finishing production locations
- Country where the product is assembled

Figure 6 shows an example of laser marking.

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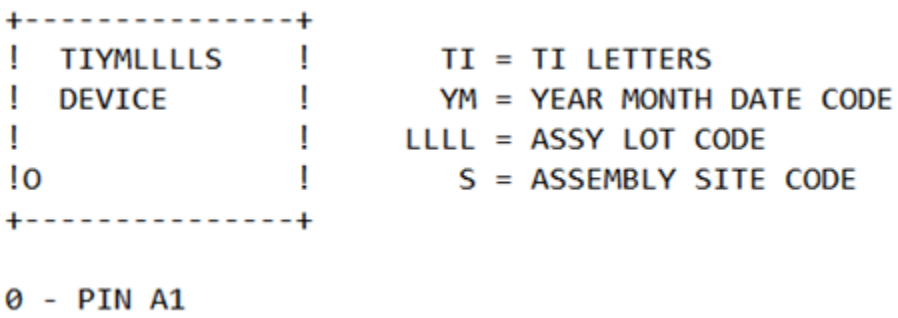

Figure 6. Laser Marking Example

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3 Surface Mount Assembly Considerations

DSBGA surface mount assembly operations include:

- Printing solder paste onto a PCB
- Component placement using standard pick and place equipment
- Solder reflow and cleaning (depending on flux type)

Advantages of DSBGA during SMT assembly include:

- Standard SMT pick and place equipment
- Standard reflow process

3.1 WCSP Surface Mount Flow

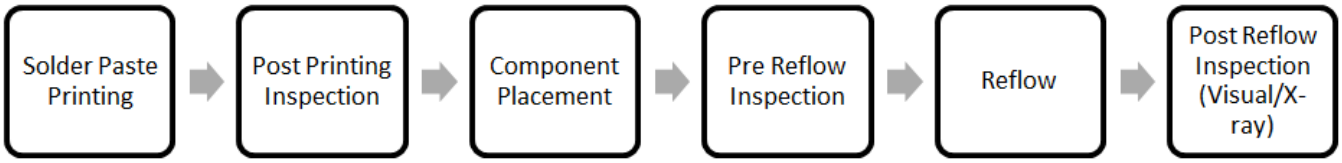

Figure 7. Typical WCSP Surface Mount Flow

3.2 Special Considerations for PowerWCSP

SMI using solder paste for PowerWCSP should follow recommendations for Standard WCSP. Optimization of the SMT process for PowerWCSP is required to avoid issues, like tilting. Contact a TI representative for more information regarding PowerWCSP.

3.3 Special Considerations for PicoStar SMT

General PCB board and stencil design recommendations specific for PicoStar SMT are in Figure 8. Contact a TI representative for more information.

PicoStar™ Package		PCB		Stencil
Bump Pitch	Typical Bump Diameter	Copper Pad* "A"	Solder Mask Opening "B"	Aperture Opening
0.4 mm	0.200 mm	0.230 mm	0.310 mm	0.275 mm
0.5 mm	0.245 mm	0.275 mm	0.375 mm	0.300 mm

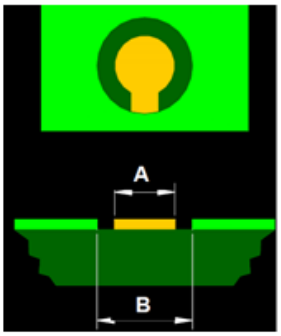

Figure 8. PicoStar SMT Non-Solder Mask Defined (NMSD) Pad Geometry Recommendation

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4 PCB Layout

4.1 NMSD versus SMD

Two types of PCB land patterns are used for surface mount packages:

1. Non-solder mask defined (NSMD
2. Solder mask defined (SMD)

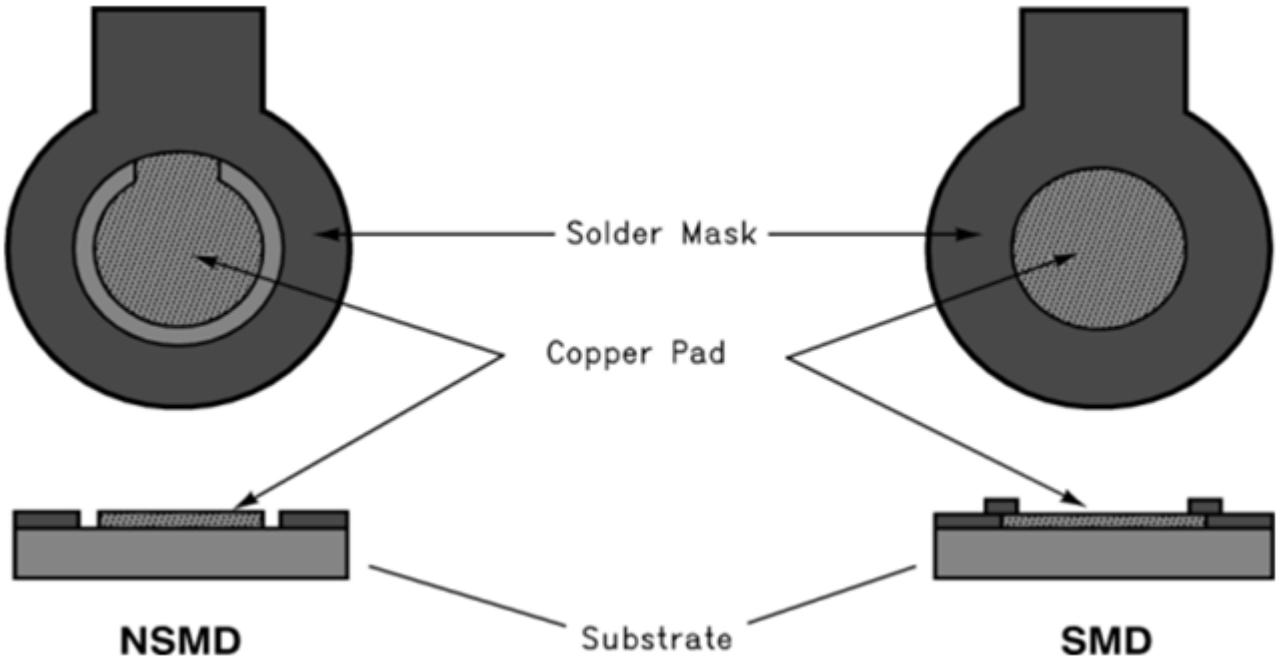

Figure 9. NSMD and SMD Pad Definition

1. The NSMD configuration is preferred due to its tighter control of the copper etch process and a reduction in the stress concentration points on the PCB side compared to SMD configuration.
2. A copper layer thickness of less than 1 oz is recommended to achieve higher solder joint stand-off. A 1 oz. (30 micron) or greater copper thickness causes a lower effective solder joint stand-off, which can compromise solder joint reliability.
3. For the NSMD pad geometry, the trace width at the connection to the land pad should not exceed 2/3 of the pad diameter.

4.2 PCB Pad Geometry Recommendation

Refer to device data table and TI representative for more information.

4.3 Finish

Organic solderability preservative coating (OSP) as well as ENIG (Electroless Nickel Immersion Gold) finish is preferred.

- For ENIG (Electroless Nickel Immersion Gold), gold thickness must be less than 0.2 microns to avoid solder joint embrittlement.
- The fan-out for the traces should be symmetrical across X and Y directions to avoid part rotation due to surface tension of solder.
- HASL (Hot Air Solder Leveled) board finish is not recommended.

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4.4 Vias

For PCB layouts employing via-in-pad structures (micro-via), NSMD pad definition should be used, since this ensures adequate wetting area on the copper pads, hence a better joint. It is also recommended that the wall thickness of the microvias is a minimum of 15 microns. Additionally, it is recommended that 'offset' vias be used when microvias are required for routing on the PCB.

5 Stencil Printing Process

- Use laser cutting followed by electro-polishing for stencil fabrication. Chemical etch is not recommended.
- If possible, offset apertures from land pads to maximize separation and minimize possibility of bridging for DSBGA packages with less than 10 bump counts with small bump size. No print offset is required for higher bump counts and larger bump size.
- Use Type 3 paste (25 to 45 micron particle size range) or finer solder paste for printing.
- Using Type 2 or Type 1 paste (Particle size > 45 μm) is not recommended.

6 Component Placement

Standard pick-and-place machines can be used for placing the DSBGA. Either one of the following methods can be used for recognition and positioning.

- Vision system to locate package silhouette
- Vision system to locate individual bumps. It is recommended that side-lighting on the vision system of the pick-and-place machine be used when attempting to use individual bump recognition.

Other recommendations for DSBGA placement:

- It is preferable to use IC placement/fine pitch placement machines over chip-shooters for better accuracy.
- DSBGA solder bumps self-align when placed at an offset due to self-centering nature of solder bumps.
- Though DSBGA can withstand a placement force of up to 1 kg for 0.5 seconds, little or no force needs to be exerted during placement. It is recommended that bumps be immersed into the solder paste on the PCB to greater than 20% of paste block height.

7 Solder Paste, Reflow, and Cleaning

- DSBGA is compatible with industry standard reflow.
- DSBGA is qualified for up to three reflow operations (260°C peak) per J-STD-020.
- Use of Pb-free DSBGA with eutectic solder paste is not recommended. Such an application can result in assemblies that will not meet desired reliability standards.
- Type 3 (25 to 45 μm particle size range) or finer solder paste is recommended, while type 2 or type 1 is not recommended.
- It is recommended to match solder paste alloy and assembly process with the component bumps alloy (for example, Pb-free paste and process to be used with Pb-free components).

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8 Rework

The key features for the DSBGA rework are the following:

1. Rework procedure used is identical to the one used for most BGA and CSP packages.
2. Rework reflow process should duplicate original reflow profile used for SMT assembly.
3. Rework system should include localized convection heating element with profiling capability, a bottom side pre-heater and a part pick and placer with image overlay.
4. A DSBGA should not be reused.

9 Qualification

TI qualifies all devices to JEDEC reliability standards. Component level tests are performed such as High Temperature Operating Life, Biased HAST (highly accelerated stress test), Unbiased HAST, and Temperature Cycle and High Temperature Storage Bake. Board level thermal cycling and board level drop test are also performed. Refer to JEDEC for conditions and consult TI representative for specific device reliability data.

10 Thermal Characterization

Thermal performance of DSBGA packages are assessed using low effective thermal conductivity test boards per EIA/JESD51-3. The performance of the DSBGA product depends on product die size and application (PCB layout and design), and the details of Theta JA values are available in product data sheets at www.ti.com. For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

11 Conclusion

Texas Instruments DSBGA devices are introduced in this application note. Key features of this product include:

- PCB space saving: package size is equal to die size and reduced thickness and weight.
- Enhanced electrical performance: shorter electrical parts than in standard plastic packages improves electrical performance

Adhering to the recommendations and references in this document ensures high quality and consistent assembly yield.

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Revision History

REVISION DATE	DESCRIPTION
December 2004	Replaced Table 6. Current Figure 6 was Figure 8. Replaced Figure 7 and Figure 8. Modified Do's and don'ts tables.
August 2005	Added 0.4 mm pitch information.
September 2005	Added “Large Dome Bump” paragraph to the Surface Mount Assembly Considerations section.
August 2006	General review, minor edits.
October 2006	Modify 0.5 mm Pitch (0.3 mm dia) Do's and Don'ts
December 2006	Add a bullet to the Solder Paste Reflow and Cleaning section.
March 2007	Modify Table 1. Recommended PCB Pad Geometry
June 2007	Update Figure 1. Remove 36 bump references. Replace Figure 4. Update all Do's and Don'ts
December 2007	Add 0.3 mm pitch information
September 2009	Add in 0.4 mm pitch 64 bumps DSBGA package information
January 2010	Add dome bump, ultra-thin and extreme-thin package information.
September 2011	Added 0.35 mm pitch info to Recommended PCB pad and Recommended Stencil Apertures tables.
April 2012	Added more 0.35 mm pitch information.
May 2012	Insert Appendix A. Modify Appendix B.
March 2015	Removed “Use of underfill is not recommended” from section 1 and 8. Added “The use of an underfill with a CTE matching the solder will enhance the board level performance” to section 1. Added “Refer to Application Report, Forward/Backward Compatibility snoa923 for details” to section 1. Corrected figure 1 from “DSBGA 4-30 Bump” to “DSBGA 4-25 Bump” Updated table 3. Changed “micro SMD” to “DSBGA” in section 4, 7, and 11. Changed “Ni-Gold board finish” to “Electroless Nickel Immersion Gold “
August 2015	TI DSBGA products are designed and tested to ensure excellent board-level thermal cycling reliability without the need for underfill in intended applications. If a customer chooses to underfill a DSBGA product, TI recommends following the guidelines below to maximize reliability. – The underfill fillet should extend partially up the die edges. Underfill that ends at the bottom (ball side) of the die will degrade reliability. – The underfill should have a CTE closely matched to the CTE of the solder interconnect. – The underfill should have a Tg above the expected maximum exposure temperature.
May 2019	Added “PowerWCSP” section to document.
December 2019	Edited application report for clarity.

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