

TLV1805-Q1 EVM ISO testing results

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ABSTRACT

This Application Note presents the testing results of subjecting the [TLV1805-Q1 Reverse Current Evaluation Module](#) to selected ISO 7637-2 and 16750-2 type automotive transients.

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1 Introduction

Automotive battery power supply lines are prone to transients while running the system. Typical protections required for such a system are overvoltage, overload, reverse polarity, and jump start. Electronic Circuits powered by direct battery lines need to be protected from such transients. The TLV1805Q1EVM provides reverse voltage and current protection, which is part of a total automotive power input protection system.

The Automotive Industry has developed several standard tests for electrical systems, the earliest being the ISO 7637-2 and ISO 16750-2 transient tests. There are hundreds of variations of these types of tests defined by the various Automotive Manufacturers based on these ISO tests. Relevant tests from ISO 7637-2 and ISO 16750-2 were selected to broadly represent these various standards.

ISO 7637 is titled "Road vehicles – Electrical disturbances from conduction and coupling", and part 2 is specifically "Electrical transient conduction along supply lines only" (referred to as ISO 7637-2). The standard defines a test procedure, including the description of test pulses, to test the susceptibility of an electrical subsystem to transients, which could potentially be harmful to device operation. Each pulse is modeled to simulate a transient that could be created by a real event in the car. This design mainly focus for reverse polarity protection and supply OR'ing applications, which is predominantly used in parallel battery or redundant bus power supplies.

ISO 16750 is titled "Road vehicles – Environmental conditions and testing for electrical and electronic equipment", and part 2 is specifically "Electrical Loads" (referred to as ISO 16750-2). An easy way to think of this standard is that it essentially defines a series of "supply voltage quality" events—variations of the battery supply voltage under various conditions. For the most part, these conditions are not harmful to the electrical subsystem, but can affect its state of operation. The tests in this standard are designed to see how the subsystem behaves before, during, and after these events.

The TLV1805-Q1 Reverse Current Evaluation Module was subjected to relevant waveforms from the ISO 7637-2 and ISO 16750-2 standards.

NOTE: This exercise was not a full ISO certification. The ISO testing performed does not imply the TLV1805-Q1 provides blanket ISO certification or entire circuit protection alone. This EVM represents only a portion of a total input protection scheme. This circuit must be used with proper supply input transient protection devices (TVS's, EMI Filters, fuses, PTC, etc.) to form the total circuit protection. No ISO, or any other, certifications are inferred or implied. End equipments must be subjected to full testing by the manufacturer.

2 Tests Performed

Section 2 lists the tests performed.

Test Standard	Simulates
ISO 7637-2 Pulse 1	Negative 2ms Micro Transients (Inductive load switching)
ISO 7637-2 Pulse 1 Positive (not std)	Positive 2ms Micro Transients (Inductive load switching - Not part of standard)
ISO 7637-2 Pulse 2A	Positive Inductive Interruption
ISO 7637-2 Pulse 2B	Key-off Motor Rundown
ISO 7637-2 Pulse 3A	Positive HV Fine Transients Burst (Contact Bounce / Arc)
ISO 7637-2 Pulse 3B	Negative HV Fine Transients Burst (Contact Bounce / Arc)
ISO 7637-2 Pulse 4	Starting Profile
ISO 7637-2 Pulse 5 Clamped	Clamped Alternator Load Dump (Clamped @ 38V)
ISO 16750-2 DC Reversed Voltage	60 Seconds Reverse Voltage (-14V)
ISO 16750-2 DC Overvoltage	60 Seconds Over Voltage (18V)
ISO 16750-2 Superimposed AC	10Hz to 30kHz, 2Vpp AC superimposed on 12V DC

2.1 Test Description

ISO waveforms were generated by a Teseq NSG5500 test system, as shown in Figure 1.



Figure 1. TLV1805-Q1 EVM Setup on Teseq NSG5500 Test System

Eight EVM boards were subjected to the tests loaded with a 12 Ohm resistor on the output to simulate a 1 Amp load at 12V, as shown in Figure 2. The parameters of the boards were tested before and after the individual tests to monitor for any parametric shifts. If the board stayed within specifications after all tests, it was considered a "pass". All boards passed.

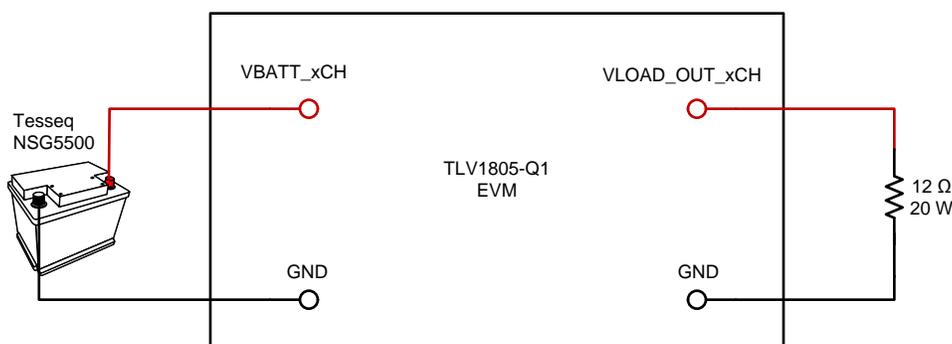


Figure 2. TLV1805-Q1 EVM Test Setup Connections

The actual test and scope photo example behavior measurements were performed separately. The ISO spec disallows measuring the DUT input during the test, so the scope photos that follow were done in a separate session from the actual test run. The N-Channel and P-Channel sections were tested separately.

3 ISO Pulse Summary

3.1 ISO 7637-2 Pulse 1

This test is a simulation of transients due to supply disconnection from inductive loads. It is applicable to DUTs which remain connected directly in parallel with an inductive load, such as a relay coil or motor.

Pulse 1 occurs when the switch is opened. The pulse itself, simulating an inductive kick in a parallel system, is a high voltage, negative-going transient. The waveform and its parameters are given in [Figure 3](#) and [Table 1](#):

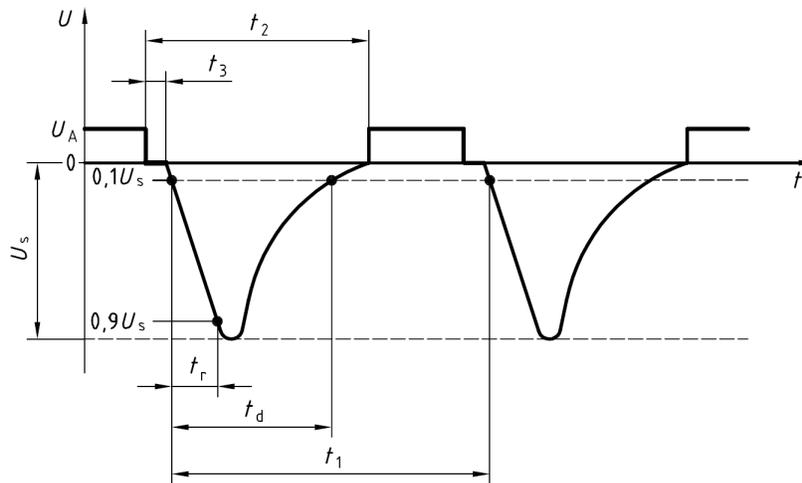


Figure 3. ISO 7637-2 Pulse 1 Waveform

Table 1. ISO 7637-2 Pulse 1 Generator Setting

PARAMETER	12-V SYSTEM
Us	-100 V
Ri	10
td	2 ms
tr	1 μs
t1 ⁽¹⁾	0.5 s
t2	200ms
t3 ⁽²⁾	100μs

⁽¹⁾ t1 must be chosen such that the DUT is correctly initialized before the application of the next pulse.

⁽²⁾ t3 is the smallest possible time necessary between the disconnection of the supply source and the application of the pulse.

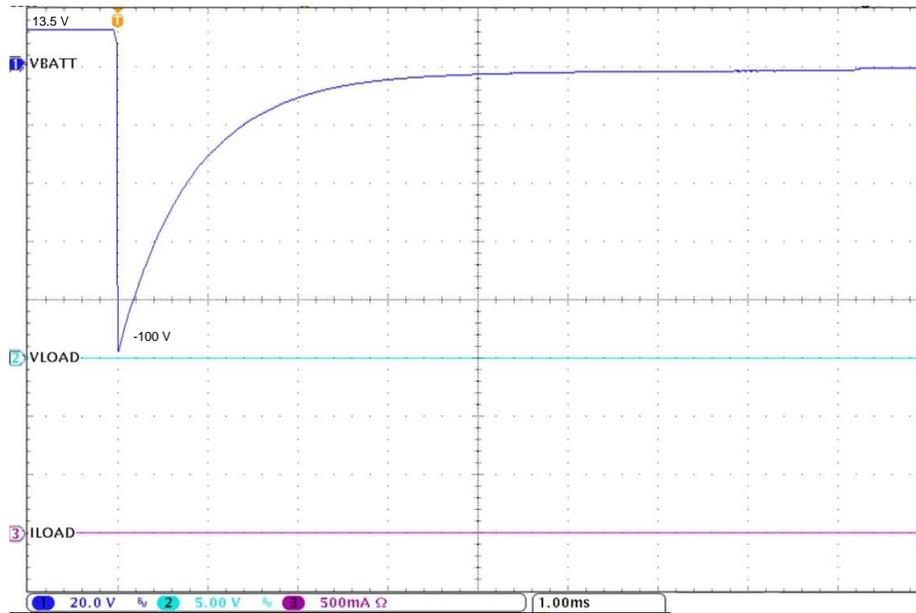


Figure 4. Pulse 1 Negative, Generator Output, No Board

Figure 4 shows the unloaded output waveform of the generator without the evaluation board connected.

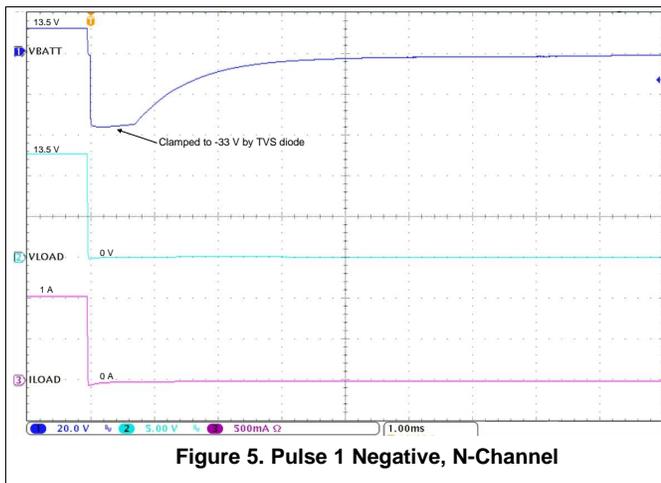


Figure 5. Pulse 1 Negative, N-Channel

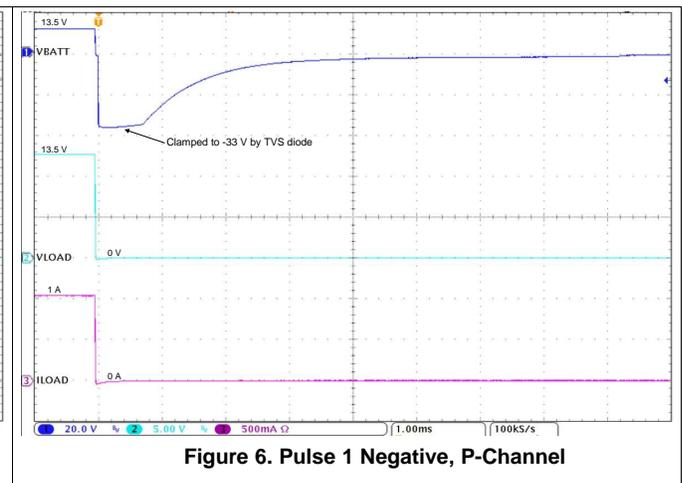


Figure 6. Pulse 1 Negative, P-Channel

Results Summary

Figure 5 and Figure 6 show the load outputs of the N-Channel and P-Channel boards. The negative pulse was clamped at -33V by the input TVS. Since the pulse was negative, the negative voltage was blocked and clamped to less than -0.5V at the load.

3.2 ISO 7637-2 Pulse 1 Positive

This pulse is not part of the ISO standard. It is simply the Pulse 1 with the impulse waveform inverted ($U_s = +100\text{ V}$).

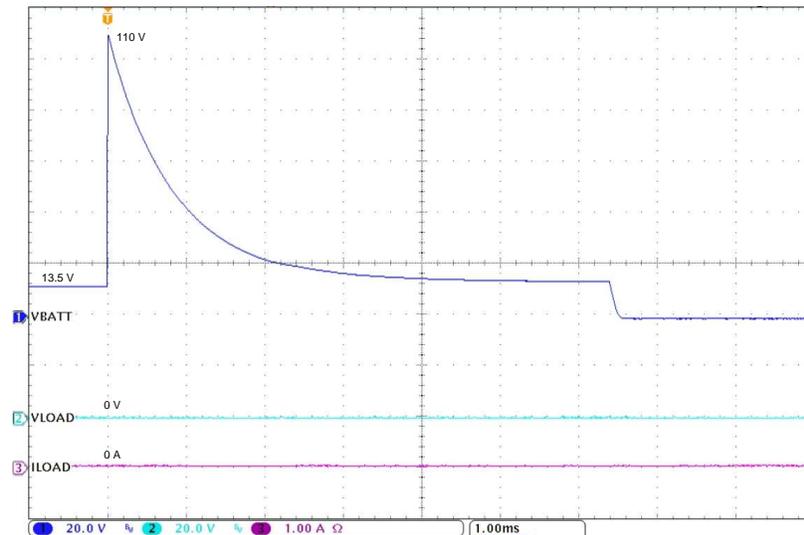


Figure 7. Pulse 1 Positive, No Board

Figure 7 shows the unloaded output waveform of the generator without the evaluation board connected.

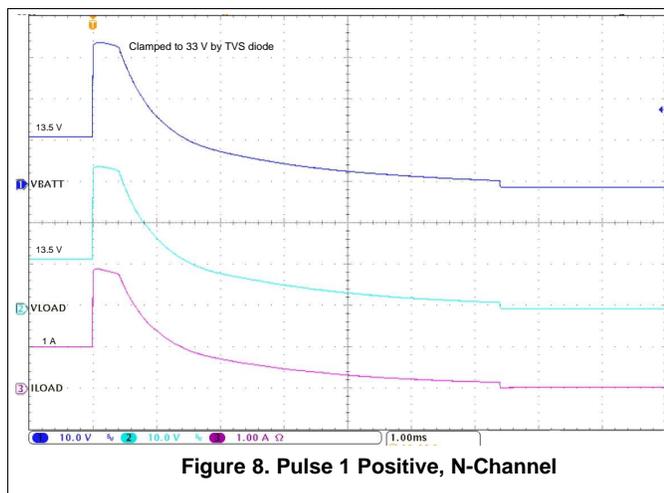


Figure 8. Pulse 1 Positive, N-Channel

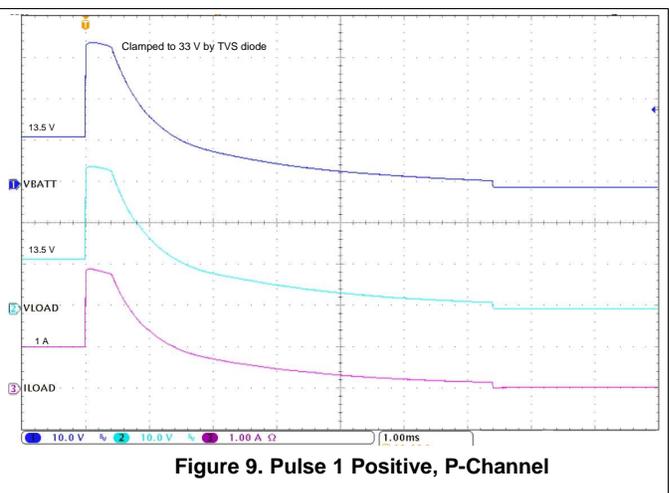


Figure 9. Pulse 1 Positive, P-Channel

Results Summary

As in the pulse 1a, the positive high voltage pulse was clamped at 33V by the input TVS. Since the pulse was positive, both circuits passed it through uninterrupted as the polarity is positive and no reverse current occurred.

3.3 ISO 7637-2 Pulse 2a

Pulse 2a simulates transients due to sudden interruption of currents to a device connected in parallel with the DUT due to inductance of the wiring harness.

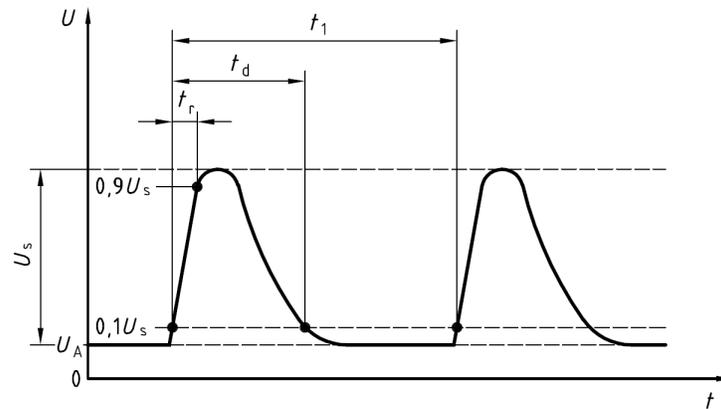


Figure 10. ISO 7637-2 Pulse 2a Waveform

Table 2. ISO 7637-2 Pulse 2a Generator Setting

PARAMETER	12-V SYSTEM
U_s	37 to 50 V
R_i	2 Ω
t_d	0.05 ms
t_r	1 μ s
$t_1^{(1)}$	0.2 s

⁽¹⁾ The repetition time t_1 can be short, depending on the switching. The use of a short repetition time reduces the test time.

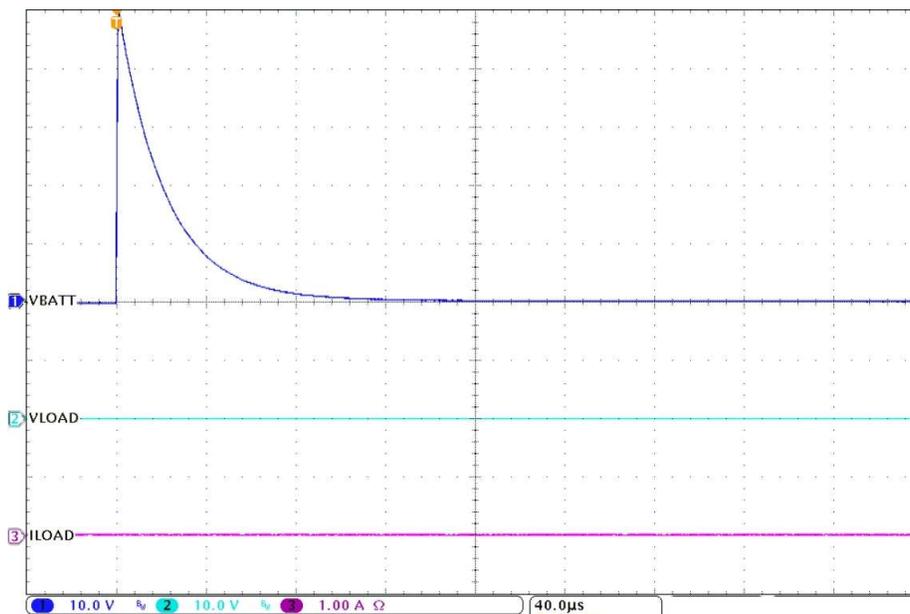


Figure 11. Pulse 2a, No Board

Figure 11 shows the unloaded output waveform of the generator without the evaluation board connected.

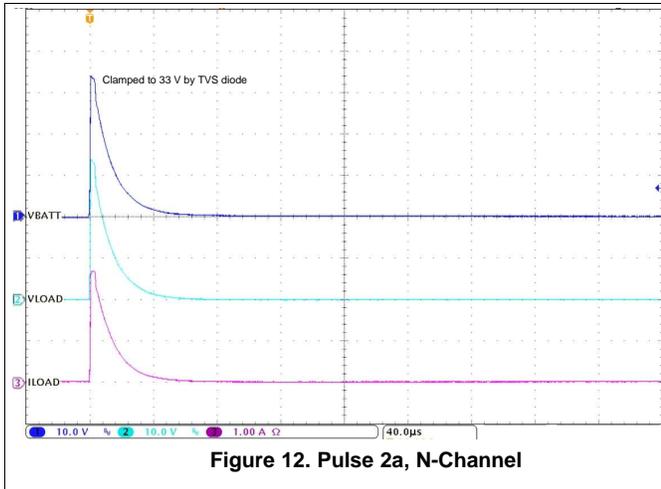


Figure 12. Pulse 2a, N-Channel

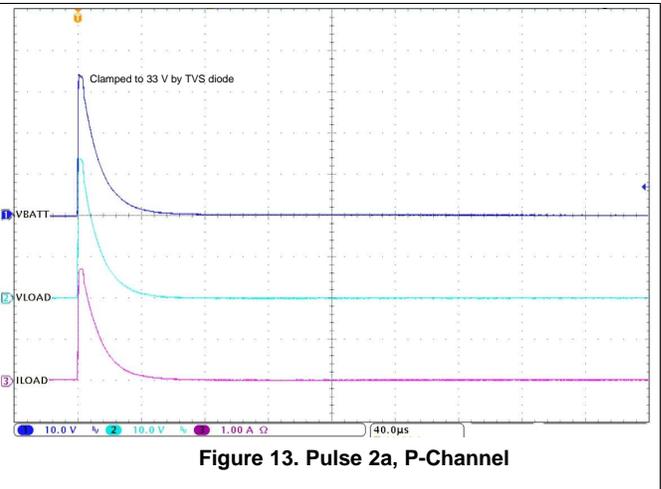


Figure 13. Pulse 2a, P-Channel

Results Summary

The positive pulse was clamped at 33V by the input TVS diode. Since the pulse was positive, both circuits passed it through uninterrupted as no reverse current occurred.

3.4 ISO 7637-2 Pulse 2b

Pulse 2b simulates slower negative transients from parallel connected DC motors acting as generators after the ignition is switched off due to spinning mass inertia (such as fan or blower motors).

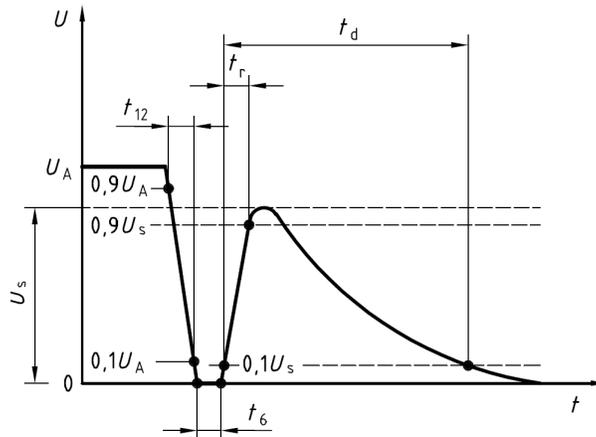


Figure 14. ISO 7637-2 Pulse 2b Waveform

Table 3. ISO 7637-2 Pulse 2b Parameters

PARAMETER	12-V SYSTEM
U_s	50 V (more than spec)
R_i	2 Ω
t_d	0.2 s
t_r	1 ms
t_{12}	1 ms
t_6	1 ms

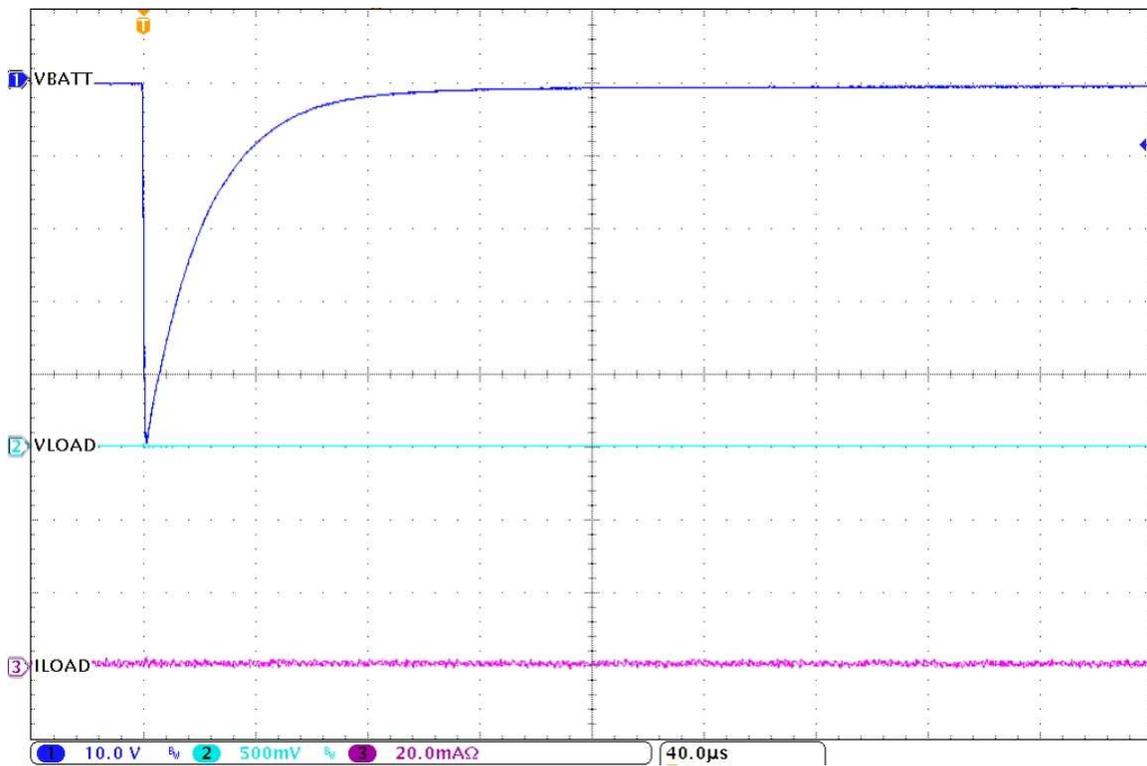


Figure 15. Pulse 2b, No Board

Figure 15 shows the unloaded output waveform of the generator without the evaluation board connected.

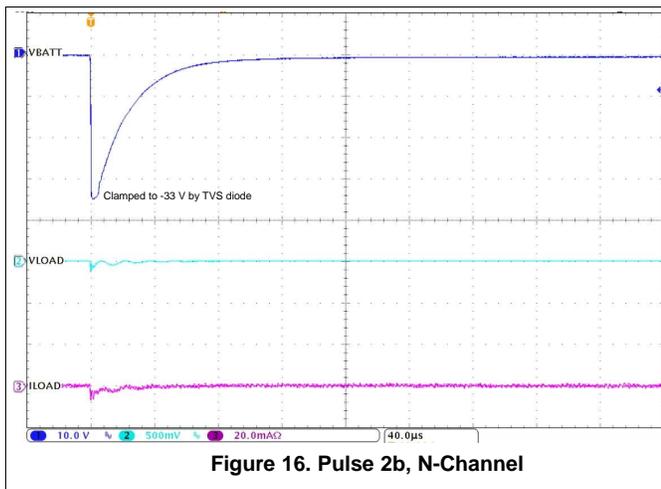


Figure 16. Pulse 2b, N-Channel

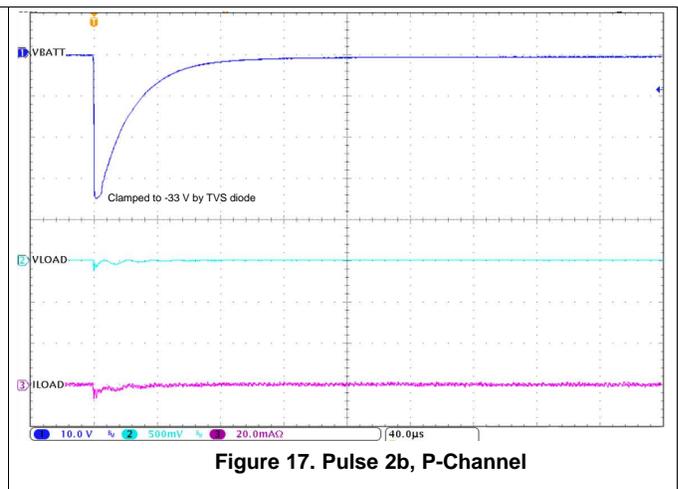


Figure 17. Pulse 2b, P-Channel

Results Summary

The high pulse was clamped at -33V by the input TVS. Since the pulse was negative, the negative voltage was blocked and clamped to less than -0.5V.

3.5 ISO 7637-2 Pulse 3a

Pulse 3a simulates arcing of contacts controlling an inductive load. These are simulated with bursts of 100 close-spaced, fast-risetime high voltage pulses (also referred to as "micro-transients").

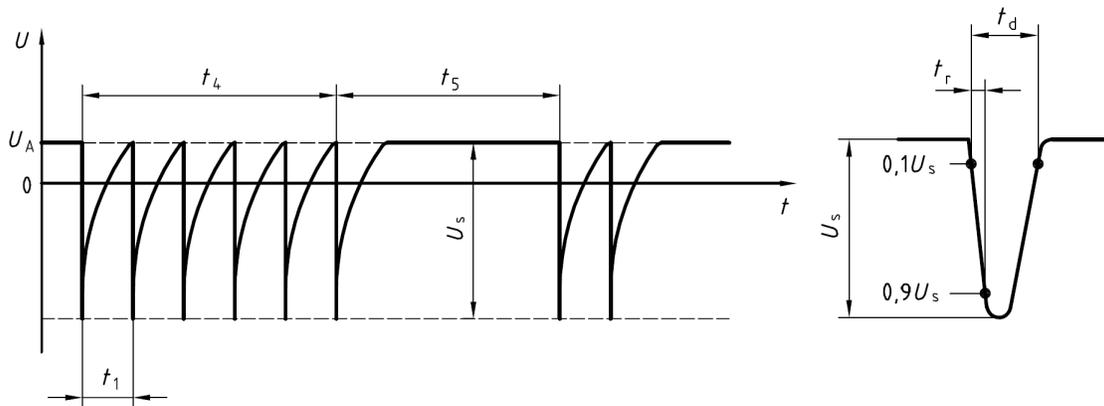


Figure 18. ISO 7637-2 Pulse 3a Waveform

Table 4. ISO 7637-2 Pulse 3a Generator Settings

PARAMETER	12-V SYSTEM
Us	-100 V
Ri	50 Ω
td	100 ns
tr	5 ns
t1	100us
t4	10 ms
t5	90 ms

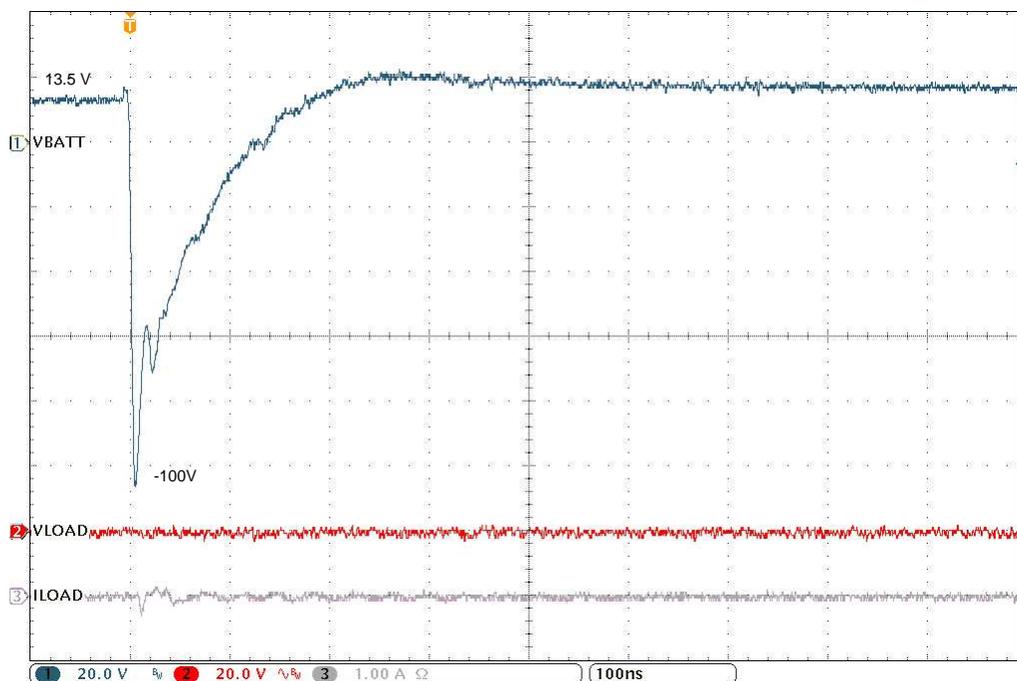
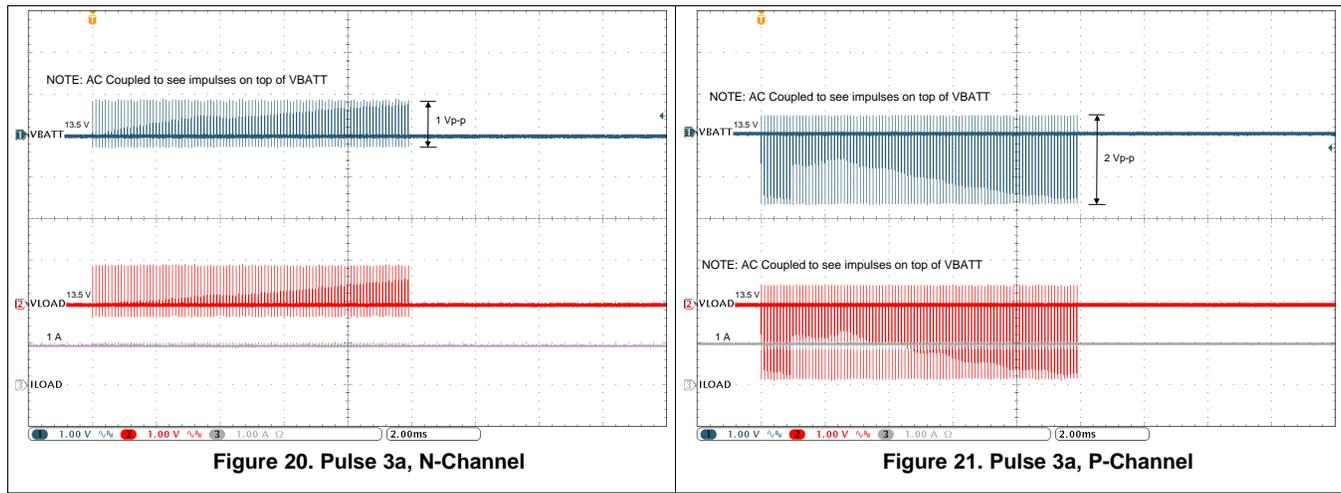


Figure 19. Pulse 3a, No Board, Zoomed in to show one pulse

Figure 19 shows a zoomed-in view of one pulse of the unloaded output of the generator without the evaluation board connected.



Results Summary

Notice the change in the vertical volts per division scaling between Figure 19 , Figure 20 and Figure 21. The oscilloscope inputs were AC coupled to remove the baseline 13.5V DC to better view the attenuated transients. The fast 100ns, 100V pulses were suppressed by the input bypass capacitors to less than 2V at the input. The remnants of the pulses did pass through the circuit, but this is expected as the majority of the current is in the forward direction. Further load bypassing and filtering would minimize these transients.

3.6 ISO 7637-2 Pulse 3b

Pulse 3b is the inverse (positive-going) version of Pulse 3a. Timings are identical but waveform voltages are positive.

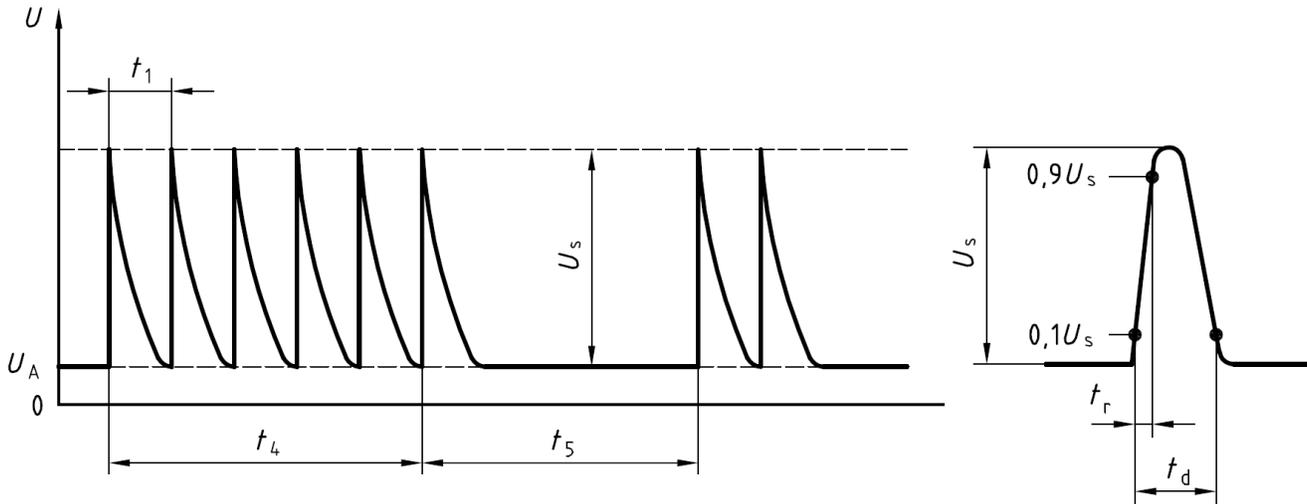


Figure 22. Pulse 3b Waveform

Table 5. ISO 7637-2 Pulse 3b Parameters

PARAMETER	12-V SYSTEM
U_s	+100 V
R_i	50 Ω
t_d	100 ns
t_r	5 ns
t_1	100 μ s
t_4	10 ms
t_5	90 ms

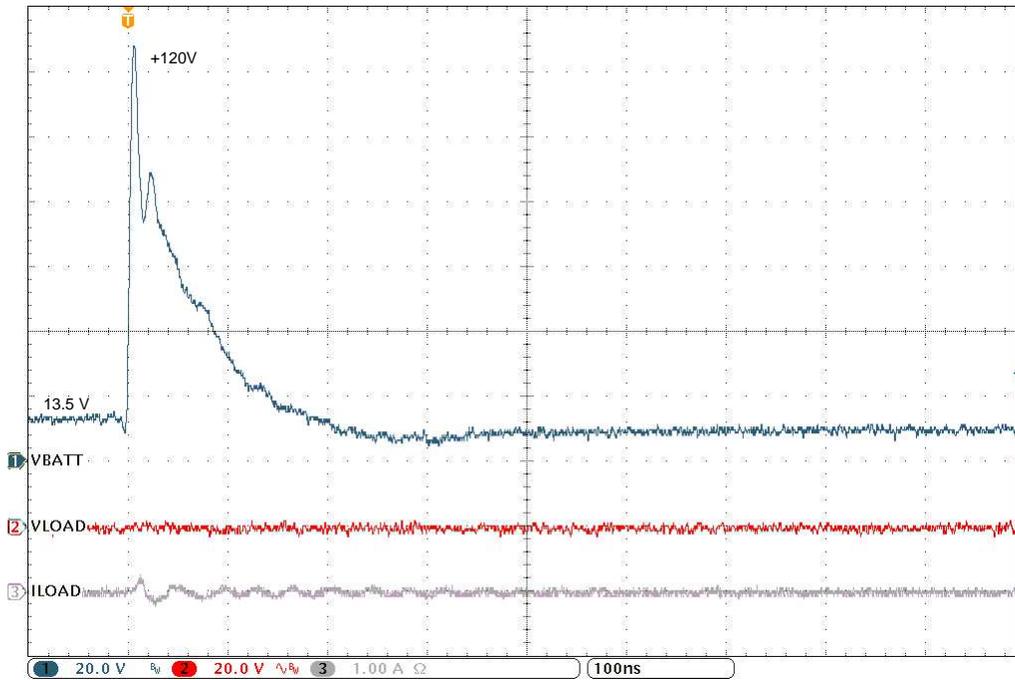


Figure 23. Pulse 3b, No Board, Zoomed-In

Figure 23 shows the unloaded output waveform of the generator without the evaluation board connected.

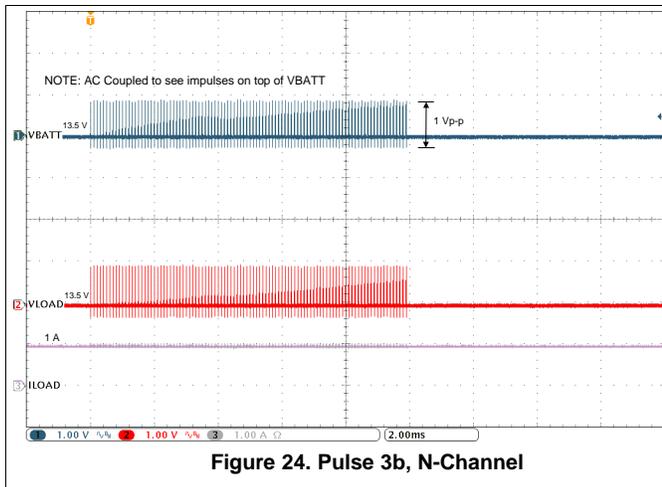


Figure 24. Pulse 3b, N-Channel

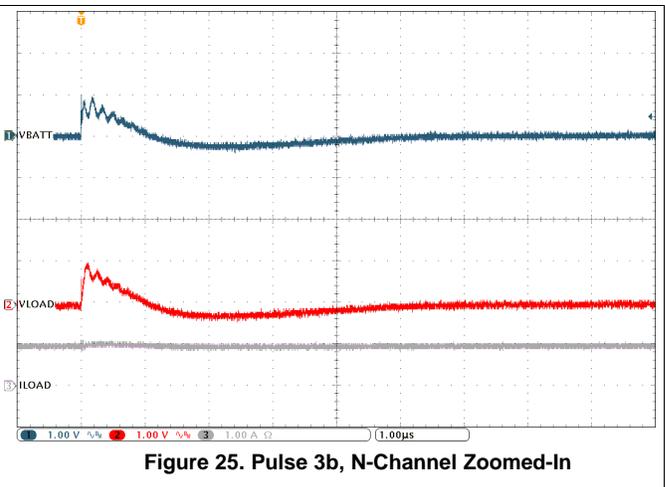
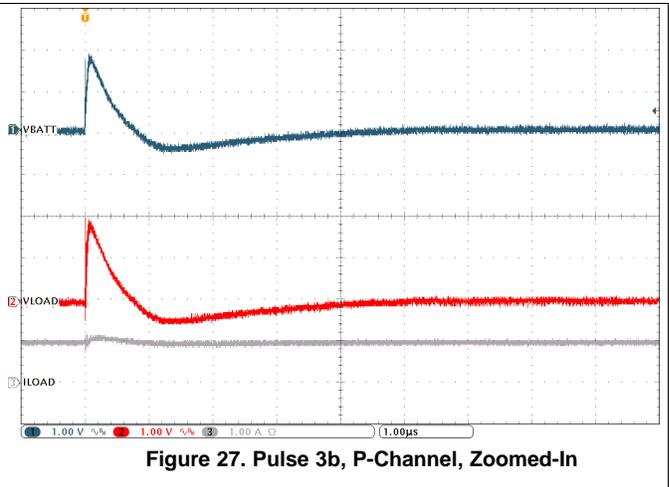
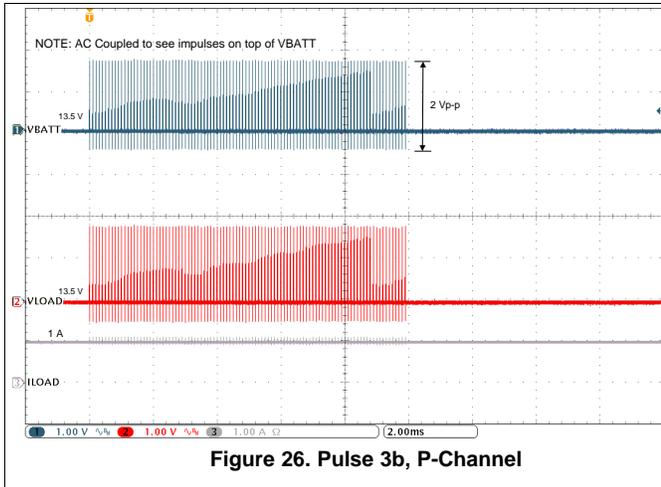


Figure 25. Pulse 3b, N-Channel Zoomed-In



Results Summary

Notice the change in the vertical volts per division scaling between the input [Figure 23](#) and the output [Figure 24](#) and [Figure 26](#). The oscilloscope inputs were AC coupled to remove the baseline 13.5V DC in order to closer view the attenuated transients. Similar to the [3a pulse](#), the fast 100ns edge rate, 100V pulses were suppressed by the input bypass capacitors. The result is the pulses were reduced to less than 2V at the input. The remnants of the pulses did pass through the circuit, but this is expected as the majority of the current is in the forward direction.

3.7 ISO 7637-2 Pulse 4

Pulse 4 simulates supply voltage reduction caused by the energizing the starter-motor, excluding spikes associated with starting. A 2Vp-p, 2Hz signal is superimposed during the t9 time period to simulate a starter motor cranking load for several seconds.

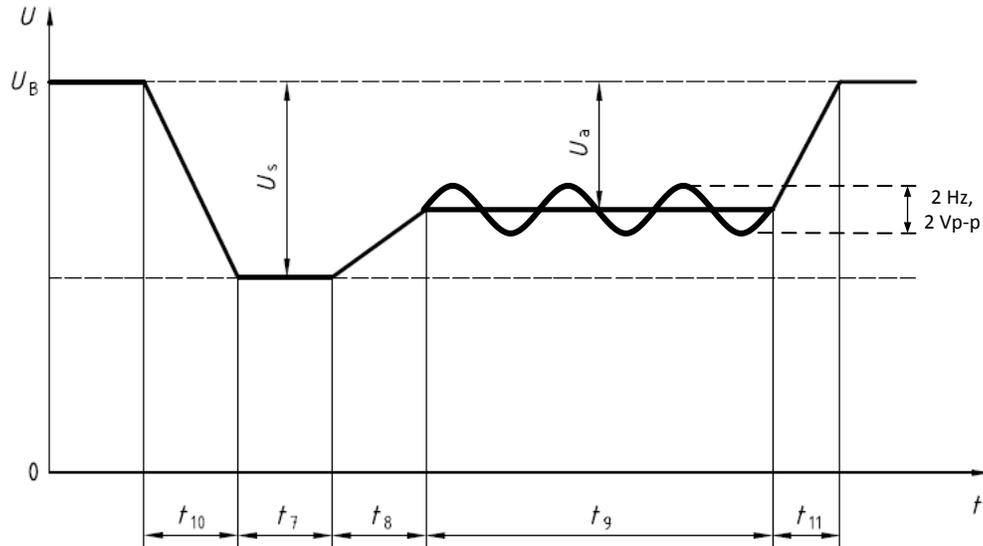


Figure 28. ISO 7637-2 Pulse 4 Waveform

Table 6. ISO 7637-2 Pulse 4 Generator Settings

PARAMETER	12-V SYSTEM
U_B	12 V
U_S	-9 V
U_A	-5 V
R_i	0.02 Ω
t8	50 ms
t9	10 s
t10	5 ms
t11	100 ms

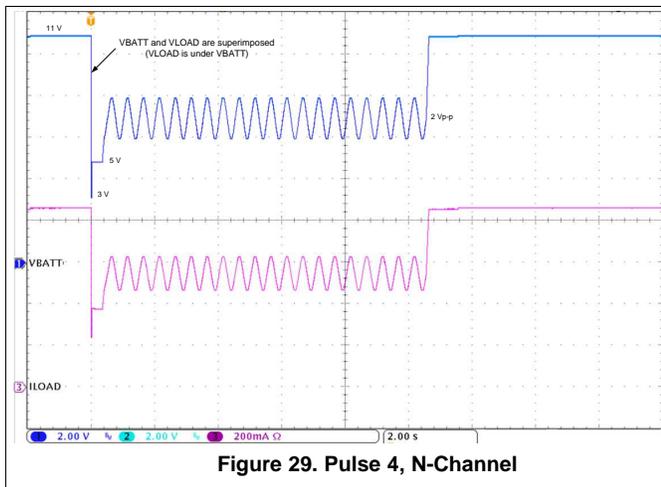


Figure 29. Pulse 4, N-Channel

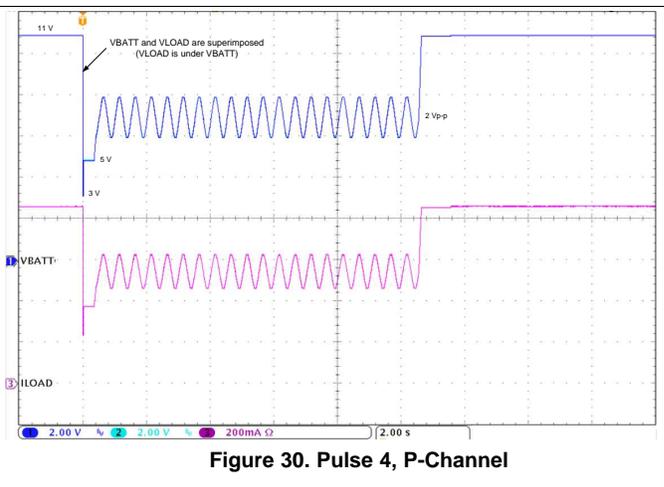


Figure 30. Pulse 4, P-Channel

Results Summary

The circuit was not expected to have any issues with the starting waveform. The V_{BATT} and V_{LOAD} traces are overlapping each other, showing that the output tracked the input tightly with little loss, even through the fast 3V drop. The "floating" comparator supply architecture of both circuits allows the comparator bypass capacitor to briefly retain charge during negative and low voltage transients and provide high VGS drive through the 3V transient, resulting in full reverse-current circuit protection during the entire waveform.

3.8 ISO 7637-2 Pulse 5b (Clamped)

Pulse 5b simulates a clamped alternator "Load Dump" condition. This occurs when a battery is disconnected while the alternator is actively charging, resulting in a momentary output voltage overshoot while the alternator regulator recovers. Modern alternators now contain an internal clamping circuit to minimize this overshoot, though older unclamped alternators can rise to 90V or more (as covered by the "Unclamped" Pulse 5a). This test mainly stresses the TVS diode as it dissipates the majority of the transient energy.

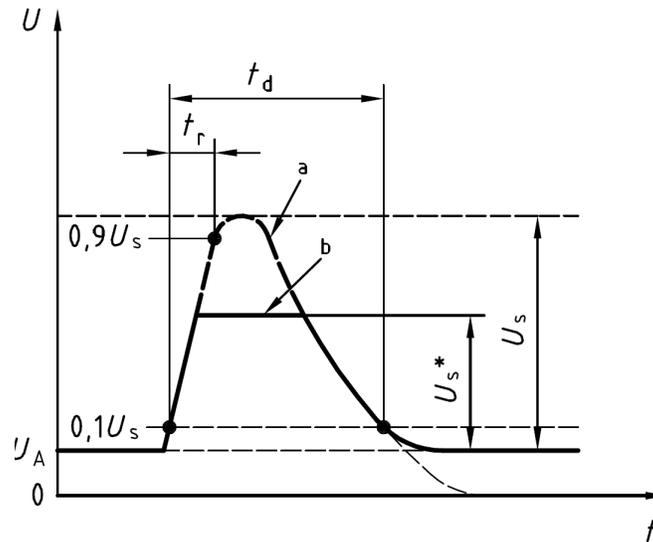


Figure 31. ISO 7637-2 Pulse 5b Waveform

Figures [Figure 32](#) and [Figure 32](#) below show the P and N Channel responses to Pulse 5b.

Table 7. ISO 7637-2 Pulse 5b Generator Settings

PARAMETER	12-V SYSTEM
U_s^*	25V
R_i	0.5 Ω
t_d	100 ms
t_r	5 ms

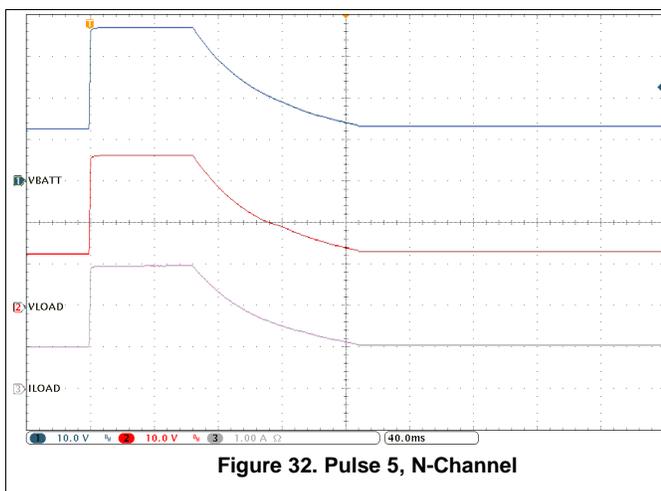


Figure 32. Pulse 5, N-Channel

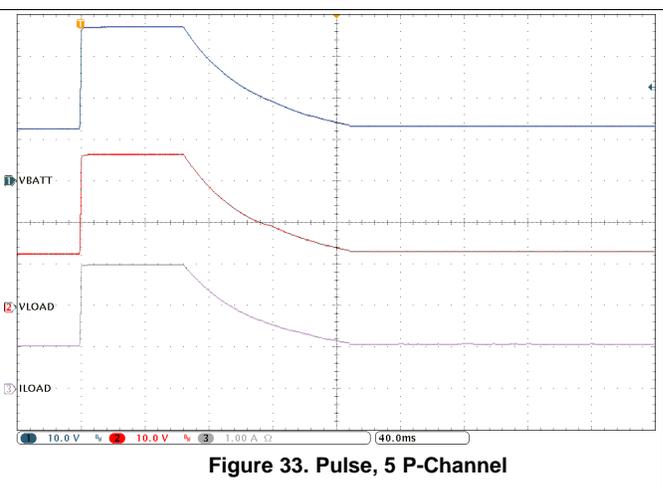


Figure 33. Pulse, 5 P-Channel

Results Summary

The circuit was not expected to have any issues with the starting waveform. The V_{BATT} and V_{LOAD} traces are overlapping each other, showing that the output tracked the input tightly without any loss, even through the fast 3V key-on drop. The diode isolated "floating" ground architecture of both circuits allows the comparator bypass capacitor to retain charge during negative and low voltage transients, keeping the reverse current circuits in full operation during the transient (full gate drive).

It should be noted that the largest stress occurs in the TVS protection diode, as it is absorbing the majority of the energy. The 0.5Ω R_i option can create as much as 1000 peak amps through the TVS.

3.9 ISO 16750-2 DC Reversed Voltage

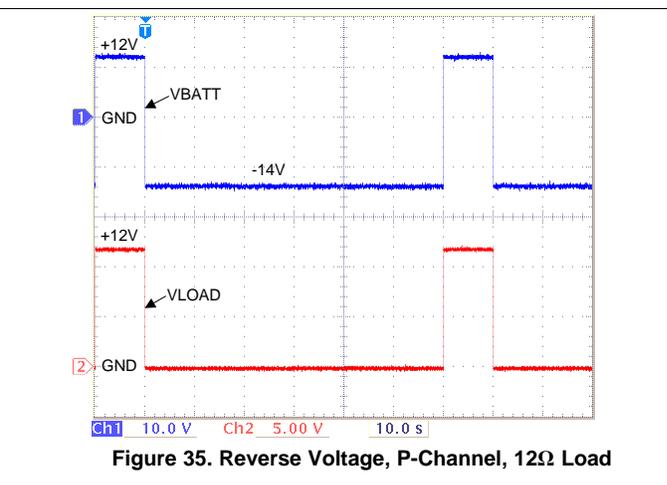
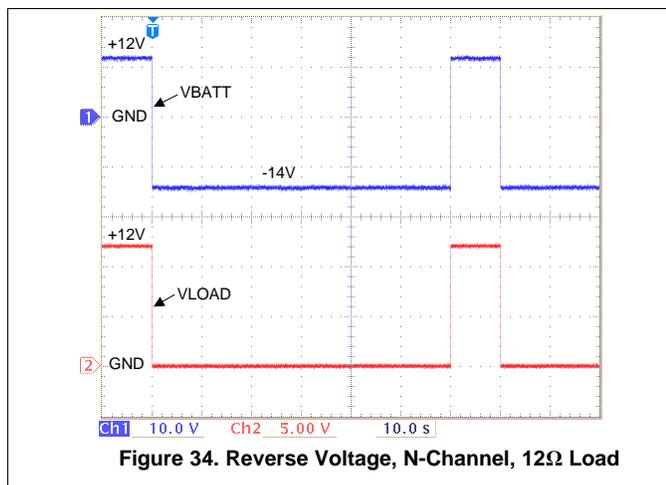
ISO 16750-2 Reversed Voltage test simulates a reversed battery due to improper battery installation or reversed jump. A reversed (negative) battery voltage is applied for 60 seconds.

Table 8. ISO 16750-2 Reversed Voltage Parameters

PARAMETER	12-V SYSTEM
U_A	-14 V
R_i	0.01 Ω
t_d	60 s

3.9.1 DC Reverse Voltage Results Under Load

Figures [Figure 34](#) and [Figure 35](#) show the response of the N-Channel and P-Channel boards to the reverse voltage test.



[Table 9](#) shows the actual measured DC voltages and currents with a 12 ohm, 1A load.

Table 9. Measured DC Parameters with 12 Ohm Load

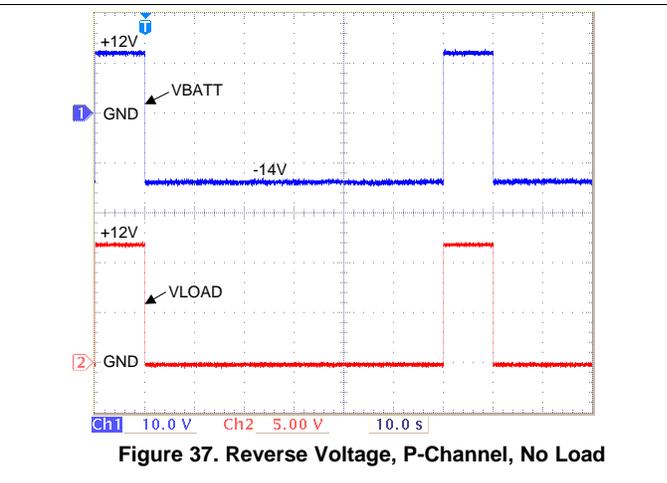
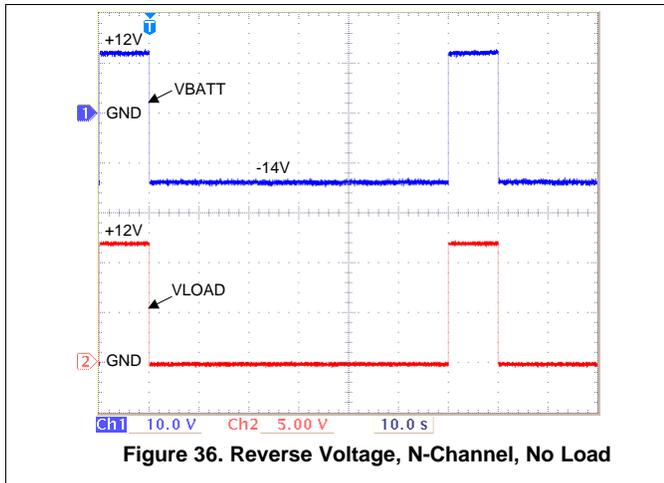
Parameter	N-Channel - Forward Current	N-Channel - Reverse Current	P-Channel - Forward Current	P-Channel - Reverse Current
V_{BATT}	12.002 V	-14.002 V	12.025 V	-14.033 V
V_{LOAD}	11.973 V	-15 mV	11.952 V	-1.49 mV
I_{BATT}	1 A	-1.37 mA	.997 A	-13.3 mA

Loaded Reverse Voltage Results Summary

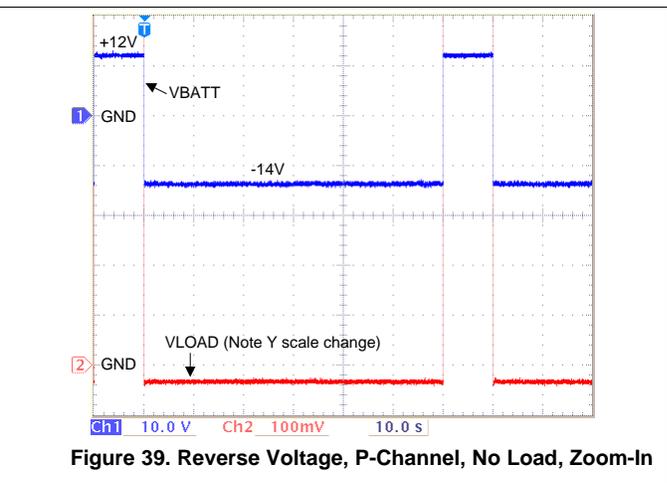
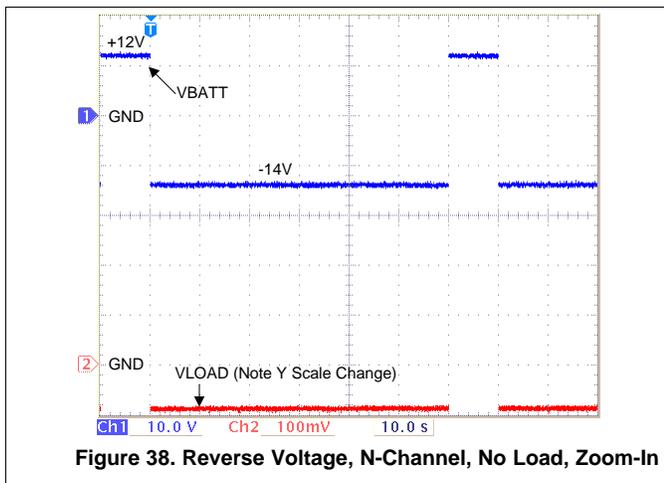
The top blue waveforms show the source transition from +12V to -14V. The load output drops to near zero volts, as shown in [Table 9](#). The higher reverse voltage supply current is due to the reverse clamping circuits conducting.

3.9.2 DC Reverse Voltage Results with No Load

Figures [Figure 36](#) and [Figure 37](#) show the response of the N-Channel and P-Channel boards to the reverse voltage test with no load on the output.



[Figure 38](#) and [Figure 39](#) shows a zoomed-in view of the output voltage of the N-Channel and P-Channel circuits with no load on the output (note the Ch. 2 vertical scale change).



[Table 10](#) shows the actual measured DC voltages and currents with no load (EVM output open).

Table 10. Measured DC Parameters with No Load

Parameter	N-Channel Forward Current	N-Channel Reverse Current	P-Channel Forward Current	P-Channel Reverse Current
VBATT	12.002 V	-14.002 V	11.972 V	-14.025 V
VLOAD	12.002 V	-86 mV	11.971 V	-37.5 mV
IBATT	1.13mA	-1.36 mA	539 μ A	-130 μ A

No Load Reverse Voltage Results Summary

The top blue waveforms show the source transition from +12V to -14V. The load output drops to near zero volts, as shown in [Figure 36](#). The higher reverse voltage supply current is due to the reverse clamping circuits conduct.

3.10 ISO 16750-2 Overvoltage

ISO 16750-2 Overvoltage test simulates a jump-start from a 24V vehicle to a 12V vehicle (such as a commercial truck to a passenger vehicle). 24V is applied for 60 seconds.

Table 11. ISO 16750-2 Over-Voltage Parameters

PARAMETER	12-V SYSTEM
U_A	+24 V
R_i	0.01 Ω
t_d	60 s

Results Summary

This test presented no issues for either circuit. Both channels are designed to handle up to 28V maximum. Quiescent supply current for both channels does increase to 15mA due to the internal comparator supply zener clamping circuit activating. Because the EVM does not implement overvoltage protection or voltage regulation, the 24V is passed to the output unimpeded.

3.11 ISO 16750-2 Superimposed AC

ISO 16750-2 Superimposed AC test simulates residual large AC ripple current on a the DC supply, such as from a switching supplies or traction motor drives.

An AC sine wave is superimposed on top of the battery voltage, and swept logarithmically from 50Hz up to 25kHz and back over a period of 120 seconds (60 sec up, 60 sec down). A power amplifier was used to generate the V_{BATT} waveform.

Table 12. ISO 16750-2 Superimposed AC Parameters

PARAMETER	12-V SYSTEM
U_S	12 V
R_I	0.1 Ω
U_{pp}	2 V
t	120 Sec
Frequency Range	50 to 30000 Hz

Results Summary

Both circuits had no issues passing the test due to the "floating" nature of both circuits with large comparator bypass capacitors. The circuits were able to "ride-out" the AC waveforms. Because of the resistive load, the current was always positive, so the MOSFETS were conducting during the entire time.

Creating Reverse Current

Some readers may be interested in the reverse current behavior during the superimposed AC test. Commonly this is done by adding a large capacitor to the load. To clearly observe the switching action, a resistive load with a DC bias was used to avoid the frequency dependance of the AC current due to the capacitive impedance (X_C) and provide greater control of the current waveform.

The negative current is created by placing the load resistor R_L in series with the EVM between two controllable voltage sources driven by arbitrary waveform generators. The difference in the generated voltages across the load resistor determines the current direction and magnitude.

As shown in [Figure 40](#), when the 12V V_{BATT} voltage is modulated (superimposed) with a $\pm 1V$ AC signal, a $\pm 2A$ AC current is generated across R_L .

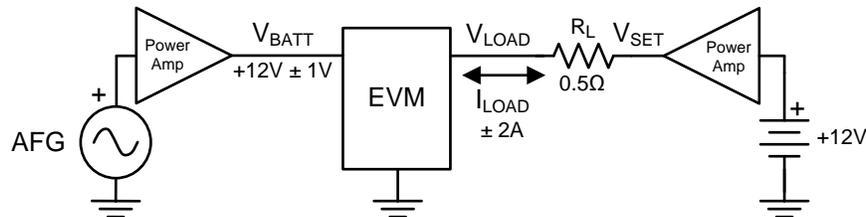


Figure 40. AC Reverse Current Test Circuit

It should be noted that the majority of bench power supplies cannot sink current needed to create the negative current. To create the negative currents, a power amplifier, similar to a DC coupled audio power amplifier, was used to generate the V_{BATT} and V_{LOAD} buffer voltages.

Figure 41 and Figure 42 shows the response of the N-Channel and P-Channel circuit to the 1kHz superimposed waveform.

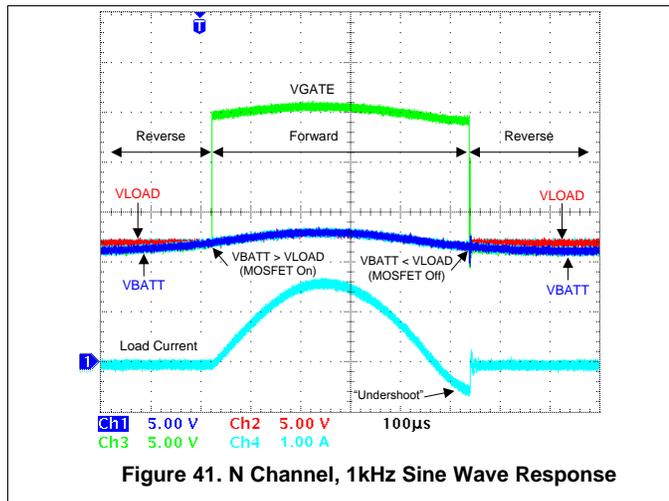


Figure 41. N Channel, 1kHz Sine Wave Response

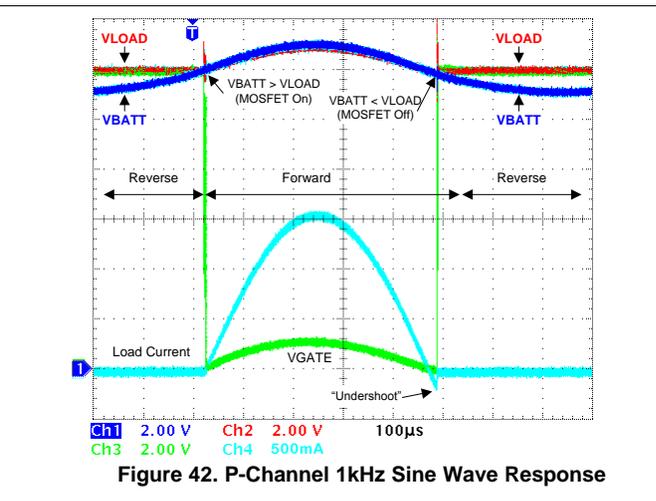


Figure 42. P-Channel 1kHz Sine Wave Response

When V_{BATT} (blue) rises above V_{LOAD} (red), the comparator detects this condition and sets the MOSFET gate (yellow) "high" to turn on the N-Channel MOSFET, or "low" to turn on the P-Channel MOSFET. While the MOSFET is conducting, V_{BATT} and V_{LOAD} are nearly identical due to the low voltage drop (the V_{LOAD} trace is under the V_{BATT} trace during the "Forward" portion of the scope photo).

The load current (cyan) rises and falls with the forward portion of the waveform. When V_{BATT} drops below V_{LOAD} , the MOSFET is turned off. The expected "undershoot" negative current is visible at the start of the reverse transition point. The "undershoot" is due to the lower $R_{DS(ON)}$ of the MOSFET while conducting which requires a larger negative current to generate the needed detection voltage to turn the MOSFET off.

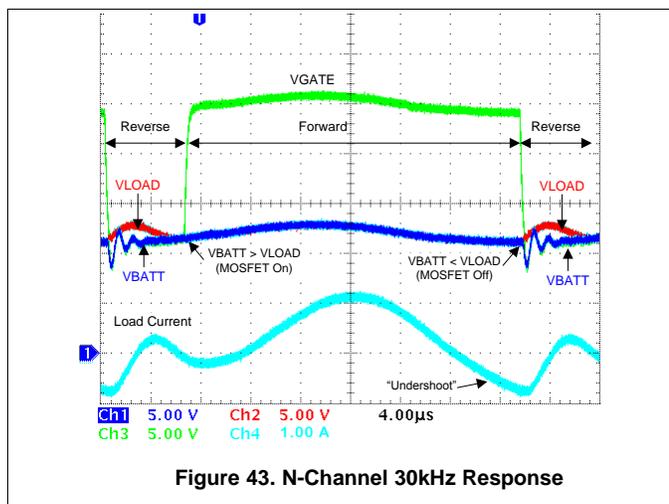


Figure 43. N-Channel 30kHz Response

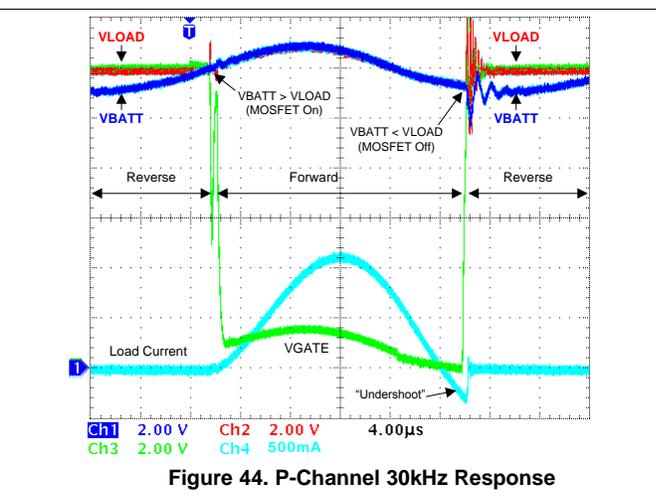


Figure 44. P-Channel 30kHz Response

Figure 43 and Figure 44 show the response to a 30kHz superimposed waveform. As previously, when V_{BATT} rises above V_{LOAD} , the MOSFET is turned on.

The Figure 43 N-Channel waveform shows the effects of the combination of $R_{DS(ON)}$ and comparator prop delay contribution causing a larger "undershoot" current. The N-Channel waveform looks worse due to the larger current transients challenging the stability of the driving power amplifier.

4 Summary

The TLV1805-Q1 EVM performed as expected and no issues were observed. The large overvoltages are clamped by the TVS diodes, and the high frequency transients are diminished by the input EMI filters.

5 References

- "TLV1805-Q1 Comparator Based Discreet Reverse Current Protection Circuit Evaluation Module", <http://www.ti.com/tool/TLV1805EVMQ1>
- "TLV1805-Q1EVM Evaluation Board Users Manual", Texas Instruments, Literature Number [SNOU158](#)
- TLV1805 Datasheet, Texas Instruments, Literature Number [SNOSD50](#)
- TLV1805-Q1 Datasheet, Texas Instruments, Literature Number [SNOSD52](#)
- ISO Standard "7637-2:2011 Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only", section 5.6 6, <http://www.iso.org>
- ISO Standard "16750-2:2012 Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads", section 4.6, <http://www.iso.org>
- "Reverse Current Protection Using MOSFET and Comparator to Minimize Power Dissipation", Texas Instruments Application Note, Literature Number [SNOA971](#)
- Cranking Simulator Reference Design for Automotive Applications, Texas Instruments, Reference Design Number [PMP7233](#)
- "Automotive Cranking Simulator User's Guide", Texas Instruments, Literature Number [SLVU984](#)
- TI Training & Video "ISO 7637 Standards & Solutions Series", "ISO7637 Test Pulses, section 1.3", Texas Instruments, <https://training.ti.com/iso7637-test-pulses>

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