Programmer's Guide

DS320PR810, DS320PR822 Programming Guide

ABSTRACT

This user's guide provides a programming reference for the DS320PR810 Octal-Channel PCI-Express Gen-5 Linear Redriver and the DS320PR822 PCI-Express Gen-5 Linear Redriver (hereafter referred to as DS320PR810, excluding the SEL bit selection programming example). This document contains detailed information related to the DS320PR810 advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with the appropriate device-specific data sheets (*DS320PR810 Eight-Channel Linear Redriver for PCIe 5.0, CXL 1.1 Data Sheet* or *DS320PR822 Linear Redriver for PCIe 5.0, CXL 2.0 with Four 2x2 Crosspoint Mux Data Sheet*). This document and all other collateral data related to the DS320PR810 redriver (application notes, models, and so forth) are available to download from the TI website. Alternatively, contact your local Texas Instruments field sales representative.

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1 Access Methods

There are two ways to access the DS320PR810 registers. The methods are:

- Register control through the Serial Management Bus (SMBus/I^{2}C)
- Automatic configuration through an external EEPROM

1.1 Register Programming Through SMBus

The DS320PR810 internal registers can be accessed through standard SMBus protocol. The DS320PR810 features two banks of channels, Bank 0 (Channels 0-3) and Bank 1 (Channels 4-7), each featuring a separate register set and requiring a unique SMBus slave address. The SMBus secondary address pairs (one for each channel bank) are determined at power up based on the configuration of the EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

The EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins along with the MODE, GAIN0, GAIN1, EQ0_1, EQ1_1, and RX_DET pins are 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the four valid levels as shown in Table 1-1.

Table 1-1. DS320PR810 5-Level Control Pin Settings

Pin Level	Pin Setting
L0	1kΩ to GND
L1	8.25kΩ to GND
L2	24.9kΩ to GND
L3	75kΩ to GND
L3	F (Float)

There are 16 unique SMBus slave address pairs (one address for each channel bank) that can be assigned to the device by placing external resistor straps on the EQ0_0 / ADDR1 and EQ1_0 / ADDR0 pins as shown in Table 1-2. When multiple DS320PR810 devices are on the same SMBus interface bus, each channel bank of each device must be configured with a unique SMBus slave address pair.

Table 1-2. DS320PR810 SMBus Address Map

EQ1 / ADDR1 Pin Level	EQ0 / ADDR0 Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1: Channels 4-7: 7-Bit Address [HEX]
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L0	L4	Reserved	Reserved
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L1	L4	Reserved	Reserved
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L2	L4	Reserved	Reserved
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

Table 1-2. DS320PR810 SMBus Address Map (continued)

EQ1 / ADDR1 Pin Level	EQ0 / ADDR0 Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1: Channels 4-7: 7-Bit Address [HEX]
L3	L4	Reserved	Reserved

1.2 Device Configuration Through External EEPROM

The DS320PR810 can automatically read its initial configuration from an external EEPROM at power up. Detailed information on EEPROM hex file generation for this device is available in the *Understanding EEPROM Programming for PCI-Express Gen-4 Redriver* (SNLA342) application note.

2 Register Map Overview

The DS320PR810 has two types of registers:

- **Share Registers** – These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers** – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

Both Share and Channel registers of a single channel bank are contained within a single register page as shown in Table 2-1.

Table 2-1. Register Map Overview

Address Range	Channel Bank 0 Access	Channel Bank 1 Access
0x00 - 0x1F	Channel 0 registers	Channel 4 registers
0x20 - 0x3F	Channel 1 registers	Channel 5 registers
0x40 - 0x5F	Channel 2 registers	Channel 6 registers
0x60 - 0x7F	Channel 3 registers	Channel 7 registers
0x80 - 0x9F	Broadcast write channel bank 0 registers, read channel 0 registers	Broadcast write channel bank 1 registers, read channel 4 registers
0xA0 - 0xBF	Broadcast write channel 0-1 registers, read channel 0 registers	Broadcast write channel 4-5 registers, read channel 4 registers
0xC0 - 0xDF	Broadcast write channel 2-3 registers, read channel 2 registers	Broadcast write channel 6-7 registers, read channel 6 registers
0xE0 - 0xFF	Bank 0 Share registers	Bank 1 Share registers

Complex bit access types are encoded to fit into small table cells. Table 2-2 shows the codes that are used for access types in this section.

Table 2-2. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read only access.
Write Type		
R/W	R/W	Read / Write access.
R/W/SC	R/W/SC	Read / Write access, self-clearing
Reset or Default Value		
-n		Value after reset or the default value.

2.1 Share Registers

Table 2-3. General Register (Offset = 0xE2) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device Reset Control: Reset all I^2C registers to default values (self- clearing).
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM Configuration Load.

Table 2-4. EEPROM_Status Register (Offset = 0xE3) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	0x0	EEPROM load complete.
6	eecfg_fail	R	0x0	EEPROM load failed.
5	eecfg_atmpt_1	R	0x0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_0	R	0x0	See MSB.
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

Table 2-5. DEVICE_ID0 Register (Offset = 0xF0) [reset = 0x06]

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011 (DS320PR810)
2	device_id0_2	R	0x1	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

Table 2-6. DEVICE_ID1 Register (Offset = 0xF1) [reset = 0x29]

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1001: DS320PR810
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x1	see MSB

2.2 Channel Registers

The DS320PR810 features two banks of channels, Bank 0 (Channels 0-3) and Bank 1 (Channels 4-7), each featuring a separate register set and requiring a unique SMBus secondary address.

Table 2-7. RX Detect Status Register (channel register base + offset = 0x00) [reset = 0x00]

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx Detect Positive Polarity Status: 0: Not detected 1: Detected - the value is latched.
6	rx_det_comp_n	R	0x0	Rx Detect Negative Polarity Status: 0: Not detected 1: Detected - the value is latched.
5:0	RESERVED	R	0x0	Reserved

Table 2-8. EQ Control Register (channel register base + offset = 0x01) [reset = 0x00]

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ Stage 1 Bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage1_3	R/W	0x0	EQ Boost Stage 1 Control. For details, see the DS320PR810 data sheet.
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost Stage 2 Control. For details, see the DS320PR810 data sheet.
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

Table 2-9. Mute EQ Control Register (channel register base + offset = 0x02) [reset = 0x00]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3	mute_eq	R/W	0x0	Mute EQ output
2:0	RESERVED	R	0x0	Reserved

Table 2-10. EQ Gain / Flat Gain Control Register (channel register base + offset = 0x03) [reset = 0x05]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile For details, see the DS320PR810 data sheet.
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	flat_gain_2	R/W	0x1	Flat Gain Select. For details, see the DS320PR810 data sheet.
1	flat_gain_1	R/W	0x0	
0	flat_gain_0	R/W	0x1	

Table 2-11. RX Detect Control Register (channel register base + offset = 0x04) [reset = 0x0]

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect_p/n decision: 0: Rx Detect state machine is enabled 1: Rx Detect state machine is overridden – always valid Rx termination detected
1	en_rx_det_count	R/W	0x0	Enable additional Rx detect polling: 0: Additional Rx Detect Polling disabled 1: Additional Rx Detect Polling enabled
0	sel_rx_det_count	R/W	0x0	Select number of Valid Rx detect polls - gated by en_rx_det_count = 1. 0: 2x consecutive valid detections 1: 3x consecutive valid detections

Table 2-12. PD Override Register (channel register base + offset = 0x05) [reset = 0x7F]

Bit	Field	Type	Reset	Description
7	device_en_override	R/W	0x0	Enable power down overrides through SMBus/I^2C 0: Manual override disabled 1: Manual override enabled
6:0	device_en	R/W	0x7F	Manual power down of redriver various blocks – gated by device_en_override = 1 0x00: All blocks are disabled 0x7F: All blocks are enabled

Table 2-13. Bias Register (channel register base + offset = 0x06) [reset = 0x20]

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	bias_current_2	R/W	0x1	Control bias current
4	bias_current_1	R/W	0x0	See MSB.
3	bias_current_0	R/W	0x0	See MSB.
2:0	RESERVED	R	0x0	Reserved

3 Equalization Control Settings

The DS320PR810 employs a Continuous Time Linear Equalizer (CTLE) to provide a programmable high-frequency boost. Table 3-1 provides guidance on how to write the desired CTLE Index to the EQ and Flat Gain control registers.

Table 3-1. CTLE Index Equalization Settings

Equalization Setting					Typical EQ Boost (dB)	
	SMBus/I²C Mode					
EQ Index	EQ Control Register Eq_stage1_3:0	EQ Control Register Eq_stage2_2:0	EQ GAIN / Flat Gain Control Register Eq_profile_3:0	EQ Control Register Eq_stage1_bypass	@ 8GHz	@ 16GHz
0	0	0	0	1	For values, see the DS320PR810 data sheet	For values, see the DS320PR810 data sheet
1	1	0	0	1		
2	3	0	0	1		
Default	0	0	0	0		
5	0	0	1	0		
6	1	0	1	0		
7	2	0	1	0		
8	3	0	3	0		
9	4	0	3	0		
10	5	1	7	0		
11	6	1	7	0		
12	8	1	7	0		
13	10	1	7	0		
14	10	2	15	0		
15	11	3	15	0		
16	12	4	15	0		
17	13	5	15	0		
18	14	6	15	0		
19	15	7	15	0		

4 CTLE Index and Flat Gain Selection Matrix

Section 4 details the register offsets and values which can be written to select the desired CTLE Index and Flat Gain settings of the DS320PR810.

Table 4-1. CTLE Index/Flat Gain Setting Matrix

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
0	-6dB	0x80	0x00
0	-4dB	0x80	0x01
0	-2dB	0x80	0x03
0	0dB (Default)	0x80	0x05
0	2dB	0x80	0x07
1	-6dB	0x88	0x00
1	-4dB	0x88	0x01
1	-2dB	0x88	0x03
1	0dB (Default)	0x88	0x05
1	2dB	0x88	0x07
2	-6dB	0x98	0x00
2	-4dB	0x98	0x01

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
2	-2dB	0x98	0x03
2	0dB (Default)	0x98	0x05
2	2dB	0x98	0x07
Default	-6dB	0x00	0x00
Default	-4dB	0x00	0x01
Default	-2dB	0x00	0x03
Default	0dB (Default)	0x00	0x05
Default	2dB	0x00	0x07
5	-6dB	0x00	0x08
5	-4dB	0x00	0x09
5	-2dB	0x00	0x0B
5	0dB (Default)	0x00	0x0D
5	2dB	0x00	0x0F
6	-6dB	0x08	0x08
6	-4dB	0x08	0x09
6	-2dB	0x08	0x0B
6	0dB (Default)	0x08	0x0D
6	2dB	0x08	0x0F
7	-6dB	0x10	0x08
7	-4dB	0x10	0x09
7	-2dB	0x10	0x0B
7	0dB (Default)	0x10	0x0D
7	2dB	0x10	0x0F
8	-6dB	0x18	0x18
8	-4dB	0x18	0x19
8	-2dB	0x18	0x1B
8	0dB (Default)	0x18	0x1D
8	2dB	0x18	0x1F
9	-6dB	0x20	0x18
9	-4dB	0x20	0x19
9	-2dB	0x20	0x1B
9	0dB (Default)	0x20	0x1D
9	2dB	0x20	0x1F
10	-6dB	0x29	0x38
10	-4dB	0x29	0x39
10	-2dB	0x29	0x3B
10	0dB (Default)	0x29	0x3D
10	2dB	0x29	0x3F
11	-6dB	0x31	0x38
11	-4dB	0x31	0x39
11	-2dB	0x31	0x3B
11	0dB (Default)	0x31	0x3D
11	2dB	0x31	0x3F
12	-6dB	0x41	0x38
12	-4dB	0x41	0x39
12	-2dB	0x41	0x3B
12	0dB (Default)	0x41	0x3D

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
12	2dB	0x41	0x3F
13	-6dB	0x51	0x38
13	-4dB	0x51	0x39
13	-2dB	0x51	0x3B
13	0dB (Default)	0x51	0x3D
13	2dB	0x51	0x3F
14	-6dB	0x52	0x78
14	-4dB	0x52	0x79
14	-2dB	0x52	0x7B
14	0dB (Default)	0x52	0x7D
14	2dB	0x52	0x7F
15	-6dB	0x5B	0x78
15	-4dB	0x5B	0x79
15	-2dB	0x5B	0x7B
15	0dB (Default)	0x5B	0x7D
15	2dB	0x5B	0x7F
16	-6dB	0x64	0x78
16	-4dB	0x64	0x79
16	-2dB	0x64	0x7B
16	0dB (Default)	0x64	0x7D
16	2dB	0x64	0x7F
17	-6dB	0x6D	0x78
17	-4dB	0x6D	0x79
17	-2dB	0x6D	0x7B
17	0dB (Default)	0x6D	0x7D
17	2dB	0x6D	0x7F
18	-6dB	0x76	0x78
18	-4dB	0x76	0x79
18	-2dB	0x76	0x7B
18	0dB (Default)	0x76	0x7D
18	2dB	0x76	0x7F
19	-6dB	0x7F	0x78
19	-4dB	0x7F	0x79
19	-2dB	0x7F	0x7B
19	0dB (Default)	0x7F	0x7D
19	2dB	0x7F	0x7F

5 Example Programming Sequences

The DS320PR810 is highly programmable and customizable for multiple applications. The following sections provide guidance for programming the DS320PR810 for common applications.

The following information is provided in each sequence:

- **Step**: Many sequences contain several steps. The order in which actions are to be taken is indicated by the step number.
- **Register Set**: Actions are intended for either the Shared or Channel register of either Bank 0 or Bank 1. Since each channel bank has its own SMBus address, no explicit channel bank selection is necessary.
- **Operation**: Read or Write. If it is a Read operation, a register value or write mask is not associated.
- **Register Address**: Select the register to write to.
- **Register Value**: Value to write to register address.
- **Write Mask**: Unless the write mask is 0xFF, all writes can be performed as a read/modify/write operation. Only the bits identified by the mask should be modified.

5.1 Set CTLE Gain Level

The DS320PR810 requires manual CTLE tuning. The CTLE gain level can be changed by modifying the value of each CTLE stage (CTLE Boost Stage 1 and 2) or by bypassing the EQ1 stage. The CTLE level may be set individually for each channel or broadcast to all channels. Table 5-1 shows an example sequence for setting the CTLE gain level to CTLE Index 2, Flat Gain (DC Gain) to 0dB on the Bank 0 channels and to CTLE Index 6, Flat Gain (DC Gain) to 0dB on the Bank 1 channels using individual writes to each channel. Use register values provided in Table 4-1 to set the CTLE gain level to any other available index.

Table 5-1. Sequence to Set CTLE Level on Each Channel Individually

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channel 0	Write	0x01	0x98	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 2 on Channel 0.
2	Bank 0: Channel 0	Write	0x03	0x05	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 2 on Channel 0.
3	Bank 0: Channel 1	Write	0x21	0x98	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 2 on Channel 1.
4	Bank 0: Channel 1	Write	0x23	0x05	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 2 on Channel 1.
5	Bank 0: Channel 2	Write	0x41	0x98	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 2 on Channel 2.
6	Bank 0: Channel 2	Write	0x43	0x05	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 2 on Channel 2.
7	Bank 0: Channel 3	Write	0x61	0x98	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 2 on Channel 3.
8	Bank 0: Channel 3	Write	0x63	0x05	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 2 on Channel 3.
9	Bank 1: Channel 4	Write	0x01	0x08	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 6 on Channel 4.
10	Bank 1: Channel 4	Write	0x03	0x0D	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 6 on Channel 4.

Table 5-1. Sequence to Set CTLE Level on Each Channel Individually (continued)

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
11	Bank 1: Channel 5	Write	0x21	0x08	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 6 on Channel 5.
12	Bank 1: Channel 5	Write	0x23	0x0D	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 6 on Channel 5.
13	Bank 1: Channel 6	Write	0x41	0x08	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 6 on Channel 6.
14	Bank 1: Channel 6	Write	0x43	0x0D	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 6 on Channel 6.
15	Bank 1: Channel 7	Write	0x61	0x08	0x7F	Set CTLE Stage 1 & 2 1st Order Boost Control to Index 6 on Channel 7.
16	Bank 1: Channel 7	Write	0x63	0x0D	0x78	Set CTLE Stage 1 2nd Order Boost Control to Index 6 on Channel 7.

Assuming 0x18 and 0x19 are the SMBus addresses for Channel Banks 0 and 1, respectively, the following is the XML batch script of the sequence in Table 5-1:

```
<i2c_write addr="0x18" count="0" radix"16">01 98</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">03 05</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">21 98</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">23 05</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">41 98</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">43 05</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">61 98</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">63 05</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">01 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">03 0D</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">21 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">23 0D</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">41 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">43 0D</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">61 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">63 0D</i2c_write>
```

Table 5-2 shows an example sequence to set the CTLE gain level to CTLE Index 2, 0dB Flat Gain (DC Gain) on Bank 0 channels and to CTLE Index 6, 0dB Flat Gain (DC Gain) on Bank 1 channels using a broadcast write to each channel bank.

Table 5-2. Sequence to Broadcast CTLE Level to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x81	0x98	0x7F	Set EQ to Index 2 on Channels 0-3.
2	Bank 0: Channels 0-3	Write	0x83	0x05	0x78	Set EQ to Index 2 on Channels 0-3.
3	Bank 1: Channels 4-7	Write	0x81	0x08	0x7F	Set EQ to Index 6 on Channels 4-7.
4	Bank 1: Channels 4-7	Write	0x83	0x0D	0x78	Set EQ to Index 6 on Channels 4-7.

Assuming 0x18 and 0x19 are the SMBus addresses for Channel Banks 0 and 1, respectively, the following is the XML batch script of the sequence in Table 5-2:

```
<i2c_write addr="0x18" count="0" radix"16">81 98</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">83 05</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">81 08</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">83 0D</i2c_write>
```

5.2 Set CTLE Flat Gain Level

The CTLE Flat Gain (DC Gain) value can be set individually for each channel or broadcast to all channels. Table 5-3 shows an example sequence to set the Flat Gain (DC Gain) on Bank 0 and Bank 1 channels to 0dB or -4dB.

Table 5-3. Sequence to Broadcast Flat Gain Level to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x83	0x05	0x07	Set Flat Gain on Bank 0 channels to: 0dB (Default).
				0x01	0x07	Set Flat Gain on Bank 0 channels to: -4dB.
2	Bank 1: Channels 4-7	Write	0x83	0x05	0x07	Set Flat Gain on Bank 1 channels to: 0dB (Default).
				0x01	0x07	Set Flat Gain on Bank 1 channels to: -4dB.

Assuming 0x18 and 0x19 are the SMBus addresses for Channel Banks 0 and 1, respectively, the following is the XML batch script of the 0dB Flat Gain example sequence shown in Table 5-3.

```
<i2c_write addr="0x18" count="0" radix"16">83 05</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">83 05</i2c_write>
```

5.3 Set PD Control

The PD functionality of the DS320PR810 can be controlled individually for each channel or broadcast to all channels. This can be particularly useful for applications which require power-down functionality for PCIe link-widths which are smaller than x4 (such as x2 or x1). Table 5-4 shows an example sequence to **power down** or **power on** all channels.

Table 5-4. Sequence to Broadcast Power Down or On to All Channels

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0: Channels 0-3	Write	0x85	0x80	0xFF	Power down all channels 0-3
				0x7F	0xFF	Power on all channels 0-3
2	Bank 1: Channels 4-7	Write	0x85	0x80	0xFF	Power down all channels 4-7
				0x7F	0xFF	Power on all channels 4-7

Assuming 0x18 and 0x19 are the SMBus addresses for Channel Banks 0 and 1, respectively, the following is the XML batch script of the sequence in Table 5-4:

```
<i2c_write addr="0x18" count="0" radix"16">85 80</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">85 80</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">85 7F</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">85 7F</i2c_write>
```

5.4 Set SEL Input (DS320PR822)

Note

This section applies to the DS320PR822 only.

On the DS320PR822, the inputs SEL0 and SEL1 can be manually set to select the cross-point data path for the respective channel banks. Note that the SEL0 pin configures the cross-point for channels 0-3 and the SEL1 pin configures the cross-point for channels 4-7. Table 5-5 shows an example sequence for setting the SELx pin on Bank 0 and Bank 1 to the straight data path or cross-point data path.

Table 5-5. Sequence to set Cross-Point SEL Pins by Register Bank

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Bank 0 Share	Write	0xEE	0x44	0x44	Set SEL0 override bit for all Bank 0 channels.
2	Bank 0 Share	Write	0xEF	0x00	0x44	Set SEL0 bit low for all Bank 0 channels to select straight data path.
				0x44	0x44	Set SEL0 bit high for all Bank 0 channels to select cross-point data path.
3	Bank 1 Share	Write	0xEE	0x44	0x44	Set SEL1 override bit for all Bank 0 channels.
4	Bank 1 Share	Write	0xEF	0x00	0x44	Set SEL1 bit low for all Bank 0 channels to select straight data path.
				0x44	0x44	Set SEL1 bit high for all Bank 0 channels to select cross-point data path.

Assuming 0x18 and 0x19 are the SMBus addresses for Banks 0 and 1, respectively, the following is the XML batch script of the cross-point data path selection sequence in Table 5-5:

```
<i2c_write addr="0x18" count="0" radix"16">EE 44</i2c_write>
<i2c_write addr="0x18" count="0" radix"16">EF 44</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">EE 44</i2c_write>
<i2c_write addr="0x19" count="0" radix"16">EF 44</i2c_write>
```

6 References

- Texas Instruments, *DS320PR810 Eight-Channel Linear Redriver for PCIe 5.0, CXL 1.1 Data Sheet*
- Texas Instruments, *DS320PR822 Linear Redriver for PCIe 5.0, CXL 2.0 with Four 2x2 Crosspoint Mux Data Sheet*
- Texas Instruments, *Understanding EEPROM Programming for DS160PR810 PCI-Express Gen-4 Redriver* (SNLA342)

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