User's Guide

DS320PR810-SMP-EVM User's Guide

ABSTRACT

The DS320PR810-SMP-EVM evaluation modules provides a complete high-bandwidth platform for evaluating the signal conditioning features of the Texas Instruments DS320PR810 Octal-Channel PCI-Express 5.0 Linear Redriver. This evaluation board can be used for electrical testing and performance evaluation of the high-speed differential signals interfacing directly to test equipment via SMP connector interface.

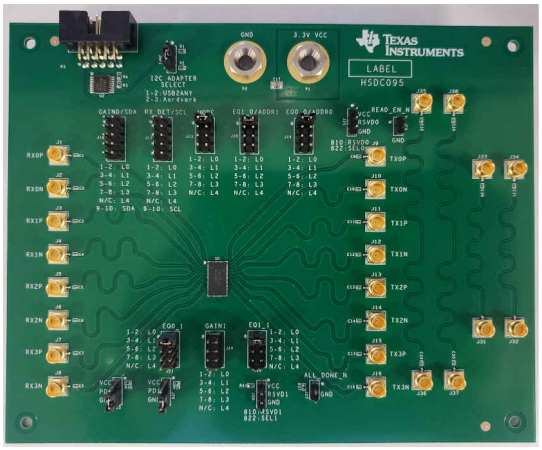

Figure 1-1. DS320PR810-SMP-EVM Top Side View

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1 Introduction

The DS320PR810-SMP-EVM features one DS320PR810 linear redriver that routes the redriver channels 0-3 to SMP connectors to interface directly to test equipment for signal measurements.

1.1 Features

- SMP connector interface on high-speed signal channels 0-3
- Linear equalization for seamless support of link training and PCIe channel extension
- CTLE boosts up to 24dB at 16GHz
- Programmable device configuration through GPIO or I2C
- Industrial temperature range: –40°C to 85°C
- Flow-through layout in 5.5 mm × 10 mm, 64-pin, leadless WQFN 0.4-mm pitch package

1.2 Applications

- PCI Express Gen-1, 2, 3, 4 and 5
- High-speed interfaces up to 32Gbps
- Enterprise server motherboard, workstation
- Enterprise storage
- Enterprise add-in card, end-point

2 Description

2.1 DS320PR810 5-Level I/O Control Inputs

The DS320PR810 features 5-level input pins (MODE, GAIN0, GAIN1, RX_DET, EQ0_0/ADDR0, EQ1_0/ADDR1, EQ0_1, and EQ1_1) that are used to control the configuration of the device. These 5-level inputs use a resistor divider to set the valid levels to provide a wider range of control settings.

Table 2-1. Five-Level Control Pin Settings

PIN LEVEL	PIN SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	Float

2.2 DS320PR810 Modes of Operation

Each DS320PR810 can be configured to operate in either Pin Mode or I2C Mode. The mode of operation of the DS320PR810 is determined by the pin strap setting on the MODE pin as shown in Table 2-2.

Table 2-2. Modes of Operation

MODE PIN LEVEL	MODE OF OPERATION
L0	Pin Mode
L1	SMBus Mode or I2C Primary Mode
L2	SMBus Mode or I2C Secondary Mode
L3	RESERVED
L4	RESERVED

2.3 DS320PR810 SMBus or I2C Register Control Interface

The DS320PR810 internal registers can be accessed through standard SMBus protocol. The DS320PR810 features two banks of channels, Bank 0 (Channels 0–3) and Bank 1 (Channels 4–7), each featuring a separate register set and requiring a unique SMBus secondary address. The SMBus secondary address pairs (one for each channel bank) are determined at power up based on the configuration of the EQ0_0/ADDR1 and EQ1_0/ ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

There are 16 unique SMBus secondary address pairs (one address for each channel bank) that can be assigned to the device by placing external resistor straps on the EQ0_0/ADDR1 and EQ1_0/ADDR0 pins as shown in Table 2-3. When multiple DS320PR810 devices are on the same SMBus interface bus, each channel bank of each device must be configured with a unique SMBus slave address pair. In this EVM,only Bank 0 channels are routed to SMP connectors, thus only Bank 0 registers need to be programmed.

Table 2-3. DS320PR810 SMBus Address Map

ADDR1 Pin Level	ADDR0 Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1 Channels 4-7: 7-Bit Address [HEX]
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L0	L4	Reserved	Reserved
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L1	L4	Reserved	Reserved
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L2	L4	Reserved	Reserved
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37
L3	L4	Reserved	Reserved

2.4 DS320PR810 Equalization Control

Each channel of the DS320PR810 features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 2-4 shows available equalization boost through EQ control pins (EQ1_0 and EQ0_0 for channels 0–3 and EQ1_1 and EQ0_1 for channels 4–7) when in Pin Control mode (MODE = L0).

Table 2-4. Equalization Control Settings

EQ INDEX	EQ1 PIN LEVEL	EQ0 PIN LEVEL	CTLE BOOST AT 8GHz (dB)	CTLE BOOST AT 16GHz (dB)
0	L0	L0	Refer to data sheet	Refer to data sheet
1	L0	L1		
2	L0	L2		
3	L0	L3		
4	L0	L4		
5	L1	L0		
6	L1	L1		
7	L1	L2		
8	L1	L3		
9	L1	L4		
10	L2	L0		
11	L2	L1		
12	L2	L2		
13	L2	L3		
14	L2	L4		
15	L3	L0		
16	L3	L1		
17	L3	L2		
18	L3	L3		
19	L3	L4		

The equalization gain of each channel of each device can also be set by writing to SMBus, I2C registers in I2C Mode.

2.5 DS320PR810-SMP-EVM Controls

Section 2.5 shows DS320PR810-SMP-EVM controls.

Table 2-5. DS320PR810-SMP-EVM Controls

COMPONENT	NAME	Shunt Position / DESCRIPTION
JMP1	I2C Adapter Select	I2C Mode Select: 1-2 USB2ANY 2-3 Aardvark
J17	RX_DET/SCL	RX DET/SCL: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 9-10: SCL N/C: L4
J18	GAIN0/SDA	GAIN0/SDA: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 9-10: SDA N/C: L4
J19	EQ0/ADDR0	EQ0/ADDR0: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4
J20	EQ1/ADDR1	EQ1/ADDR1: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4
J21	EQ0_1	EQ0_1: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4
J22	EQ1_1	EQ1_1: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4
J23	MODE	MODE: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4

Table 2-5. DS320PR810-SMP-EVM Controls (continued)

COMPONENT	NAME	Shunt Position / DESCRIPTION
J24	GAIN1	GAIN1: 1-2: L0 3-4: L1 5-6: L2 7-8: L3 N/C: L4
J25	PD0	PD0: 1-2: Pull-Up – 3.3V 2-3: GND
J26	PD1	PD1: 1-2: Pull-Up – 3.3V 2-3: GND
J27	ALL_DONE_N	ALL_DONE_N: 1-2: GND N/C: Pull-Up to 3.3V
J28	READ_EN_N	READ_EN_N: 1: READ_EN_N 2: GND
J29	RSVD0	RSVD0: 1-2: Pull-Up – 3.3V 2-3: GND
J30	RSVD1	RSVD1: 1-2: Pull-Up – 3.3V 2-3: GND

2.6 Quick-Start Guide (Pin Mode)

Check that the shunts are at the following positions as shown below:

1. The redriver is configured to operate in Pin Mode (MODE pin tied to L0 using J23 header).
2. RX_Detect state machine is enabled by leaving J17 No Connect (Redriver Channel Tx must detect termination to enable the channel).
3. The redriver is enabled (PD0 and PD1 pins tied to GND using J25 and J26 headers).
4. EQ level of the RX CTLE of the redrivers is set by using J19 - J22.Gain is set by headers J18 and J24. Please refer to datasheet for CTLE and GAIN values.

2.7 Quick-Start Guide (SMBus Slave Mode)

1. Configure all devices to operate in the SMBus Secondary Mode by setting the MODE pin to the L2 level. This is accomplished by placing a shunt on J23 - L2 location.
2. Set a unique SMBus Secondary address by placing shunts on J19 (ADDR0) and J20 (ADDR1). Refer to Table 2-3 for details.
3. Move shunts on J17 and J18 to pins 9-10 to connect SCL and SDA.
4. Select I2C controller (Aardvark or USB2ANY) by placing shunts on JMP1.
5. Connect the USB2ANY (Or aardvark) Adapter to P3 (Note that the Adapter is not supplied with the DS160PR810-SMP-EVM).
6. Install SigCon Architect Version 3.0.1.0 application and the DS320PRxx profile.
7. Power-up the EVM board (P1=3.3V, P2=GND).
8. Start the SigCon Architect application.
9. Select the DS320PR8xx Configuration Page and click on "Apply" box to enable the device profile. If necessary, edit devices addresses in the Edit Device Addresses box.
10. In the DS320PR8xx High Level Page, select Block Diagram as shown in Figure 2-1.
11. Select the desired EQ Settings and Driver VOD.
12. Select channels to which you want to apply the selected settings and click "Apply to All Channels".

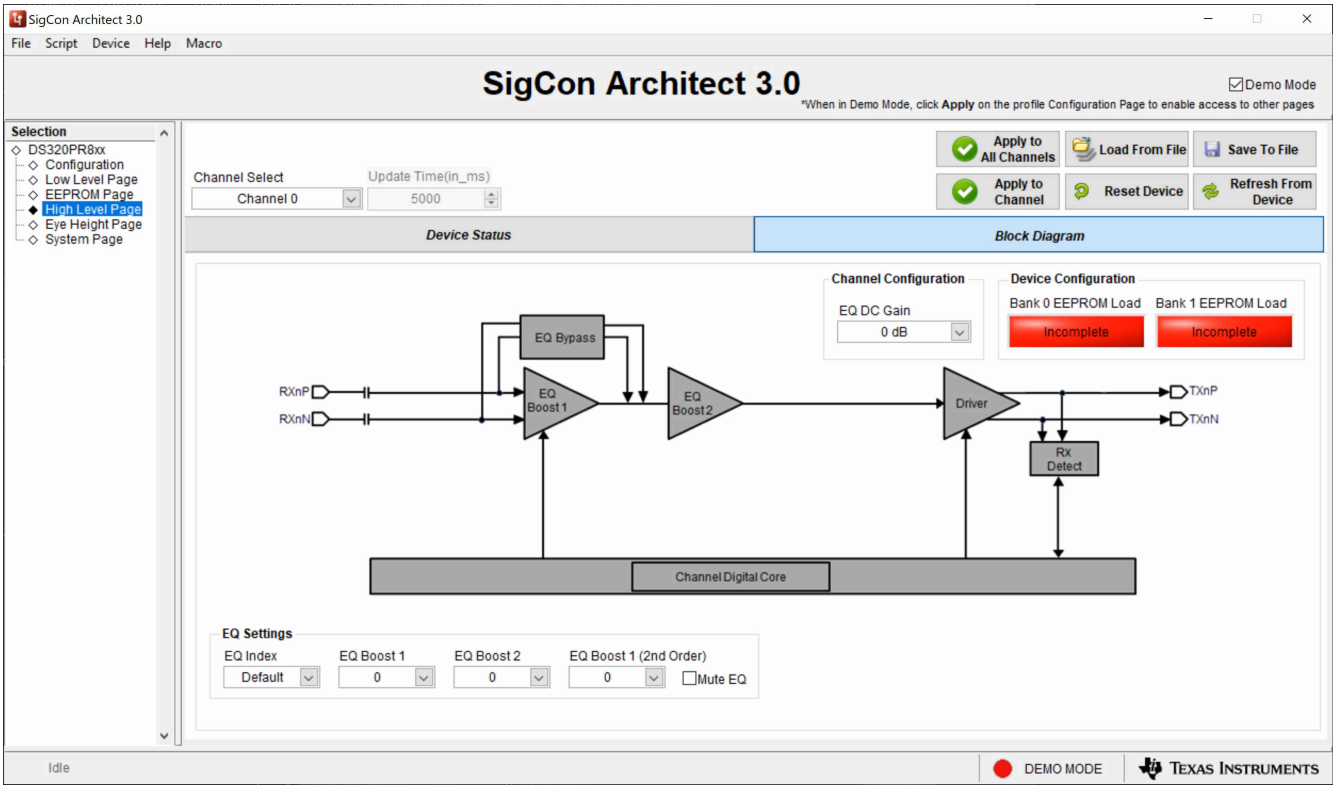

Figure 2-1. SigCon Architect DS320PR810 High Level Page

3 Schematics

Figure 3-1 through Figure 3-2 illustrate the EVM schematics.

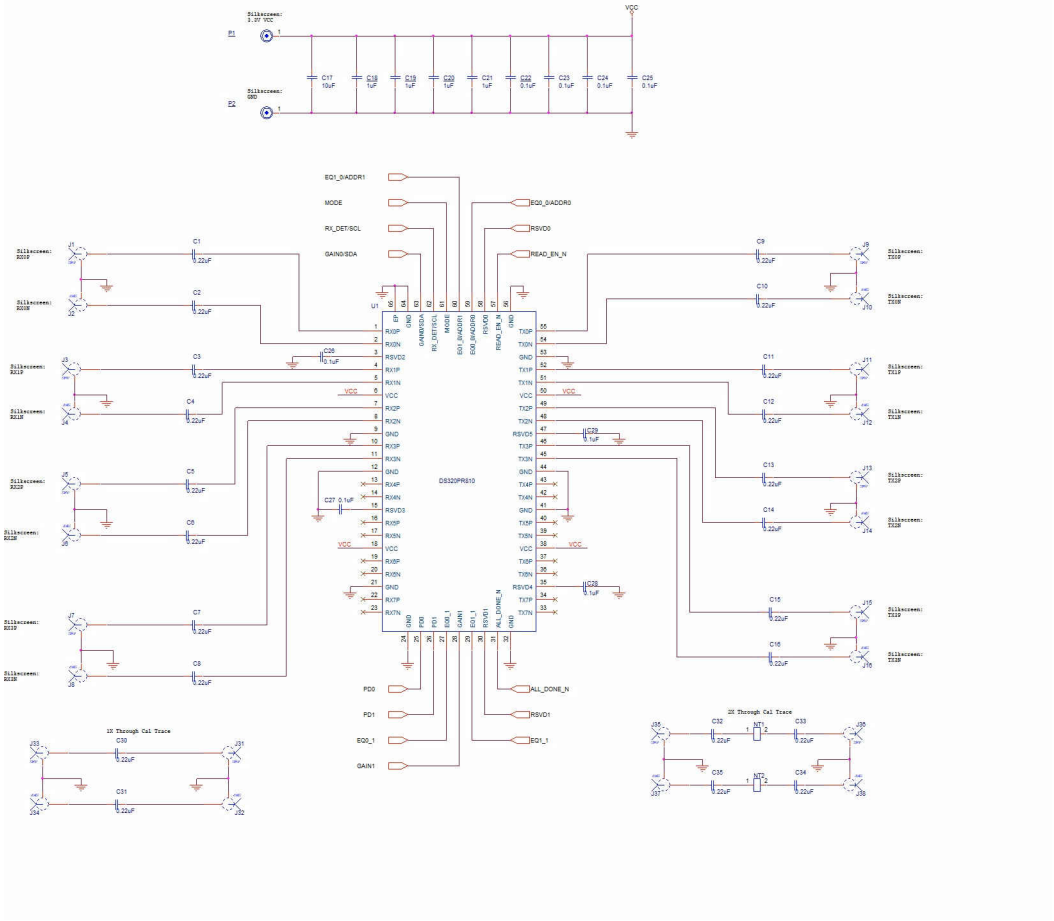

Figure 3-1. Schematic Page 1

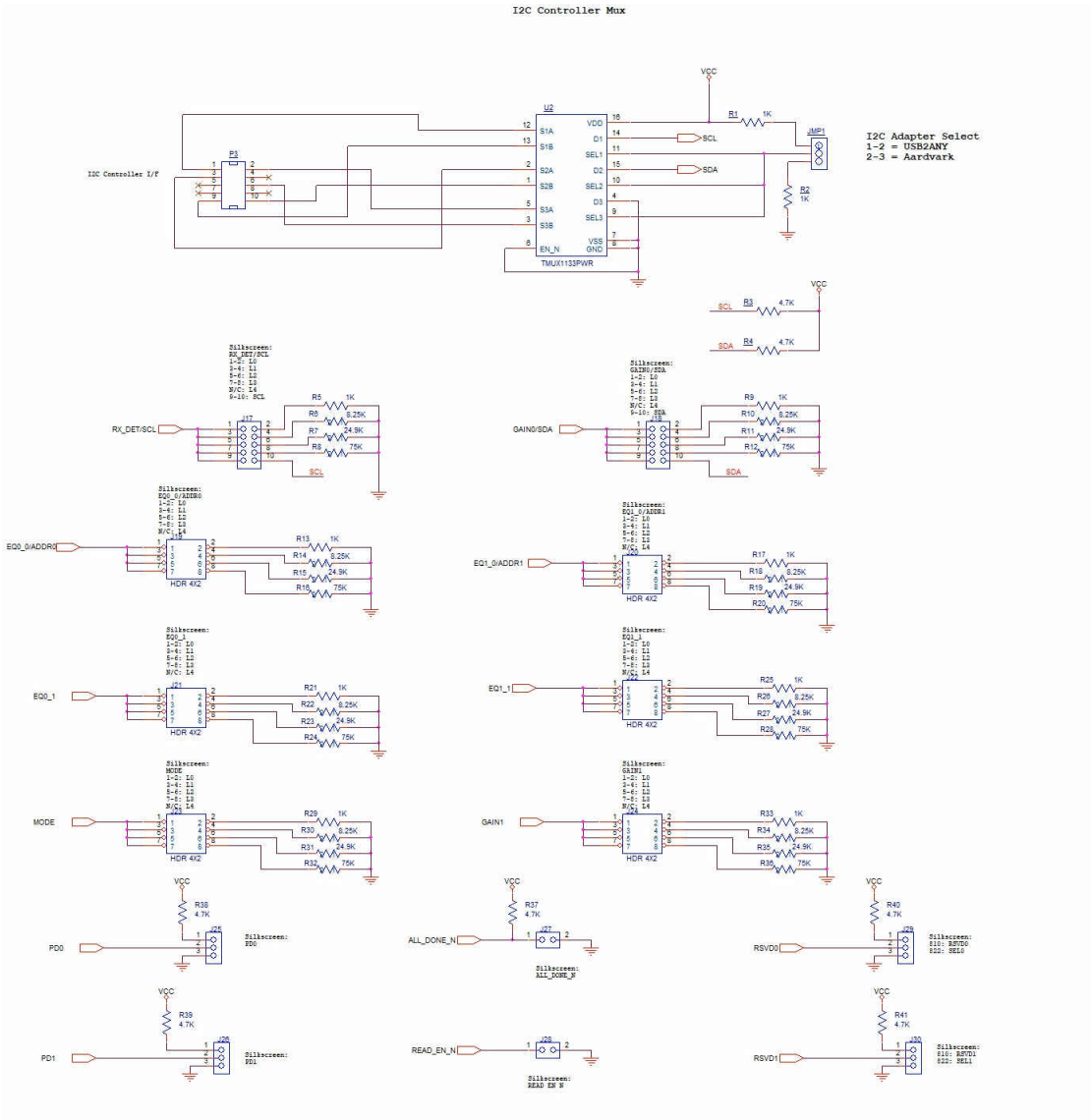

Figure 3-2. Schematic Page 2

4 Board Layout

Figure 4-1 and Figure 4-2 illustrate the EVM board layouts.

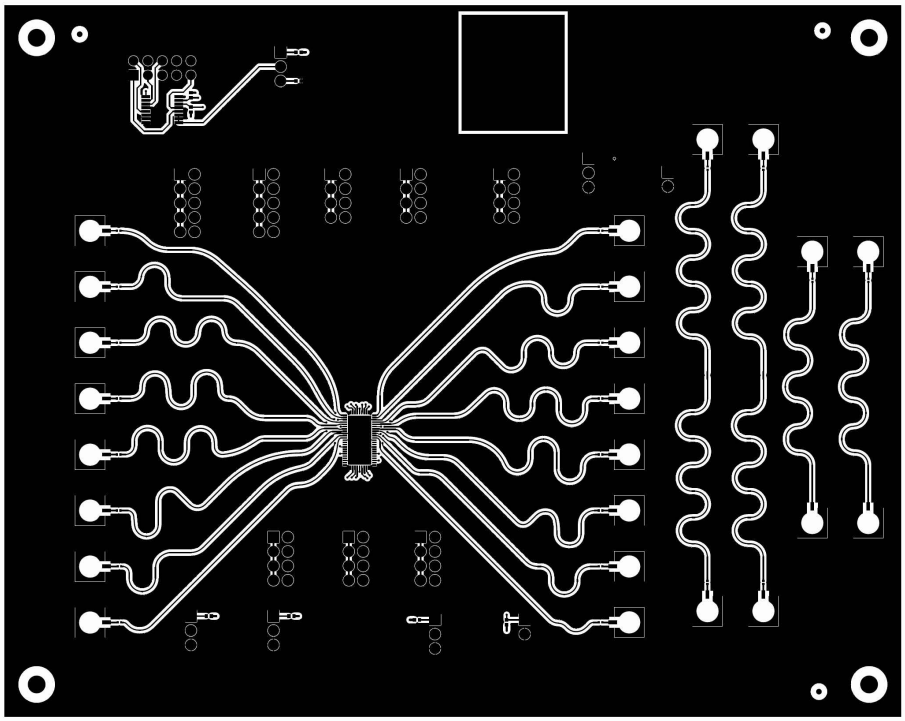

Figure 4-1. Top Layer

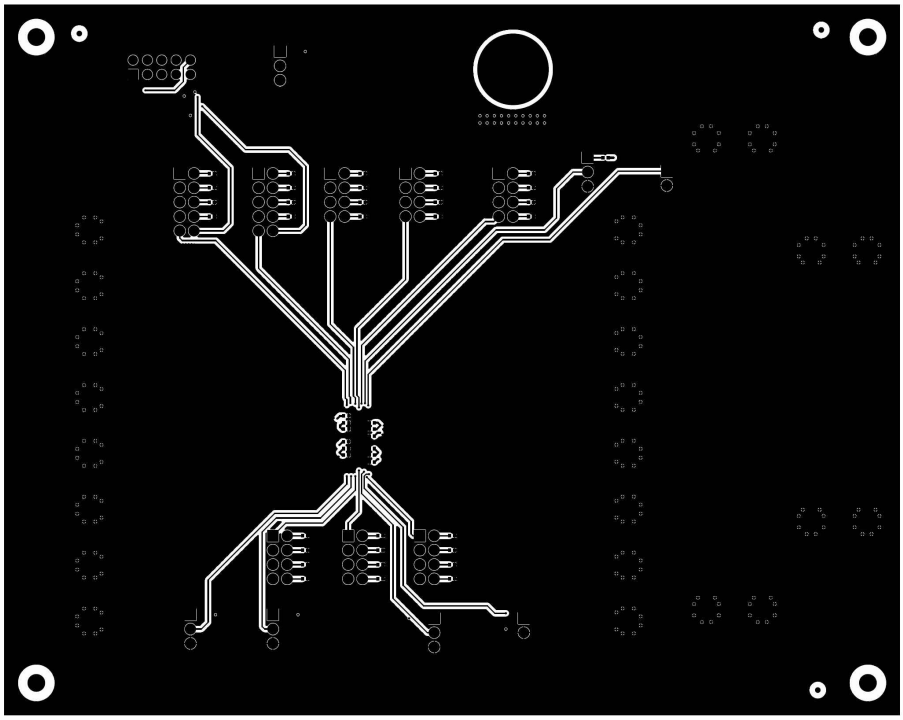

Figure 4-2. Bottom Layer

5 Bill of Materials

Section 5 lists the EVM bill of materials.

Item	Quantity	Reference	Value	Manufacturer	Manufacturer_Part_Number
1	22	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C30,C31,C32,C33,C34,C35	0.22uF	TDK Corporation	C0603X5R0J224K030BB
2	1	C17	10uF	TDK Corporation	C2012X6S1C106K085AC
3	4	C18,C19,C20,C21	1uF	TDK Corporation	C1005X6S1C105K050BC
4	8	C22,C23,C24,C25,C26,C27,C28,C29	0.1uF	TDK Corporation	C1005X7R1C104K050BC
5	1	JMP1	Header 3x1	AMP	
6	24	J1,J2,J3,J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15,J16,J31,J32,J33,J34,J35,J36,J37,J38	SMP	Rosenberger	
7	2	J17,J18	HDR5X2 .1X.1	ANY	
8	6	J19,J20,J21,J22,J23,J24	HDR 4X2	ANY	
9	4	J25,J26,J29,J30	HDR3X1 M .1	ANY	
10	2	J27,J28	HDR2X1 M .1	ANY	
11	2	P1,P2	Banana-Jack	ANY	
12	1	P3	Header 5x2 0.1" Shroud RA thru-hole	3M	
13	10	R1,R2,R5,R9,R13,R17,R21,R25,R29,R33	1K	Panasonic Electronic Components	ERJ-2GEJ102X
14	7	R3,R4,R37,R38,R39,R40,R41	4.7K	Panasonic Electronic Components	ERJ-2GEJ472X
15	8	R6,R10,R14,R18,R22,R26,R30,R34	8.25K	Panasonic Electronic Components	ERJ-2RKF8251X
16	8	R7,R11,R15,R19,R23,R27,R31,R35	24.9K	Panasonic Electronic Components	ERJ-2RKF2492X
17	8	R8,R12,R16,R20,R24,R28,R32,R36	75K	Panasonic Electronic Components	ERA-2AED753X
18	1	U1	DS320PR810	Texas Instruments	DS320PR810
19	1	U2	TMUX1133PWR	Texas Instruments	TMUX1133PWR

6 References

For references, see the following:

1. Texas Instruments, *DS320PR810 Octal-Channel PCI-Express 5.0 Linear Redriver* data sheet.

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