Technical Article

Troubleshooting Guidelines when Display Not Available to DS90UB936-Q1

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Introduction

DS90UB936-Q1 is a vehicle-grade FPD-LINK III camera-side deserializer chip that enables two serializers to transmit data simultaneously, supporting up to 3Gbps per port. In the automotive industry, it is widely used in related applications such as e-mirrors and surround-view cameras. This document mainly describes the situation under which the display is not properly seen when debugging the system. For this reason, you need to troubleshoot the hardware design, signal link, power management, and software configuration in multiple dimensions and provide the corresponding solutions.

Description of the faults

In a practical application case, the problem can be mainly described as that the rear-level SoC does not properly display the image transmitted from the camera side. The situation where this problem occurs shall be considered from both the hardware and software perspectives, and the specific problem points shall be gradually investigated and confirmed.

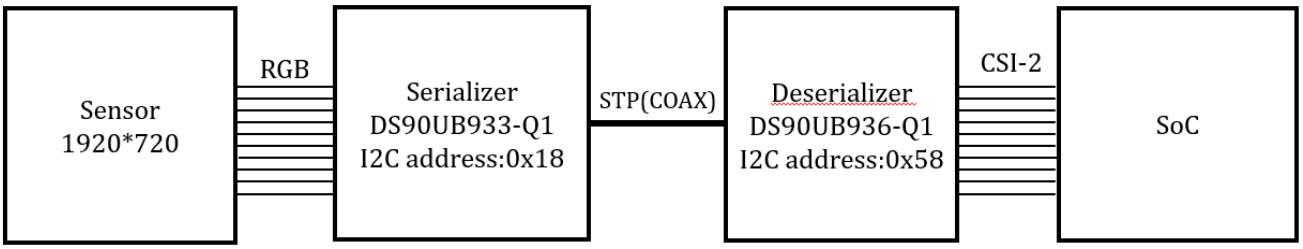


Figure 1. Block diagram of the system

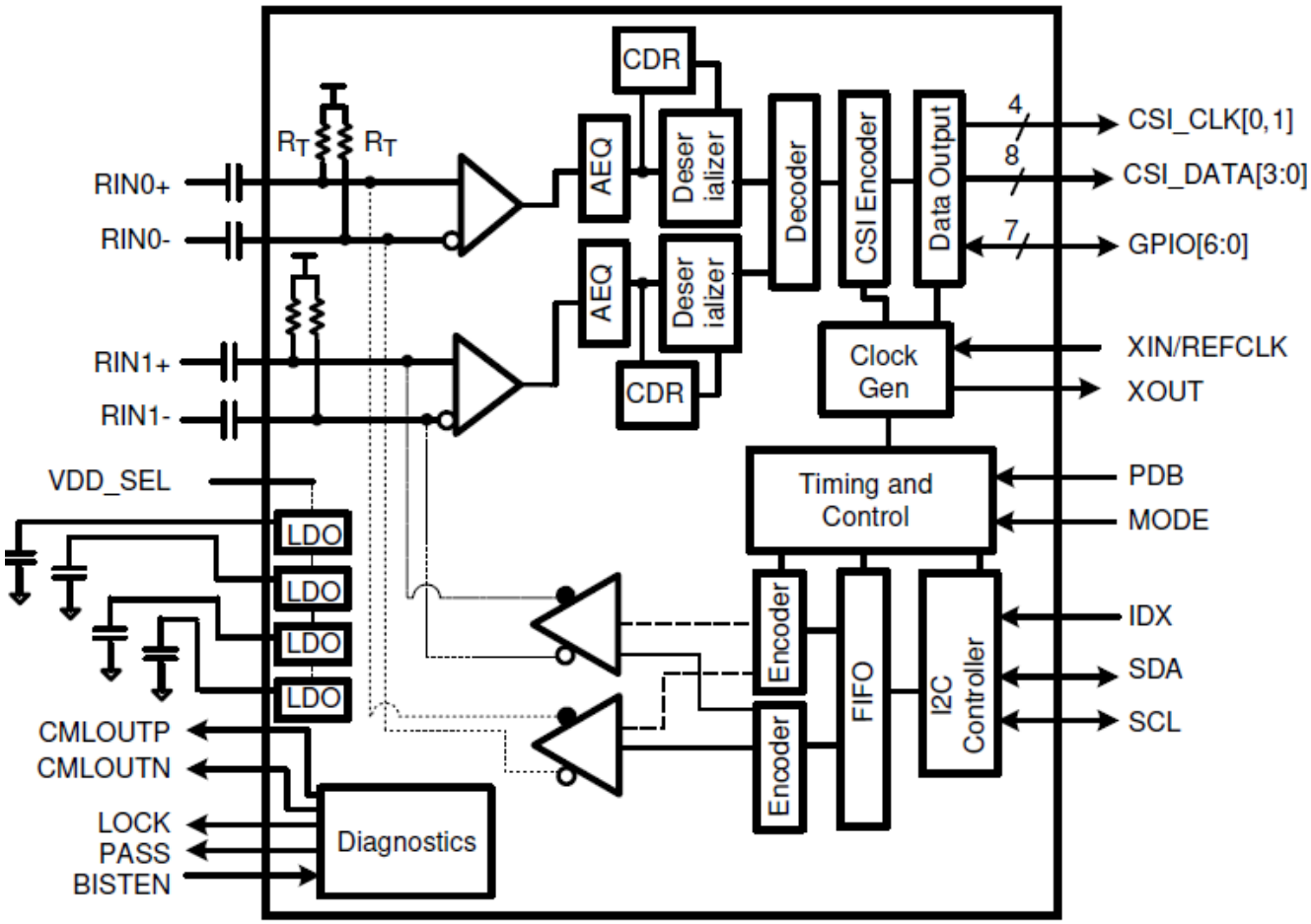


Figure 2. DS90UB936-Q1 block diagram

Hardware perspective

1. Power-up sequencing, and power stability

   The detailed requirements for power-up sequencing, are proposed for DS90UB936-Q1, as shown in the following diagram. All power supplies can be probed with an oscilloscope to meet sequencing requirements. One of the key troubleshooting issues to be addressed is whether the PDB powers up after VDD18/VDDIO. DS90UB936-Q1 can be powered up in two ways:

   a. VDD11 is supplied by an internal LDO

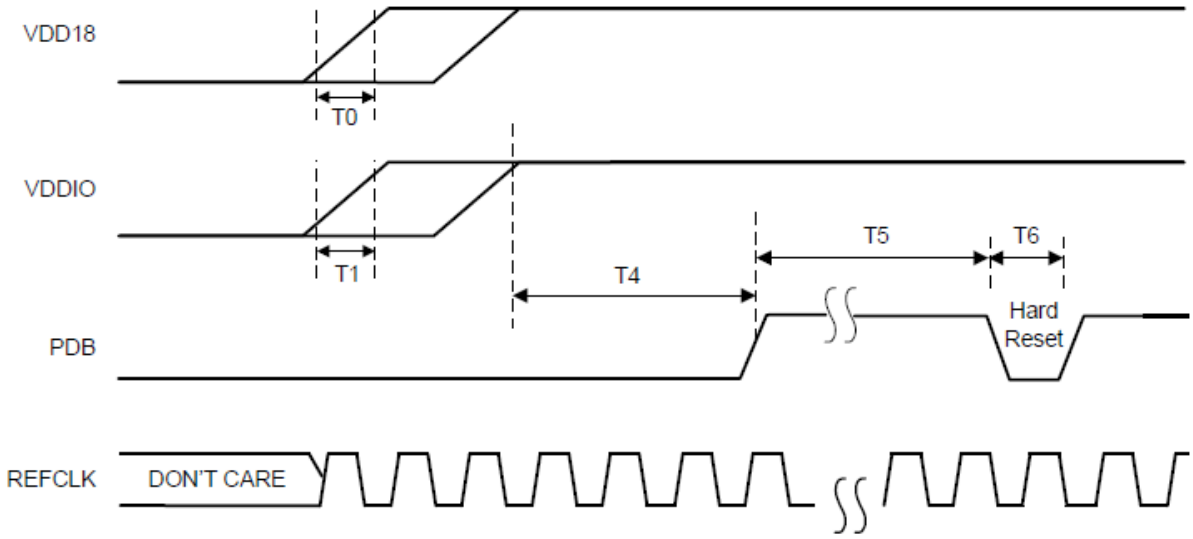


Figure 3. DS90UB936-Q1 power-up sequencing (a)

b. VDD11 is supplied by an external LDO

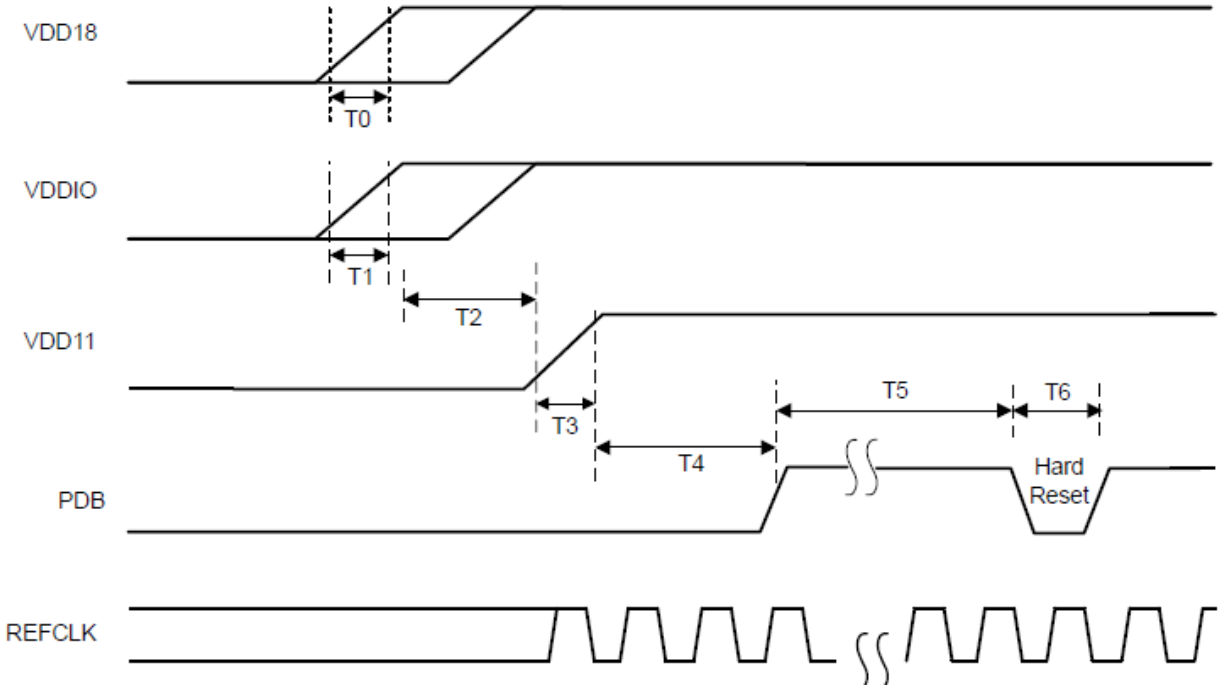


Figure 4. DS90UB936-Q1 power-up sequencing (b)

In addition to the sequencing between different voltage rails, check if the power-up time of each rail meets the requirements. If VDD18 requires that a power-up time shall not be less than 0.05ms, the too fast power-up time may cause an internal module error.

	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
T0	VDD18 rise time	0.05			ms	at 10/90%
T1	VDDIO rise time	0.2	1		ms	at 10/90%
T2	VDD18 High to VDD11 applied	0			ms	N/A when VDD_SEL = LOW
T3	VDD11 rise time	0.2	1		ms	at 10/90%
T4	VDD to PDB	0			ms	After all VDD are stable
T5	PDB high time before PDB hard reset	1			ms	
T6	PDB high to low pulse width	2			ms	Hard reset (optional)
T7	PDB to I2C ready (IDX and MODE valid) delay	2			ms	

Figure 5. Power-up sequencing requirements of DS90UB936-Q1 power

In addition to the corresponding sequencing, during the troubleshooting, check if the individual power rails are working properly, for example, VDD18 being 1.8V or within the required range. VDD18 mainly powers the internal LDO and output modules, so the ripple of VDD18 is required to be 50mV. VDD11 primarily powers digital modules and requires a ripple within 25mV if VDD11 is supplied externally. In practical applications, VDD18 requires a maximum of 279mA and is recommended to be powered by LDO (such as the TPS745-Q1); To prevent excessive ripple in VDD11 from affecting the digital module, it is recommended that VDD11 shall be powered by an internal LDO. The corresponding power voltages are shown in Figure 6.

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD18)}$	1.71	1.8	1.89	V
	$V_{(VDD11)}$ (VDD_SEL = HIGH ONLY)	1.045	1.1	1.155	V
Supply voltage offset	$V_{(VDD11)}$ - $V_{(VDDIO)}$, $V_{(VDDIO)}$ = 1.8V	-50		50	mV
LVCMOS supply voltage	$V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
	OR $V_{(VDDIO)}$ = 3.3 V	3	3.3	3.6	V
Open-drain voltage	GPIO3/INTB = $V_{(INTB)}$, I2C_SDA, I2C_SCL = $V_{(I2C)}$	1.71		3.6	V
Supply noise(1)	$V_{(VDD11)}$			25	mV_{P-P}
	$V_{(VDD18)}$			50	mV_{P-P}
	$V_{(VDDIO)}$ = 1.8 V			50	mV_{P-P}
	$V_{(VDDIO)}$ = 3.3 V			100	
	RIN0+, RIN1+		10		mV_{P-P}

Figure 6. DS90UB936-Q1 power voltage and ripple requirements

Please verify with an oscilloscope that the VDD power meets the voltage range and ripple requirements. When the voltage range and ripple do not meet the requirements, the internal modules may operate in an improper status, then resulting in abnormal output.

2. Clock status

DS90UB936-Q1 requires a stable clock signal input. The clock source can be either an active crystal oscillator or a passive crystal. DS90UB936-Q1 proposes accuracy and error requirements for the clock signal, as shown in Figure 7. If the clock source is a crystal oscillator, you shall note the high and low levels of the crystal oscillator circuit output. When VDDIO is set to 3.3V, it requires that the high level of clock signal is more than 2V and a low level less than 0.8V. And the duty cycle shall be between 40%-60%. A wrong clock signal can cause an abnormal or no CSI output.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK					
Frequency tolerance	–40°C ≤ T_A ≤ 105°C			±50	ppm
Frequency stability	Aging			±50	ppm
Amplitude		800	1200	$V_{(VDDIO)}$	mVp-p
Symmetry	Duty Cycle	40%	50%	60%	
Rise and fall time	10% – 90%			6	ns
Jitter	200 kHz – 10 MHz		50	200	ps p-p
Frequency		23	25	26	MHz
Spread-spectrum clock modulation percentage	Center Spread	-0.5		+0.5	%
	Down Spread	-1		0	%
Spread-spectrum clock modulation frequency				33	KHz

Figure 7. DS90UB936-Q1 clock signal requirements

Software perspective

1. Check if pattern mode is displayed

   The pattern mode of DS90UB936-Q1 can be used to troubleshoot the problems from DS90UB936-Q1 to SoC section when the problem occurs. Enable pattern mode via the upper computer software ALP of DS90UB936-Q1, as shown in Figure 8. Once the parameters are set, SoC receiving can be used to confirm whether the signal is normal, while the dedicated CSI software can be used to monitor whether the signal flow is normal.

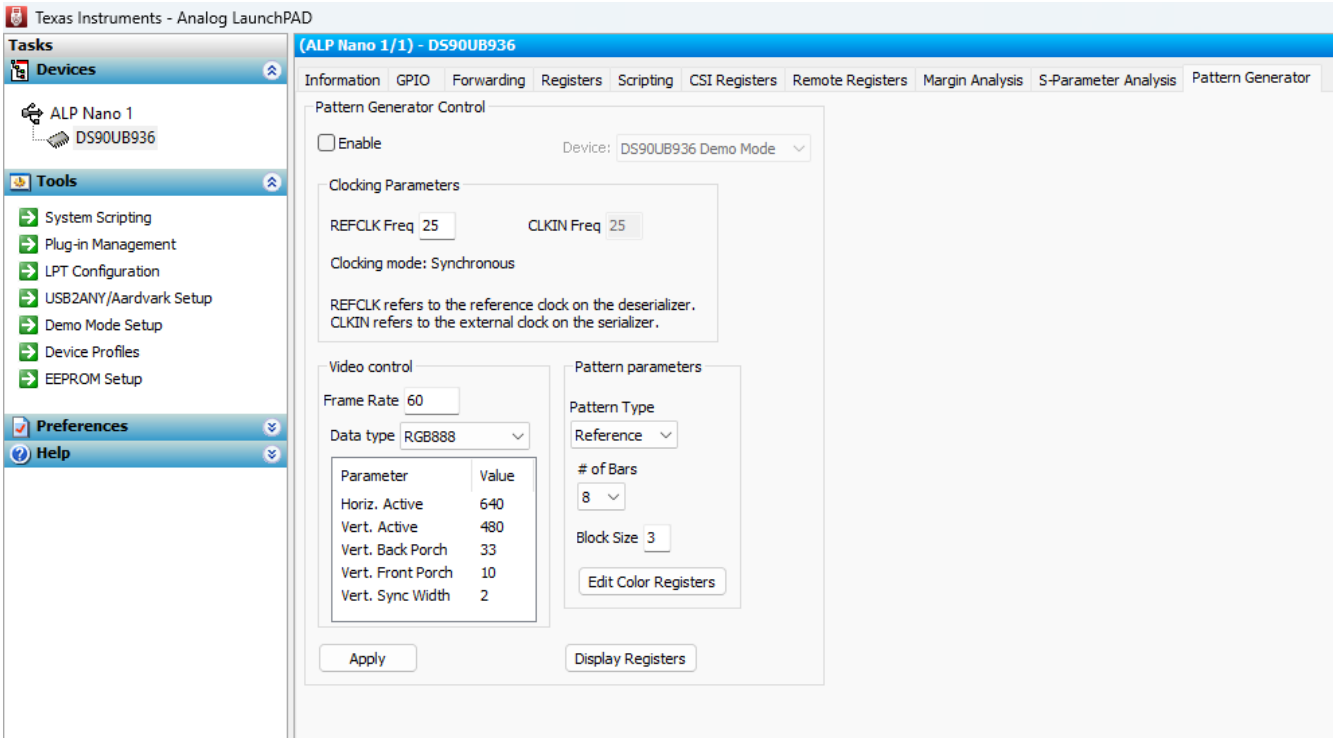


Figure 8. DS90UB936-Q1 upper computer ALP enters pattern mode

If pattern mode is normal, you shall see a color bar on the screen. If there is no picture, you shall verify that the settings at the SoC receiving end match those of the pattern. On the hardware troubleshooting, CSI clock signal (PIN11/PIN12) is tested by a high-speed oscilloscope (bandwidth greater than 2G). If CSI clock is set to 800MHz, you shall see a clock signal at 400MHz frequency on the oscilloscope, as shown in Figure

9. If no similar signal is available, please verify through a register whether DS90UB936-Q1 receives a stable clock signal, and troubleshoot the clock circuits.

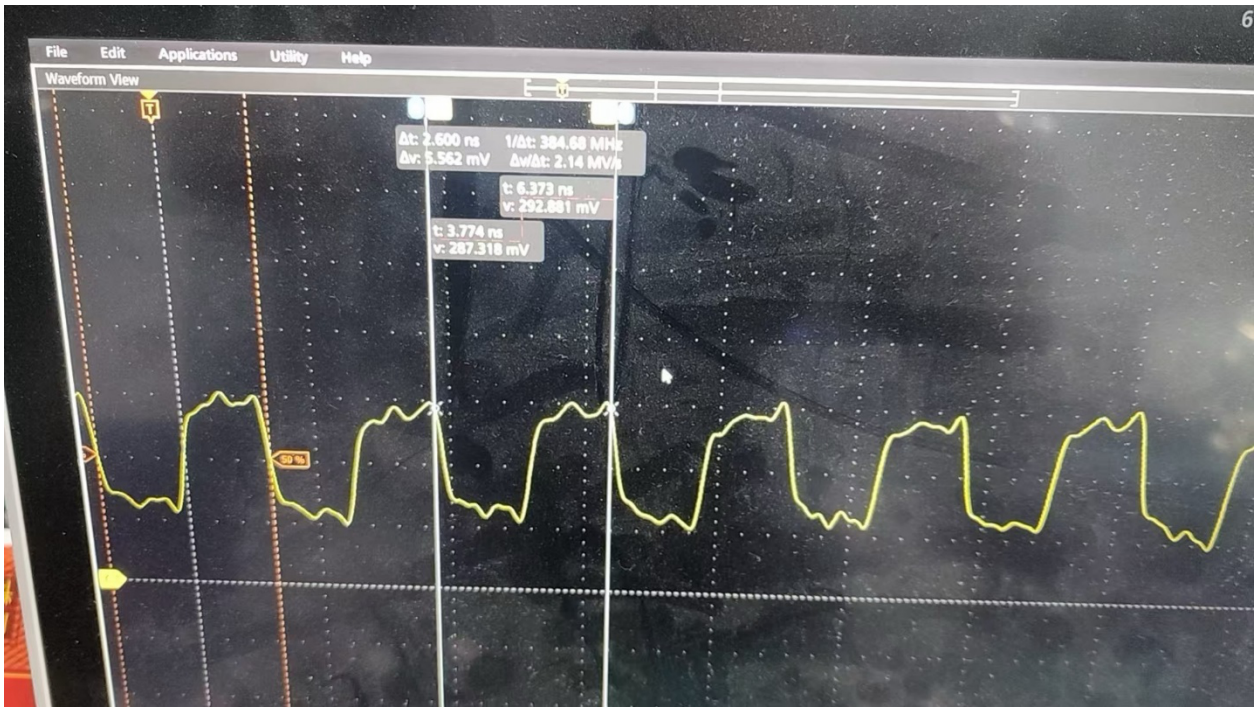


Figure 9. DS90UB936-Q1 CSI clock test

2. Related configuration of DS90UB936-Q1

After the pattern mode is displayed normally, since some serializers do not support pattern mode by themselves, a complete test is usually performed directly with the camera. Configuration codes of DS90UB936-Q1 are given in the annex at the end of the document and the code parameters can be adjusted as required actually. Next, the key points of configuration in those codes are mainly introduced as follows:

a. CSI mode configuration

The protocol needs to be negotiated from the Sensor to the serializer, and from the deserializer to the SoC before data transmission, otherwise the receiving end will not receive data correctly. The specific protocol between DS90UB936-Q1 and SoC needs to be configured, and the data format for all protocols is given in Figure 10. Populate this data format into the register in Figure 11. If the data format for sensor and serializer is RAW10, populate the data format of Figure 10 into the RAW10 register. If it is RAW12 or CSI-2 format, it shall be populated into RAW12 or CSI-2 register respectively, as shown in Figure 11.

As an example, if Sensor transfers data to DS90UB933-Q1 via RAW10 format and DS90UB936-Q1 via YUV422 10BIT format to SoC, 0x1F shall be written to 0x70 register of DS90UB936-Q1. If the Sensor is transferred to the DS90UB935-Q1 via CSI-2 format, simply adjust 0x72 register to meet actual needs.

Incorrect register configuration can also cause that SoC cannot receive signals properly.

Table 19 YUV Image Data Types

Data Type	Description
0x18	YUV420 8-bit
0x19	YUV420 10-bit
0x1A	Legacy YUV420 8-bit
0x1B	Reserved
0x1C	YUV420 8-bit (Chroma Shifted Pixel Sampling)
0x1D	YUV420 10-bit (Chroma Shifted Pixel Sampling)
0x1E	YUV422 8-bit
0x1F	YUV422 10-bit

Table 25 RGB Image Data Types

Data Type	Description
0x20	RGB444
0x21	RGB555
0x22	RGB565
0x23	RGB666
0x24	RGB888

Data Type	Description
0x27	RAW24
0x28	RAW6
0x29	RAW7
0x2A	RAW8
0x2B	RAW10
0x2C	RAW12
0x2D	RAW14
0x2E	RAW16
0x2F	RAW20

Figure 10. Image transfer data format

7.6.104 RAW10_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

RAW10 virtual channel mapping only applies when FPD-Link III operating in RAW10 input mode. See register 0x71 for RAW12 and register 0x72 for CSI-2 mode operation.

Table 7-122. RAW10_ID (Address 0x70)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_VC	R/W	<RX Port #>	RAW10 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW10 data. The field value defaults to the FPD-Link III receive port number (0 or 1)
5:0	RAW10_DT	R/W	0x2B	RAW10 DT This field configures the CSI data type used in RAW10 mode. The default of 0x2B matches the CSI specification.

7.6.105 RAW12_ID Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

RAW12 virtual channel mapping only applies when FPD-Link III operating in RAW12 input mode. See register 0x70 for RAW10 and register 0x72 for CSI-2 mode operation.

Table 7-123. RAW12_ID (Address 0x71)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW12_VC	R/W	<RX Port #>	RAW12 Mode Virtual Channel This field configures the CSI Virtual Channel assigned to the port when receiving RAW12 data. The field value defaults to the FPD-Link III receive port number (0 or 1)

7.6.106 CSI_VC_MAP Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

CSI virtual channel mapping only applies when FPD-Link III operating in CSI-2 input mode. See registers 0x70 and 0x71 for RAW mode operation.

Table 7-124. CSI_VC_MAP (Address 0x72)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	CSI_VC_MAP	R/W	0xE4	CSI-2 Virtual Channel Mapping Register This register provides a method for replacing the Virtual Channel Identifier (VC-ID) of incoming CSI packets. [7:6] : Map value for VC-ID of 3 [5:4] : Map value for VC-ID of 2 [3:2] : Map value for VC-ID of 1 [1:0] : Map value for VC-ID of 0

Figure 11. The data format corresponds to the register

b. 10bit to 8bit conversion

In practice, there may be a possibility that the input is 10bit format and the output is 8bit format. For example, Sensor transfers data to the DS90UB933-Q1 via RAW10 format and DS90UB936-Q1 via YUV422 8BIT format to SoC. At this moment, the input format is 10bit, and the output format is 8bit, which means that DS90UB936-Q1 needs to convert 10bit to 8bit. In this case, the sensor at the previous stage is required to confirm whether the high or low 8bit in the transmitted 10bit is significant, and 0x7C register in the DS90UB936-Q1 is modified accordingly. When it is set to be 10, high 8bit is significant. When it is set to be 11, low 8bit is significant.

7.6.116 PORT_CONFIG2 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 7-134. PORT_CONFIG2 (Address 0x7C)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RAW10_8BIT_CTL	R/W	0x0	Raw10 8-bit mode When Raw10 Mode is enabled for the port, the input data is processed as 8-bit data and packed accordingly for transmission over CSI. 00 : Normal Raw10 Mode 01 : Reserved 10 : 8-bit processing using upper 8 bits. When selecting this value, change CSI data type value RAW10_DT in register 0x70[5:0] 11 : 8-bit processing using lower 8 bits. When selecting this value, change CSI data type value RAW10_DT in register 0x70[5:0]
5	DISCARD_ON _PAR_ERR	R/W	0x1	Discard frames on Parity Error 0 : Forward packets with parity errors 1 : Truncate Frames if a parity error is detected
4	DISCARD_ON _LINE_SIZE	R/W	0x0	Discard frames on Line Size 0 : Allow changes in Line Size within packets 1 : Truncate Frames if a change in line size is detected
3	DISCARD_ON _FRAME_SIZE	R/W	0x0	Discard frames on change in Frame Size When enabled, a change in the number of lines in a frame will result in truncation of the packet. The device will resume forwarding video frames based on the PASS_THRESHOLD setting in the PORT_PASS_CTL register. 0 : Allow changes in Frame Size 1 : Truncate Frames if a change in frame size is detected
2	RESERVED	R/W	0x0	Reserved
1	LV_POLARITY	R/W	0x0	LineValid Polarity This register indicates the expected polarity for the LineValid indication received in Raw mode. 1 : LineValid is low for the duration of the video line 0 : LineValid is high for the duration of the video line
0	FV_POLARITY	R/W	0x0	FrameValid Polarity This register indicates the expected polarity for the FrameValid indication received in Raw mode. 1 : FrameValid is low for the duration of the video frame 0 : FrameValid is high for the duration of the video frame

Figure 12. x7C register

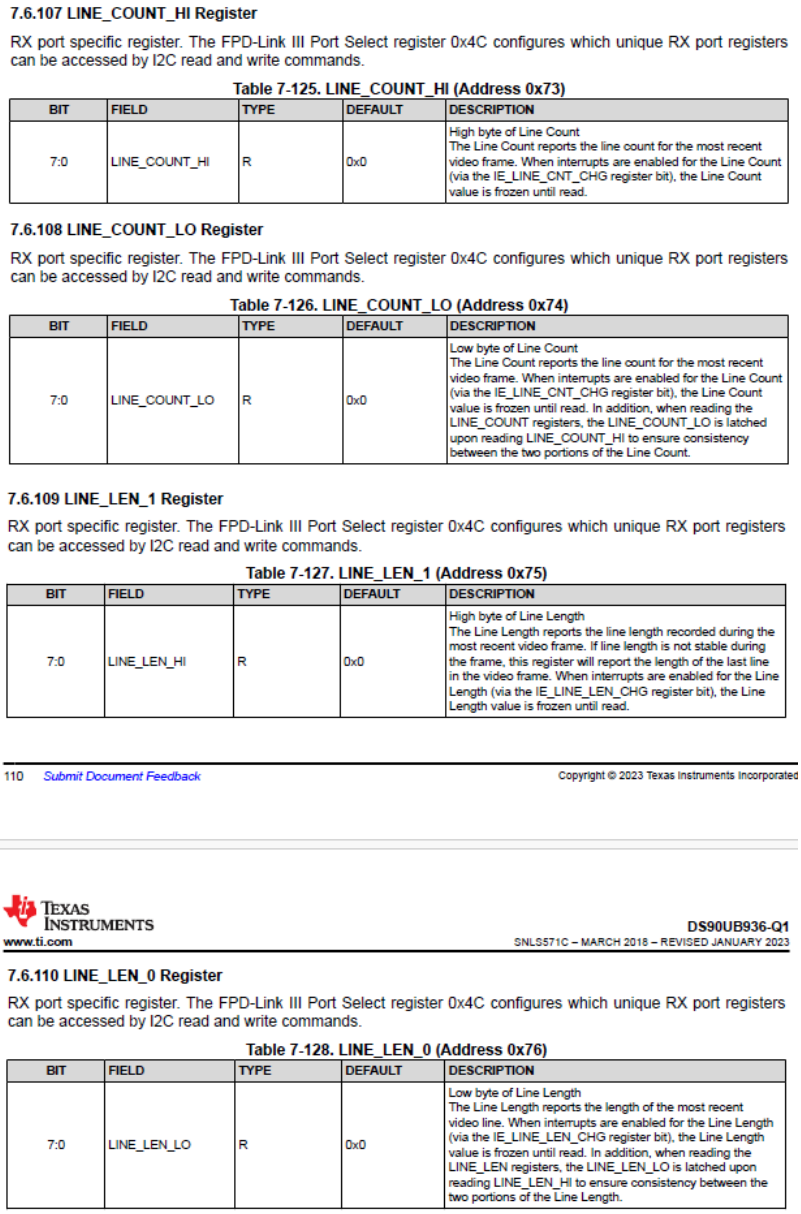
c. Hsync/Vsync settings

If the serializer is a DS90UB933-Q1, Sensor may input Hsync/Vsync signal. Hsync/Vsync of some sensors is highly significant and some are lowly significant. This shall be set in 0x7C register of the DS90UB936-Q1 as shown in Figure 12. Bit1/bit0 is set with the corresponding significant level. LV_POLARITY corresponds to Hsync, while FV_POLARITY corresponds to Vsync. Both bits are set to 1, it enables low, while being set to 0, it enables high. Incorrect setting results in no output.

3. SoC configuration

When DS90UB936-Q1 is fully set up correctly, LINE_COUNT and LINE_LEN registers of DS90UB936-Q1 can be checked as shown in Figure 13. LINE_COUNT represents the number of active lines received by the DS90UB936-Q1 in one frame and the LINE_LEN register represents the active length received by the DS90UB936-Q1 in one line. When these two numbers match the data transmitted by the Sensor, DS90UB936-Q1 is proven to receive valid data and output.

If you do not see the normal picture at this point, you shall check whether configuration at SoC receiving end matches the requirements: the length and width set at the receiving end shall match exactly with the actual values, and the data format set at the receiving end shall match exactly with DS90UB936-Q1 setting.



7.6.107 LINE_COUNT_HI Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 7-125. LINE_COUNT_HI (Address 0x73)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_HI	R	0x0	High byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read.

7.6.108 LINE_COUNT_LO Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 7-126. LINE_COUNT_LO (Address 0x74)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_COUNT_LO	R	0x0	Low byte of Line Count The Line Count reports the line count for the most recent video frame. When interrupts are enabled for the Line Count (via the IE_LINE_CNT_CHG register bit), the Line Count value is frozen until read. In addition, when reading the LINE_COUNT registers, the LINE_COUNT_LO is latched upon reading LINE_COUNT_HI to ensure consistency between the two portions of the Line Count.

7.6.109 LINE_LEN_1 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 7-127. LINE_LEN_1 (Address 0x75)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_HI	R	0x0	High byte of Line Length The Line Length reports the line length recorded during the most recent video frame. If line length is not stable during the frame, this register will report the length of the last line in the video frame. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read.

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7.6.110 LINE_LEN_0 Register

RX port specific register. The FPD-Link III Port Select register 0x4C configures which unique RX port registers can be accessed by I2C read and write commands.

Table 7-128. LINE_LEN_0 (Address 0x76)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	LINE_LEN_LO	R	0x0	Low byte of Line Length The Line Length reports the length of the most recent video line. When interrupts are enabled for the Line Length (via the IE_LINE_LEN_CHG register bit), the Line Length value is frozen until read. In addition, when reading the LINE_LEN registers, the LINE_LEN_LO is latched upon reading LINE_LEN_HI to ensure consistency between the two portions of the Line Length.

Figure 13. LINE_COUNT register and LINE_LEN register

Summary

This document analyzes the causes of the DS90UB936-Q1 black screen in application, proposes troubleshooting guidelines from the hardware and software perspective, and provides appropriate solutions to help engineers troubleshoot problems faster. In addition, an actual configuration code is given for reference.

References

DS90UB936-Q1 Dual 3 Gbps FPD-Link III Deserializer Hub With MIPI CSI-2 Outputs datasheet (Rev. C)

Reference codes

```
//CSI setting Board.writeI2C(DESaddr, 0x4C, 0x01);
                //port0 select Board.writeI2C(DESaddr, 0x33, 0x00); //disable CSI
                Board.writeI2C(DESaddr, 0x1F, 0x0E); //CSI datarate: 800Mbps Board.writeI2C(DESaddr,
                0x20, 0x20);//Enable RX port0; if both ports are used, set to 0x30;
                Board.writeI2C(DESaddr, 0x70, 0x1E); // CSI format setting: YUV422 8bit
                Board.writeI2C(DESaddr, 0x7C, 0xE3); // RAW10 to 8bit setting: lower 8 bits;
                LineValid(Hsync) low, FrameValid(Vsync) low //Framesync setting(unnecessary for only
                port0) Board.writeI2C(DESaddr, 0x4C, 0x01); //port0 select Board.writeI2C(DESaddr,
                0x6E, 0xAA); //BC GPIO1/0 value 1 Board.writeI2C(DESaddr, 0x4C, 0x12); //port1
                select Board.writeI2C(DESaddr, 0x6E, 0xAA); //BC GPIO1/0 value 1
                Board.writeI2C(DESaddr, 0x4C, 0x01); //port0 select Board.writeI2C(DESaddr, 0x10,
                0x1A);// GPIO0 setting Board.writeI2C(DESaddr, 0x19, 0x0A);//FS_HIGH_TIME
                Board.writeI2C(DESaddr, 0x1A, 0xD9) );//FS_HIGH_TIME Board.writeI2C(DESaddr, 0x1B,
                0x61) );//FS_LOW_TIME Board.writeI2C(DESaddr, 0x1C, 0xA7) );//FS_HIGH_TIME
                Board.writeI2C(DESaddr, 0x18, 0x01);//Enable Framesync //GPIO setting
                Board.writeI2C(DESaddr, 0x0F, 0x0E); //GPIO0 output Enable; Board.writeI2C(DESaddr,
                0x10, 0x01); //GPIO0 link to forward channel received GPIO0 from RX port0 SER;
                //Enable CSI Board.writeI2C(DESaddr, 0x33, 0x03); //Enable CSI(remember to enable
                CSI even if you use pattern mode)
```

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