Application Note

Interfacing LVDS Driver With a Sub-LVDS Receiver

ABSTRACT

Sub-LVDS is a reduced voltage version of the LVDS electrical specification. Sub-LVDS varies from LVDS in that its common mode and differential signal levels are reduced, but are still able to drive an LVDS receiver. The problem arises when an LVDS driver needs to interface with a sub-LVDS receiver. Since the drivers' signal voltage levels are not in a suitable range to ensure proper communication with the receiver, it is necessary to alter the drivers output to guarantee appropriate voltage levels. This application report discusses how to interface between an LVDS driver and sub-LVDS receiver and how a simple resistor network can be used to modify the signal voltage levels in a way to ensure compatibility.

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Trademarks

1 Introduction

In order to use an LVDS driver such as the TI DS90LV011A and pair it with a Sub-LVDS receiver, a step-down resistor network must be used in order to provide the proper interface between the LVDS driver and Sub-LVDS receiver. Since an LVDS driver has a typical fixed common mode voltage output of 1.2 V and typical differential voltage swing of 350 mV, the goal of the step-down resistor network is to achieve a fixed common mode voltage of 0.9 V as well as output differential voltage swing of 150 mV. Table 1-1 shows the differences between LVDS driver output levels and Sub-LVDS receiver input levels.

There are two methods in which you could implement this step-down resistor network. The method chosen depends on whether or not your receiver has internal termination integrated into it or not. The first section will focus on the formulas and simulations in a device without internal termination, while the second portion will focus on a device that includes internal termination.

Table 1-1. LVDS Driver Output and Sub-LVDS Receiver Input

	LVDS Driver Output Levels			**SubLVDS Receiver Input Levels**			
Parameter	Min	Typ	Max	Min	Typ	Max	Unit
V_{CMF} Fixed Common Mode Voltage	0.05	1.2	2.35	0.5	0.9	1.3	V
V_{OD} Differential Voltage Swing	247	350	454	100	150	200	mV
V_{TH} Threshold Voltage				-25		25	mV

2 Simulation Setup

The simulations will be done using Keysight ADS with the TI DS90LV011A IBIS model (ds90lv001atmf.ibs) that can be downloaded from the URL: .

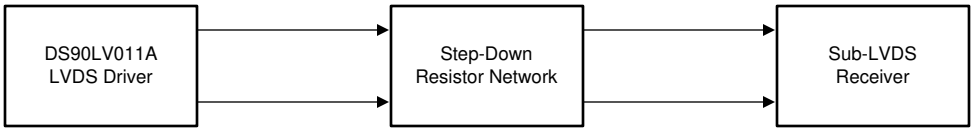


Figure 2-1. Simulation Block Diagram

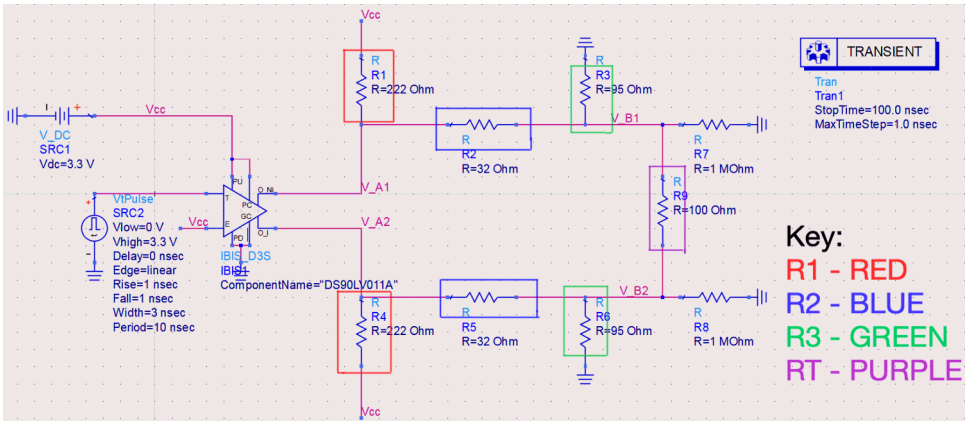


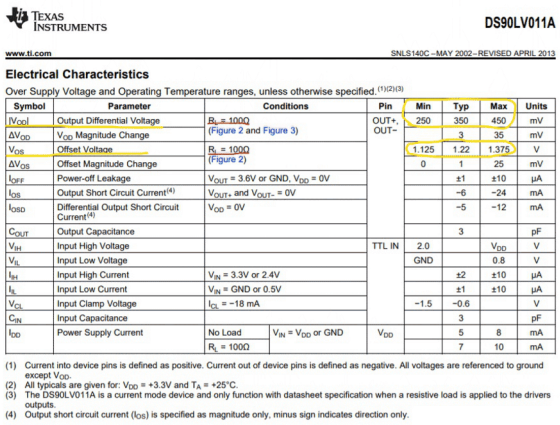
Figure 2-2. Schematic Breakdown

- R_1, R_2, & R_3 make up the resistor network that needs to be created to interface between LVDS and Sub-LVDS. Each differential pair will be made up of these three resistors.
- R_T is the value of the termination resistor for devices that contain internal termination (100Ω will be used for this simulation).
- R_E is the equivalent resistance of all the resistors in the resistor network

Note

The Thevenin resistance of these resistors must be approximately 50Ω if the device does or does not contain internal termination; this ensures that the circuit will have a 100Ω equivalent termination resistance between the transmitter and receiver for both differential pairs. The appropriate formulas for each scenario can be seen in the sections below.

- V_A is equivalent to the fixed common mode voltage (V_{CMF}) of the LVDS driver output (1.2 V will be used for this simulation).
- V_{OD} is the output differential voltage from the LVDS driver.
  - The values used can be obtained from the “Electrical Characteristics” section of the data sheet for your specific device.
  - For more information, see the *DS90LV011A 3V LVDS Single High Speed Differential Driver Data Sheet*.



TEXAS INSTRUMENTS DS90LV011A

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Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100Ω (Figure 2 and Figure 3)		OUT+, OUT−	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change					3	35	mV
V_{OS}	Offset Voltage	R_L = 100Ω (Figure 2)			1.125	1.22	1.375	V
ΔV_{OS}	Offset Magnitude Change				0	1	25	mV
I_{OFF}	Power-off Leakage	V_{OUT} = 3.6V or GND, V_{DD} = 0V				±1	±10	µA
I_{OS}	Output Short Circuit Current(4)	V_{OUT+} and V_{OUT-} = 0V				−6	−24	mA
I_{OSD}	Differential Output Short Circuit Current(4)	V_{OD} = 0V				−5	−12	mA
C_{OUT}	Output Capacitance					3		pF
V_{IH}	Input High Voltage			TTL IN	2.0		V_{DD}	V
V_{IL}	Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3V or 2.4V				±2	±10	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5V				±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.6		V
C_{IN}	Input Capacitance					3		pF
I_{DD}	Power Supply Current	No Load	V_{IN} = V_{DD} or GND	V_{DD}		5	8	mA
		R_L = 100Ω				7	10	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
(3) The DS90LV011A is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Figure 2-3. DS90LV011A Data Sheet Electrical Characteristics

- V_B is equivalent to the fixed common mode voltage (V_{CMF}) of typical Sub-LVDS driver outputs (0.9V will be used for this simulation).
- V_{ID} is the output differential voltage of a Sub-LVDS driver. The goal of the simulation is to obtain a value in the operating range for Sub-LVDS transmitters.
  - The values for a Sub-LVDS driver output can be seen in Table 2-1.
  - The values for a Sub-LVDS receiver input can be seein in Table 2-2.

Table 2-1. SubLVDS Driver Electrical Specifications

	SubLVDS Driver Output Levels			
Parameter	Min	Typ	Max	Unit
V_{CMF} Fixed Common Mode Voltage	0.8	0.9	1	V
V_{OD} Differential Voltage Swing	100	150	200	mV

Table 2-2. SubLVDS Receiver Electrical Specifications

	SubLVDS Receiver Input Levels			
Parameter	Min	Typ	Max	Unit
Input Voltage	0.5	0.9	1.3	V
Threshold Voltage	-25		25	mV
Termination Resistance Value	80	100	120	Ω

3 Devices Without Termination Resistors

- Verify in your data sheet whether the receiver that you are using for your design contains an internal termination resistor. The formulas used are similar to obtain values with small differences taking the termination resistor into consideration.
- If your device does not contain internal termination then the equations shown in Figure 3-1 will be used.

a. $V_A = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{CC}$

b. $V_B = \frac{R_3}{R_2 + R_3} \times V_A$

c. $R_E = R_1 \,||\, (R_2 + R_3)$

d. $V_{ID} = \frac{R_3}{R_2 + R_3} \times V_{OD}, 100\ mV > V_{ID} > 200\ mV$

Figure 3-1. Equations for a Receiver Without Internal Termination

- For the simulation, the following values will be used:
  - V_{CC} = 3.3 V
  - V_A = 1.2 V, LVDS driver output fixed common mode voltage
  - V_B = 0.9 V, Sub-LVDS driver output fixed common mode voltage
  - R_E = 50Ω
- Using the formulas a, b, and c from Section 2, create a system of equations in order to solve for the resistance values that will best fit the desired parameters for Sub-LVDS. The following values were obtained from the system of equations:
  - R_1 = 110Ω
  - R_2 = 35Ω
  - R_3 = 50Ω

Now proceed to simulate the circuit in order to verify the behavior.

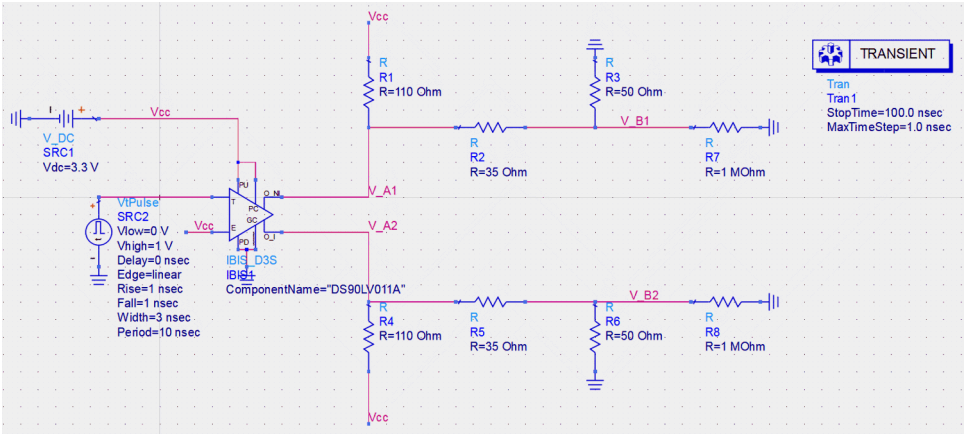

Figure 3-2. Schematic for Receivers Without Internal Termination

Note

R_7 and R_8 are used to imitate the high impedance inputs of a receiver.

- The simulation shown in Figure 3-3 demonstrates a voltage swing of approximately:
  - V_{ID} ≈ 185 mV
  - V_{OD} ≈ 320 mV
- V_{ID} falls within the desired range. If the formulas are used to obtain values for V_{ID}, V_{CMF}, and R_E with the resistor values and the measured values for V_{OD} & V_A, then the following results can be obtained:
  - V_{ID} = 188 mV
  - V_B = 0.85 V

– R_E = 48Ω

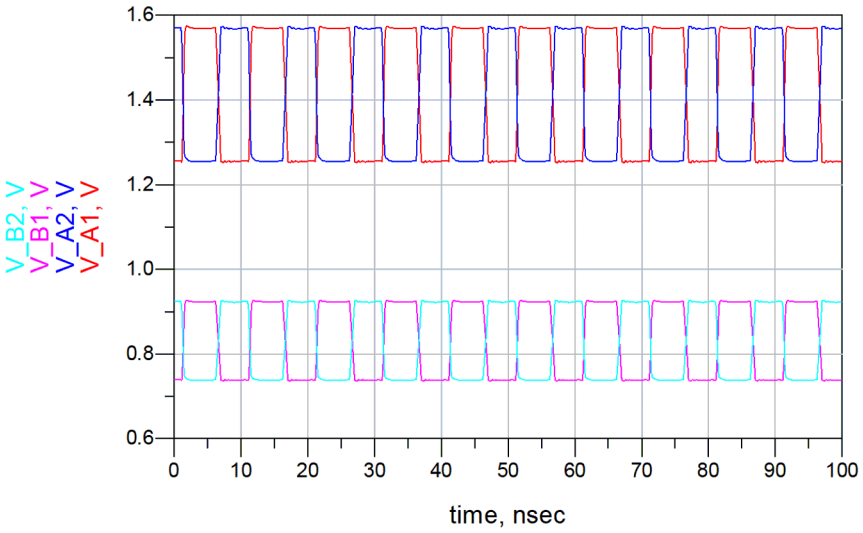

Figure 3-3. Simulation Results for Devices Without Internal Termination

4 Devices With Termination Resistors

- The following scenario is used when the device that is being used for the receiver already contains a termination resistor. The process and the equations are roughly the same with just a few adjustments due to the added resistance. Ensure that the receiver being used contains a termination resistor and obtains the value of the resistance from the data sheet.
- If your device does contains internal termination, then the equations shown in Figure 4-1 will be used.

$$\text{a. } V_A = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{CC}$$

$$\text{b. } V_B = \frac{R_3}{R_2 + R_3} \times V_A$$

$$\text{c. } R_E = R_1 \,||\left(R_2 + \left(R_3 \,||\, \frac{R_T}{2}\right)\right)$$

$$\text{d. } V_{ID} = \frac{\left(R_3 \,||\, \frac{R_T}{2}\right)}{R_2 + \left(R_3 \,||\, \frac{R_T}{2}\right)} \times V_{OD}, 100\text{ mV} > V_{ID} > 200\text{ mV}$$

Figure 4-1. Equations for a Receiver With Internal Termination

- For the simulation, the following values will be used:
  - V_{CC} = 3.3 V
  - V_A = 1.2 V, LVDS driver output fixed common mode voltage
  - V_B = 0.9 V, Sub-LVDS driver output fixed common mode voltage
  - R_E = 50Ω
  - R_T = 100Ω, value of termination resistor inside device
- Using the formulas a, b, and c from Section 2 creates a system of equations in order to solve for the resistance values that will best fit the desired parameters for Sub-LVDS. The following values were obtained from the system of equations:
  - R_1 = 222Ω
  - R_2 = 32Ω
  - R_3 = 95Ω

Proceed to simulate the circuit in order to verify the correct behavior.

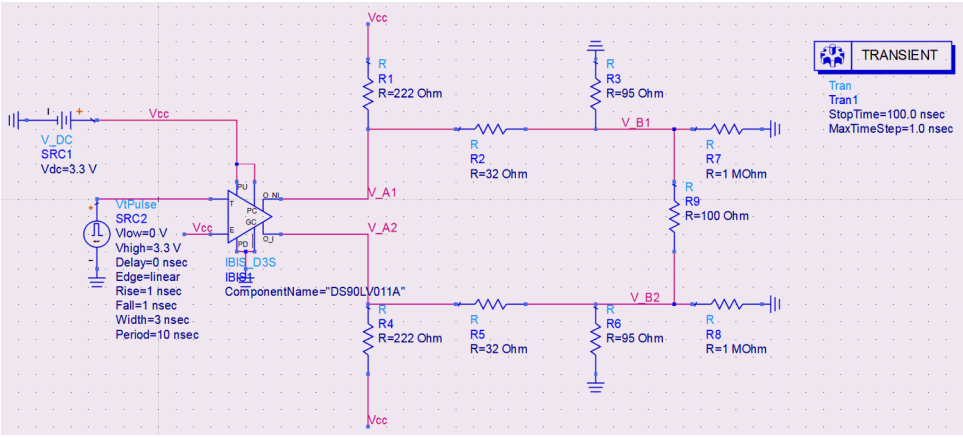

Figure 4-2. Schematic for Receivers With Internal Termination

Note

Resistors R_7 and R_8 are used to imitate the high impedance inputs of a receiver.

- The simulation shown in Figure 4-3 demonstrates a voltage swing of approximately:

  - V_{ID} ≈ 160 mV
  - V_{OD} ≈ 325 mV
- V_{ID} falls within the desired range. If the formulas are used to obtain values for V_{ID}, V_{CMF}, and R_E with the resistor values and the measured values for V_{OD} and V_A then we obtain the following results:
  - V_{ID} = 163 mV
  - V_B = 0.9 V
  - R_E = 50Ω

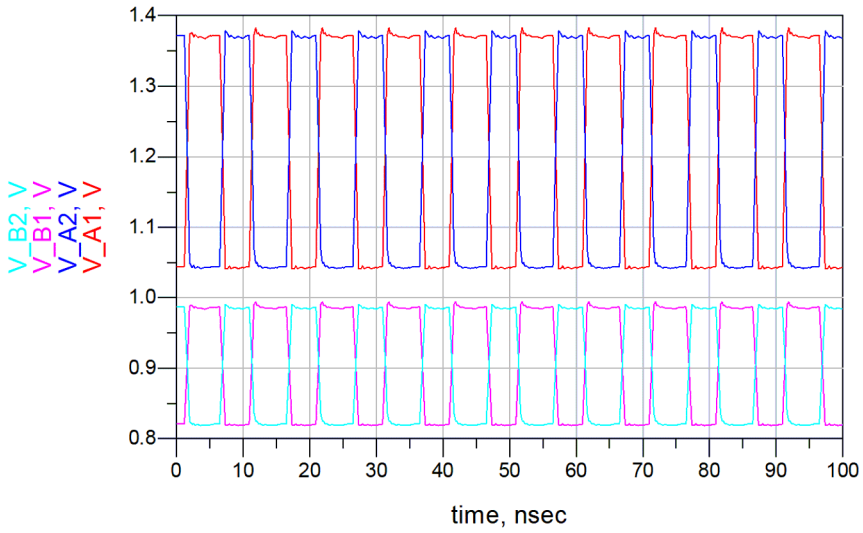

Figure 4-3. Simulation Results for Devices With Internal Termination

5 Other Applications

The method described above specifically details how to apply the step-down resistor network in order to interface between an LVDS driver and the sub-LVDS receiver. It may be useful to note that the same network can also be used to interface between an LVPECL driver and an LVDS receiver. The formulas used are the same, the main difference comes in the values used in the formulas. The values for an LVPECL driver output and an LVDS receiver would instead replace the values used in the calculations in order to solve for the ideal resistor values used in the network.

6 Summary

In conclusion, using a simple resistor network to interface between an LVDS driver and a sub-LVDS receiver is a viable and economical option to support the lower signal voltage levels required by a sub-LVDS receiver.

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